CYPRESS SEMICONDUCTOR

PRELIMINARY

CY7B1094
CY7B1095
CY7B1096

64K x 4 Static R/W RAM

Features

- **High speed**
  — t_{AA} = 6 ns
- **BiCMOS for optimum speed/power**
- **Low active power**
  — 900 mW
- **Low standby power**
  — 350 mW
- **Automatic power-down when deselected**
- **Output enable ($\overline{OE}$) feature**
- **Both 5V and 3.3V TTL-compatible inputs and outputs**

Functional Description

The CY7B1094, CY7B1095, and CY7B1096 are high-performance BiCMOS static RAMs organized as 65,536 words by 4 bits. All devices have a revolutionary center power/ground configuration. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}_1$), an active LOW chip enable ($\overline{CE}_2$, CY7B1096 only), an active LOW output enable ($\overline{OE}$), and three-state drivers. All devices have an automatic power-down feature that reduces power consumption by more than 54% when deselected. Also, for 3.3V systems, V_{OH} is limited to 3.3V max.

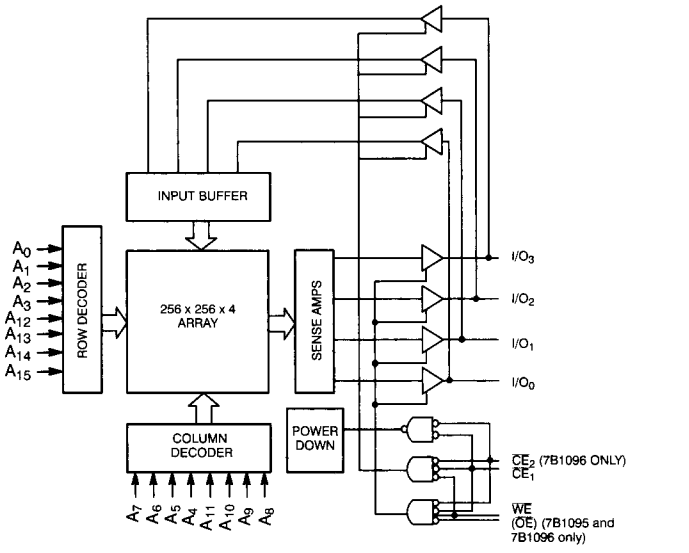
Writing to the device is accomplished by taking chip enable one ($\overline{CE}_1$) and write enable ($\overline{WE}$) inputs and chip enable two ($\overline{CE}_2$, CY7B1096 only) LOW. Data on the I/O pins (I/O_0 through I/O_3) is then written into the location specified on the address pins (A_0 through A_{15}).

Reading from the device is accomplished by taking chip enable one ($\overline{CE}_1$), chip enable two ($\overline{CE}_2$, CY7B1096 only), and output enable ($\overline{OE}$) LOW, while forcing write enable ($\overline{WE}$) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The four input/output pins (I/O_0 through I/O_3) are placed in a high-impedance state when the device is deselected ($\overline{CE}_1$ HIGH or $\overline{CE}_2$ HIGH for the CY7B1096), the outputs are disabled ($\overline{OE}$ HIGH), or during a write operation ($\overline{CE}_1$, $\overline{CE}_2$ for the CY7B1096, and $\overline{WE}$ all LOW).

The CY7B1094, CY7B1095, and CY7B1096 are available in leadless chip carriers, 300-mil-wide center power/ground DIPs, and SOJs.

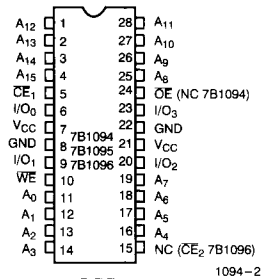
Logic Block Diagram



1094–1

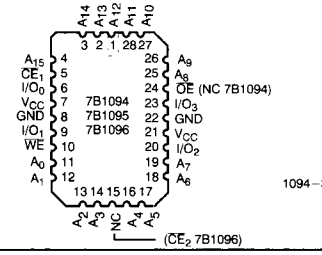
Pin Configurations

DIP/SOJ
Top View



1094–2

LCC
Top View



1094–3

Selection Guide

		7B1094–6 7B1095–6 7B1096–6	7B1094–8 7B1095–8 7B1096–8	7B1094–9 7B1095–9 7B1096–9
Maximum Access Time (ns)		6	8	9
Maximum Operating Current (mA)	Commercial	180	180	
	Military		180	180
Maximum Standby Current (mA)	Commercial	70	70	
	Military		80	80

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... − 65°C to +150°C

Ambient Temperature with Power Applied ..... − 55°C to +125°C

Supply Voltage on V_{CC} Relative to GND[1] . − 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State[1] ..... − 0.5V to +7.0V

DC Input Voltage[1] ..... − 0.5V to +7.0V

Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature[2]	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Military	− 55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[3]

Parameter	Description	Test Conditions		7B1094−6 7B1095−6 7B1096−6 Min.	7B1094−6 7B1095−6 7B1096−6 Max.	7B1094−8, 9 7B1095−8, 9 7B1096−8, 9 Min.	7B1094−8, 9 7B1095−8, 9 7B1096−8, 9 Max.	Unit
V_{OH}[4]	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 4.0 mA		2.4	3.3	2.4	3.3	V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage[1]			− 0.3	0.8	− 0.3	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		− 10	+10	− 10	+10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled		− 10	+10	− 10	+10	µA
I_{OS}	Output Short Circuit Current[5]	V_{CC} = Max., V_{OUT} = GND			− 300		− 300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$	Com'l		180		180	mA
			Mil				180	
I_{SB1}	Automatic $\overline{CE}$ Power-Down Current	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH} f = f_{MAX} = $1/t_{RC}$	Com'l		70		70	mA
			Mil				80	
I_{SB2}[4]	Automatic CE Power-Down Current	Max. V_{CC}, $\overline{CE}$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V, f = 0	Com'l		20		20	mA
			Mil				30	

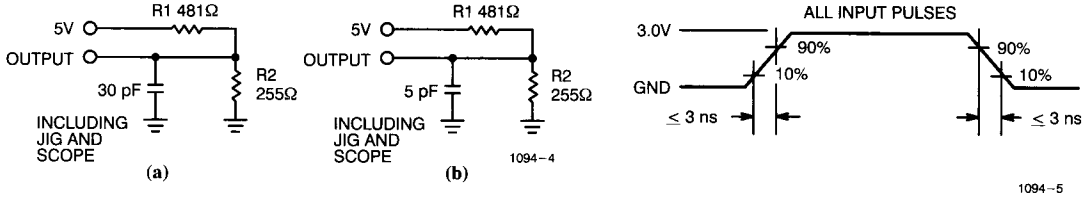
Capacitance[6]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	5	pF
C_{OUT}	Output Capacitance		6	pF

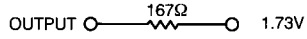
Notes:

1. $V_{IL\,(min.)}$ = − 3.0V for pulse durations of less than 20 ns.
2. T_A is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.
4. V_{OH} maximum is limited by internal temperature-compensated band-gap reference. The output will not go above 3.3V unless externally pulled to above 3.3V.
5. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
6. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT



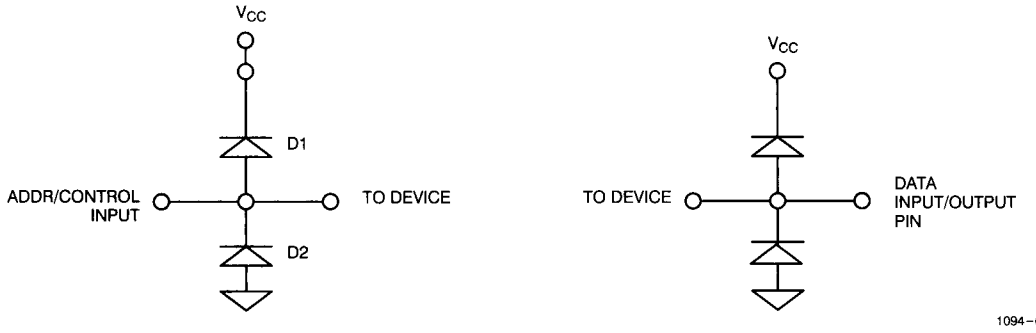
Switching Characteristics Over the Operating Range[3, 7]

Parameter	Description	7B1094–6 7B1095–6 7B1096–6 Min.	7B1094–6 7B1095–6 7B1096–6 Max.	7B1094–8 7B1095–8 7B1096–8 Min.	7B1094–8 7B1095–8 7B1096–8 Max.	7B1094–9 7B1095–9 7B1096–9 Min.	7B1094–9 7B1095–9 7B1096–9 Max.	Unit
READ CYCLE								
t_{RC}	Read Cycle Time	6		8		9		ns
t_{AA}	Address to Data Valid		6		8		9	ns
t_{OHA}	Data Hold from Address Change	2.5		2.5		2.5		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		6		8		9	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		3.5		4		5	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z[8]	0		0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[8, 9]		3		4		4.5	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[8]	0		0		0		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[8, 9]		3		4		4.5	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up		0		0		0	ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		6		10		12	ns
WRITE CYCLE[10, 11]								
t_{WC}	Write Cycle Time	6		8		9		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	5		6		7		ns
t_{AW}	Address Set-Up to Write End	4		6		7		ns
t_{HA}	Address Hold from Write End	0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	4		6		7		ns
t_{SD}	Data Set-Up to Write End	3		4		5		ns
t_{HD}	Data Hold from Write End	0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[8]	0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[8, 9]	0	3	0	4	0	4.5	ns

Notes:

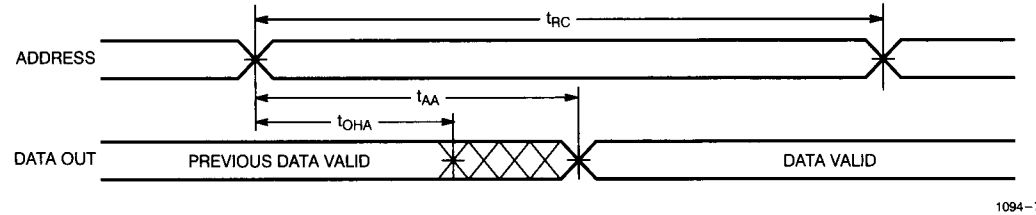
7. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
8. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
9. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads and Waveforms. Transition is measured ±500 mV from steady-state voltage.
10. The internal write time of the memory is defined by the overlap of $\overline{CE}_1$ LOW, $\overline{CE}_2$ LOW, and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal will terminate a write by going HIGH. The input data set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
11. The minimum write cycle time for Write Cycle No. 3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.

Input/Output ESD and Clamp Diode Protection

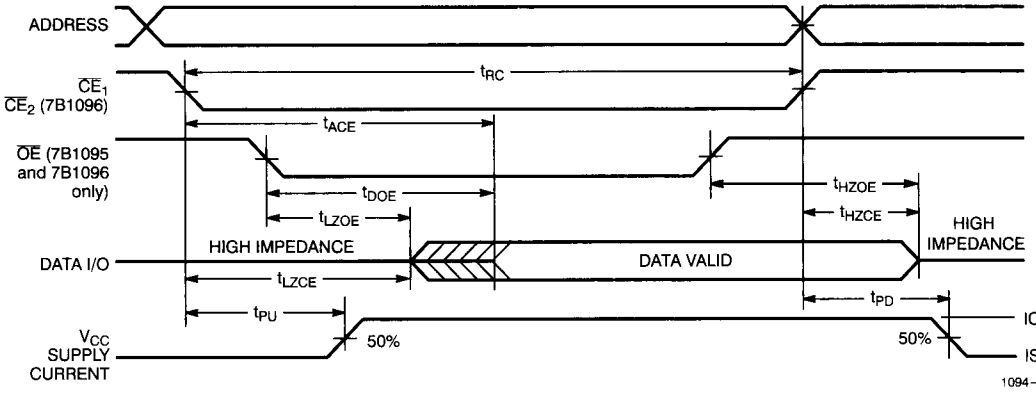


Switching Waveforms

Read Cycle No. 1[12, 13]



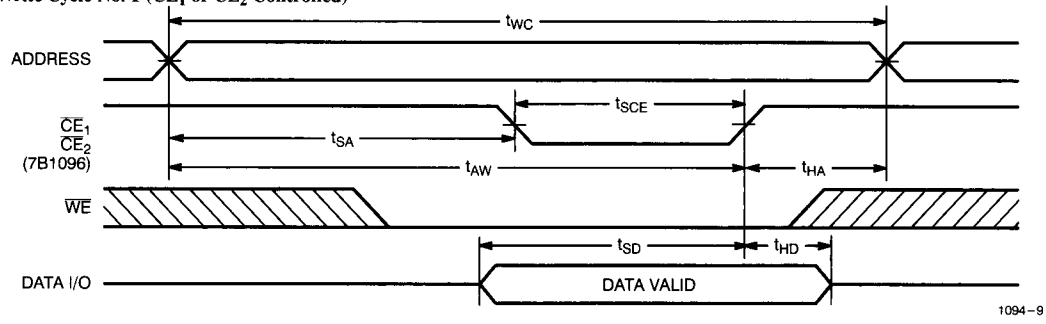
Read Cycle No. 2[13, 14]



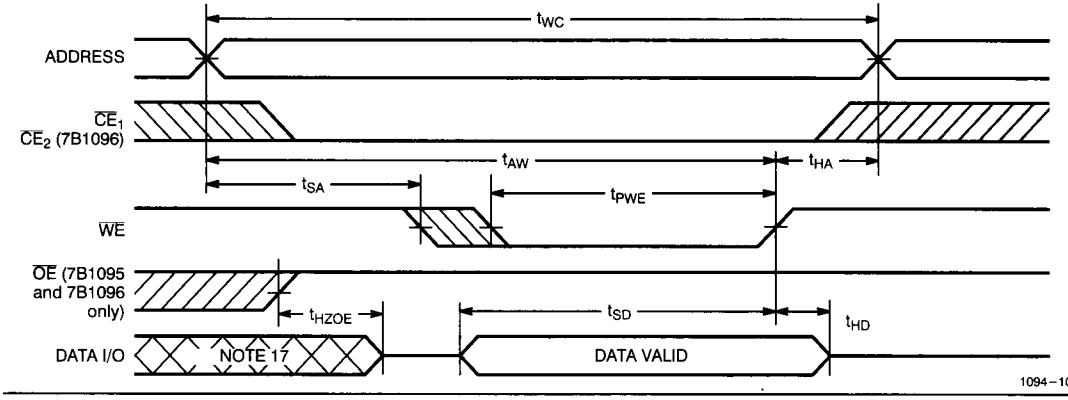
Notes:
12. Device is continuously selected. $\overline{CE}$ and $\overline{OE}$ = V_{IL}.
13. $\overline{WE}$ is HIGH for read cycle.
14. Address valid prior to or coincident with $\overline{CE}$ transition LOW.

Switching Waveforms (continued)

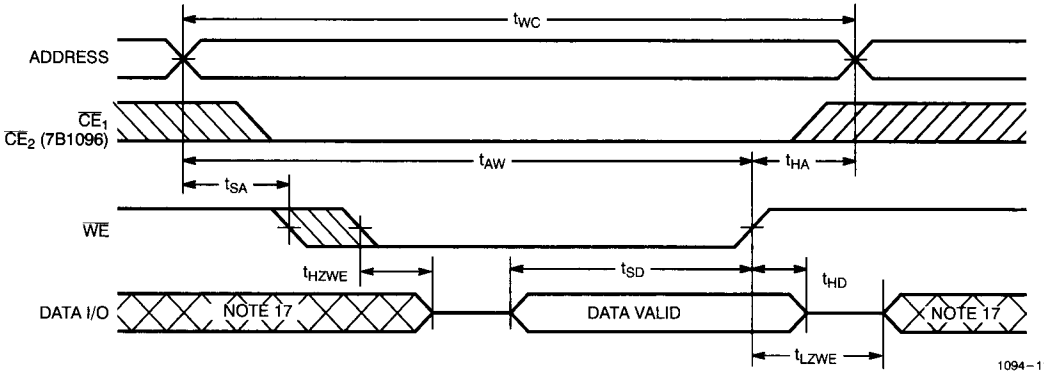
Write Cycle No. 1 ($\overline{CE_1}$ or $\overline{CE_2}$ Controlled)[15, 16]



Write Cycle No. 2 ($\overline{WE}$ Controlled, $\overline{OE}$ HIGH During Write for CY7B1095 and CY7B1096 only)[15, 16]



Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)[11, 16]



Notes:

15. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
16. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.
17. During this time the I/Os are in the output mode and input signals must be applied.

7B1094 Truth Table

$\overline{CE}_1$	$\overline{WE}$	Input/Output	Mode	Power
H	X	High Z	Power-Down	Standby (I_{SB})
L	H	Data Out	Read	Active (I_{CC})
L	L	Data In	Write	Active (I_{CC})

7B1095 Truth Table

$\overline{CE}_1$	$\overline{WE}$	$\overline{OE}$	Input/Output	Mode	Power
H	X	X	High Z	Power-Down	Standby (I_{SB})
L	H	L	Data Out	Read	Active (I_{CC})
L	L	X	Data In	Write	Active (I_{CC})
L	H	H	High Z	Selected, Output Disabled	Active (I_{CC})

7B1096 Truth Table

$\overline{CE}_1$	CE_2	$\overline{WE}$	$\overline{OE}$	Input/Output	Mode	Power
H	X	X	X	High Z	Power-Down	Standby (I_{SB})
X	H	X	X	High Z	Power-Down	Standby (I_{SB})
L	L	H	L	Data Out	Read	Active (I_{CC})
L	L	L	X	Data In	Write	Active (I_{CC})
L	L	H	H	High Z	Selected, Output Disabled	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
6	CY7B1094–6VC	V21	28-Lead Molded SOJ	Commercial
8	CY7B1094–8PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7B1094–8VC	V21	28-Lead Molded SOJ	
	CY7B1094–8DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7B1094–8LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
9	CY7B1094–9DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7B1094–9LMB	L54	28-Pin Rectangular Leadless Chip Carrier	

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
6	CY7B1095–6VC	V21	28-Lead Molded SOJ	Commercial
8	CY7B1095–8PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7B1095–8VC	V21	28-Lead Molded SOJ	
	CY7B1095–8DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7B1095–8LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
9	CY7B1095–9DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7B1095–9LMB	L54	28-Pin Rectangular Leadless Chip Carrier	

Ordering Information (continued)

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
6	CY7B1096–6VC	V21	28-Lead Molded SOJ	Commercial
8	CY7B1096–8PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7B1096–8VC	V21	28-Lead Molded SOJ	
	CY7B1096–8DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7B1096–8LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
9	CY7B1096–9DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7B1096–9LMB	L54	28-Pin Rectangular Leadless Chip Carrier	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
t_{DOE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11

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CYPRESS SEMICONDUCTOR

PLCC and CLCC Packaging for High-Speed Parts

The semiconductor industry is constantly searching for package options that enhance the capabilities of high-performance devices. For fast device performance with minimal ground bounce, electrical characteristics must include low inductance and capacitance from external pin to die bond-wire pad. A package should also furnish good thermal characteristics for reliability over extended temperature ranges.

Other major properties sought after are low cost, as well as standardized outline/pin configurations for compatibility, ease of manufacturing, and handling throughput. The package must also work with surface mount technology and have a small footprint to save board space.

The package that best meets all these requirements is the PLCC (plastic leaded chip carrier). In the past, utilization of PLCCs was not practical for high-power, bipolar devices. However, the advent of low-power bipolar and BiCMOS ECL-compatible SRAMs and PLDs now provides the opportunity for high-volume usage. As manufacturers switch from bipolar to BiCMOS, the lower power dissipation of high-density ECL SRAMs and complex PLDs promise to give PLCC packages a bright future. For military applications and extended temperature environments or for devices with higher power dissipation, you can substitute the CLCC (ceramic leaded chip carrier).

The PLCC has many desirable qualities:

- Suitable for surface mounting with J-type leads
- Small footprint to save board space
- Low inductance and capacitance for high speed with little ground-bounce
- Good thermal characteristics for reliability over temperature range
- Ease of manufacturing and handling for production throughput
- Low cost compared to CERDIP, flatpack, LCC
- Standard package outline and pin-configuration compatibility

The PLCC's J-type surface-mount leads have the advantage over gull-wing leads, which are susceptible to fatigue. J leads also enhance handling ease in test and burn-in fixtures. The PLCC's 1-pF capacitance compares favorably with the 3 and 6 pF for plastic DIPs and CERDIPs, and inductance is equally impressive: 2 nH versus 6 and 11 nH for plastic DIP and CERDIP. Unlike flatpacks, PLCCs are available in standard tooling. PLCCs come in a variety of pin configurations, from 18 to over 200 pins, versus a maximum of 40 pins for plastic DIPs.

The Ceramic Leaded Chip Carrier

For high-temperature environments and high-power devices, you can make use of the ceramic leaded chip carrier (CLCC, Y package), which can also be surface mounted. The Y package has the same footprint and J leads as the PLCC (*Figure 1*) and works well for the faster PLDs and SRAMs.

If you do not know system temperature in the early stages of a design, you can substitute the Y package for the PLCC and vice versa, so long as the device's die junction temperature does not exceed 150°C. The Y package is slightly more expensive than the PLCC, but with a thermal resistance from junction to ambient (Θ_{JA}) of 35°C/W at 500 LFPM, the Y package can dissipate heat more efficiently.

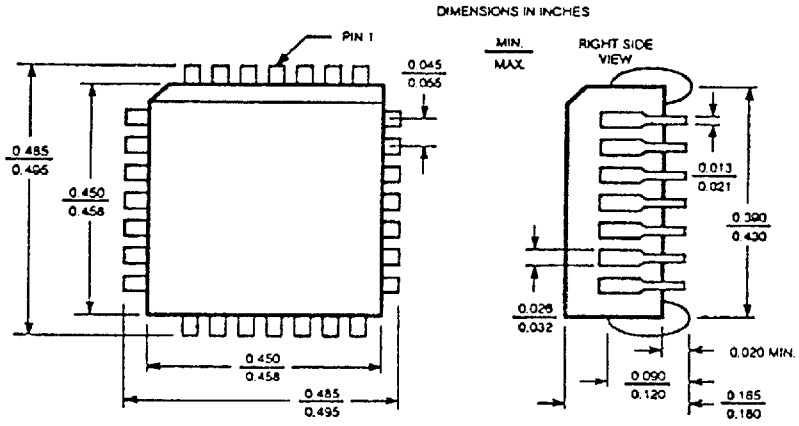
Reliability

Cypress's bipolar and BiCMOS products in PLCC and CLCC packages go through extensive burn-in and testing at elevated temperature to guarantee package integrity. Cypress strongly recommends 500-LFPM system forced air flow but guarantees reliability in systems with or without the flow if the ambient air does not cause the junction temperature (T_J) to exceed 150°C.

The PLCC's Θ_{JA} is approximately 45°C/W. The SRAMs have power dissipation that ranges from 780 mW max for the CY100E422L-5 up to 1097 mW max for the CY10E474L-5. This dissipation results in junction temperature rises from 35 to 49°C. The 16P4-type PLD (CY100E302L-6) has a temperature rise of 39°C, and the

T-90-20

28-Lead Plastic Leaded Chip Carrier J64



28-Pin Ceramic Leaded Chip Carrier Y64

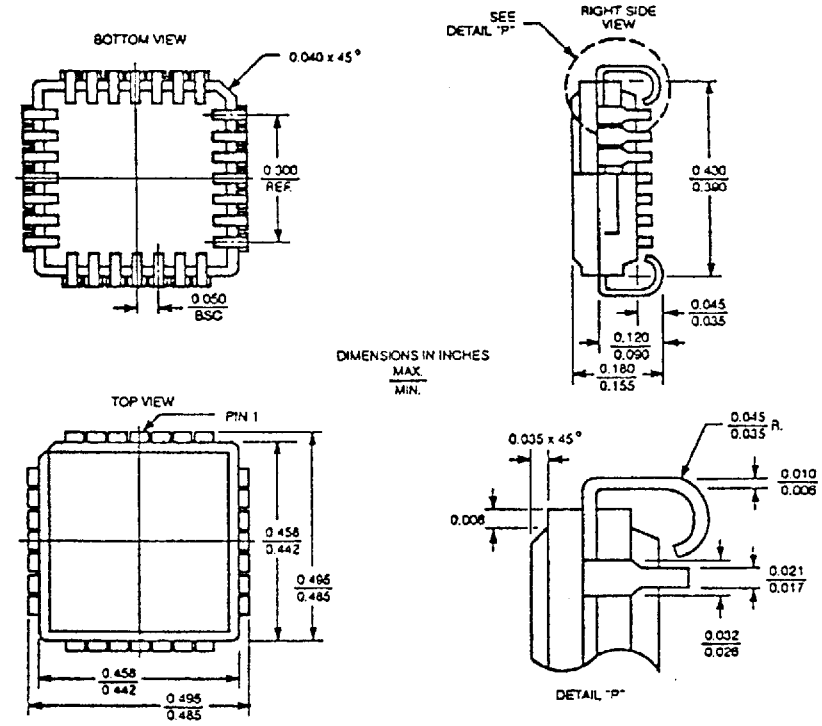


Figure 1. Diagrams of 28-Lead Chip Carriers

16P8-type PLD (CY10E301L-6) has a temperature rise of 47°C. The CLCC package's Θ_{JA} equals 35°C/W for temperature rises of up to 55°C (CY10E474-3).

Finding Chip-Level Junction Temperature

The following relationship determines chip-level junction temperature for the PLCC package:

$T_J = \Delta T + T_A$

where

$\Delta T = P_D \times \Theta_{JA}$

and

$\Theta_{JA} = \Theta_{JC} + \Theta_{CS} + \Theta_{SA}$

To calculate worst case junction temperature (T_J) use maximum supply V_{EE} and I_{EE} for power dissipation and maximum T_A for the temperature range of interest. For the 10K/10KH CY10E301L in a PLCC, for example, device I_{EE} = 170 mA max and V_{EE} = 5.46V max for P_D = 928 mW. Add 15 mW per output for a total output P_D = 120 mW. Therefore, the total P_D = 1048 mW.

For a PLCC, Θ_{JA} = 45°C/W at 500 LFPM, and Θ_{JA} = 64°C/W for still air.

For a CLCC, Θ_{JA} = 35°C/W at 500 LFPM, and Θ_{JA} = 54°C/W for still air.

Because

T_J = total $P_D \times \Theta_{JA} + T_A$

and

T_A = 75°C worst-case commercial temperature range, for the PLCC:

$T_J = (1.048\ W)(45°C/W) + 75°C = 122°C$ at 500 LFPM

$T_J = (1.048\ W)(64°C/W) + 75°C = 142°C$ in still air

This calculation is for absolute worst-case data sheet conditions. The burn-in temperature used by Cypress (T_J) is much higher than the device will ever see in a system. Note that *most systems will not run at worst case due to guard-banding*. For this reason, use V_{EENOM} = 5.2V or 4.5V and $I_{EENOM} = (I_{EEMAX})(85\%)$ for nominal-condition calculations.

Real-World Values

Obviously, most systems do not operate at the worst-case conditions. Therefore, *Figures 2* through *5* show graphs over different operating conditions to determine failures in time (FITs) and mean time between failure (MTBF) for a typical system or in a worst-case scenario.

The graphs are based on a linear method of interpreting the failures observed at burn-in and indicate the long-term reliability of Cypress devices. You can use the graphs to determine MTBF and FITs for any Cypress device in any package after calculating the appropriate ΔT.

The X-axis on the graphs indicates junction temperature. These values are determined by adding the ΔT to ambient temperature, as described earlier. As an example, *Figures 2* and *3* note the following critical points for a CY10E301L ECL PLD under three different operating conditions:

- Point A — 10K/10KH typical data sheet conditions: 25°C ambient, nominal V_{EE} and I_{EE}, 50Ω loads, 500 LFPM air flow, T_J = 64°C, FITs = 7, MTBF = 18,000 yrs.
- Point B — 10K/10KH typical operating conditions: 55°C ambient, nominal V_{EE} and I_{EE}, 50Ω loads, 500 LFPM air flow, T_J = 94°C, FITs = 45, MTBF = 2800 yrs.
- Point C — 10K/KH absolute worst-case conditions: 75°C ambient, 5.46 V max and 170 mA max, 50Ω loads, 500 LFPM air flow, T_J = 122°C, FITs = 225, MTBF = 525 yrs.

The activation energy used for the MTBF and FITs information is 0.7 eV. This is an average number for die-surface-related defects, such as metal and oxide pinholes, etc., but is very conservative for silicon defects or mechanical interfaces to packages. The number is usually 1.0 eV. A small change here results in a significant change in MTBF or FITs. A change to 0.8 eV equates to a 33% reduction in FITs rate or a 50% increase in MTBF.

The Packages of Choice

The PLCC and CLCC are accepted as the packages of choice by many manufacturers of high-speed devices. Motorola Semiconductor uses the PLCC as the only package for the company's very high speed ECL$_{INPS}$ ECL logic family, which stands for "ECL in picoseconds" and is pronounced "eclipse." This family has set-up times and propagation delays in the sub-nanosecond range, with power dissipation of over 1W. Fully compatible with Cypress SRAMs and PLDs, the ECL$_{INPS}$ family includes many 10K, 10KH, and 100K standard logic gates, building blocks, and transceivers.

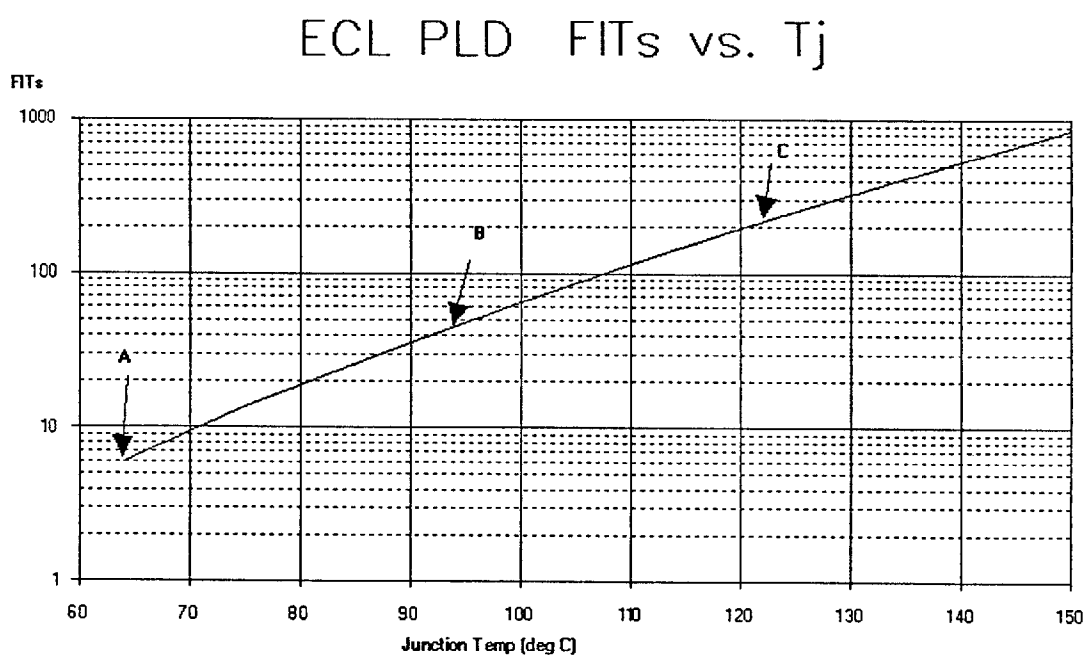


Figure 2. Failures in Time vs Junction Temperature

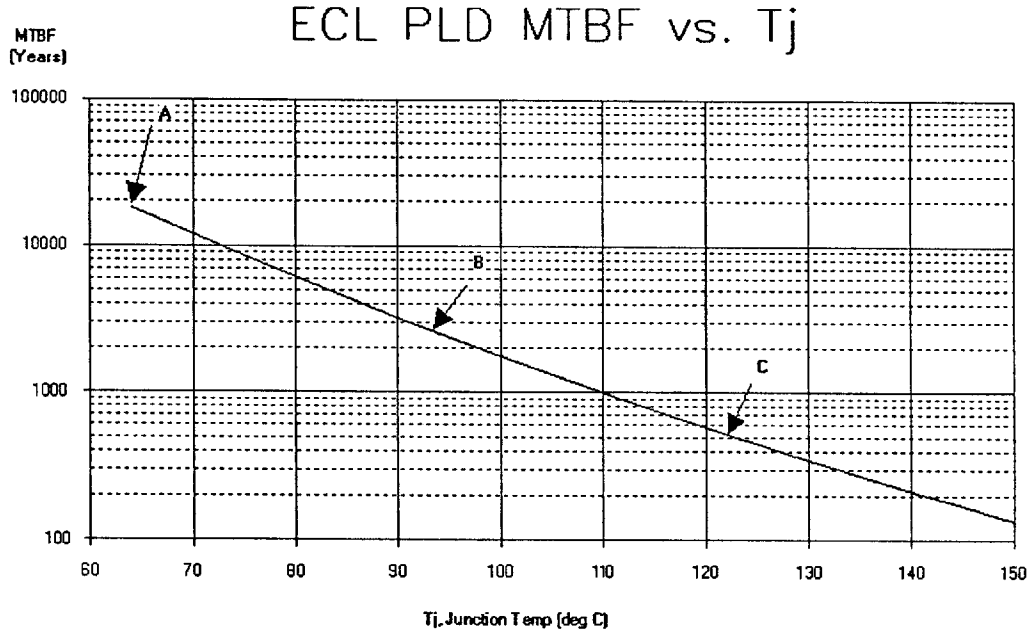


Figure 3. Mean Time Between Failures vs Junction Temp.

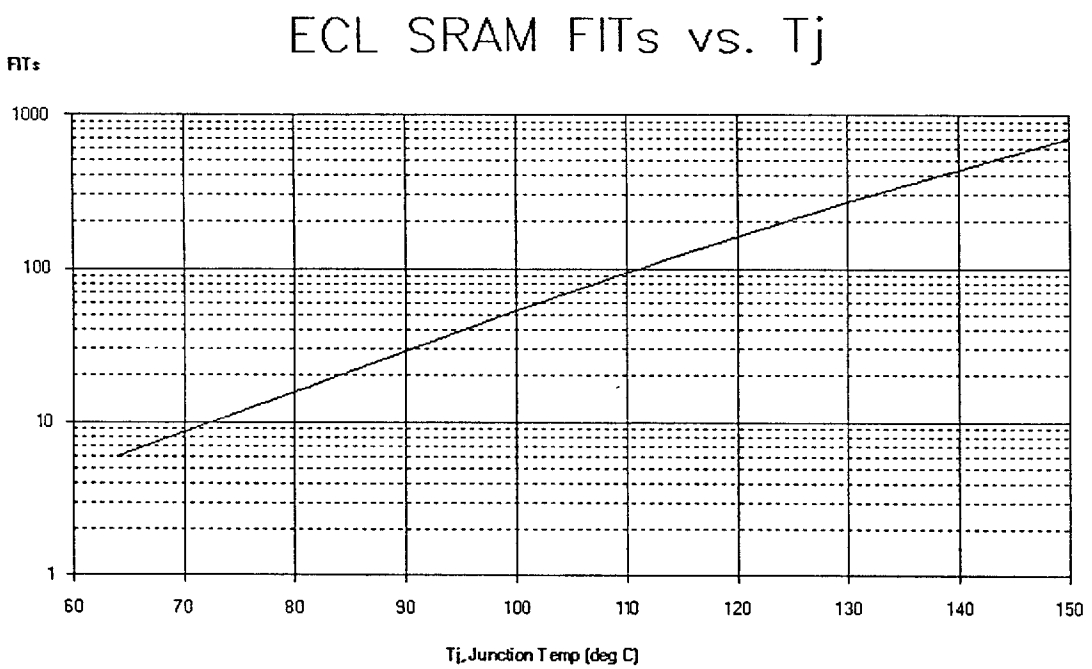


Figure 4. Failures in Time vs Junction Temperature

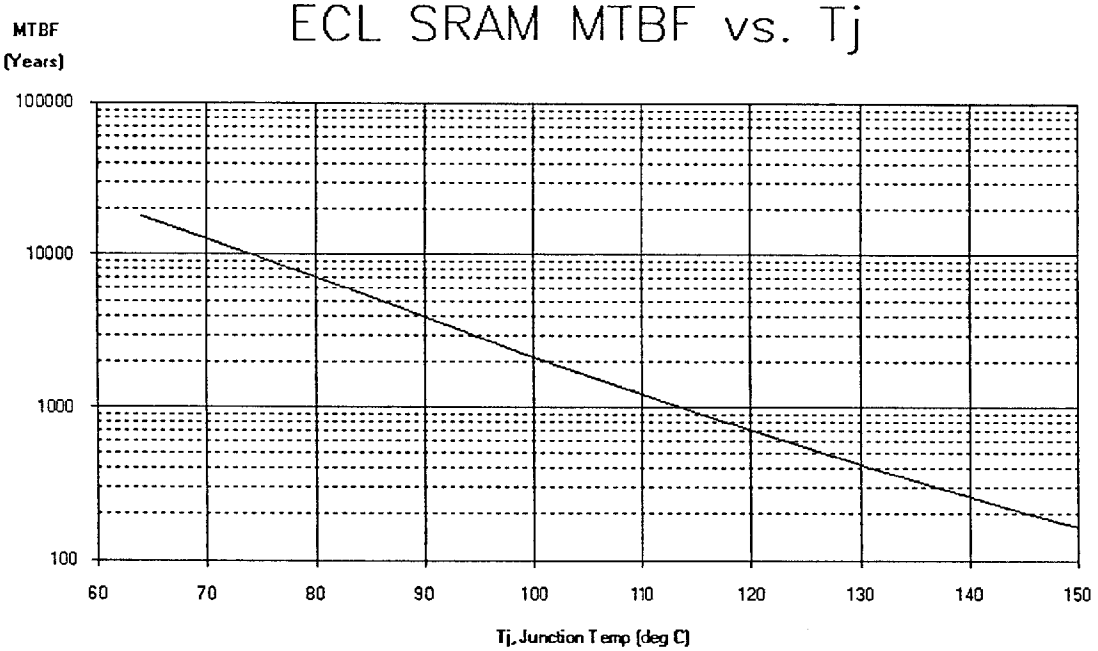


Figure 5. Mean Time Between Failure vs Junction Temp.