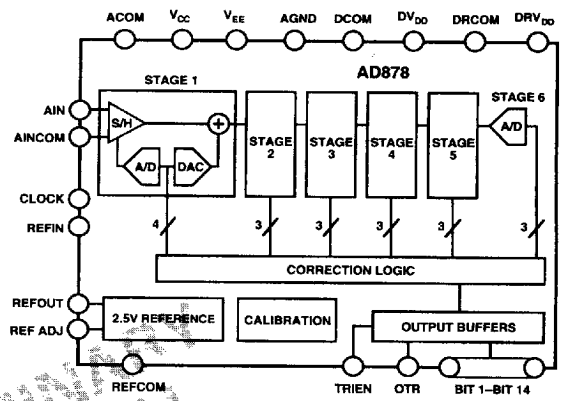
Complete 14-Bit 2.2 MSPS Monolithic A/D Converter

AD878

FEATURES

Monolithic 14-Bit 2.2 MSPS A/D Converter
Low Power Dissipation: 500 mW
No Missing Codes Guaranteed
Differential Nonlinearity Error: 0.5 LSB
Complete: On-Chip Track-and-Hold Amplifier and Voltage Reference
Signal-to-Noise and Distortion Ratio: 80 dB
Spurious-Free Dynamic Range: 85 dB
Out-of-Range Indicator
44-Pin PLCC

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD878 is a monolithic 14-bit, 2.2 Msps analog-to-digital converter with an on-chip, high performance sample-and-hold amplifier and voltage reference. The AD878 uses a multistage pipelined architecture with factory programmed calibration circuitry and output error correction logic to provide 14-bit accuracy at 2.2 Msps data rates. The AD878 combines a merged high speed bipolar/CMOS process and a novel architecture to achieve the resolution and speed of hybrid implementations at a fraction of the power consumption. Additionally, the greater reliability of monolithic construction offers improved system reliability and lower costs than hybrid designs.

The high input impedance, fast-settling input sample-and-hold (S/H) amplifier is well suited for both multiplexed systems that switch negative to positive full-scale voltage levels in successive channels and sampling single-channel inputs at frequencies up to the Nyquist rate. The AD878's wideband input combined with the power and cost savings over previously available hybrids will allow new design opportunities in communications, imaging and medical applications. The AD878 provides both reference output and reference input pins, allowing the on-board reference to serve as a system reference. An external reference can also be substituted to suit the dc accuracy and temperature drift requirements of the application. A single clock input is used to control all internal conversion cycles. The digital output data is presented in binary output format. An out-of-range signal indicates an overflow condition. It can be used with the most significant bit to determine low or high overflow.

The AD878 is fabricated on Analog Devices' ABCMOS process which utilizes high speed bipolar and CMOS transistors on a single chip. High speed, precision analog circuits are now combined with high density logic circuits.

The AD878 is packaged in a 44-pin plastic leaded chip carrier (PLCC) package and is specified for operation from 0°C to +70°C and –40°C to +85°C.

PRODUCT HIGHLIGHTS

The AD878 offers a complete single-chip sampling 14-bit, 2.2 Msps analog-to-digital conversion function in a 44-pin PLCC surface mount package.

Low Power: The AD878 at 650 mW max consumes a fraction of the power of presently available hybrids.

On-Chip Sample-and-Hold (S/H): The high impedance S/H input eliminates the need for external buffers.

Out of Range (OTR): The OTR output bit indicates when the input signal is beyond the AD878's input range.

Ease-of-Use: The AD878 is complete with S/H and voltage reference.

This is a preliminary data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

AD878–SPECIFICATIONS

DC SPECIFICATIONS (T_{MIN} to T_{MAX} with V_{CC} = +5 V, DV_{DD} = +5 V, DRV_{DD} = +5 V, V_{EE} = –5 V, f_{SAMPLE} = 2.2 Msps, unless otherwise noted)

Parameter	J Grade[1]	A Grade[1]	Units
RESOLUTION	14	14	Bits min
MAX CONVERSION RATE	2.2	2.2	MHz min
ACCURACY			
Integral Nonlinearity (INL)	±2.5	±2.5	LSB typ
Differential Nonlinearity (DNL)	±0.5	±0.5	LSB typ
No Missing Codes	14	14	Bits Guaranteed
Zero Error (@ +25°C)[2]	±TBD	±TBD	% FSR max
Gain Error (@ +25°C)[2]	±TBD	±TBD	% FSR max
TEMPERATURE DRIFT[3]			
Zero Error	±TBD	±TBD	% FSR max
Gain Error[3, 4]	±TBD	±TBD	% FSR max
Gain Error[3, 5]	±TBD	±TBD	% FSR max
POWER SUPPLY REJECTION[6]			
V_{CC} (+5 V ± 0.25 V)	±TBD	±TBD	% FSR max
DV_{DD} (+5 V ± 0.25 V)	±TBD	±TBD	% FSR max
V_{EE} (–5 V ± 0.25 V)	±TBD	±TBD	% FSR max
ANALOG INPUT			
Input Range	±2.5	±2.5	Volts max
Input Resistance	1	1	MΩ typ
Input Capacitance	10	10	pF typ
INTERNAL VOLTAGE REFERENCE			
Output Voltage	2.5	2.5	Volts typ
Output Voltage Tolerance	±25	±25	mV max
Output Current (Available for External Loads) (External Load Should Not Change During Conversion)	2.5	2.5	mA typ
REFERENCE INPUT RESISTANCE	2	2	kΩ typ
POWER SUPPLIES			
Supply Voltages			
V_{CC}	+5	+5	V (±5% V_{CC} Operating)
V_{EE}	–5	–5	V (±5% V_{EE} Operating)
DV_{DD}, DRV_{DD}	+5	+5	V (±5% DV_{DD}, DRV_{DD} Operating)
Supply Current			
IV_{CC}	80	80	mA max
IV_{EE}	45	45	mA max
$IDRV_{DD}$, IDV_{DD}	5	5	mA max
POWER CONSUMPTION	500 650	500 650	mW typ mW max

NOTES
[1]Temperature ranges are as follows: J Grade: 0°C to +70°C; A Grade: –40°C to +85°C.
[2]Adjustable to zero with external potentiometers (See Zero and Gain Error Calibration section).
[3]+25°C to T_{MIN} and +25°C to T_{MAX}.
[4]Includes internal voltage reference error.
[5]Excludes internal reference drift.
[6]Change in Gain Error as a function of the dc supply voltage.
Specification subject to change without notice.

AC SPECIFICATIONS (T_{MIN} to T_{MAX} with V_{CC} = +5 V, DV_{DD} = +5 V, DRV_{DD} = +5 V, V_{EE} = –5 V, f_{SAMPLE} = 2.2 Msps, unless otherwise noted)[1]

Parameters	J Grade	A Grade	Units
SIGNAL-TO-NOISE AND DISTORTION RATIO (S/N+D)			
f_{INPUT} = 100 kHz	80	80	dB typ
	TBD	TBD	dB min
f_{INPUT} = 1 MHz	TBD	TBD	dB typ
TOTAL HARMONIC DISTORTION (THD)			
f_{INPUT} = 100 kHz	–83	–83	dB typ
	TBD	TBD	dB max
f_{INPUT} = 1.0 MHz	TBD	TBD	dB typ
SPURIOUS FREE DYNAMIC RANGE (SFDR)			
f_{INPUT} = 100 kHz	85	85	dB typ
INTERMODULATION DISTORTION (IMD)[2]			
Second Order Products	80	80	dB typ
Third Order Products	80	80	dB typ
FULL POWER BANDWIDTH	2.0	2.0	MHz typ
SMALL SIGNAL BANDWIDTH	5	5	MHz typ
APERTURE DELAY	TBD	TBD	ns typ
APERTURE JITTER	20	TBD	ps rms typ
ACQUISITION TO FULL-SCALE STEP	200	200	ns typ
OVERVOLTAGE RECOVERY TIME	TBD	TBD	ns typ

NOTES
[1]f_{IN} amplitude = –0.5 dB full scale unless otherwise indicated. All measurements referred to +0 dB (2.5 V pk) input signal unless otherwise indicated.
[2]fa = 100 kHz, fb = 95 kHz with f_{SAMPLE} = 2.2 MHz.
Specifications subject to change without notice.

DIGITAL SPECIFICATIONS (T_{MIN} to T_{MAX} with V_{CC} = +5 V, DV_{DD} = +5 V, DRV_{DD} =+5 V, V_{EE} = –5 V, f_{SAMPLE} = 2.2 Msps, unless otherwise noted)

Parameters	Symbol	J, A Grades	Units
LOGIC INPUTS			
High Level Input Voltage	V_{IH}	+3.8	V min
Low Level Input Voltage	V_{IL}	+0.95	V max
High Level Input Current (V_{IN} = DV_{DD})	I_{IH}	±10	µA max
Low Level Input Current (V_{IN} = 0 V)	I_{IL}	±10	µA max
Input Capacitance	C_{IN}	5	pF typ
LOGIC OUTPUTS			
High Level Output Voltage (I_{OH} = 0.5 mA)	V_{OH}	+2.4	V min
Low Level Output Voltage (I_{OL} = 1.6 mA)	V_{OL}	+0.4	V max
Output Capacitance	C_{OUT}	5	pF typ

Specifications subject to change without notice.

SWITCHING SPECIFICATIONS (T_{MIN} to T_{MAX} with V_{CC} = +5 V, DV_{DD} = +5 V, DRV_{DD} = +5 V, V_{EE} = –5 V; V_{IL} = 0.95 V, V_{IH} = 3.8 V, V_{OL} = 0.4 V and V_{OH} = 2.4 V)

Parameters	Symbol	J, A Grades	Units
Clock Period[1]	t_C	455	ns min
CLOCK Pulse Width High	t_{CH}	227	ns min
CLOCK Pulse Width Low	t_{CL}	227	ns min
Clock Duty Cycle[2]		TBD	% min (50% typ)
		TBD	% max
Output Delay	t_{OD}	20	ns min
Pipeline Delay (Latency)		4	Clock Cycles max
Data Access Time	t_{DD}	TBD	ns typ (100 pF Load)
Output Float Delay	t_{HL}	TBD	ns typ (10 pF Load)

NOTES
[1]Conversion rate is operational to TBD without degradation in specified performance.
[2]See Clock Input section for clock periods of TBD ns or greater.
Specifications subject to change without notice.

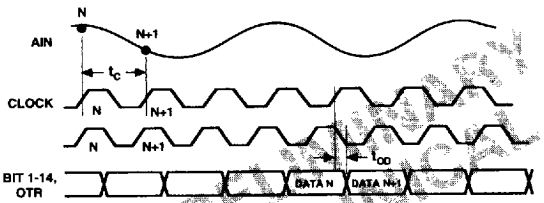


Figure 1. Timing Diagram

ABSOLUTE MAXIMUM RATINGS*

Parameter	With Respect to	Min	Max	Units
V_{CC}	ACOM	–0.5	+6.5	Volts
V_{EE}	ACOM	–6.5	+0.5	Volts
DV_{DD}	DCOM	–0.5	+6.5	Volts
DRV_{DD}	DRCOM	–0.5	+6.5	Volts
ACOM	DCOM	–1.0	+1.0	Volts
AINCOM	ACOM	–1.0	+1.0	Volts
REFCOM	ACOM	–1.0	+1.0	Volts
DRCOM	DCOM	–1.0	+1.0	Volts
V_{CC}	DV_{DD}	–6.5	+6.5	Volts
Clock Input	DCOM	–0.5	DV_{DD} + 0.5	Volts
Digital Outputs	DCOM	–0.5	DRV_{DD} + 0.3	Volts
AIN, REF IN	AGND	TBD	TBD	Volts
REF IN	V_{CC}	V_{EE}	0	Volts
REF IN	V_{EE}	0	V_{CC}	Volts
Junction Temperature			+150	°C
Storage Temperature		–65	+150	°C
Lead Temperature (10 sec)			+300	°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may effect device reliability.