CS- 5121

Nonsynchronous NFET Buck Controller with V^2 Architecture

Description

The CS- 5121 is a nonsynchronous single N-Channel buck controller. It is designed to provide unprecedented transient response for today's demanding high-density, high-speed logic. The regulator operates using a proprietary control method, which allows a 100ns response time to load transients. The CS- 5121 is designed to operate over a 4.25-20V range (V_{CC}) using 12V to run the part and 5V as the main supply for conversion.

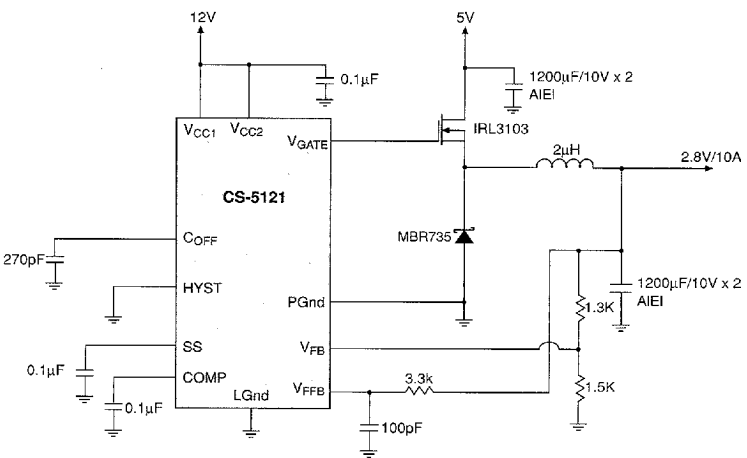
The CS- 5121 is specifically designed to power Intel-based CPUs and other high performance core logic. The CS-5121 includes the following features: short circuit protection, 1% output tolerance, on-board driver with 1.5A peak output current, and programmable soft start capability. The CS- 5121 is available in 16 pin surface mount and DIP packages.

Features

- Single N-Channel Design
- Excess of 1MHz Operation
- 100ns Response to Step Load
- 30ns Gate Rise/Fall Times
- 1% Reference Accuracy
- 5V & 12V Operation
- Remote Sense
- Programmable Soft Start
- Lossless Short Circuit Protection
- V^2 Control Topology
- Adaptive Voltage Positioning
- Compatible with CS-5150/5151/5155/5156 CPU Controllers

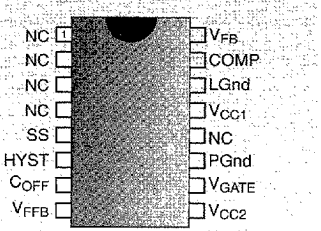
Application Diagram

Pentium® Pro Converter



Package Options

16 Lead SO Narrow & PDIP



Pentium is a registered trademark of Intel Corporation.

Cherry Semiconductor
Cherry Semiconductor Corporation
2000 South County Trail
East Greenwich, Rhode Island 02818-1530
Tel: (401)885-3600 Fax (401)885-5786
email: info@cherry-semi.com

Absolute Maximum Ratings

Pin Name	Max Operating Voltage	Max Current
V_{CC1}	14V/-0.3V	25mA DC/1.5A peak
V_{CC2}	20V/-0.3V	20mA DC/1.5A peak
SS	6V/-0.3V	-100µA
COMP	6V/-0.3V	200µA
V_{FB}	6V/-0.3V	-0.2µA
C_{OFF}	14V (connected to V_{CC1}) - 0.3V	-0.2µA
V_{FFB}	5V/-0.3V	-0.2µA
V_{GATE}	20V/-0.3V	100mA DC/1.5A peak
HYST	5V/-0.3V	100µA
LGnd	0V	25mA
PGnd	0V	100mA DC/1.5A peak

Lead Temperature Soldering: Wave Solder (through hole styles only) . . . . . 10 sec. max, 260°C peak
Reflow (SMD styles only) . . . . . 60 sec. max above 183°C, 230°C peak

Electrical Characteristics: $0°C < T_A < +70°C$; $0°C < T_J < +125°C$; $8V < V_{CC1} < 14V$; $5V < V_{CC2} < 20V$; $CV_{GATE} = 1nF$; $C_{OFF} = 330pF$; $C_{SS} = 0.1µF$, unless otherwise specified.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
■ Error Amplifier					
V_{FB} Leakage Current	$V_{FB} = 0V$		0.3	1.0	µA
Open Loop Gain	$1.25V < V_{COMP} < 4V$	50	60		dB
Unity Gain Bandwidth	Note 1	500	3000		kHz
COMP SINK Current	$V_{COMP} = 1.5V$; $V_{FB} = 1.7V$; $V_{SS} > 2V$	500	2500	8000	µA
COMP SOURCE Current	$V_{COMP} = 4.0V$; $V_{FB} = 1.3V$; $V_{SS} = 5V$	120	200	280	µA
COMP Clamp Current	V_{COMP}=0V;V_{FB}=1.3V;V_{SS}=5V	0.4	1.0	1.6	mA
COMP High Voltage	$V_{FB} = 1.3V$; $V_{SS} = 5V$	4.0	4.3	5.0	V
COMP Low Voltage	V_{FB} =1.7V		160	300	mV
PSRR	$8V < V_{CC1} < 14V$ @ 1kHz; Note 1	60	85		dB
■ Internal Voltage Reference					
Reference Voltage	Measure $V_{FB} = V_{COMP}$	1.455	1.470	1.485	V
■ Minimum Input Voltage (V_{CC1})					
Start Threshold	Output switching		4.175	4.250	V
■ V_{GATE}					
Out SOURCE Sat at 100mA	Measure $V_{CC2} - V_{GATE}$		1.2	2.0	V
Out SINK Sat at 100mA	Measure V_{GATE} – VPGnd		1.0	1.5	V
Out Rise Time	$1V < V_{GATE} < 9V$; $V_{CC1} = V_{CC2} = 12V$		30	50	ns
Out Fall Time	$9V > V_{GATE} > 1V$;$V_{CC1} = V_{CC2} = 12V$		30	50	ns
Shoot-Through Current	Note 1			50	mA
V_{GATE} Resistance	Resistor to LGnd	20	50	100	kΩ
V_{GATE} Schottky	LGnd to V_{GATE} @ 10mA		600	800	mV
■ Soft Start (SS)					
Charge Time		1.6	3.3	5.0	ms
Pulse Period		25	100	200	ms
Duty Cycle	(Charge Time/Pulse Period) × 100	1.0	3.3	6.0	%
COMP Clamp Voltage	$V_{FB} = 1.3V$; $V_{SS} = 0$	0.50	0.95	1.10	V
V_{FFB} SS Fault Disable	V_{GATE} = Low	0.9	1.0	1.1	V

Electrical Characteristics: $0°C < T_A < +70°C$; $0°C < T_J < +70°C$; $8V < V_{CC1} < 14V$; $5V < V_{CC2} < 20V$; $CV_{GATE} = 1nF$; $C_{OFF} = 330pF$; $C_{SS} = 0.1\mu F$, unless otherwise specified.

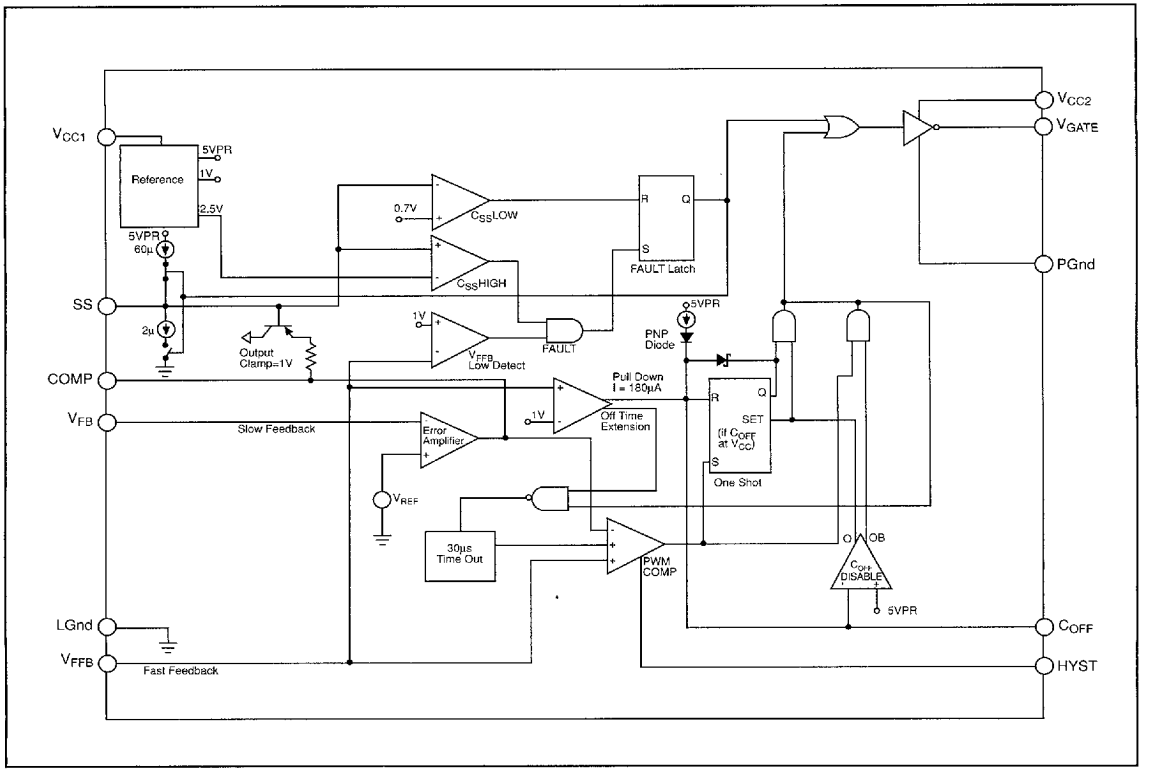
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
■ Transient Response					
V_{FFB}, Constant Off Time	C_{OFF} = 0pF, V_{FFB} High (0 to 5V) to GATE Low (< 1V)		100	125	ns
■ Supply Current					
I_{CC1}	No Switching		8.5	13.5	mA
I_{CC2}	No Switching		1.6	3.0	mA
Operating I_{CC1}	V_{FB} = COMP = V_{FFB}		8	13	mA
Operating I_{CC2}	V_{FB} = COMP = V_{FFB}		2	5	mA
■ C_{OFF}					
Normal Charge Time	V_{FFB} = 1.5V; V_{SS} = 5V	1.2	1.6	2.0	µs
Extension Charge Time	V_{SS} = V_{FFB} = 0	6.0	8.0	10.0	µs
Discharge Current	C_{OFF} to 5V; V_{FB} >1V	2.0	3.5		mA
Disable Voltage	V_{FFB} = 0V	7.4	8.7	10.0	V
■ Maximum ON-Time					
Time Out Time	V_{FB} = V_{COMP}; V_{FFB} = 2V; V_{HYST} = 0; Record V_{GATE} Pulse High Duration	10	30	50	µs

Note 1: Guaranteed by design, not 100% tested in production.

Package Pin Description

PACKAGE PIN #	PIN SYMBOL	FUNCTION
16L SO Narrow & PDIP		
1,2,3,4,12	NC	No connection.
5	SS	Soft Start Pin. A capacitor from this pin to LGnd in conjunction with internal 60µA current source provides soft start function for the controller. This pin disables fault detect function during Soft Start. When a fault is detected, the soft start capacitor is slowly discharged by internal 2µA current source setting the time out before trying to restart the IC. Charge/discharge current ratio of 30 sets the duty cycle for the IC when the power supply output is permanently shorted.
6	HYST	Voltage at this pin sets the hysteresis for the PWM comparator. This pin is grounded when the IC operates in the constant OFF time mode as set by the C_{OFF} pin. Otherwise, the hysteresis defines switching frequency by setting the output ripple voltage.
7	C_{OFF}	A capacitor from this pin to ground sets the time duration for the on-board one-shot, which is used for the constant off-time architecture.
8	V_{FFB}	Fast feedback connection. This pin is connected directly to the output filter capacitor. The inner feedback loop is used to terminate on-time.
9	V_{CC2}	Boosted power for the gate driver.
10	V_{GATE}	FET driver pin capable of 1.5A peak switching current.
11	PGnd	High current ground for the IC. The MOSFET driver is referenced to this pin. Input capacitor ground should be tied to this pin.
13	V_{CC1}	Input power for the IC.
14	LGnd	Signal ground for the IC. All control circuits are referenced to this pin.
15	COMP	Error amplifier compensation pin. A capacitor to ground should be provided externally to compensate the amplifier.
16	V_{FB}	Error amplifier DC feedback input. This is the master voltage feedback which sets the output voltage. This pin can be connected directly to the output through a resistor divider.

Block Diagram



Theory of Operation

V^2 Control Method

The V^2 method of control uses a ramp signal that is generated by the ESR of the output capacitors. This ramp is proportional to the AC current through the main inductor and is offset by the value of the DC output voltage. This control scheme inherently compensates for variation in either line or load conditions, since the ramp signal is generated from the output voltage itself. This control scheme differs from traditional techniques such as voltage mode, which generates an artificial ramp, and current mode, which generates a ramp from inductor current.

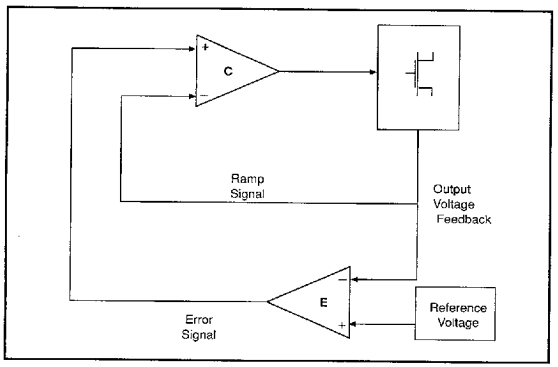


Figure 1: V^2 Control Diagram

The V^2 control method is illustrated in Figure 1. Notice that the output voltage is used to generate both the error signal and the ramp signal. Since the ramp signal is simply the output voltage, it is affected by any change in the output regardless of the origin of that change. The ramp signal also contains the DC portion of the output voltage, which allows the control circuit to drive the main switch to 0% or 100% duty cycle when required.

A change in line voltage changes the current ramp in the inductor, affecting the ramp signal, which causes the V^2 control scheme to compensate duty cycle. Since the change in inductor current modifies the ramp signal, like in current mode control, the V^2 control scheme has the same advantages in line transient response.

A change in load current will have an affect on the output voltage, thus altering the ramp signal. Remarkably, a load step can immediately change the state of the comparator output, which controls the main switch. Load transient response is determined only by the comparator response time and the transition speed of the main switch. The reaction time to an output load step has no relation to the crossover frequency of the error signal loop, as in traditional control methods.

The error signal loop can have a low crossover frequency, since transient response is handled by the ramp signal loop. The main purpose of this 'slow' feedback loop is to provide DC accuracy. Noise immunity is significantly improved, since the error amplifier bandwidth can be rolled off at a low frequency. Enhanced noise immunity improves remote sensing of the output voltage, since the noise associated with long feedback traces can be effectively filtered.

Line and load regulation are drastically improved due to the fact that there are two independent voltage loops. A voltage mode controller relies on a change in the error signal to compensate for a deviation in either line or load voltage. This change in the error signal causes the output voltage to change corresponding to the gain of the error amplifier, which is normally specified as line and load regulation. A current mode controller maintains fixed error signal under deviation in the line voltage, since the slope of the ramp signal changes, but still relies on a change in the error signal for a deviation in load. The V^2 method of control maintains a fixed error signal for both line and load variation, since the ramp signal is affected by both line and load.

Constant Off-Time Architecture

The V^2 control method can be used with most controller architectures, such as fixed frequency, constant off-time, hysteretic, etc. The CS- 5121 operates using constant off-time architecture. The off-state of the switch is terminated after a fixed period every cycle, which is determined by the C_{OFF} capacitor. The on-time of the switch is terminated by monitoring the output voltage ramp, which is fed to the PWM comparator.

Protection and Monitoring Features

Short Circuit Protection

The CS- 5121 uses a unique short circuit protection scheme that provides very low power dissipation under an output short circuit condition. When a short circuit is detected the CS- 5121 shuts down the power supply. After a time out period the CS- 5121 attempts to power the load, but if the short persists the power supply will be shut down again. In a short circuit condition the power supply will be on about 3% of the time, drastically reducing power dissipation. This technique will improve short circuit reliability and allow higher peak currents that are required by the load.

Applications Diagrams

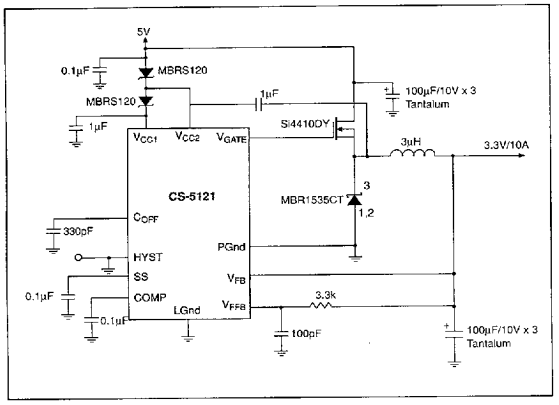


Figure 1: 5V to 3.3V/10A converter.

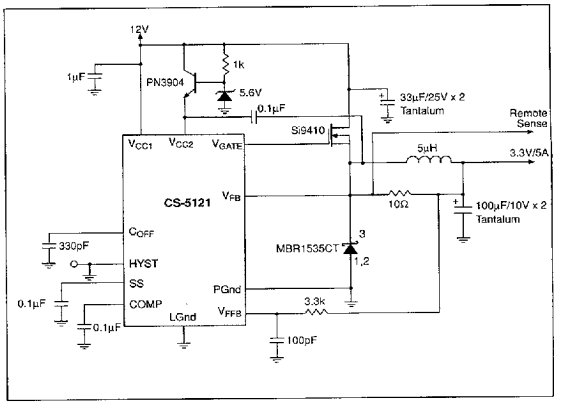


Figure 3: 12V to 3.3V/5A converter with remote sense.

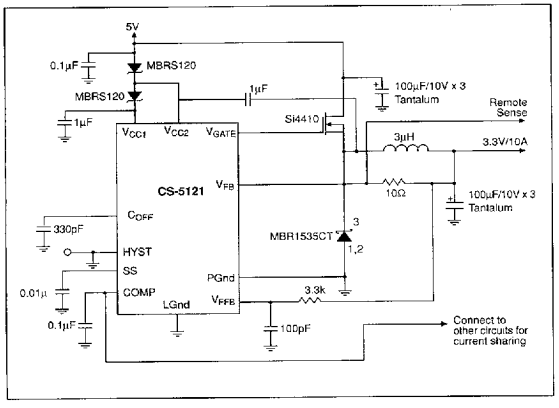


Figure 2: 5V to 3.3V/10A converter with current sharing.

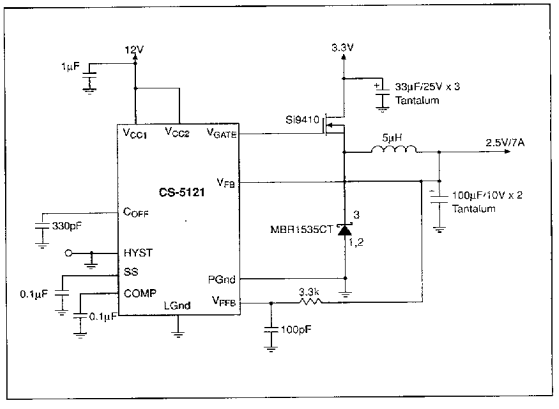


Figure 4: 3.3V to 2.5V/7A converter with 12V bias.

Package Specification

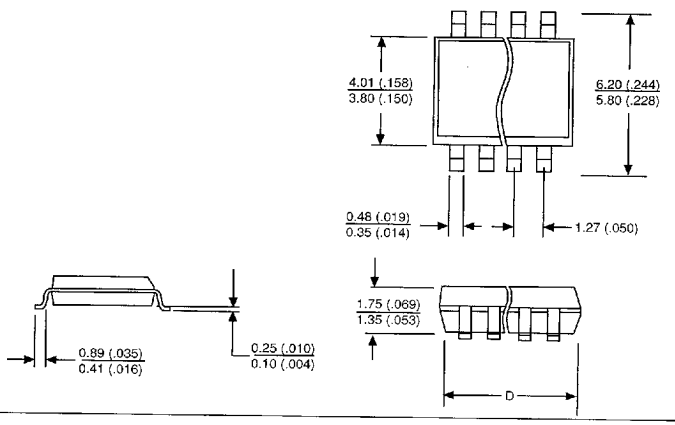
PACKAGE DIMENSIONS IN mm (INCHES)

Lead Count	D			
	Metric		English	
	Max	Min	Max	Min
16L SO Narrow	10.00	9.80	.394	.385
16L PDIP	19.18	18.92	.755	.745

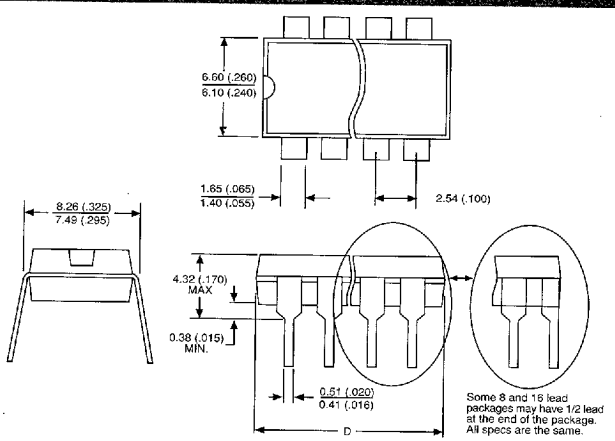
PACKAGE THERMAL DATA

Thermal Data		16L SO Narrow	16L PDIP	
$R_{\Theta JC}$	typ	28	42	°C/W
$R_{\Theta JA}$	typ	115	80	°C/W

Surface Mount Narrow Body (D); 150 mil wide



Plastic DIP (N); 300 mil wide



Ordering Information

Part Number	Description
CS-5121D16	16L SO Narrow
CS-5121N16	16L PDIP

Preliminary

This product is in the preproduction stages of the design process. The data sheet contains preliminary data. CSC reserves the right to make changes to the specifications without notice. Please contact CSC for the latest available information.