L64724
Satellite Receiver

Technical Manual

April 2000

LSI LOGIC®

Orner Number I14030

Document DB14-000032-03, April 2000
This document describes release B of LSI Logic Corporation's L64724 Satellite Receiver and will remain the official reference source for all revisions/releases of this product until rescinded by an update.

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Preface

This manual is the primary reference and technical manual for the L64724 Satellite Receiver. It contains a complete functional description for the L64724 and includes complete physical and electrical specifications.

Audience

This document assumes that you have some familiarity with digital satellite communications, microprocessors, and related support devices. The people who benefit from this book are:

- Engineers and managers who are evaluating the L64724 for possible use in a digital satellite receiver
- Engineers who are designing the L64724 into a digital satellite receiver

Organization

This document has the following chapters and appendices:

- Chapter 1, **Introduction**, defines the general characteristics and capabilities of the L64724 Satellite Receiver.
- Chapter 2, **L64724 Signal Definitions**, describes the characteristics of the L64724 signals that are used to interface with an external channel and microcontroller.
- Chapter 3, **L64724 Registers**, provides a summary of the registers in the L64724.
- Chapter 4, **Channel Interfaces and Data Control**, discusses the Input Channel and Output Channel interfaces and the circuitry that supports them.

- Chapter 5, **Demodulator Module Functional Description**, describes the operation of the Demodulator portion of the Satellite Receiver.
- Chapter 6, **Decoding Pipeline Synchronization**, discusses the mechanism for synchronizing the internal decoder modules to the incoming data stream.
- Chapter 7, **The FEC Decoder Pipeline**, describes the various logic modules that comprise the FEC decoding pipeline.
- Chapter 8, **L64724 Specifications**, describes the electrical and mechanical characteristics of the L64724.
- Appendix A, **Programming the L64724 Using the Serial Bus Protocol**, provides information on how to program the L64724 using its Serial Bus protocol.
- Appendix B, **L64724 Application Notes**, provides application information on connecting the L64724 in your circuit and programming it to meet your needs.
- Appendix C, **Programming the Serializer**, discusses the programming of the Serializer module.
- Appendix D, **A/D Converters**, discusses the Analog-to-Digital Converters used in the L64724 device.
- Appendix E, **L64724 On-chip Microcontroller**, summarizes the features of the L64724 on-chip microcontroller.

Related Publications

European Digital Video Broadcast Standard, DTVB 1110 Revision 7. This document is available from:

DVB Project Office
European Broadcasting Union
Ancienne Route, 17A
Grand Saconnex
Geneva, Switzerland

LSI Logic *L64002 MPEG-2 Audio/Video Decoder Technical Manual*, Document No. DB14-000004-00. Order No. I14011

LSI Logic *L64007 MPEG-2, DVB and TSAT Transport Demultiplexer Technical Manual,* Document No. DB14-000007-00.

Conventions Used in This Manual

The first time a word or phrase is defined in this manual, it is *italicized.*

The word *assert* means to drive a signal true or active. The word *deassert* means to drive a signal false or inactive.

Hexadecimal numbers are indicated by the prefix “0x” before the number—for example, 0x32CF. Binary numbers are indicated by the prefix “0b” before the number—for example, 0b0011.

Operations on registers are referred to using the binary numbers 0 and 1. Output signal levels are referred to by the designations HIGH and LOW. Example: Set the XCTR0 register bit to 1 to force the XCTR_OUT0 pin HIGH.

Chapter 1
Introduction

This chapter introduces the L64724 Satellite Receiver from LSI Logic. The L64724 is designed specifically to meet the needs of satellite broadcast digital TV and is compliant with the European digital video broadcast (DVB-S) standard and the technical specifications for DSS systems.

The sections in this chapter are:

- Section 1.1, “General Description”
- Section 1.2, “Typical Application”
- Section 1.3, “Features Summary”

1.1 General Description

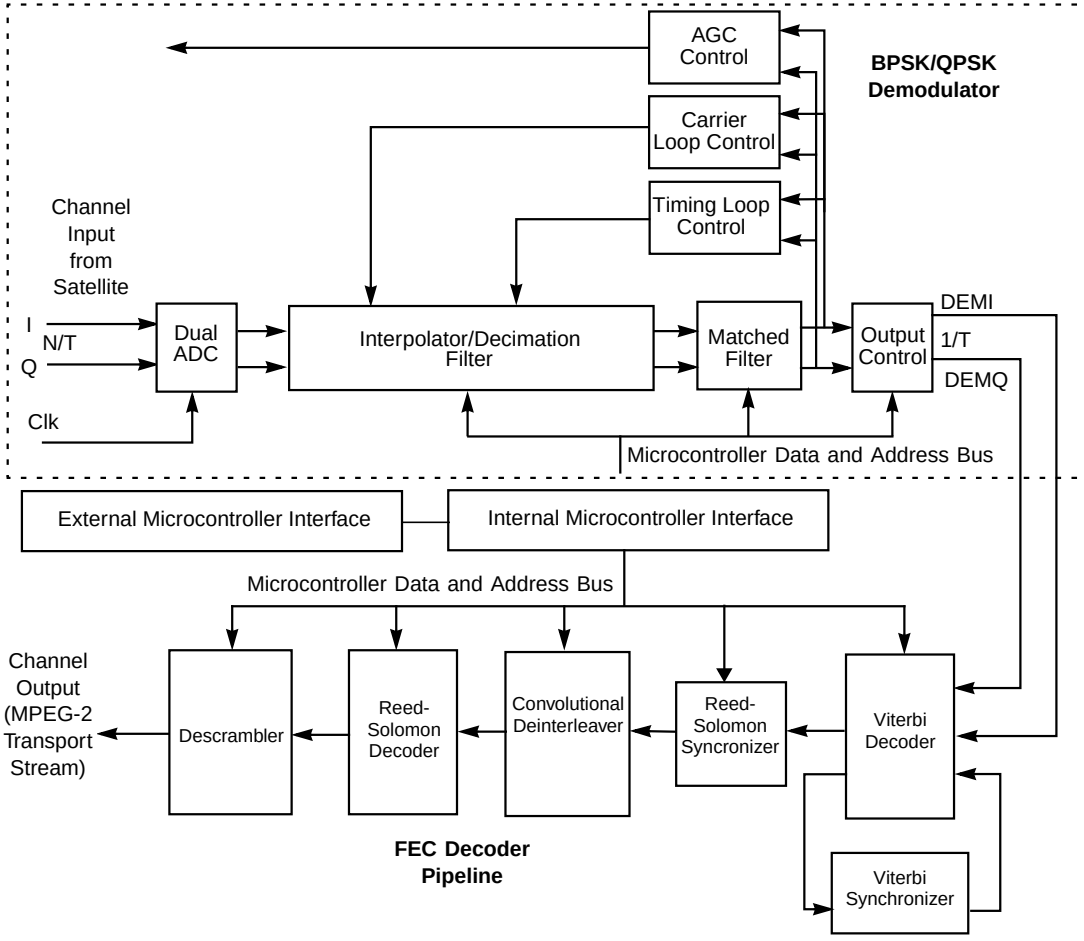
The L64724 Satellite Receiver contains two main blocks: a BPSK/QPSK Demodulator and a Concatenated FEC Decoder. The BPSK/QPSK module performs binary and quadrature phase-shift keying (BPSK/QPSK) demodulation, a method of extracting a digital signal from a phase-modulated analog signal.

The Concatenated FEC Decoder is a complete concatenated Forward Error Correction decoder that uses a Viterbi inner code and a Reed-Solomon outer code. The FEC decoding pipeline also contains all of the necessary synchronization, deinterleaving, and scrambling functions for a complete decoding solution. LSI Logic fabricates the L64724 using a 3.3-volt HCMOS process technology.

The L64724 provides maximum integration and flexibility for system designers at a minimum cost. It contains an on-chip dual 6-bit analog-to-digital converter (ADC) as well as an on-chip microcontroller. The microcontroller controls the tuner as well as acquisition and tracking,

which eliminates interaction from the main CPU, freeing up the CPU to perform other functions. The number of external components required to build a system is minimal because both clock and carrier loops are incorporated into the device. Figure 1.1 is a block diagram of the L64724.

Figure 1.1 L64724 Block Diagram

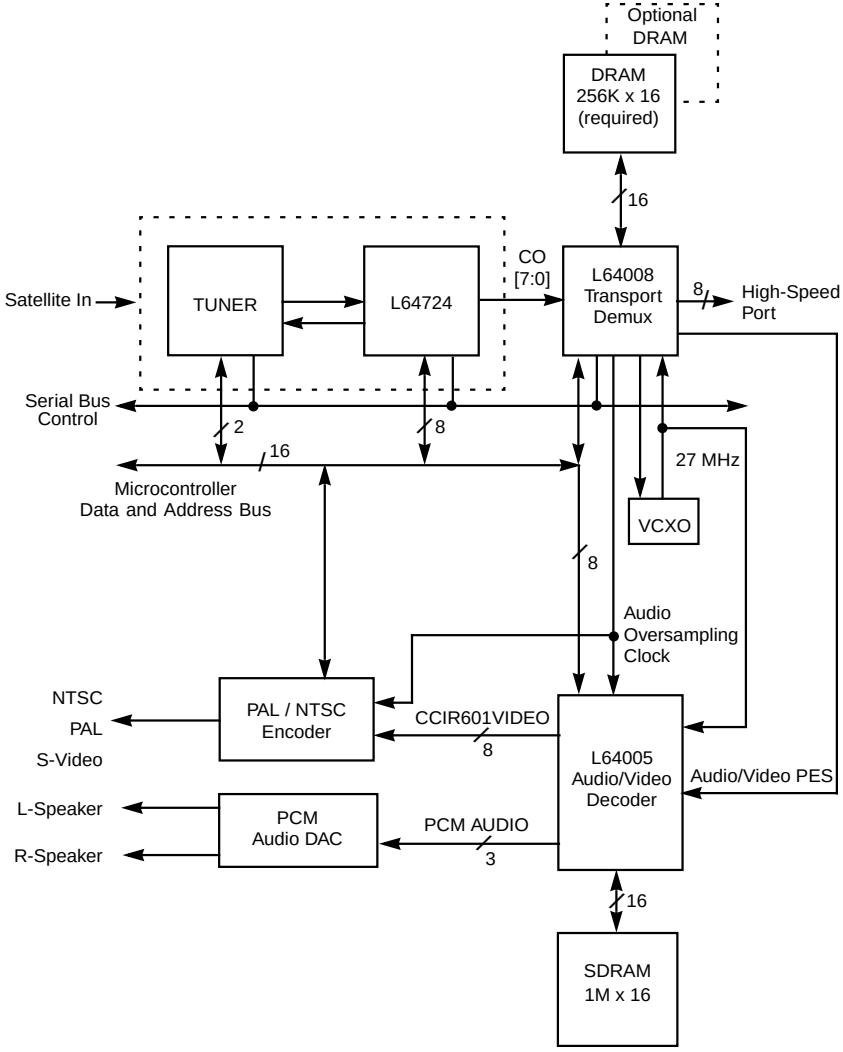


1.2 Typical Application

A typical application of the L64724 is satellite digital TV reception in accordance with the DVB 1110 Rev. 7 standard. Figure 1.2 shows the L64724 satellite receiver implemented in a typical satellite receiver set-top decoder box. Also shown are two other LSI Logic products:

- L64008 MPEG-2 CPU Transport Demultiplexer
- L64005 MPEG-2 Audio/Video Decoder

Figure 1.2 Set-Top Decoder Box Block Diagram



1.3 Features Summary

This section summarizes the main features of the L64724. Subsequent chapters describe these features in more detail.

- On-chip self-tuning microcontroller acquisition and tracking, eliminating microprocessor interaction, and simplifying software development.
- Supports DVB and DSS system specifications.
- BPSK/QPSK demodulation rates from 1 to 45 Mbaud.
- Matched filter (square root raised cosine filter with roll-off factor of 20% or 35%).
- Antialiasing filters for operation from 1 to 45 MBaud without switching external SAW filters or the need for low-pass filters.
- On-chip digital clock synchronization.
- On-chip digital carrier synchronization, featuring a frequency sweep capability for signal acquisition.
- Auto-acquisition demodulator mode and tuner control through an on-chip microcontroller.
- Integrated phase-locked loop (PLL) for clock synthesis, allowing the use of a fundamental mode crystal.
- Dual ADC.
- Fast channel switching mode.
- Power estimation for AGC control.
- Programmable Viterbi decoder module for the following rates: 1/2, 2/3, 3/4, 5/6, 6/7, and 7/8.
- (204/188), (146/130) Reed-Solomon decoder.
- Auto-synchronization for the Viterbi decoder.
- Programmable synchronization for the deinterleaver, Reed-Solomon decoder, and descrambler.
- Bit error monitoring for channel performance measurements.
- Deinterleaver (DVB and DSS).

- Serial host interface compatible with the LSI Logic Serial Control bus interface.
- Power-down mode.

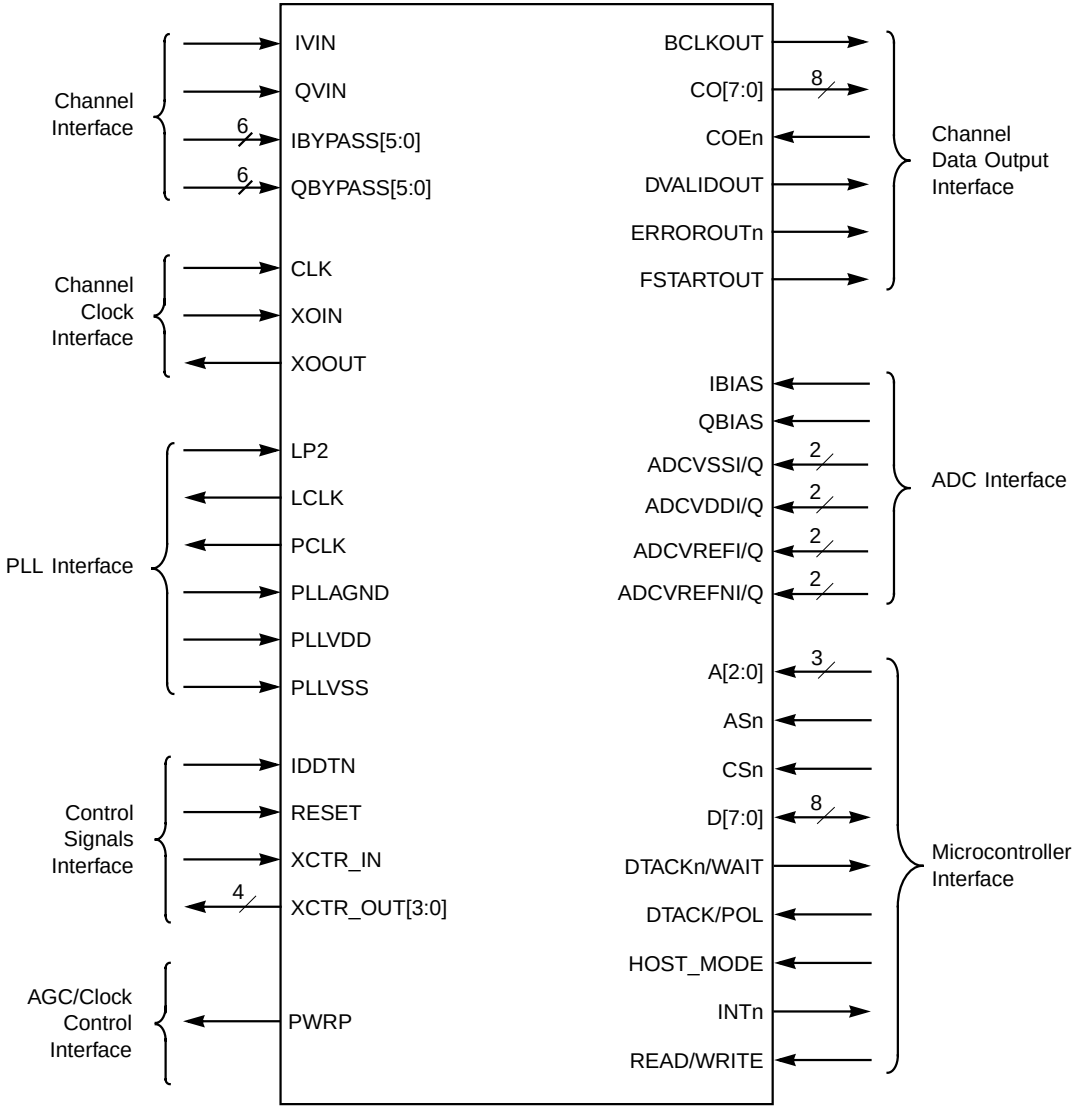
Chapter 2
L64724 Signal Definitions

This chapter describes the L64724 signals and is divided into the following sections:

- Section 2.1, “Channel Interface”
- Section 2.2, “Channel Clock Interface”
- Section 2.3, “Phase-Locked Loop (PLL) Interface”
- Section 2.4, “Control Signals Interface”
- Section 2.5, “AGC/Clock Control Interface”
- Section 2.6, “Channel Data Output Interface”
- Section 2.7, “Analog-to-Digital Converter (ADC) Interface”
- Section 2.8, “Microcontroller Interface”

Figure 2.1 shows the logic symbol for the L64724.

Figure 2.1 L64724 Logic Symbol



As shown in Figure 2.1, the L64724 has the following major interfaces:

- Channel
- Channel Clock
- PLL

- Control Signals
- AGC/Clock Control
- Channel Data Output
- ADC
- Microcontroller

The following signal descriptions are listed according to the major interface groups.

2.1 Channel Interface

The Channel interface is the input path to the L64724 satellite receiver. The two signals IVIN and QVIN are the I and Q streams from the satellite tuner circuit. The CLK signal strobes in the data signals.

IBYPASS[5:0] **Channel Data** **Input**
The IBYPASS[5:0] signals form the Digital Received I Channel data input bus, which supplies the I Stream to the L64724 when the ADC is bypassed.

IVIN **I Channel Data** **Input**
The IVIN signal is the Analog Received I Channel data input bus, which supplies the I Stream to the L64724.

QBYPASS[5:0]
Q Channel Data **Input**
The QBYPASS[5:0] signals form the Digital Received Q Channel data input bus, which supplies the Q Stream to the L64724 when the ADC is bypassed.

QVIN **Q Channel Data** **Input**
The QVIN signal is the Analog Received Q Channel data input bus, which supplies the Q Stream to the L64724.

2.2 Channel Clock Interface

The Channel Clock interface consists of the clock and crystal oscillator signals.

CLK **IVIN/QVIN Input Clock** **Input**
CLK is a positive, edge-triggered clock that strobes input data to the L64724.

XOIN **Crystal Oscillator In** **Input**
The XOIN pin is used for a crystal oscillator or external reference clock input.

XOOUT **Crystal Oscillator Out** **Output**
The XOOUT pin is the crystal oscillator output pin.

2.3 Phase-Locked Loop (PLL) Interface

The PLL circuitry multiplies the external clock signal by 2, 3, or 4 times the symbol rate, based on the Viterbi code rate.

LCLK **Decimated Clock Output** **Output**
The L64724 internal clock generation module generates the LCLK signal. LCLK is derived from CLK by dividing by the value of the CLK_DIV2 parameter (Group 4, APR 22 and 23).

LP2 **Input to VCO** **Input**
The LP2 signal is the input to the internal voltage-controlled oscillator. It is normally connected to the output of an external RC timing circuit.

PCLK **PLL Clock Output** **Output**
The L64724 internal PLL clock synthesis module generates the PCLK signal. The CLK signal drives the PLL. The PLL clock synthesis module can be configured to generate a PCLK rate that is appropriate for all data rates.

PLLAGND **PLL Analog Ground** **Input**
PLLAGND is the analog ground pin for the PLL module and is normally connected to the system ground plane.

PLLVDD **PLL Power** **Input**
PLLVDD is the power supply pin for the PLL module and is normally connected to the system power (V_{DD}) plane.

PLLVSS **PLL Ground** **Input**
PLLVSS is the ground pin for the PLL module and is normally connected to the system ground plane.

2.4 Control Signals Interface

The Control Signals Interface controls the operation of the L64724 and is not associated with any particular interface.

IDDTN **Test** **Input**
The IDDTN pin is an LSI Logic internal test pin. Set the IDDTN pin LOW for normal operation.

RESET **Reset** **Input**
RESET is an active-HIGH signal that, when asserted, resets all internal data paths. The RESET signal resets all of the Group 2 and Group 3 registers and some of the Group 5 register bits. Group 4 registers are unaffected. RESET timing is asynchronous to the device clocks. The RESET signal performs the same operation as the reset bits specified in the Group 4 APR 55 register. PCLK must be running for RESET to take effect.

XCTR_IN **Control Input** **Input**
The XCTR_IN pin is an external input control pin. It is sensed by reading the XCTR_IN bit (D6) in the Group 3, APR 6 register.

XCTR_OUT[3] **Control Output/Sync Status Flag** **Output**
The XCTR_OUT[3] pin indicates the synchronization status for one of three synchronization modules in the L64724. The modules are the Viterbi Decoder, Reed-Solomon Deinterleaver (DI/RS), and Descrambler. For any of the three synchronization outputs, the XCTR_OUT[3] signal, when asserted, indicates that synchronization has been achieved for the sync module chosen using the SSS[1:0] bits (Group 4, APR16). When deasserted, the signal indicates an out-of-synchronization condition.

XCTR_OUT[2:0]

Control Output **Output**

The XCTR_OUT[2:0] pins are external output control pins. They are set by programming the corresponding bits in the Group 4, APR 55 register. XCTR_OUT[1] can function as the Serial Clock (SCLK) signal, and XCTR_OUT[0] can function as the Serial Data (SDATA) signal.

2.5 AGC/Clock Control Interface

PWRP **Power Control** **Output**

The PWRP signal is the positive modulated output used for power control and can drive an external passive RC filter that feeds the tuner gain control stage.

2.6 Channel Data Output Interface

The Channel Data Output Interface is the output path from the L64724. It is typically connected to the input of the transport demultiplexer in a set-top decoder application.

BCLKOUT **Byte Clock Out** **Output**

The BCLKOUT output signal is a strobe that indicates valid data bytes on the CO[7:0] bus when the L64724 is in Parallel Channel Output mode. The BCLKOUT signal cycles once every valid output data byte and is used by the transport demultiplexer to latch output data from the L64724 at the BCLKOUT rate. The BCLKOUT signal must be disregarded in Serial Channel Output mode.

CO[7:0] **Channel Data Out** **Output**

The CO[7:0] signals form the decoded output data port. When the OF bit is 1 (Group 4, APR17), the L64724 operates in the Parallel Channel Output mode. In this mode, the L64724 outputs the channel data as 8-bit wide parallel data on the CO[7:0] signals. In Serial Channel Output mode (OF = 0) the L64724 outputs the channel data as serial data on CO[0]. The data is latched on every bit clock cycle. The chronological ordering in Serial Channel output mode is MSB oldest, LSB newest.

COEn **Channel Output Enable** **Input**
When asserted, the COEn signal enables the ERROROUTn, CO[7:0], DVALIDOUT, BCLKOUT, and FSTARTOUT pins. Operation of the receiver continues regardless of the state of the COEn signal.

DVALIDOUT **Valid Data Out** **Output**
The DVALIDOUT signal indicates that the CO[7:0] signals contain the corrected channel data. New data is valid on the CO[7:0] signals when the DVALIDOUT signal is asserted. DVALIDOUT is not asserted during the propagated check and GAP bytes. The DVALIDOUT signal is deasserted after the FEC_RST register bit (Group 4, APR 55) is set to a 1.

ERROROUTn **Error Detection Flag** **Output**
The L64724 asserts the ERROROUTn pin (LOW) to flag uncorrectable errors. The L64724 asserts the ERROROUTn signal at the beginning of any frame that contains an uncorrectable error, and deasserts it at the end of the frame if the error condition is removed. The ERROROUTn signal is exactly aligned with the output data stream and is asserted after the FEC_RST register bit (Group 4, APR 55) is set to a 1. The Errorout_Invert bit (Group 4, APR 31), when set to 1, changes the active state of the ERROROUTn signal from active-LOW to active-HIGH.

FSTARTOUT **Frame Start Output** **Output**
The L64724 asserts the FSTARTOUT signal during the first bit of every frame with valid data in Serial Channel Output mode and during the first byte in Parallel Channel Output mode. FSTARTOUT is valid only when the DVALIDOUT signal is asserted. The FSTARTOUT signal is deasserted after the FEC_RST register bit (Group 4, APR 55) is set to a 1.

2.7 Analog-to-Digital Converter (ADC) Interface

The ADC module converts the incoming IVIN and QVIN signals into an internal 6-bit digital representation for processing. The following pins support the ADC module.

ADCVDDI/Q **ADC Power** **Input**
ADCVDDI/Q are the analog power supply pins for the ADC module and are normally connected to the system power (V_{DD}) plane.

ADCVREFI **ADC I Reference** **Input**
This pin supplies VDD to the internal reference generator.

ADCVREFNI **ADC Negative I Reference** **Input**
This pin supplies VREFN to the internal ADC cells.

ADCVREFQ **ADC Q Reference** **Input**
This pin is not used and should be left unconnected. Any other connection will cause unpredictable and unreliable operation of the device.

ADCREFNQ **ADC Negative Q Reference** **Input**
This pin supplies the ground to the internal ADC cell.

ADCVSSI/Q **ADC Analog Ground** **Input**
ADCVSSI/Q are the analog ground pins for the ADC module and are normally connected to the system ground plane.

IBIAS **Current Bias I** **Input**
The IBIAS pin supplies the current bias for the ADCs.

QBIAS **Current Bias Q** **Input**
This pin is used by LSI Logic for internal purposes, and should be connected as shown in Figure D.2. Any other connection will cause unpredictable and unreliable operation of the device.

2.8 Microcontroller Interface

The Microcontroller Interface connects the L64724 to a microcontroller such as the 64008.

A[2:0] **Address** **Input**
The A[2:0] signals form the receiver address bus. The address bus is used in conjunction with an 8-bit data bus D[7:0], a read/write strobe (READ/WRITE), a chip select strobe (CS), and an address strobe (AS) to select, read, and write internal registers.

ASn **Address Strobe** **Input**

The ASn signal is an active-LOW address strobe input. The L64724 latches the address on the A[2:0] signals on the falling edge of the ASn signal.

CSn **Chip Select** **Input**

The CSn signal is an active-LOW chip select strobe input. During a read cycle, the microcontroller must assert CSn (LOW) to access the on-chip data registers. The microcontroller must latch the data from the L64724 on the rising edge of CSn. During a write cycle, CSn must be asserted prior to data being valid from the microcontroller to the L64724. After the data has met the minimum setup time, the microcontroller deasserts CSn (HIGH) to strobe the data. There is a minimum write time to allow for internal synchronization. Setup and hold times are measured with respect to the falling edge of CSn.

D[7:0] **Data** **Bidirectional**

The D[7:0] signals form the bidirectional data bus, which is an input data bus when data is written to the L64724 chip and a data output bus when the L64724 chip is read in Parallel Host Interface mode[1] (HOST_MODE pin HIGH). The data lines are 3-stated when not being read or written. When Serial Host Interface mode is selected (HOST_MODE pin LOW), D[0] is used as the Serial Clock (SCLK) signal to synchronize the transfer of serial data on the Serial Data (SDATA) pin. In Serial Host interface mode, XCTR_OUT[1] functions as SDATA, D[1] is used as the SDATA signal to transfer serial data, and D[3:2] are used as the two LSBs of the L64724 slave address.

DTACK/POL **Data Acknowledge/Wait Polarity** **Input**

The DTACK/POL signal determines the polarity of the Data Acknowledge/Wait Signal. When the DTACK/POL signal is LOW, DTACKn/WAIT is active-LOW. When the DTACK/POL signal is HIGH, the DTACKn/WAIT signal is active-HIGH.

1. Serial Mode is the recommended interface mode. LSI Logic does not recommend parallel mode for new designs.

DTACKn/WAIT

Data Acknowledge/Wait **Output**

The DTACKn/WAIT signal is an output indicating that the transaction on the D[7:0] bus has been completed. It is active-LOW when DTACK/POL is LOW and active-HIGH when DTACK/POL is HIGH. Do not base the chip programming on this signal.

HOST_MODE **Serial or Parallel Host Interface Select** **Input**

When the HOST_MODE signal is deasserted, it selects the Serial Host Interface mode. When it is asserted, it selects the Parallel Host Interface mode[1].

INTn **Interrupt** **Output**

The L64724 asserts the INTn signal (LOW) when an internal unmasked interrupt flag is set. The INTn signal remains asserted as long as the interrupt condition persists and the interrupt flag is not masked.

READ/WRITE **Read/Write Strobe** **Input**

The microcontroller asserts the READ/WRITE signal (HIGH) to indicate that the current transaction is a read from the L64724, and deasserts it (LOW) to indicate that it is a write to the L64724.

1. Serial Mode is the recommended interface mode. LSI Logic does not recommend parallel mode for new designs.

Chapter 3
L64724 Registers

This chapter discusses the L64724 internal registers. It also provides a description of the internal memory mapping and describes how to access the registers from the system interface. This chapter is intended primarily for system programmers who are developing software drivers and contains the following sections:

- Section 3.1, “L64724 Register Overview”
- Section 3.2, “Reset and How it Affects Registers”
- Section 3.3, “Groups 0 and 1: Address Pointer Register”
- Section 3.4, “Group 2: System Mode and System Status Registers”
- Section 3.5, “Group 3: Status Registers”
- Section 3.6, “Group 4: Configuration Registers”
- Section 3.7, “Group 5: Self-Tuning Microcontroller Registers”
- Section 3.8, “Group 6: Reserved (Internal Use Only)”
- Section 3.9, “Group 7: Arbiter Control Register”
- Section 3.10, “Reset Effect on Register Bits”
- Section 3.11, “Internal Data Path Reset Effects”

This chapter provides complete information on how to use these registers, but does not provide information on how to program the registers for a specific application. See Appendix B, "L64724 Application Notes," for some programming examples.

3.1 L64724 Register Overview

The L64724 registers and memory resources are divided into eight groups, Group 0 through Group 7.

- Groups 0 and 1 contain the Address Pointer Register. This pointer is used to address the registers in Groups 2, 3, and 4.
- Group 2 addresses the System Mode Register when written and the System Status Register when read.
- Group 3 contains the Status Registers.
- Group 4 contains the Configuration Registers.
- Group 5 contains the program space for the on-board microprocessor.
- Group 6 is reserved for internal use only.
- Group 7 is used for Arbiter control.

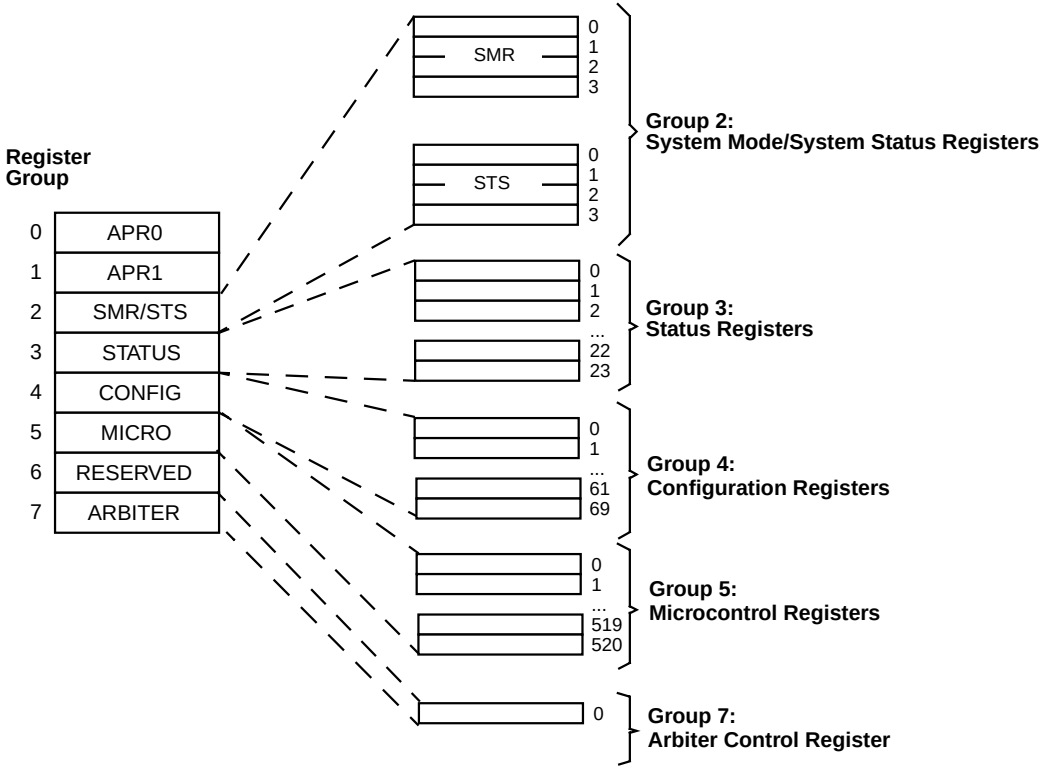
Table 3.1 shows the complete Register Map for the L64724 Satellite Receiver.

Table 3.1 Register Overview

Group	Name	Function	Page
0	APR0	Address Pointer Register, LSB	3-8
1	APR1	Address Pointer Register, MSB	3-8
2	SMR/STS	System Mode/System Status Registers	3-9
3	STATUS	Status Registers	3-23
4	CONFIG	Configuration Registers	3-33
5	MICRO	Microcontrol Registers	3-77
6	RESERVED	Reserved	3-81
7	ARBITER	Arbiter Control Register	3-81

Figure 3.1 shows a simplified diagram of the L64724 register groups.

Figure 3.1 Register File Structure



To reduce the number of memory locations occupied by the L64724 in microprocessor memory, the L64724 uses a pair of Address Pointer Registers (APR0 and APR1). The Address Pointer Registers have an auto-increment feature that simplifies the initialization procedure and reduces the number of memory cycles needed to read or write the registers. The address pointer and auto-increment features are used whenever you access Groups 2, 3, and 4. The L64724 automatically points to the next register entry after you complete an access to one of the three groups. When writing or reading register groups 3 and 4, it is easier to initially set APR0 and APR1 to zero and let the auto-increment mechanism step through all the locations within the group.

For example, to access the PLL_N configuration register 0 (Group 4, APR 0), first set APR0 and APR1 to 0x00 by writing a zero to addresses 0 and 1, then set A[2:0] to 0b100. The value of 0b100 for address A[2:0] selects Group 4.

The L64724 has an internal 8-bit architecture. Most registers are 8 bits wide, while some are either 16 or 24 bits wide. All registers are memory-mapped to the system with 8-bit resolution. When you are accessing a register that is wider than 8 bits, you must read or write two or three 8-bit sections. The sections are divided into the least-significant byte (LSB), the middle-significant byte (MB), and the most-significant byte (MSB). Each 8-bit section is assigned a specific address, and requires an individual memory cycle during programming.

3.1.1 Parallel Host Interface Mode[1]

The L64724 is addressable through either a serial or a parallel host interface. The interface used depends on the state of the HOST_MODE input pin when the L64724 is reset. The interface is selected as follows:

- HOST_MODE pin HIGH = Parallel Host Interface mode
- HOST_MODE pin LOW = Serial Host Interface mode

The interface mode cannot be changed once the part is in operation. The following paragraphs show the steps required to read and write the L64724 registers when you are in Parallel Host Interface mode. Serial Host Interface mode is discussed in Section 3.1.2, “Serial Host Interface Mode,” page 3-6, and Appendix A, "Programming the L64724 Using the Serial Bus Protocol,".

Figure 3.2 through Figure 3.5 demonstrate read and write operation through the parallel microprocessor interface.

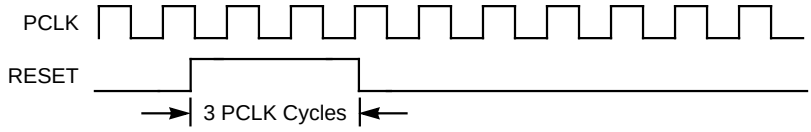
> Note: The PCLK signal must operate for the user to be able to access Groups 2 and 3. Group 4, however, can be programmed in the absence of PCLK.

To read and write registers using the parallel interface mode, follow these steps:

1. Issue a hard reset to the L64724 for three clock cycles, as shown in Figure 3.2. Wait for the wake-up time (t_{WK}), which is 280 PCLK cycles, before continuing.

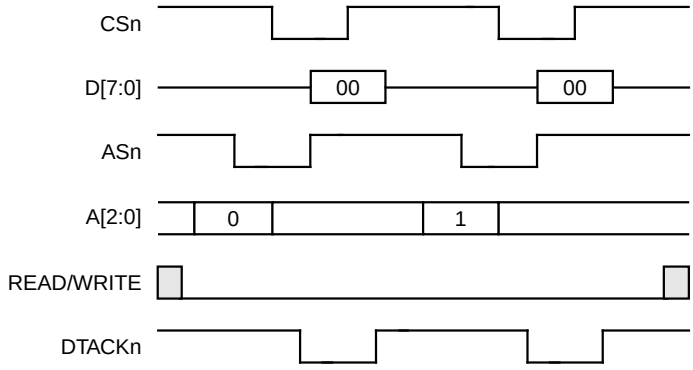
1. Serial Mode is the recommended interface mode. LSI Logic does not recommend parallel mode for new designs.

Figure 3.2 Issue a Hard Reset



2. Set the APR0 and APR1 registers to zero by writing a zero to Groups 0 and 1. See Figure 3.3.

Figure 3.3 Initialize APR0 and APR1 to Zero

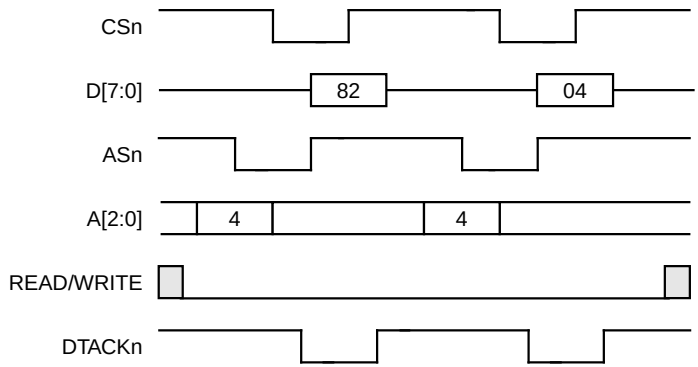


3. Write to the Configuration registers in Group 4.

   Because the APRs were both initialized to zero, the first location written in Group 4 is location zero, the second location written is 1, and so on. As long as the address lines A[2:0] contain the value 4, the auto-increment mechanism advances to the next location in Group 4 with every low-to-high transition of CSn.

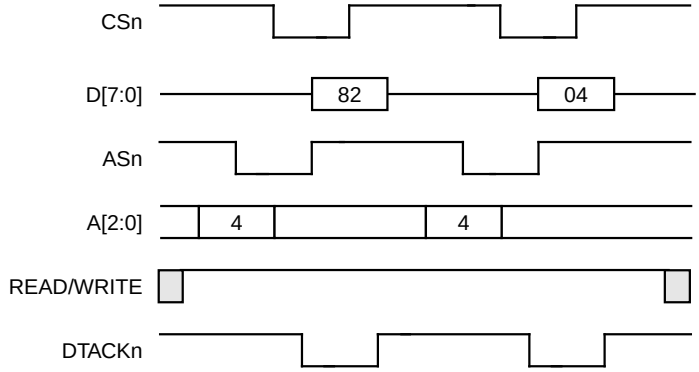
Figure 3.4 and Figure 3.5 show the first two writes to Group 4. The 0x82 and 0x04 values shown for D[7:0] are typical values for locations 0 and 1, respectively. See Section 3.6, “Group 4: Configuration Registers,” page 3-33, for more details on the data values.

Figure 3.4 Write Locations 0 and 1 in Group 4



4. You can also choose to read back the Group 4 Configuration registers, as demonstrated in Figure 3.5. Just set APR0 and APR1 to zero (see Figure 3.3) and step through the configuration locations using a value of 4 for A[2:0]. The READ/WRITE signal is asserted, and the auto-increment mechanism selects location 0, then location 1, and so on.

Figure 3.5 Read Back Group 4



3.1.2 Serial Host Interface Mode

Setting the HOST_MODE pin LOW during reset places the L64724 in Serial Host Interface mode. When the L64724 is addressed using the serial interface, it must first be programmed with a 2-bit slave address before any other read or write cycles. Appendix A, "Programming the L64724 Using the Serial Bus Protocol," contains a detailed description of the protocol used when programming the L64724 in Serial Host Interface mode.

3.2 Reset and How it Affects Registers

There are three separate resets available on the L64724, as follows:

- The hardware RESET pin
- The DEMOD_RST register bit (Group 4, APR 55, bit 1)
- The FEC_RST register bit (Group 4, APR 55, bit 0).

Each reset affects the registers differently, as follows:

- Toggling the hardware RESET pin resets all of the Group 2 and Group 3 registers and some of the Group 4 registers. Registers in Group 4 are unaffected.
- Setting the DEMOD_RST bit in the External Output Control bits and Reset Register (Group 4, APR 55, bit 1) affects only the bits in Group 3 registers that are directly concerned with the demodulator circuitry.
- Setting the FEC_RST bit in the External Output Control bits and Reset Register (Group 4, APR 55, bit 0) resets the System Mode/Status registers (Group 2) and any bits in Group 3 registers that are directly concerned with the FEC circuitry.

Registers in Group 4 are unaffected by any of the reset operations. The contents of the Group 4 registers are random immediately after power-up, and retain their last known value after any of the three reset operations listed above.

The following steps should be followed when resetting the L64724:

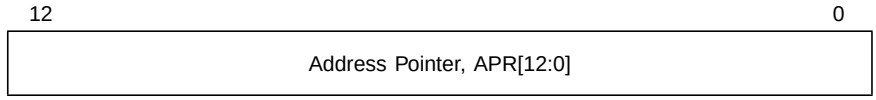
1. Issue an active-HIGH reset pulse to the RESET pin. The reset pulse width must be in accordance with the parameter t_{RWH} (see Figure 8.4).
2. Program the Configuration (Group 4) registers to their proper values.
3. Issue a soft reset by setting the DEMOD_RST bit and the FEC_RST bits to a 1 (Group 4, APR 55). The bits are self-resetting, and do not have to be cleared.
4. After the RESET pin has been deasserted (LOW), wait the wake-up time amount specified by the parameter t_{WK} (see Figure 8.4).

5. The L64724 is now in the acquisition mode. When data is applied at the L64724 input, it is ready to start demodulating and decoding.

For details on how reset affects the various register bits, see Section 3.10, “Reset Effect on Register Bits,” page 3-82.

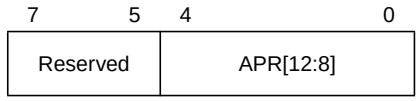
3.3 Groups 0 and 1: Address Pointer Register

The Address Pointer Register (APR) is a 13-bit R/W register that points to the registers in Groups 2, 3, and 4. It is accessed when A[2:0] = 0b000 and 0b001. Before accessing a register location from Group 2, 3, or 4, you must initialize the APR contents with the address of the first register entry that you are going to read or write. The APR automatically increments after reading or writing a byte within a Group 2 (A[2:0] = 0b010), Group 3 (A[2:0] = 0b011) Group 4 (A[2:0] = 0b100) or Group 5 (A[2:0] = 0b101) register.

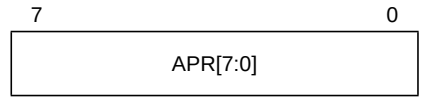


Two consecutive writes are required to load the complete APR. The first write is to Group 0 to load the eight LSBs, the second to Group 1 to load the five MSBs. The APR can be read as well as written.

Group 1, Data Bus D[7:0]



Group 0, Data Bus D[7:0]



The reserved bits in these registers are for LSI internal test procedures and future expansion and should always be set to zero.

To access a Group 2, 3, or 4 register:

1. Initialize the APR with the address of the first register you want to access within a particular register group. You should write both bytes of the APR.
2. Read or write the first register within the register group you are accessing using the appropriate register group address. The addresses are:

   Group 2—0b010

   Group 3—0b011

   Group 4—0b100

   Group 5—0b101
3. If the register is a 16-bit register, just perform another read or write to the group register address to access the second byte. The APR increments automatically.

When you are through, the APR automatically points to the next register in the group.

3.4 Group 2: System Mode and System Status Registers

Group 2 contains two 32-bit registers, the System Mode Register (SMR) and the System Status Register (STS). The System Mode Register is accessed by writing the Group 2 address, and the System Status Register is accessed by reading the Group 2 address. Because the L64724 has an 8-bit architecture, each 32-bit register is accessed as four 8-bit registers.

The microprocessor accesses these registers by setting A[2:0] = 0b010. It can access these registers at any point during Satellite Receiver operation without interrupting the internal processing unit.

Note: The phase-locked loop must be locked (PCLK running) for the status signals to be valid.

3.4.1 System Mode Register (SMR)

The 32-bit System Mode Register (SMR) is a write-only register that allows the external microprocessor to control the L64724. Table 3.2 shows the SMR map.

Table 3.2 Group 2 System Mode Register Map (Write-Only)

APR	D7	D6	D5	D4	D3	D2	D1	D0
0	SMR[7:0]							
	VBER_IE	S3_LS_IE	S3_S_IE	S2_LS_IE	S2_S_IE	S1_LS_IE	S1_S_IE	Reserved
1	SMR[15:8]							
	CLK_LK_IE	CLK_LLK_IE	CP_LK_IE	CP_LLK_IE	Reserved = 0		CL_FS_LL_IE	CL_FS_UL_IE
2	SMR[23:16]							
	Reserved						TL_FS_LL_IE	TL_FS_UL_IE
3	SMR[31:24]							
	uC_IE7	uC_IE6	uC_IE5	uC_IE4	uC_IE3	uC_IE2	uC_IE1	uC_IE0

The bits in the register are allocated as follows:

- SMR[7:0] enable FEC module interrupts.
- SMR[23:8] enable the Demodulator interrupts.
- SMR[31:24] enable interrupts for the on-chip microcontroller.

Because the SMR is arranged as four 8-bit registers, the microprocessor must perform four consecutive writes to the register address. The lower eight bits of the APR must be set to 0x00 in order to access bits SMR[7:0]. The eight LSBs of the SMR are accessed first. The auto-increment mechanism toggles the Address Pointer Register after the first access so that the next write goes to the SMR[15:8] bits.

If you want to access the SMR starting with bytes 1, 2, or 3, set the APR equal to 0b01, 0b10, or 0b11, respectively.

The following register diagram shows the bit organization of SMR[7:0]. Descriptions of the bits follow the register diagram. The L64724 clears all bits in the SMR to zero after a software or hardware reset.

APR	D7	D6	D5	D4	D3	D2	D1	D0
0	SMR[7:0]							
	VBER_IE	S3_LS_IE	S3_S_IE	S2_LS_IE	S2_S_IE	S1_LS_IE	S1_S_IE	Reserved

VBER_IE **Viterbi Bit Error Rate Monitor Interrupt Enable** **7**

The microprocessor sets the VBER_IE bit to enable an interrupt when the Viterbi decoder reaches the period specified by VMDC2 (the period over which the Viterbi bit errors are counted). The L64724 always sets the VBER bit in the STS register when this condition occurs.

VBER_IE	Definition
0	Disable Interrupt for Viterbi BER count
1	Enable Interrupt for Viterbi BER count

S3_LS_IE **Stage 3 Loss of Synchronization Interrupt Enable** **6**

The microprocessor sets the S3_LS_IE bit to enable an interrupt when Descrambler synchronization is lost. S3_LS_IE is not used in DSS mode.

S3_LS_IE	Definition
0	Disable Interrupt for Stage 3 Loss of Synchronization
1	Enable Interrupt for Stage 3 Loss of Synchronization

S3_S_IE **Stage 3 Synchronization Interrupt Enable** **5**

The microprocessor sets the S3_S_IE bit to enable an interrupt when Descrambler synchronization is established. S3_S_IE is not used in DSS mode.

S3_S_IE	Definition
0	Disable Interrupt for Stage 3 Synchronization
1	Enable Interrupt for Stage 3 Synchronization

S2_LS_IE **Stage 2 Loss of Synchronization Interrupt Enable 4**
The microprocessor sets the S2_LS_IE bit to enable an interrupt when Deinterleaver/Reed-Solomon Decoder synchronization is lost.

S2_LS_IE	Definition
0	Disable Interrupt for Stage 2 Loss of Synchronization
1	Enable Interrupt for Stage 2 Loss of Synchronization

S2_S_IE **Stage 2 Synchronization Interrupt Enable 3**
The microprocessor sets the S2_S_IE bit to enable an interrupt when Deinterleaver/Reed-Solomon Decoder synchronization is established.

S2_S_IE	Definition
0	Disable Stage 2 Synchronization Interrupt
1	Enable Stage 2 Synchronization Interrupt

S1_LS_IE **Stage 1 Loss of Synchronization Interrupt Enable 2**
The microprocessor sets the S1_LS_IE bit to enable an interrupt when Viterbi Decoder synchronization is lost.

S1_LS_IE	Definition
0	Disable Stage 1 Loss of Synchronization Interrupt
1	Enable Stage 1 Loss of Synchronization Interrupt

S1_S_IE **Stage 1 Synchronization Interrupt Enable 1**
The microprocessor sets S1_S_IE to enable an interrupt when Viterbi Decoder synchronization is established.

S1_S_IE	Definition
0	Disable Stage 1 Synchronization Interrupt
1	Enable Stage 1 Synchronization Interrupt

Reserved **Reserved 0**
The Reserved bit is for LSI Logic internal use only and should always be cleared to 0.

The following register diagram shows the bit organization of SMR[15:8]. Descriptions of the bits follow the register diagram. The L64724 sets all the bits in SMR[15:8] to 0 after a software or a hardware reset.

APR	D7	D6	D5	D4	D3	D2	D1	D0
1	SMR[15:8]							
	CLK_LK_IE	CLK_LLK_IE	CP_LK_IE	CP_LLK_IE	Reserved = 0		CL_FS_LL_IE	CL_FS_UL_IE

CLK_LK_IE **Timing Lock Detect Interrupt Enable** **15**

The microcontroller sets the CLK_LK_IE bit to enable an interrupt when timing lock is detected. The L64724 always sets the CLK_LK bit in the STS register when this condition occurs.

CLK_LK_IE	Definition
0	Disable Interrupt for Timing Lock Detect
1	Enable Interrupt for Timing Lock Detect

CLK_LLK_IE **Timing Lock Lost Detect Interrupt Enable** **14**

The microcontroller sets the CLK_LLK_IE bit to enable an interrupt when timing lock loss is detected. The L64724 always sets the CLK_LLK bit in the STS register when this condition occurs.

CLK_LLK_IE	Definition
0	Disable Interrupt for Timing Lock Lost Detect
1	Enable Interrupt for Timing Lock Lost Detect

CP_LK_IE **Carrier Phase Lock Detect Interrupt Enable** **13**

The microprocessor sets the CP_LK_IE bit to enable an interrupt when Carrier Phase Lock is detected (CAR_LC = 1 in Group 3, APR11). The L64724 always sets the CP_LK bit in the STS register when this condition occurs.

CP_LK_IE	Definition
0	Disable Interrupt for Carrier Phase Lock Detect
1	Enable Interrupt for Carrier Phase Lock Detect

CP_LLK_IE **Carrier Phase Lock Lost Detect Interrupt Enable** **12**

The microprocessor sets the CP_LLK_IE bit to enable an interrupt when Carrier Phase Lock Loss is detected

(CAR_LC = 0 in Group 3, APR11). The L64724 always sets the CP_LLK bit in the STS register when this condition occurs.

CP_LLK_IE	Definition
0	Disable Interrupt for Carrier Phase Lock Loss Detect
1	Enable Interrupt for Carrier Phase Lock Loss Detect

Reserved **Reserved** **[11:10]**

The Reserved bits are for LSI Logic internal use only and must always be cleared to 0.

CL_FS_LL_IE

Frequency Sweep Lower Limit Reached Interrupt Enable **9**

The microprocessor sets the CL_FS_LL_IE bit to enable an interrupt when the Carrier Loop Frequency Sweep has reached its lower limit. The L64724 always sets the CL_FS_LL bit in the STS register when this condition occurs.

CL_FS_LL_IE	Definition
0	Disable Interrupt for Frequency Sweep Lower Limit Reached Detect
1	Enable Interrupt for Frequency Sweep Lower Limit Reached Detect

CL_FS_UL_IE

Frequency Sweep Upper Limit Reached Interrupt Enable **8**

The microprocessor sets the CL_FS_UL_IE bit to enable an interrupt when the Carrier Loop Frequency Sweep has reached its upper limit. The L64724 always sets the CL_FS_UL bit in the STS register when this condition occurs.

CL_FS_UL_IE	Definition
0	Disable Interrupt for Frequency Sweep Upper Limit Reached
1	Enable Interrupt for Frequency Sweep Upper Limit Reached Detect

The following register diagram shows the bit organization of SMR[23:16]. Descriptions of the fields follow the register diagram. The L64724 sets all the bits in SMR[23:16] to 0 after a software or a hardware reset.

APR	D7	D6	D5	D4	D3	D2	D1	D0
2	SMR[23:16]							
	Reserved						TL_FS_LL_IE	TL_FS_UL_IE

Reserved **Reserved** **[23:18]**

The Reserved bits are for LSI Logic internal use only and must always be cleared to 0.

TL_FS_LL_IE **Frequency Sweep Lower Limit Reached Interrupt Enable** **17**

The microprocessor sets the TL_FS_LL_IE bit to enable an interrupt when the Timing Loop Frequency Sweep has reached its lower limit. The L64724 always sets the TL_FS_LL bit in the STS register when this condition occurs.

TL_FS_LL_IE	Definition
0	Disable Interrupt for Frequency Sweep Lower Limit Reached Detect
1	Enable Interrupt for Frequency Sweep Lower Limit Reached Detect

TL_FS_UL_IE **Frequency Sweep Upper Limit Reached Interrupt Enable** **16**

The microprocessor sets the TL_FS_UL_IE bit to enable an interrupt when the Frequency Sweep has reached its upper limit. The L64724 always sets the TL_FS_UL bit in the STS register when this condition occurs.

TL_FS_UL_IE	Definition
0	Disable Interrupt for Frequency Sweep Upper Limit Reached
1	Enable Interrupt for Frequency Sweep Upper Limit Reached Detect

The following register diagram shows the bit organization of SMR[31:24]. Descriptions of the bits follow the register diagram. The L64724 clears all the bits in SMR[31:24] to 0 after a software or a hardware reset.

APR	D7	D6	D5	D4	D3	D2	D1	D0
3	SMR[31:24]							
	uC_IE7	uC_IE6	uC_IE5	uC_IE4	uC_IE3	uC_IE2	uC_IE1	uC_IE0

uC_IE7 **uC Interrupt 7 Enable** **31**

The microprocessor sets the uC_IE7 bit to enable interrupt 7 from the on-chip microcontroller. The microcode can define the meaning of interrupt 7; therefore this is a user-programmable interrupt.

uC_IE6 **uC Interrupt 6 Enable** **30**

The microprocessor sets the uC_IE6 bit to enable interrupt 6 from the on-chip microcontroller. The microcode can define the meaning of interrupt 6; therefore, this is a user-programmable interrupt.

uC_IE5 **uC Interrupt 5 Enable** **29**

The microprocessor sets the uC_IE5 bit to enable interrupt 5 from the on-chip microcontroller. The microcode can define the meaning of interrupt 5; therefore, this is a user-programmable interrupt.

uC_IE4 **uC Interrupt 4 Enable** **28**

The microprocessor sets the uC_IE4 bit to enable interrupt 4 from the on-chip microcontroller. The microcode can define the meaning of interrupt 4; therefore, this is a user-programmable interrupt.

uC_IE3 **uC Interrupt 3 Enable** **27**

The microprocessor sets the uC_IE3 bit to enable interrupt 3 from the on-chip microcontroller. The microcode can define the meaning of interrupt 3; therefore, this is a user-programmable interrupt.

uC_IE2 **uC Interrupt 2 Enable** **26**

The microprocessor sets the uC_IE2 bit to enable interrupt 2 from the on-chip microcontroller. The microcode can define the meaning of interrupt 2; therefore, this is a user-programmable interrupt.

uC_IE1 **uC Interrupt 1 Enable** **25**

The microprocessor sets the uC_IE1 bit to enable interrupt 1 from the on-chip microcontroller. The microcode can define the meaning of interrupt 1; therefore, this is a user-programmable interrupt.

uC_IE0 **uC Interrupt 0 Enable** **24**

The microprocessor sets the uC_IE0 bit to enable interrupt 0 from the on-chip microcontroller. The microcode can define the meaning of interrupt 0; therefore, this is a user-programmable interrupt.

3.4.2 System Status Register (STS)

The STS Register is a read-only register that provides the external microprocessor access to L64724 status information. Table 3.3 shows the STS map.

Table 3.3 Group 2 System Status Register Map (Read-Only)

APR	D7	D6	D5	D4	D3	D2	D1	D0
0	STS[7:0]							
	VBER	S3_LS	S3_S	S2_LS	S2_S	S1_LS	S1_S	Reserved
1	STS[15:8]							
	CLK_LK	CLK_LLK	CP_LK	CP_LLK	Set to 0		CL_FS_LL	CL_FS_UL
2	STS[23:16]							
	Reserved						TL_CL_FS_LL	TL_CL_FS_UL
3	STS[31:24]							
	uC_I7	uC_I6	uC_I5	uC_I4	uC_I3	uC_I2	uC_I1	uC_I0

The STS register bits indicate the event that generated an internal interrupt condition. The interrupt status bits are set regardless of the enable interrupt bits in the SMR Register. The internal status is updated every L64724 CLK. When the microprocessor reads the status, the current information is buffered in a special-purpose 32-bit STS buffer that locks the STS value until the end of the microprocessor read operation.

Four consecutive read operations must be done to the same Group 2 address (A[2:0] = 0b010) to access all four bytes of the status registers.

The STS register bits are cleared to 0 after a hardware reset. They are also cleared each time a register byte is read—when you read the eight LSBs, the eight LSB interrupts are cleared, and when you read the eight MSBs, the eight MSB interrupts are cleared.

The following register diagram shows the bit organization of STS[7:0]. Descriptions of the bits follow the register diagram.

APR	D7	D6	D5	D4	D3	D2	D1	D0
0	STS[7:0]							
	VBER	S3_LS	S3_S	S2_LS	S2_S	S1_LS	S1_S	Reserved

VBER **Viterbi Bit Error Rate Flag** **7**

The L64724 sets the VBER bit when the period specified by VMDC2 (Group 4—APR 5, 6, and 7) is reached. The L64724 also generates an interrupt if the VBER_IE bit in the SMR is set. The L64724 clears the VBER bit to 0 after a reset or a Group 2 (STS) read.

VBER	Definition
0	VMDC2 period not reached
1	VMDC2 period reached

S3_LS **Stage 3 Loss of Synchronization Flag** **6**

The L64724 sets the S3_LS bit when the Descrambler synchronization module determines that synchronization is lost. It also generates an interrupt if the S3_LS_IE bit is set in the SMR. The L64724 clears the S3_LS bit to 0 after a reset or a Group 2 (STS) read.

S3_LS	Definition
0	Stage 3 Synchronization status unchanged
1	Loss of Stage 3 Synchronization detected

S3_S **Stage 3 Synchronization Flag** **5**

The L64724 sets the S3_S bit when the Descrambler synchronization module acquires synchronization. The L64724 also generates an interrupt if the S3_S_IE bit is

set in the SMR. The L64724 clears the S3_S bit to 0 after a reset or a Group 2 (STS) read.

S3_S	Definition
0	Stage 3 Synchronization status unchanged
1	Stage 3 Synchronization acquired

S2_LS **Stage 2 Loss of Synchronization Flag** **4**

The L64724 sets the S2_LS bit when the Deinterleaver/Reed-Solomon Decoder synchronization module determines that synchronization is lost. The L64724 also generates an interrupt if the S2_LS_IE bit is set in the SMR. The L64724 clears the S2_LS bit to 0 after a reset or a Group 2 (STS) read.

S2_LS	Definition
0	Stage 2 Synchronization status unchanged
1	Loss of Stage 2 Synchronization detected

S2_S **Stage 2 Synchronization Flag** **3**

The L64724 sets the S2_S bit when the Deinterleaver/Reed-Solomon Decoder synchronization module acquires synchronization. The L64724 also generates an interrupt if the S2_S_IE bit is set in the SMR. The L64724 clears the S2_S bit to 0 after a reset or a Group 2 (STS) read.

S2_S	Definition
0	Stage 2 Synchronization status unchanged
1	Stage 2 Synchronization acquired

S1_LS **Stage 1 Loss of Synchronization Flag** **2**

The L64724 sets the S1_LS bit when the Viterbi Decoder synchronization module determines that synchronization is lost. The L64724 also generates an interrupt if the S1_LS_IE bit is set in the SMR. The L64724 clears S1_LS to 0 after a reset or a Group 2 (STS) read.

S1_LS	Definition
0	Stage 1 Synchronization status unchanged
1	Loss of Stage 1 Synchronization detected

S1_S **Stage 1 Synchronization Flag** **1**

The L64724 sets the S1_S bit when the Viterbi Decoder synchronization module has acquired synchronization. The L64724 also generates an interrupt if the S1_S_IE bit is set in the SMR. The L64724 clears S1_S to 0 after a reset or a Group 2 (STS) read.

S1_S	Definition
0	Stage 1 Synchronization status unchanged
1	Stage 1 Synchronization acquired

Reserved **Reserved** **0**

This bit is reserved for LSI Logic internal use only. Reading this bit will give unpredictable results.

The following register diagram shows the bit organization of STS[15:8]. Descriptions of the bits follow the register diagram.

APR	D7	D6	D5	D4	D3	D2	D1	D0
1	STS[15:8]							
	CLK_LK	CLK_LLK	CP_LK	CP_LLK	Reserved = 0		CL_FS_LL	CL_FS_UL

CLK_LK **Timing Lock Established** **15**

The L64724 sets the CLK_LK bit when Timing Lock is established.

CLK_LK	Definition
0	Timing Lock Status Unchanged
1	Timing Lock Established

CLK_LLK **Timing Lock Lost** **14**

The L64724 sets the CLK_LLK bit when Timing Lock is lost.

CLK_LLK	Definition
0	Timing Lock Status Unchanged
1	Timing Lock Lost

CP_LK **Carrier Phase Lock Established** **13**

The L64724 sets the CP_LK bit when Carrier Phase Lock is established.

CP_LK	Definition
0	Carrier Phase Lock Status Unchanged
1	Carrier Phase Lock Established

CP_LLK **Carrier Phase Lock Lost** **12**

The L64724 sets the CP_LLK bit when Carrier Phase Lock is lost.

CP_LLK	Definition
0	Carrier Phase Lock Status Unchanged
1	Carrier Phase Lock Lost

Reserved **Reserved** **[11:10]**

The Reserved bits are for LSI Logic internal use only and must always be cleared to 0.

CL_FS_LL **Frequency Sweep Lower Limit Reached** **9**

The L64724 sets the CL_FS_LL bit when the lower limit of the Carrier Loop Frequency Sweep is reached.

FS_LL	Definition
0	Frequency Sweep Status Unchanged
1	Frequency Sweep Lower Limit Reached

CL_FS_UL **Frequency Sweep Upper Limit Reached** **8**

The L64724 sets the CL_FS_UL bit when the upper limit of the Carrier Loop Frequency Sweep is reached.

FS_UL	Definition
0	Frequency Sweep Status Unchanged
1	Frequency Sweep Upper Limit Reached

The following register diagram shows the bit organization of STS[23:16]. Descriptions of the fields follow the register diagram.

APR	D7	D6	D5	D4	D3	D2	D1	D0
2	STS[23:16]							
	Reserved						TL_CL_FS_LL	TL_CL_FS_UL

Reserved **Reserved** **[23:18]**

These bits are reserved for LSI Logic internal use only. The bits, when read, return a value of zero.

TL_CL_FS_LL

Frequency Sweep Lower Limit Reached **17**

The L64724 sets the TL_CL_FS_LL bit when the lower limit of the Timing Loop Frequency Sweep is reached.

TL_CL_FS_LL	Definition
0	Frequency Sweep Status Unchanged
1	Frequency Sweep Lower Limit Reached

TL_CL_FS_UL

Frequency Sweep Upper Limit Reached **16**

The L64724 sets the TL_CL_FS_UL bit when the upper limit of the Timing Loop Frequency Sweep is reached.

TL_CL_FS_UL	Definition
0	Frequency Sweep Status Unchanged
1	Frequency Sweep Upper Limit Reached

The following register diagram shows the bit organization of STS[31:24].

APR	D7	D6	D5	D4	D3	D2	D1	D0
3	STS[31:24]							
	uC_I7	uC_I6	uC_I5	uC_I4	uC_I3	uC_I2	uC_I1	uC_I0

The microcontroller interrupt register (uC_I) bits are reset after a hardware reset. They are also reset each time the register byte is read. The definition of each interrupt bit can be determined by the microcode. The interrupts are user-defined.

3.5 Group 3: Status Registers

Group 3 consists of a number of internal status registers that are used for diagnostics and performance evaluation purposes. The registers are internally updated every PCLK cycle and are read asynchronously. When the microprocessor reads the register, the current information is buffered in a special-purpose buffer that stores the value of the respective register until the end of the read operation. In particular, registers that occupy more than one byte are frozen when the first byte is read. With the exception of the uC_Status_bytes, the L64724 clears all the bits in the Group 3 registers to 0 after a software or a hardware reset. The uC_Status_bytes are cleared through hardware reset or the Reset_Mode bit, located in Group 5, APR 520, bit 1. For a definition of software reset, see Group 4, APR 55, FEC_RST and DEMOD_RST. Table 3.4 shows the addresses and fields of the Group 3 registers.

Table 3.4 Group 3 Register Map

APR	D7	D6	D5	D4	D3	D2	D1	D0
0	Reed-Solomon Corrected Error Count low byte, CEC[7:0]							
1	Reed-Solomon Corrected Error Count high byte, CEC[15:8]							
2	Reed-Solomon Uncorrected Error Count low byte, UEC[7:0]							
3	Reed-Solomon Uncorrected Error Count high byte, UEC[15:8]							
4	Viterbi Bit Error Rate Count low byte, VBERC[7:0]							
5	Viterbi Bit Error Rate Count high byte, VBERC[15:8]							
6	Demod_SNR	XCTR_IN	Reserved					Chip_ID
7	NCO Frequency Deviation, CAR_NCOF[7:0]							
8	NCO Frequency Deviation, CAR_NCOF[15:8]							
9	NCO Frequency Deviation, CAR_NCOF[23:16]							
10	AGC Loop Voltage Meter, PWR_LVL[7:0]							
11	Reserved	uC_ Active	Reserved	CAR_LC	Reserved	S3	S2	S1
12	Reserved		RI Read Back, RI[5:0]					
13	Reserved		RQ Read Back, RQ[5:0]					

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Table 3.4 Group 3 Register Map (Cont.)

APR	D7	D6	D5	D4	D3	D2	D1	D0
14	Reserved				IMQ_ Active	Viterbi Code Rate[2:0]		
15	Reserved							
16	Reserved							
17	uC_Status_byte0 [7:0]							
18	uC_Status_byte1 [7:0]							
19	uC_Status_byte2 [7:0]							
20	uC_Status_byte3 [7:0]							
21	uC_Status_byte4 [7:0]							
22	Demodulator SNR Estimate, SNR[7:0]							
23	Reserved				Demodulator SNR Estimate, SNR[11:8]			
(Sheet 2 of 2)								

3.5.1 Reed-Solomon Corrected Error Count (Group 3: APR 0 and 1)

When read, the Reed-Solomon Corrected Error Count (CEC) register presents the corrected byte or bit error count since it was last reset. The bit or byte error count is a function of the RS_Bit/Byte_Select configuration bit (Group 4, APR 31, D7). When the bit error count mode is chosen, the value in the register represents the bit error count, which is the CEC multiplied by eight. When written, the register is reset to 0.

The CEC field is 16 bits long. The LSB is located at APR 0, bit 0, and the MSB at APR 1, bit 7. The CEC count saturates (stops) when it reaches its maximum count (65,535), and the counter is not reset after it is read. When the register is written, the CEC bits are cleared to 0.

Read/Write: R/W **Reset Value: 0x0000**

APR	D7	D0
0	Reed-Solomon Corrected Error Count low byte, CEC[7:0]	

APR	D15	D8
1	Reed-Solomon Corrected Error Count high byte, CEC[15:8]	

3.5.2 Reed-Solomon Uncorrected Error Count (Group 3: APR 2 and 3)

When read, the Reed-Solomon Uncorrected Error Count (UEC) register presents the uncorrected blocks count since it was last reset. When written, the register is cleared to 0. The UEC field is 16 bits long. The LSB is located at APR 2, bit 0, and the MSB at APR 3, bit 7. The UEC count saturates (stops) when it reaches its maximum count (65,535), and the counter is not reset after it is read. When the register is written, the UEC bits are cleared.

Read/Write: R/W **Reset Value: 0x0000**

APR	D7	D0
2	Reed-Solomon Uncorrected Error Count low byte, UEC[7:0]	
APR	D15	D8
3	Reed-Solomon Uncorrected Error Count high byte, UEC[15:8]	

3.5.3 Viterbi Bit Error Rate Count (Group 3: APR 4 and 5)

When read, the Viterbi Bit Error Rate Count register presents the Viterbi decoder bit error count during the time period specified by VMDC2 (Group 4, APR 5,6,7). The Viterbi Bit Error rate Count (VBERC) field is 16 bits long. The LSB is located at APR 4, bit 0, and the MSB at APR 5, bit 7. The actual number of errors is equal to four times VBERC. VBERC is updated each time a Viterbi error is encountered, and is reset at the beginning of each VMDC2 period.

Read/Write: R **Reset Value: 0x0000**

APR	D7	D0
4	Viterbi Bit Error Rate Count low byte, VBERC[7:0]	
APR	D15	D8
5	Viterbi Bit Error Rate Count high byte, VBERC[15:8]	

3.5.4 Control Input, SNR, and Chip_ID register (Group 3: APR 6)

The Control Input, SNR, and Chip_ID register contains the Demodulator Signal-to-Noise Ratio (Demod_SNR) bit, the Control Input bit (XCTR_IN), and the Chip_ID bit.

Read/Write: R **Reset Value: 0x0000**

APR	D7	D6	D5	D1	D0
6	Demod _SNR	XCTR_IN	Reserved		Chip_ID

Demod_SNR **Demodulator Signal to Noise Ratio** **7**
When read, the Demod_SNR bit gives an indication of the SNR. When the SNR is bad (above the threshold), the bit is 0. When the SNR is good (below the threshold), the bit is 1. The thresholds are discussed in Section 5.7.2.1, "Phase Error Estimator," page 5-16, and shown in Figure 5.7.

XCTR_IN **External Control Input Bit** **6**
When read, the XCTR_IN bit shows the logic level applied to the External Control Input (XCTR_IN) pin.

Reserved **Reserved** **[5:1]**
These bits are reserved.

Chip_ID **Chip Identification** **0**
When read, this bit shows the stepping of the L64724 IC. When the Chip_ID bit is 1, it indicates that the L64724 IC is an L64724b. When the bit is 0, it indicates that the IC is an L64724a.

3.5.5 NCO Frequency Deviation (Group 3: APR 7, 8, and 9)

The L64724 puts the result of the Carrier Loop NCO (number-controlled oscillator) frequency measurement into the NCO Frequency Deviation 24-bit register. The value, in Hz, corresponds to the frequency deviation observed in the carrier loop as a function of the Low Noise Block Converter (LNB) drift. To see the updated 24-bit CAR_NCOF value, first access APR7.

ReaPBd/WPBrite: R **Reset Value: 0x0000**

APR	D7	D0
7	CAR_NCOF[7:0]	

APR	D15	D8
8	CAR_NCOF[15:8]	

APR	D23	D16
9	CAR_NCOF[23:16]	

3.5.6 Automatic Gain Control (AGC) Loop Voltage Meter (Group 3: APR 10)

The L64724 stores the AGC loop control voltage in the AGC Loop Voltage Meter register. See Section 5.8.3, “Power Level,” page 5-22, for an equation that relates V_{AGC} and PWR_LVL[7:0]. See Section B.1, “L64724 QPSK Demodulator Acquisition and Debugging Tips,” for more details on PWR_LVL[7:0].

Read/Write: R **Reset Value: 0x00**

APR	D7	D0
10	PWR_LVL[7:0]	

3.5.7 Carrier and FEC Synchronization Status (Group 3: APR 11)

The Carrier and FEC Synchronization Status register contains the Carrier Loop and FEC pipeline synchronization status bits.

Read/Write: R **Reset Value: 0x00**

APR	D7	D6	D5	D4	D3	D2	D1	D0
11	Reserved	uC_Active	Reserved = 0	CAR_LC	Reserved	S3	S2	S1

Reserved **Reserved** **7**
This bit is reserved for LSI Logic internal use only. When read, it returns an indeterminate value.

uC_Active **Microcontroller Active Flag** **6**

The L64724 sets the uC_Active bit to 1 to indicate that the internal microcontroller is running.

uC_Active	Definition
0	Internal microcontroller not active
1	Internal microcontroller running

Reserved **Reserved** **5**

The Reserved bit is for LSI Logic internal use only and must always be set to 0.

CAR_LC **Carrier Phase Lock Flag** **4**

The L64724 sets the CAR_LC bit to 1 to indicate that the carrier phase lock detector is locked.

CAR_LC	Definition
0	Carrier Phase Lock detector out of lock
1	Carrier Phase Lock detector locked

Reserved **Reserved** **3**

This bit is reserved for LSI Logic internal use only. When read, it returns an indeterminate value.

S3 **Stage 3 Synchronization Flag** **2**

The L64724 sets the S3 bit to 1 when the Descrambler synchronization module is in synchronization. When this bit is 0, the Descrambler module is not synchronized. The S3 bit is not valid in DSS Mode.

S3	Definition
0	Descrambler Out of Sync
1	Descrambler In Sync

S2 **Stage 2 Synchronization Flag** **1**

The L64724 sets the S2 bit to 1 when the Deinterleaver/Reed-Solomon Decoder synchronization module is in synchronization. When the bit is 0, the

Deinterleaver/Reed-Solomon Decoder is not synchronized.

S2	Definition
0	Deinterleaver/Reed-Solomon Decoder Out of Synchronization
1	Deinterleaver/Reed-Solomon Decoder In Synchronization

S1 **Stage 1 Synchronization Flag** **0**

The L64724 sets the S1 bit to 1 when the Viterbi Decoder synchronization module is in synchronization. When the bit is 0, the Viterbi Decoder is not synchronized.

S1	Definition
0	Viterbi Decoder Out of Synchronization
1	Viterbi Decoder In Synchronization

3.5.8 RI Read Back (Group 3: APR 12)

The RI Readback register displays the digital value on the I channel input.

Read/Write: R **Reset Value: 0x00**

APR	D7	D6	D5	D0
12	Reserved		RI[5:0]	

Reserved **Reserved** **[7:6]**

These bits are reserved for LSI Logic internal use only. When read, they return an indeterminate value.

RI **RI Read Back** **[5:0]**

This register displays the value on the RI[5:0] input bus. Note that PCLK needs to be running for this feature to operate properly.

3.5.9 RQ Read Back (Group 3: APR 13)

The RQ Readback register displays the digital value on the Q channel input.

Read/Write: R **Reset Value: 0x00**

APR	D7	D6	D5	D0
13	Reserved		RQ[5:0]	

Reserved **Reserved** **[7:6]**
These bits are reserved for LSI Logic internal use only. When read, they return an indeterminate value.

RQ **RQ Read Back** **[5:0]**
This register displays the value on the RQ[5:0] input bus. Note that PCLK needs to be running for this feature to operate properly.

3.5.10 Viterbi Code Rate (Group 3: APR 14)

Read/Write: R **Reset Value: 0x00**

APR	D7	D4	D3	D2	D0
14	Reserved		IMQ_ Active	Viterbi Code Rate, VCR[2:0]	

Reserved **Reserved Bits** **[7:4]**
These bits are reserved for LSI Logic internal use only. When read, they return an indeterminate value.

IMQ_Active **IMQ Mode Active** **3**
When the IMQ_Active bit is 1, it Indicates that the state machine has detected an IMQ inversion[1] and is compensating for it automatically.

VCR **Viterbi Code Rate** **[2:0]**
These bits display the Viterbi decoder code rate that was found during the acquisition process for the convolutional decoder. The Viterbi Code Rate information in this register is meaningful only after synchronization has

1. The Q portion of the IQ spectrum is inverted and the I portion is not inverted.

been achieved as indicated when the S1 bit in APR 11 is set to 1.

VCR[2:0]			Definition
0	0	0	Rate 1/2
0	0	1	Rate 2/3
0	1	0	Rate 3/4
0	1	1	Rate 5/6
1	0	0	Rate 6/7
1	0	1	Rate 7/8
1	1	0	Unused
1	1	1	Unused

3.5.11 Reserved (Group 3: APR 15)

Read/Write: R **Reset Value: 0x00**

APR	D7	D0
15	Reserved	

Reserved **Reserved Bits** **[7:0]**
These bits are reserved for LSI Logic internal use only. When read, they will return an indeterminate value.

3.5.12 Reserved (Group 3: APR 16)

Read/Write: R **Reset Value: 0x00**

APR	D7	D0
16	Reserved	

Reserved **Reserved Bits** **[7:0]**
These bits are reserved for LSI Logic internal use only. When read, they will return an indeterminate value.

3.5.13 uC Status Bytes (Group 3: APR 17 to 21)

The uC status bytes are user-defined. They are cleared on hardware reset and when the microcontroller is disabled.

Read/Write: R **Reset Value: 0x0000**

APR	D7 D0
17	MicroController Status Byte 0, uCSB4[7:0]
18	MicroController Status Byte 1, uCSB3[7:0]
19	MicroController Status Byte 2, uCSB2[7:0]
20	MicroController Status Byte 3, uCSB1[7:0]
21	MicroController Status Byte 4, uCSB0[7:0]

uCSB0 **MicroController Status Byte 0** **[7:0]**
UCSB0 is a user-defined status byte and can be updated as defined in the microcoded instructions of the on-chip microcontroller.

uCSB1 **MicroController Status Byte 1** **[7:0]**
UCSB1 is a user-defined status byte and can be updated as defined in the microcoded instructions of the on-chip microcontroller.

uCSB2 **MicroController Status Byte 2** **[7:0]**
UCSB2 is a user-defined status byte and can be updated as defined in the microcoded instructions of the on-chip microcontroller.

uCSB3 **MicroController Status Byte 3** **[7:0]**
UCSB3 is a user-defined status byte and can be updated as defined in the microcoded instructions of the on-chip microcontroller.

uCSB4 **MicroController Status Byte 4** **[7:0]**
UCSB4 is a user-defined status byte and can be updated as defined in the microcoded instructions of the on-chip microcontroller.

3.5.14 Demodulator SNR Estimate (Group 3: APR 22 and 23)

Read/Write: R **Reset Value: 0x0000**

APR	D7			D0
22	Demod SNR Estimate, SNR[7:0]			
APR	D15	D12	D11	D8
23	Reserved		Demod SNR Estimate, SNR[11:8]	

When read, the Demodulator Signal to Noise Ratio (SNR) Estimate register presents the value for the Demodulator SNR estimate. SNR is 12 bits long. The LSB is found at APR 22, bit 0, and the MSB at APR 23, bit 3. See Section 5.7.2.1, “Phase Error Estimator,” page 5-16, for additional details on SNR[7:0].

3.6 Group 4: Configuration Registers

Although most Group 4 registers are 8 bits wide, some are as wide as 24 bits. All accesses are done in 8-bit widths. The Address Pointer Register (APR) is used to access these registers as described in Section 3.3, “Groups 0 and 1: Address Pointer Register.”

Group 4 registers are not affected by reset—the bit values are random immediately after power-up and retain their last known value after any of the three reset operations as shown in Section 3.2, “Reset and How it Affects Registers.” Table 3.5 shows the addresses and fields of the Group 4 registers.

Table 3.5 Group 4 Register Map

APR [5:0]	D7	D6	D5	D4	D3	D2	D1	DO
0	Set to 1	Reserved	PLL_N[5:0]					
1	Reserved		PLL_S[5:0]					
2	IMQ	DVB_ DSS	QB	PLL_T[4:0]				
3	Viterbi Code Rate, VCR[2:0]			TEI	SYNC2_ MOD	Reserved	PLL_M[1:0]	
4	Viterbi Max Data Bit Count 1, VMDC1[7:0]							
5	Viterbi Max Data Bit Count 2, VMDC2[7:0], low byte							
6	Viterbi Max Data Bit Count 2, VMDC2[15:8], middle byte							
7	Viterbi Max Data Bit Count 2, VMDC2[23:16], high byte							
8	Viterbi Maximum Bit Error Count[7:0], Rate 1/2							
9	Viterbi Maximum Bit Error Count[7:0], Rate 2/3							
10	Viterbi Maximum Bit Error Count[7:0], Rate 3/4							
11	Viterbi Maximum Bit Error Count[7:0], Rate 5/6							
12	Viterbi Maximum Bit Error Count[7:0], Rate 6/7							
13	Viterbi Maximum Bit Error Count[7:0], Rate 7/8							
14	Synchronization Word[7:0]							
15	Reserved	Auto Rate	Reserved		IMQ_EN	DI_ Bypass	L[1:0]	
16	Reserved		Sync Status Select, SSS[1:0]		Sync States Acq, SSA[1:0]		Sync States Track, SST[1:0]	
17	Reserved		OF	Reserved				

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Table 3.5 Group 4 Register Map (Cont.)

APR [5:0]	D7	D6	D5	D4	D3	D2	D1	DO
18	PLL_RESET							
19	DF_SELECT[2:0]			DF_GAIN[1:0]		DF_RATIO[2:0]		
20	Reserved			PD	Reserved			MF_20_35
21	PCLK_INV	PLL_BP	LCLK_OFF	CLK_DIV1[4:0]				
22	CLK_DIV2[7:0]							
23	DC_Offset_On_Off[1:0]		Reserved	CLK_DIV2[12:8]				
24	PWR_REF[7:0]							
25	Reserved					INT_DC	PWR_BW[1:0]	
26	Scale factor for DEMI, DEMQ, SCALE[7:0]							
27	SNR Estimator Threshold, SNR_THS[7:0]							
28	Carrier Loop Lambda, CAR_LAMBDA_SEL[3:0]				Carrier Loop Mu, CAR_MU_SEL[3:0]			
29	Carrier Phase Lock Detector Threshold, CAR_LC_THSL[7:0]							
30	Reserved							
31	RS Bit/Byte Select	Errorout_Invert	SPI_On_Off	Reserved				
32	Carrier Synchronizer Sweep Rate, CAR_SWR[7:0]							
33	Carrier Synchronizer Sweep Rate, CAR_SWR[15:8]							
34	Carrier Synchronizer Upper Sweep Limit, CAR_USWL[7:0]							
35	Carrier Synchronizer Upper Sweep Limit, CAR_USWL[15:8]							
36	Carrier Synchronizer Lower Sweep Limit, CAR_LSWL[7:0]							
37	Carrier Synchronizer Lower Sweep Limit, CAR_LSWL[15:8]							

(Sheet 2 of 4)

Table 3.5 Group 4 Register Map (Cont.)

APR [5:0]	D7	D6	D5	D4	D3	D2	D1	DO
38	Carrier Loop Filter Initialization, CAR_LF_INIT[7:0]							
39	Carrier Loop Filter Initialization, CAR_LF_INIT[15:8]							
40	Carrier Loop Filter Initialization, CAR_LF_INIT[23:16]							
41	CAR_ SWP_ SWAP	CAR_ ERROR_ SWAP	CAR_ AUTO_ SWP	Reserved		CAR_ PED_SEL	CAR_ OPEN	CAR_SW
42	Clock Loop Lambda, CLK_LAMBDA_SEL[3:0]				Clock Loop Mu, CLK_MU_SEL[3:0]			
43	Clock Synchronizer Sweep Rate, CLK_SWR[7:0]							
44	Clock Synchronizer Sweep Rate, CLK_SWR[15:8]							
45	Clock Synchronizer Upper Sweep Limit, CLK_USWL[7:0]							
46	Clock Synchronizer Upper Sweep Limit, CLK_USWL[15:8]							
47	Clock Synchronizer Lower Sweep Limit, CLK_LSWL[7:0]							
48	Clock Synchronizer Lower Sweep Limit, CLK_LSWL[15:8]							
49	Clock Loop Bias, CLK_BIAS[7:0]							
50	Clock Loop Bias, CLK_BIAS[15:8]							
51	Clock Loop Bias, CLK_BIAS[23:16]							
52	Reserved	Clock Loop Bias, CLK_BIAS[30:24]						
53	CLK_SWP _SWAP	CLK_ ERROR_ SWAP	CLK_ AUTO_ SWP	Set to 1	AGC_ CLK_SEL	Reserved	CLK_ OPEN	CLK_SW
54	SNR_EST	PWRP_ TRI	ADC_PD	FP_ LOCK_ LEN	PWRP	Reserved		CLK_ ALPHA_ SEL
55	ADC_BP	OB_2C	External Control Output Bits, XCTR[3:0]				DEMOD _RST	FEC_ RST
56	Reserved							
57	Reserved							

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Table 3.5 Group 4 Register Map (Cont.)

APR [5:0]	D7	D6	D5	D4	D3	D2	D1	DO
58	Reserved							
59	Serial Transmission Start Data, TXSD[6:0]							Reserved
60	Serial Transmission Data, STXD[7:0]							
61	Serial Transmission End Data, TXED[7:0]							
62	Serial_B	Serial_C[1:0]		SPI_M[3:0]				Serial_A
63	FMODE	SPI_CLK_ AND	SPI_MOD E_A_B	Re- served	SPI_N[3:0]			
64	SPI_Gain[7:0](LSB)							
65	Reserved						SPI_Gain[9:8]	
66	SPI_Bias[7:0] (LSB)							
67	SPI_Bias[15:8] (MSB)							
68	Reserved	SPI_Bias[22:16]						
69	Timing Lock Detector Threshold, CLK_LC_THSL[7:0]							

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3.6.1 PLL Parameter N (Group 4: APR 0)

The PLL Configuration Parameter N (PLL_N[5:0]) configures the PLL module for clock synthesis.

Read/Write: R/W

APR	D7	D6	D5 ... D0
0	Set to 1	Reserved	PLL_N[5:0]

Set to 1 **Set to 1** **7**
This is an internal test bit that must be set to 1.

Reserved **Reserved** **6**
This is an internal test bit that must be cleared to 0.

PLL_N **PLL Configuration Parameter N** **[5:0]**
PLL_N[5:0] is one of four parameters (PLL_S, PLL_N, PLL_T, and PLL_M) that you must set to configure the PLL module for clock synthesis. For more information, see Section 4.2, “PLL Clock Generation,” page 4-3.

3.6.2 PLL Parameter S (Group 4: APR 1)

The PLL Configuration Parameter S (PLL_S[5:0]) configures the PLL module for clock synthesis.

Read/Write: R/W

APR	D7	D6	D5	D0
1	Reserved		PLL_S[5:0]	

Reserved **Reserved** **[7:6]**
The Reserved bits are internal test bits that must be cleared to 0.

PLL_S **PLL Configuration Parameter S** **[5:0]**
PLL_S[5:0] is one of four parameters (PLL_S, PLL_N, PLL_T, and PLL_M) that you must set to configure the PLL module for clock synthesis. For more information see Section 4.2, “PLL Clock Generation.”

3.6.3 PLL Parameter T, Demodulator and Symbol Select (Group 4: APR 2)

The PLL Configuration Parameter T (PLL_T[4:0]) configures the PLL module for clock synthesis. This register also contains bits to configure the demodulator and select the symbol format.

Read/Write: R/W

APR	D7	D6	D5	D4	D0
2	IMQ	DVB_DSS	QB	PLL_T[4:0]	

IMQ **(I, -Q) Symbol Format** **7**
The IMQ bit indicates the format of the incoming symbol stream. The IMQ_EN bit (APR 15, D3) must be cleared

to 0 for IMQ to take effect. When IMQ_EN is set to a 1, IMQ will be disregarded.

IMQ	Symbol Format
0	I, Q
1	I,-Q

DVB_DSS **DVB/DSS Mode Select** **6**

The DVB_DSS bit indicates the format of the incoming symbol stream. The L64724 supports data stream formats that conform to either the Digital Video Broadcast Standard (DVB) or the specifications for the Digital Satellite System (DSS). Note that when DSS mode is selected (DVB_DSS set to 1), the TEI indicator bit (APR 3, D4) must be cleared to 0.

DVB_DSS	Symbol Format
0	DVB Format Selected
1	DSS Format Selected

QB **QPSK/BPSK Format Select** **5**

Set the QB bit to 1 to specify the format of the incoming symbol stream. The QB bit should be cleared to 0 for systems that input a QPSK symbol pair (I, Q) once per CLK cycle. The QB bit should be set to 1 for BPSK input (I stream only).

QB	Symbol Stream Format
0	QPSK
1	BPSK

PLL_T **PLL Configuration Parameter T** **[4:0]**

PLL_T[4:0] is one of four parameters (PLL_S, PLL_N, PLL_T, and PLL_M) that you must set to configure the PLL module for clock synthesis. For more information, see Section 4.2, “PLL Clock Generation,” page 4-3. Allowed values are 1 and all even numbers.

3.6.4 PLL Parameter M, Transport and Viterbi Code Rate Select (Group 4: APR 3)

The PLL Configuration Parameter M (PLL_M[1:0]) configures the PLL module for clock synthesis. This register also contains bits to set the Viterbi Decoder module code rate and configure the Transport Error Indicator.

Read/Write: R/W

APR	D7	D5	D4	D3	D2	D1	D0
3	Viterbi Code Rate, VCR[2:0]		TEI	SYNC2_MOD	Reserved	PLL_M[1:0]	

VCR **Viterbi Code Rate** **[7:5]**

Set these VCR bits to select the code rate for the L64724 Viterbi decoder module. The three bits are assigned as follows:

VCR[2:0]			Definition
0	0	0	Rate 1/2
0	0	1	Rate 2/3
0	1	0	Rate 3/4
0	1	1	Rate 5/6
1	0	0	Rate 6/7
1	0	1	Rate 7/8
1	1	0	Unused
1	1	1	Unused

The VCR bits are disregarded when automatic Viterbi rate acquisition is selected (Auto Rate bit: Group 4, APR 15, D6 = 1.)

TEI **Transport Error Indicator Select** **4**

When the Transport Error Indicator Select bit is set to 1, it activates the transport error indicator mechanism. In this mode, the first bit following the synchronization byte in a Transport Packet is forced HIGH whenever the Reed-Solomon decoder finds the data block to be uncorrectable. Otherwise, it remains unchanged. When the TEI bit is cleared to 0, the transport error indicator will not be set at any time (see the *MPEG-2 System*

Specification H.222 Transport Stream Packet Layer, paragraph 2.4.3.2). Using the TEI feature allows a simpler interface to the LSI Logic L64007 Transport Demultiplexer. For more information, see the LSI Logic *L64007 MPEG-2, DVB, and TSAT Transport Demultiplexer Technical Manual*.

SYNC2_MOD **Sync2 Modified** **3**

The SYNC2_MOD bit selects an alternate method of acquiring Sync 2. It should be set to 1 for normal operation.

Reserved **Reserved** **2**

This bit must be cleared to 0 for proper operation.

PLL_M **VCO Frequency Range for PLL Module** **[1:0]**

PLL_M is one of four parameters (PLL_S, PLL_N, PLL_T, and PLL_M) that you must set to configure the PLL module for clock synthesis. For more information see Section 4.2, "PLL Clock Generation," page 4-3. Configure the PLL_M[1:0] bits to tell the L64724 the frequency range of the PLL.

PLL_M[1:0]		PLL Range
0	0	40–50 MHz
0	1	50–60 MHz
1	0	60–70 MHz
1	1	70–90 MHz

3.6.5 Viterbi Maximum Data Bit Count 1 (Group 4: APR 4)

This register specifies the number of valid symbols, divided by 256, over which the number of Viterbi decoded symbol errors are counted for synchronization. For example, a value of VMDC1[7:0] = 0x02 specifies 512 data bits.

Equation 3.1

$$VMDC1 = \frac{Symbols}{256}$$

For more information see Section 7.1.3, “Viterbi BER Monitor,” page 7-7.

Read/Write: R/W

APR	D7	D0
4	Viterbi Maximum Data Bit Count 1, VMDC1[7:0]	

3.6.6 Viterbi Max Data Bit Count 2 (Group 4: APR 5, 6, and 7)

These registers specify the number of valid symbols, divided by four, over which the number of symbol errors in the Viterbi output data stream are counted, after synchronization. The symbol error count is then displayed as VBERC (Group 3, APR 4,5). The value for VMDC2 occupies 24 bits and is arranged as three bytes with APR 5, bit 0 being the least significant bit and APR 7, bit 7 being the most significant bit. For example, a value of VMDC2[23:0] = 0x00.00F0 specifies 960 data bits.

Equation 3.2

$$VMDC2 = \frac{Symbols}{4}$$

For more information see Section 7.1.3, “Viterbi BER Monitor.”

Read/Write: R/W

APR	D7	D0
5	Viterbi Maximum Data Bit Count 2, Low Byte, VMDC2[7:0]	

APR	D15	D8
6	Viterbi Maximum Data Bit Count 2, Middle Byte, VMDC2[15:8]	

APR	D23	D16
7	Viterbi Maximum Data Bit Count 2, High Byte, VMDC2[23:16]	

3.6.7 Viterbi Maximum Bit Error Count, Rate 1/2 (Group 4: APR 8)

This register specifies the maximum number of Viterbi symbol errors that are allowed to occur within the data period set by VMDC1 (Group 4, APR 4) to achieve Viterbi module synchronization.

Note: This register is used during Viterbi code rate acquisition for Rate 1/2.

Whenever the symbol error count from the internal bit error counter exceeds the value VMBEC_1_2[7:0], the synchronization module concludes that the Viterbi decoder module is out of synchronization and proceeds to adjust the phase of the incoming symbol stream until synchronization is reached. The symbol error count is given by Equation 3.3.

Equation 3.3

$$\text{Number of Symbol Errors} = 128\ \text{VMBEC\_1\_2} + 32$$

For example, a value of VMBEC_1_2[7:0] = 0x03 specifies 416 errors. For more information, see Section 7.1.3, “Viterbi BER Monitor,” page 7-7. Note that a software reset (FEC_RST, APR 55, bit 0) does not affect the contents of the register.

Read/Write: R/W

APR	D7	D0
8	Viterbi Maximum Bit Error Count VMBEC_1_2[7:0], Rate 1/2	

3.6.8 Viterbi Maximum Bit Error Count, Rate 2/3 (Group 4: APR 9)

This register specifies the maximum number of Viterbi symbol errors that are allowed to occur within the data period set by VMDC1 (Group 4, APR 4) to achieve Viterbi module synchronization.

Note: This register is used during Viterbi code rate acquisition for Rate 2/3.

Whenever the symbol error count from the internal bit error counter exceeds the value VMBEC_2_3[7:0], the synchronization module concludes that the Viterbi decoder module is out of synchronization and proceeds to adjust the phase of the incoming symbol stream until synchronization is reached. The symbol error count is given by Equation 3.4.

Equation 3.4

$$\text{Number of Symbol Errors} = 128\ \text{VMBEC\_2\_3} + 32$$

For example, a value of VMBEC_2_3[7:0] = 0x03 specifies 416 errors. For more information, see Section 7.1.3, “Viterbi BER Monitor.” Note that a software reset (FEC_RST, APR 55, bit 0 set to 1) does not affect the contents of the register.

Read/Write: R/W

APR	D7	D0
9	Viterbi Maximum Bit Error Count VMBEC_2_3[7:0], Rate 2/3	

3.6.9 Viterbi Maximum Bit Error Count, Rate 3/4 (Group 4: APR 10)

This register specifies the maximum number of Viterbi symbol errors that are allowed to occur within the data period set by VMDC1 (Group 4, APR 4) to achieve Viterbi module synchronization.

Note: This register is used during Viterbi code rate acquisition for Rate 3/4.

Whenever the symbol error count from the internal bit error counter exceeds the value VMBEC_3_4[7:0], the synchronization module concludes that the Viterbi decoder module is out of synchronization and proceeds to adjust the phase of the incoming symbol stream until synchronization is reached. The symbol error count is given by Equation 3.5.

Equation 3.5

$$\text{Number of Symbol Errors} = 128\ \text{VMBEC\_3\_4} + 32$$

For example, a value of VMBEC_2_3[7:0] = 0b0000.0011 specifies 416 errors. For more information, see Section 7.1.3, “Viterbi BER Monitor,” page 7-7. Note that a software reset (FEC_RST, APR 55, bit 0 set to 1) does not affect the contents of the register.

Read/Write: R/W

APR	D7	D0
10	Viterbi Maximum Bit Error Count VMBEC_3_4[7:0], Rate 3/4	

3.6.10 Viterbi Maximum Bit Error Count, Rate 5/6 (Group 4: APR 11)

This register specifies the maximum number of Viterbi symbol errors that are allowed to occur within the data period set by VMDC1 (Group 4, APR 4) to achieve Viterbi module synchronization.

Note: This register is used during Viterbi code rate acquisition for Rate 5/6.

Whenever the symbol error count from the internal bit error counter exceeds the value VMBEC_5_6[7:0], the synchronization module concludes that the Viterbi decoder module is out of synchronization and proceeds to adjust the phase of the incoming symbol stream until synchronization is reached. The symbol error count is given by Equation 3.6.

Equation 3.6

$$\text{Number of Symbol Errors} = 128\ \text{VMBEC\_5\_6} + 32$$

For example, a value of VMBEC_5_6[7:0] = 0x03 specifies 416 errors. For more information, see Section 7.1.3, “Viterbi BER Monitor,” page 7-7. Note that a software reset (FEC_RST, APR 55, bit 0 set to 1) does not affect the contents of the register.

Read/Write: R/W

APR	D7 … D0
11	Viterbi Maximum Bit Error Count VMBEC_5_6[7:0], Rate 5/6

3.6.11 Viterbi Maximum Bit Error Count, Rate 6/7 (Group 4: APR 12)

This register specifies the maximum number of Viterbi symbol errors that are allowed to occur within the data period set by VMDC1 (Group 4, APR 4) to achieve Viterbi module synchronization.

Note: This register is used during Viterbi code rate acquisition for Rate 6/7.

Whenever the symbol error count from the internal bit error counter exceeds the value VMBEC_6_7[7:0], the synchronization module concludes that the Viterbi decoder module is out of synchronization and

proceeds to adjust the phase of the incoming symbol stream until synchronization is reached. The symbol error count is given by Equation 3.7.

Equation 3.7

$$\text{Number of Symbol Errors} = 128\ \text{VMBEC\_6\_7} + 32$$

For example, a value of VMBEC_6_7[7:0] = 00x03 specifies 416 errors. For more information, see Section 7.1.3, “Viterbi BER Monitor,” page 7-7. Note that a software reset (FEC_RST, APR 55, bit 0 set to 1) does not affect the contents of the register.

Read/Write: R/W

APR	D7	D0
12	Viterbi Maximum Bit Error Count VMBEC_6_7[7:0], Rate 6/7	

3.6.12 Viterbi Maximum Bit Error Count, Rate 7/8 (Group 4: APR 13)

This register specifies the maximum number of Viterbi symbol errors that are allowed to occur within the data period set by VMDC1 (Group 4, APR 4) to achieve Viterbi module synchronization.

Note: This register is used during Viterbi code rate acquisition for Rate 7/8.

Whenever the symbol error count from the internal bit error counter exceeds the value VMBEC_7_8[7:0], the synchronization module concludes that the Viterbi decoder module is out of synchronization and proceeds to adjust the phase of the incoming symbol stream until synchronization is reached. The symbol error count is given by Equation 3.8.

Equation 3.8

$$\text{Number of Symbol Errors} = 128\ \text{VMBEC\_7\_8} + 32$$

For example, a value of VMBEC_7_8[7:0] = 0b0000.0011 specifies 416 errors. For more information, see Section 7.1.3, “Viterbi BER Monitor,” page 7-7. Note that a software reset (FEC_RST, APR 55, bit 0 set to 1) does not affect the contents of the register.

Read/Write: R/W

APR	D7	D0
13	Viterbi Maximum Bit Error Count VMBEC_7_8[7:0], Rate 7/8	

3.6.13 Synchronization Word (Group 4: APR 14)

This register contains the synchronization word used by the synchronization module in stages two and three. Within this byte, the MSB is chronologically oldest and the LSB is chronologically newest. See Section B.4, “QPSK Demodulator and FEC Configuration Example: Low Data Rates,” page B-30, for a typical setting for Synchronization Word[7:0].

Read/Write: R/W

APR	D7	D0
14	Synchronization Word[7:0]	

3.6.14 Mismatching Bits in Sync 2 Tracking Mode (Group 4: APR 15)

This register is used to set the maximum number of mismatching bits allowed to declare a match when comparing the data stream to the reference synchronization word during the tracking phase in the second synchronization stage.

Read/Write: R/W

APR	D7	D6	D5	D4	D3	D2	D1	D0
15	Reserved	Auto Rate	Reserved		IMQ_EN	DI_Bypass	L[1:0]	

Reserved **Reserved** **7**
This bit should be cleared to 0 for normal operation.

Auto Rate **Viterbi Decoder Automatic Rate Acquisition** **6**
The Auto Rate bit, when set to 1, enables automatic acquisition of the Viterbi code rate for the convolutional decoder. When DVB mode is selected (APR 2, D6, DVB_DSS = 0) the set of code rates that are being considered for automatic acquisition are 1/2, 2/3, 3/4, 5/6 and 7/8. When DSS mode is selected (APR 2, D6, DVB_DSS = 1) the rates include 2/3 and 6/7. The VCR bits (APR 3) are disregarded when the Auto Rate bit is set. The code rate identified by the Auto Rate mechanism is available under Group 3, APR 14 (Viterbi Coder Rate Registers). When the Auto Rate bit is 0, the Viterbi code rate is determined by the contents of the VCR field (APR 3).

Auto Rate	Viterbi Decoder Acquisition Mode
0	Code rate determined by VCR[2:0]
1	Automatic Code Rate Acquisition

Reserved **Reserved** **[5:4]**
The Reserved bits are for internal use only. They should always be cleared to 0, and produce random results when read.

IMQ_EN **(I, -Q) Format Resolution Enable** **3**

When the IMQ_EN bit is set to 1, the synchronization mechanism used for the convolutional decoder automatically resolves phase reflection (I, -Q). In this case, the polarity of the IMQ bit (APR 2) is disregarded. When the IMQ_EN bit is 0, the IMQ bit determines the symbol format.

IMQ_EN	Symbol Format
0	Determined by the value of IMQ (APR 2, D7)
1	Automatically determined by synchronization mechanism.

DI_Bypass **Deinterleaver Bypass** **2**

When set to 1, the DI_Bypass bit causes the Deinterleaver module to be bypassed. When the bit is 0, the deinterleaver functions according to the DVB or DSS specifications.

L[1:0] **Mismatching Bits, Tracking Mode, Sync2** **[1:0]**

This field is used to set the maximum number of mismatching bits allowed to declare a match when comparing eight bits in the data stream to the reference synchronization word during tracking phase in the second synchronization stage. The L[1:0] bits can be configured from 0b00 to 0b10. Higher values of L[1:0] result in a smaller probability of loss of lock due to random noise. Lower values result in a higher probability of loss.

L[1:0]		Number of Mismatching Bits
0	0	0
0	1	1
1	0	2
1	1	Illegal Value

3.6.15 Synchronization States and BCLKOUT Format (Group 4: APR 16)

This register is used to select the algorithms used in the synchronization modules, and which module's synchronization status will be shown on the SYNC output pin. The register also selects the frequency of the clock that will be output on the BCLKOUT pin.

Read/Write: R/W

APR	D7	D6	D5	D4	D3	D2	D1	D0
16	Reserved		SSS [1:0]		SSA [1:0]		SST [1:0]	

Reserved **Reserved** **[7:6]**
The Reserved bits must be cleared to 0 for proper operation.

SSS[1:0] **Synchronization Status/XCTR[3] Select** **[5:4]**
The SSS[1:0] bits allow you to observe the synchronization status of one of the three synchronization modules or the XCTR[3] output on the XCTR[3] output pin. The synchronization modules that may be observed are Viterbi Decoder synchronization, Deinterleaver/Reed-Solomon Decoder synchronization, and Descrambler synchronization. Program the SSS[1:0] field to determine which one of these status bits will be propagated to the XCTR[3] pin. Note that OS[4:0] (Group 4, APR 17) should be set to 0b00000.

SSS[1:0]		XCTR[3] Pin Connection
0	0	Viterbi decoder sync
0	1	DI/RS decoder sync
1	0	Descrambler sync
1	1	XCTR[3] (APR 55, D5)

SSA[1:0] **Synchronization States, Acquisition Mode** **[3:2]**
The second synchronization module (after the Viterbi Decoder and before the Deinterleaver module) allows three different state diagrams to be used in the acquisition phase. The number of properly identified synchronization words that will cause “in-synchronization” to be declared can be configured from 3 to 6. For more

information, see Section 6.3, “Reed-Solomon Deinterleaver Synchronization,” page 6-8.

SSA[1:0]		Number of Sync Words Found to Acquire
0	0	3
0	1	4
1	0	5
1	1	6

SST[1:0] **Synchronization Status, Tracking Mode** **[1:0]**
The second synchronization module (after the Viterbi decoder and before the Deinterleaver module) allows two, three, four, or five misdetected synchronization words before the L64724 declares a loss of synchronization. For more information, see Section 6.3, “Reed-Solomon Deinterleaver Synchronization.”

SST[1:0]		Number of Missed Sync Words Until Loss of Lock
0	0	2
0	1	3
1	0	4
1	1	5

3.6.16 Output Control (Group 4: APR 17)

This register is used to configure the Channel output data path.

Read/Write: R/W

APR	D7	D6	D5	D4	D0
17	Reserved		OF	Reserved	

Reserved **Reserved** **[7:6]**
The Reserved bits must be cleared to 0 for proper operation.

OF **Descrambler Output Format** **5**
Writing to the OF bit sets the descrambler output mode as shown in the following table.

OF	CO[7:0] Channel Data Out
0	Serial Channel Output Mode
1	Parallel Channel Output Mode

In Serial Channel Output mode, one bit of decoded data is presented on the CO[0] pin every PCLK cycle. In Parallel Channel Output mode, one byte of decoded data is presented on the CO[7:0] channel data out bus every eight PCLK cycles. When serial mode is selected, the BCLKOUT pin is forced LOW. When the SPI_On_Off bit (Group 4, APR 31, bit 5) is a 1, the OF bit is ignored.

Reserved **Reserved** **[4:0]**
The Reserved bits must be set to 0 for proper operation.

3.6.17 PLL Reset (Group 4: APR 18)

Read/Write: Write Only

APR	D7	D0
18	PLL_RESET	

Writing any value to APR 18 generates an internal reset pulse for the PLL module. The L64724 ignores any data on the D[7:0] bus during a write to this register. You should reset the PLL module before operating it.

The PLL Reset register (APR18) cannot be read.

3.6.18 Decimation Filter Control (Group 4: APR 19)

Read/Write: R/W

APR	D7	D5	D4	D3	D2	D0
19	DF_SELECT[2:0]		DF_GAIN[1:0]		DF_RATIO[2:0]	

The Decimation Filter Control register sets clock parameters related to the Demodulator module carrier synchronization logic.

DF_SELECT[2:0]

Decimation Filter Select **[7:5]**

Program the DF_SELECT[2:0] field to select one of the four filters contained in the decimation filter module or to bypass the decimation filter.

DF_SELECT[2:0]			Filter
1	0	0	No Filter (bypass)
0	0	0	Filter 1
0	0	1	Filter 2
0	1	0	Filter 3
0	1	1	Filter 4

DF_GAIN[1:0]

Decimation Filter Gain **[4:3]**

The table below indicates the gain of the decimation filter.

DF_GAIN[1:0]		Gain Factor
0	0	1
0	1	2
1	0	4
1	1	8

DF_RATIO[2:0]

Decimation Filter Ratio **[2:0]**

Program the DF_RATIO[2:0] field to set the amount of decimation. The value indicates the ratio of outgoing to incoming samples at the decimation filter. For more information see Section 5.4, “Decimation Filters,” page 5-4.

DF_RATIO[2:0]			Decimation Ratio
1	0	0	1
0	0	0	1/2
0	0	1	1/4
0	1	0	1/8
0	1	1	1/16

3.6.19 Clock Loop Control 2 (Group 4: APR 20)

The Clock Loop Control 2 register sets the matched filter roll-off factor, used in the Demodulator Module PLL. The register also contains the power down control bit.

Read/Write: R/W

APR	D7	D5	D4	D3	D1	D0
20	Reserved		PD	Reserved		MF_20_35

Reserved **Reserved** **[7:5]**
These Reserved bits must be cleared to 0 for proper operation.

PD **Power Down** **4**
When you set the PD bit to 1, all modules except the asynchronous microprocessor interface are turned off to minimize power consumption. No data processing occurs during power down. When you clear the PD bit to 0, all elements operate. You should apply a reset pulse after you change the PD bit from 1 to 0 (wake-up) before you start processing data.

PD	Definition
0	Normal Operation
1	Device in Power Down Mode

Reserved **Reserved** **[3:1]**
These Reserved bits must be cleared to 0 for proper operation.

MF_20_35 **Matched Filter Roll-Off Factor** **0**
The MF_20_35 bit, when set to 1, selects a roll-off factor of 0.35 for the matched filter in accordance with the DVB specifications. When the MF_20_35 bit is 0, a 0.20 roll-off factor is selected for DSS systems.

MF_20_35	Matched Filter Roll-Off Factor
0	0.20
1	0.35

3.6.20 Clock Divider (Group 4: APR 21)

This register is used to set the division ratio for the sampling clock.

Read/Write: R/W

APR	D7	D6	D5	D4	D0
21	PCLK_INV	PLL_BP	LCLK_OFF	CLK_DIV1[4:0]	

PCLK_INV **PCLK Inversion** **7**
When the PCLK_INV bit is 0, the clock signal generated internally is available on the PCLK pin. When the PCLK_INV bit is 1, the polarity of the PCLK output waveform is inverted.

PLL_BP **PLL Bypass** **6**
When the PLL_BP bit is 0, the internal PLL module is used to generate the clock for the ADC, Demodulator, and FEC modules. When the bit is a 1, the PLL module is bypassed and the PCLK signal is generated by dividing the frequency of CLK by the value of CLK_DIV1. For details, see Chapter 4.

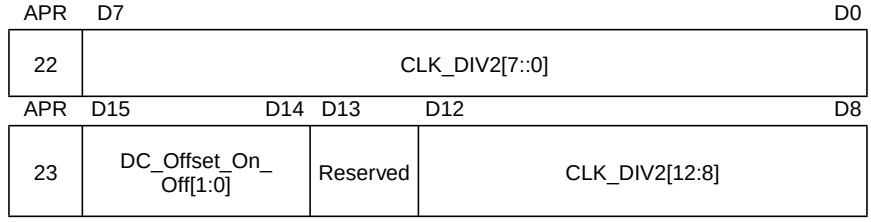
LCLK_OFF **LCLK OFF** **5**
The LCLK_OFF bit, when 0, turns off the LCLK signal. When the LCLK_OFF bit is a 1, the LCLK signal is turned on.

CLK_DIV1 **Input Division Factor for CLK** **[4:0]**
When the PLL module is bypassed (PLL_BP = 1), the CLK_DIV1[4:0] field sets the input division factor for the clock signal supplied to the L64724 on the CLK pin. The CLK_DIV1[4:0] bits are not used when the PLL_BP bit is 0.

3.6.21 Clock Divider 2 (Group 4: APR 22, 23)

This register is used to set the division ratio for the generation of LCLK.

Read/Write: R/W



DC_Offset_On_Off

DC Offset On Off[15:14]
The DC_Offset_On_Off[1:0] bits control the DC offset circuit as shown in the following table.

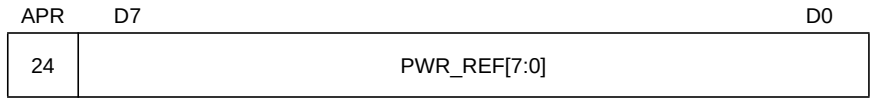
DC_Offset_On_Off[1]	DC_Offset_On_Off[0]	Definition
0	X	DC_Offset OFF
1	0	DC_Offset On; Noise Feedback Off
1	1	DC_Offset On; Noise Feedback On

Reserved **Reserved** **13**
The Reserved bit must always be cleared to 0, and produces random results when read.

CLK_DIV2 **Input Division Factor for LCLK** **[7:0], [12:8]**
The frequency of the output signal LCLK is determined by the value of CLK_DIV2[12:0] as follows:
LCLK = CLK/CLK_DIV2[12:0].

3.6.22 Power Reference Level (Group 4: APR 24)

Read/Write: R/W



This register sets the reference power level for the analog-to-digital converter. For details on setting this register, see Section 5.8.1, “ADC Range and Power Reference,” page 5-20. PWR_REF[7:0] is a positive, unsigned number.

3.6.23 Power Estimation Bandwidth and I/Q DC Offset (Group 4: APR 25)

This register is used to enable internal DC offset compensation on the I and Q signals and sets the power estimation bandwidth.

Read/Write: R/W

APR	D7	D3	D2	D1	D0
25	Reserved		INT_ DC	PWR_BW[1:0]	

Reserved **Reserved** **[7:3]**
The Reserved bits must always be cleared to 0, and will produce random results when read.

INT_DC **Internal DC Offset Compensation on I and Q** **2**
Set the INT_DC bit to 1 to enable internal DC offset compensation on the I and Q signals at the output of the matched filter.

INT_DC	Definition
0	Disabled
1	Enabled

PWR_BW **Power Estimation Bandwidth** **[1:0]**
Program the PWR_BW[1:0] bits to set the power estimation bandwidth. For more information see Section 5.8.2, “Power Control Loop,” page 5-21.

PWR_BW[1:0]		Symbol Rate (MHz)
0	0	20–45
0	1	10–20
1	0	5–10
1	1	2–5

3.6.24 Scale Factor for DEMI and DEMQ Outputs (Group 4: APR 26)

Read/Write: R/W

APR	D7	D0
26	SCALE[7:0]	

Program the SCALE[7:0] bits to set the scale factor for the DEMI and DEMQ outputs from the Demodulator to the FEC decoder. For the relationship between SCALE[7:0] and PWR_REF[7:0], see Section 5.9, “Output Control,” page 5-22. SCALE[7:0] is a positive, unsigned number.

3.6.25 SNR Estimator Threshold (Group 4: APR 27)

Read/Write: R/W

APR	D7	D0
27	SNR_THS[7:0]	

Use this register to set the value that the phase detector’s signal to noise ratio (SNR) comparator uses as a threshold when deciding which gain value to use. For details, see Figure 5.7 in Section 5.7.2, “Carrier Phase Tracking,” page 5-16. SNR_THS[7:0] is an unsigned number.

3.6.26 Carrier Loop Filter Parameters (Group 4: APR 28)

Read/Write: R/W

APR	D7	D4	D3	D0
28	CAR_LAMBDA_SEL[3:0]		CAR_MU_SEL[3:0]	

CAR_LAMBDA_SEL[3:0]

Carrier Loop Lambda **[7:4]**

Program the CAR_LAMBDA_SEL[3:0] field with values that set the parameters of the carrier recovery loop. For details, see Section 5.7.2.2, “Loop Characteristics,” page 5-17.

CAR_MU_SEL[3:0]

Carrier Loop Mu **[3:0]**

Program the CAR_MU_SEL[3:0] field with values that set the parameters of the carrier recovery loop. For details, see Section 5.7.2.2, “Loop Characteristics,” page 5-17.

3.6.27 Carrier Phase Lock Detector Threshold (Group 4: APR 29)

Read/Write: R/W

APR	D7	D0
29	CAR_LC_THSL[7:0]	

The CAR_LC_THSL[7:0] determines the threshold for the Carrier Phase Lock Detector. For details, see Section 5.7.1.5, “Phase Lock Detection,” page 5-15. CAR_LC_THSL[7:0] is an unsigned number.

3.6.28 Reserved (Group 4: APR 30)

Read/Write: R/W

APR	D7	D0
30	Reserved	

Reserved **Reserved** **[7:0]**

The Reserved bits are for LSI Logic internal use only and must be cleared to 0.

3.6.29 Bit/Byte Error Correct and SPI Mode Control (Group 4: APR 31)

The following register controls Reed Solomon Bit/Byte error count selection and the SPI mode selection.

Read/Write: R/W

APR	D7	D6	D5	D4	D0
31	RS Bit/Byte_ Select	Errorout_Invert	SPI_On_Off	Reserved	

RS Bit/Byte_Select

Reed Solomon Bit/Byte Select **7**

The RS Bit/Byte_Select bit controls the Reed-Solomon Corrected Bit Error Count/Byte Error Count selection. When the bit is 1, reading the group 3 registers (APR0 and APR1) yields the Reed-Solomon *byte* error count. When the bit is 0, reading the group 3 registers (APR0 and APR1) yields the Reed-Solomon *bit* error count, which is the CEC multiplied by eight.

Errorout_Invert

ERROROUT Signal Invert **6**

When the Error_Out_Invert bit is 1, the ERROROUT signal polarity is inverted from active-LOW to active-HIGH.

SPI_On_Off **5**

When the SPI_On_Off bit is set to 1, the SPI mode is on. When the bit is 0, the SPI mode is off. When setting this bit, bit 4 of APR63 should also be set appropriately to select the SPI mode.

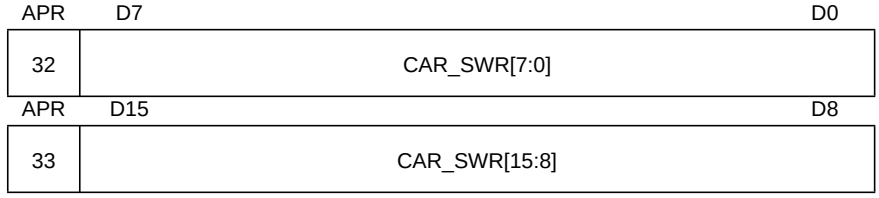
Note: The L64724 Revision B only supports modes 2 and 3 of the SPI specification, NOT mode 1.

Reserved **Reserved** **[4:0]**

These bits are reserved.

3.6.30 Carrier Synchronizer Sweep Rate (Group 4: APR 32 and 33)

Read/Write: R/W



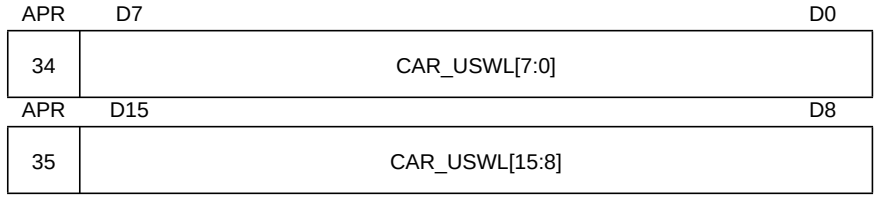
CAR_SWR **Carrier Synchronizer Sweep Rate** **[15:0]**

The CAR_SWR[15:0] value determines the Carrier Synchronizer sweep rate. For details, see Section 5.7.1.3, “Frequency Sweep Rate,” page 5-14. CAR_SWR[15:0] is a signed, two’s complement number.

3.6.31 Carrier Synchronizer Sweep Upper Limit (Group 4: APR 34 and 35)

The values in the CAR_USWL[15:0] register set the upper limits of the frequency sweep. For details, see Section 5.7.1.1, “Frequency Sweep Limits,” page 5-13. CAR_USWL[15:0] is a two’s-complement number.

Read/Write: R/W

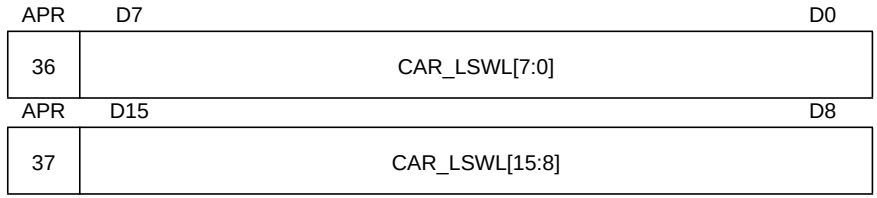


CAR_USWL **Carrier Sweep Upper Sweep Limit** **[15:0]**
Program the CAR_USWL[15:0] bits to set the upper limit of the frequency sweep.

3.6.32 Carrier Synchronizer Sweep Lower Limit (Group 4: APR 36 and 37)

Program the CAR_LSWL[15:0] register to set the lower limit of the frequency sweep. For details, see Section 5.7.1.4, “CAR_SWR,” page 5-14. CAR_LSWL[15:0] is a two’s-complement number.

Read/Write: R/W



CAR_LSWL **Carrier Sweep Lower Sweep Limit** **[15:0]**
Program the CAR_LSWL[15:0] bits to set the lower limit of the frequency sweep.

3.6.33 Carrier Loop Filter Initialization (Group 4: APR 38, 39, and 40)

Program the CAR_LF_INIT[23:0] bits with values that set the content of the Carrier Loop Filter Accumulator. For details, see Section 5.7.2.2, “Loop Characteristics,” page 5-17.

Read/Write: R/W

APR	D7	D0
38	CAR_LF_INIT[7:0]	

APR	D15	D8
39	CAR_LF_INIT[15:8]	

APRS	D23	D16
40	CAR_LF_INIT[23:16]	

CAR_LF_INIT Carrier Loop Filter Init [23:0]

Program the CAR_LF_INIT[23:0] bits to set the value for the accumulator in the loop filter of the carrier recovery loop. CAR_LF_INIT[23:0] is a two’s-complement number.

3.6.34 Carrier Loop Configuration Register (Group 4: APR 41)

This resister contains the various control bits that configure the Carrier Loop Synchronizer Loop logic. For more information, see Section 5.7, “Carrier Recovery Loop,” page 5-12.

Read/Write: R/W

APR	D7	D6	D5	D4 D3	D2	D1	D0
41	CAR_SWP_ SWAP	CAR_ERROR_ SWAP	CAR_AUTO_ SWP	Reserved	CAR_PED_ SEL	CAR_OPEN	CAR_SW

CAR_SWP_SWAP

Swap Carrier Sweep Direction 7

Set the CAR_SWP_SWAP bit to control whether the Carrier acquisition frequency sweep direction is normal or reversed. It should be toggled whenever the carrier

sweep reaches its limit without achieving carrier lock, or when the constellation has locked at 45 degrees.

CAR_SWP_SWAP	Sweep Operation
0	Increasing Frequency
1	Decreasing Frequency

CAR_ERROR_SWAP

Swap Carrier Error Detector **6**

Set the CAR_ERROR_SWAP bit to control the polarity of the Carrier Loop Error detector (NDAML, DDML). When the bit is 1, the polarity of the detector output is inverted.

CAR_ERROR_SWAP	Error Detector Output
0	Normal
1	Inverted

CAR_AUTO_SWP

Automatic Carrier Sweep Control **5**

Set the CAR_AUTO_SWP bit to enable automatic control of the carrier sweep mechanism. When the bit is 1, control of the sweep is handled internally. See Section 5.6, “Timing Clock Recovery,” page 5-8, for more information on carrier sweep.

CAR_AUTO_SWP	Sweep Mode
0	Manual sweep control by user
1	Automatic internal sweep control

Reserved **Reserved** **[4:3]**

The Reserved bits are reserved for internal use only. They should always be cleared to 0, and produce random results when read.

CAR_PED_SEL

Carrier Phase Error Detector Select **2**

Program the CAR_PED_SEL bit to select which phase error estimator will be used for carrier phase tracking. For

details, see Section 5.7.2, “Carrier Phase Tracking,” page 5-16, and Table 5.4.

CAR_PED_SEL	Estimator Selected
0	Decision Directed Maximum Likelihood (DDML)
1	Nondata Aided Maximum Likelihood (NDAML)

CAR_OPEN **Carrier Loop Open** **1**

Set the CAR_OPEN bit to 1 to disable the carrier loop (the carrier loop integrator maintains its current value). When the CAR_OPEN bit is 0, the carrier loop operates normally.

CAR_OPEN	Definition
0	Enable the Carrier Loop
1	Disable the Carrier Loop

CAR_SW **Sweep Enable for Carrier Loop** **0**

Set the CAR_SW bit to 1 to enable the carrier acquisition sweep generator. For more information see Section 5.7.1, “Carrier Acquisition,” page 5-13.

CAR_SW	Definition
0	Sweep mechanism off
1	Sweep mechanism on

3.6.35 Clock Loop Terms (Group 4: APR 42)

Read/Write: R/W

APR	D7	D4	D3	D0
42	CLK_LAMBDA_SEL[7:4]		CLK_MU_SEL[3:0]	

CLK_LAMBDA_SEL

Clock Loop Lambda **[7:4]**

Program the CLK_LAMBDA_SEL[7:4] bits with values that set the parameters of the clock recovery loop. For details, see Section 5.6.1, “Clock Acquisition and Tracking Modes,” page 5-9.

CLK_MU_SEL

Clock Loop Mu **[3:0]**

Program the CLK_MU_SEL[3:0] bits with values that set the parameters of the clock recovery loop. For details, see Section 5.6.1, “Clock Acquisition and Tracking Modes,” page 5-9.

3.6.36 Clock Synchronizer Sweep Rate (Group 4: APR 43 and 44)

This register determines the Clock Synchronizer sweep rate.

Read/Write: R/W

APR	D7						D0
43	CLK_SWR[7:0]						
APR	D15						D8
44	CLK_SWR[15:8]						

CLK_SWR **Clock Synchronizer Sweep Rate** **[15:0]**

CLK_SWR[15:0] is a signed, two’s complement number. For details, see Section 5.6.1.2, “Timing Loop Sweep Equations and Timing Loop Bias,” page 5-11.

3.6.37 Clock Synchronizer Sweep Upper Limit (Group 4: APR 45 and 46)

Read/Write: R/W

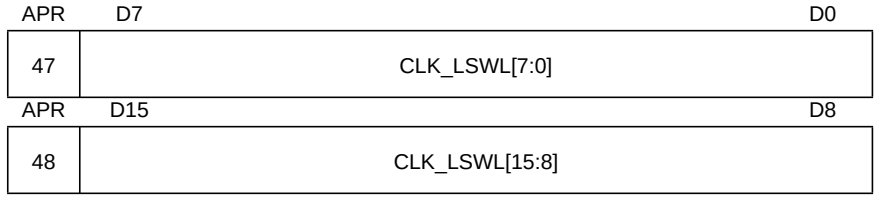
APR	D7						D0
45	CLK_USWL[7:0]						
APR	D15						D8
46	CLK_USWL[15:8]						

CLK_USWL **Clock Sweep Upper Sweep Limit** **[15:0]**

Program the CLK_USWL[15:0] register to set the upper limit of the frequency sweep. For details, see Section 5.6.1.2, “Timing Loop Sweep Equations and Timing Loop Bias,” page 5-11, CLK_USWL[15:0] is a two’s complement number.

3.6.38 Clock Synchronizer Sweep Lower Limit (Group 4: APR 47 and 48)

Read/Write: R/W

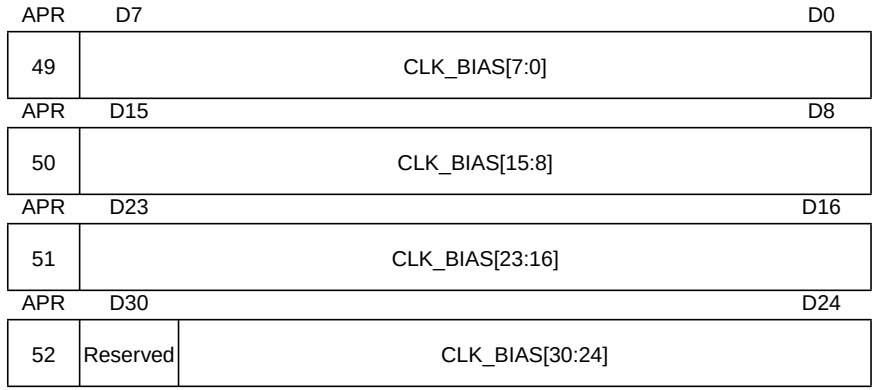


CLK_LSWL **Clock Sweep Lower Sweep Limit** **[15:0]**
Program the CLK_LSWL[15:0] register to set the lower limit of the frequency sweep. For details, see Section 5.6.1.1, “Timing Loop Sweep Limits,” page 5-10.
CLK_LSWL[15:0] is a two’s-complement number.

3.6.39 Clock Loop Bias (Group 4: APR 49 to 52)

Program the CLK_BIAS[30:0] register with values that set the parameters of the clock recovery loop. For details, see Section 5.6.1.2, “Timing Loop Sweep Equations and Timing Loop Bias,” page 5-11.

Read/Write: R/W



Reserved **Reserved** **31**
You must set the Reserved bit to 0 for normal operation.

CLK_BIAS **Clock Loop Bias** **[30:0]**

Program the CLK_BIAS registers to set the value for the bias parameter within the clock recovery loop.

3.6.40 Clock Loop Configuration Register (Group 4: APR 53)

This register contains the various control bits that are used to configure the Clock Synchronizer Loop logic.

Read/Write: R/W

APR	D7	D6	D5	D4	D3	D2	D1	D0
53	CLK_SWP_SWAP	CLK_ERROR_SWAP	CLK_AUTO_SWP	Set to 1	AGC_CLK_SEL	Reserved	CLK_OPEN	CLK_SW

CLK_SWP_SWAP

Swap Clock Sweep Direction **7**

Set the CLK_SWP_SWAP bit to control whether the Clock acquisition frequency sweep direction is normal or reversed. It should be toggled whenever the clock sweep reaches its limit without achieving clock lock.

CLK_SWP_SWAP	Sweep Operation
0	Increasing Frequency
1	Decreasing Frequency

CLK_ERROR_SWAP

Swap Timing Error Detector **6**

Set the CLK_ERROR_SWAP bit to control the polarity of the timing error detector. When the bit is set to 1, the polarity of the detector output is inverted.

CLK_ERROR_SWAP	Error Detector Output
0	Normal
1	Inverted

CLK_AUTO_SWP

Automatic Timing Sweep Control **5**

Set the CLK_AUTO_SWP bit to enable automatic control of the timing sweep mechanism. When set to 1, the control of the sweep is handled internally. See

Section 5.6, “Timing Clock Recovery,” page 5-8, for more information on timing sweep.

CLK_AUTO_SWP	Sweep Mode
0	Manual sweep control by user
1	Automatic internal sweep control

Set to 1 **Set to 1** **4**

This bit must be set to 1 for proper operation.

AGC_CLK_SEL

Sigma-Delta Clocking Select **3**

When the AGC_CLK_SEL bit is 1, the Sigma-Delta module integrates the value continuously at the sampling frequency over all samples. When the bit is 0, the Sigma-Delta module operates on valid symbols only.

AGC_CLK_SEL	Clocking Select
0	Use valid symbols only
1	All samples used for Sigma-Delta

Reserved **Reserved** **2**

This bit is reserved.

CLK_OPEN **Clock Loop Open** **1**

Set the CLK_OPEN bit to disable the clock loop. The clock loop integrator maintains its current value. When the bit is 0, the clock loop operates normally.

CLK_OPEN	Definition
0	Enable the Clock Loop
1	Disable the Clock Loop

CLK_SW **Sweep Enable for Clock Loop** **0**

Set the CLK_SW bit to enable the Clock acquisition sweep generator.

CLK_SW	Definition
0	Sweep mechanism off
1	Sweep mechanism on

3.6.41 Demodulator Configuration Register (Group 4: APR 54)

This register contains the control bits that configure the L64724 Demodulator logic.

Read/Write: R/W

APR	D7	D6	D5	D4	D3	D2	D1	D0
54	SNR_EST	PWRP_TRI	ADC_PD	FP_LOCK_ LEN	PWRP	Reserved		CLK_ ALPHA_ SEL

SNR_EST **SNR Estimator On/Off** **7**

The SNR_EST bit enables or disables the SNR Estimator circuit.

SNR_EST	SNR Estimator
0	Off
1	On

PWRP_TRI **PWRP Signal 3-state Control** **6**

The PWRP_TRI bit, when set, forces the PWRP output pin to a 3-state condition.

PWRP_TRI	PWRP Output Pin
0	Normal
1	3-State

ADC_PD **AD Converter Power-Down** **5**

The ADC_PD bit, when set to 1, turns off the AD Converter module to minimize power consumption. No data processing can occur during power-down. The AD Converter operates at full power when the ADC_PD bit is 0. When the AD Converter experiences a wakeup (ADC_PD bit changes from 1 to 0), apply a reset pulse to the L64724 before processing data.

ACD_PD	Definition
0	ADC operates normally
1	ADC in Power Down Mode

FP_LOCK_LEN

Frequency/Phase Lock Detector Length **4**

The FP_LOCK_LEN bit operates in conjunction with the Carrier Threshold field (Group 4, APR 29) to set the phase lock detector estimation period. For details, see Section 5.7.1.5, “Phase Lock Detection,” page 5-15.

FP_LOCK_LEN	Estimation Period
0	Normal (long)
1	Short

PWRP **PWRP Signal Invert** **3**

The PWRP bit, when set to 1, inverts the polarity of the signal output on the PWRP pin.

PWRP	PWRP Output Pin
0	Normal
1	Inverted

Reserved **Reserved** **[2:1]**

You must set the Reserved bits to 0 for normal operation.

CLK_ALPHA_SEL

Clock Loop Coefficient 0

The CLK_ALPHA_SEL bit configures the coefficient value (ALPHA) for the Interpolator structure within the clock recovery loop. When the bit is 0, the value for ALPHA is 0.43. When the bit is 1, the value for ALPHA is 0.5. The default value for CLK_ALPHA_SEL is 0.

3.6.42 External Output Control Bits and Reset Register (Group 4: APR 55)

This register contains the control bits for the XCTR_OUT[3:0] external output pins and the bits that reset the demodulator and FEC circuitry.

Read/Write: R/W

APR	D7	D6	D5	D2	D1	D0
55	ADC_BP	OB_2C	XCTR[3:0]		DEMOD_RST	FEC_RST

ADC_BP **AD Converter Bypass** **7**

When the ADC_BP bit is 1, the dual AD Converter modules are bypassed and the digital input signals for the I and Q channel are accepted on the IBYPASS[5:0] and QBYPASS[5:0] buses, respectively. When the bit is 0, the AD Converters are active and analog input signals are accepted on the IVIN and QVIN pins.

OB_2C **Input Format Select** **6**

When the OB_2C bit is 0, the input signal to the demodulator module is assumed to be in offset-binary format. When the bit is 1, the signal is assumed to be in two's-complement format. For operation using the AD Converters (ADC_BP = 0) OB_2C should be cleared to 0. When the ADC modules are bypassed (ADC_BP = 1), either format is acceptable through the IBYPASS and QBYPASS buses.

OB_2C	Definition
0	Offset-Binary Format
1	2's-Complement Format

XCTR **External Control Output Bits** **[5:2]**

The value of the XCTR[3:0] field appears on the external output pins XCTR_OUT[3:0] when the Serial_A bit (APR 62) is 0. When the Serial_A bit is 1, the internal microcontroller determines the values on the external output pins XCTR_OUT[3:0]. For more information see Section 5.10, "External Controls," page 5-23, and Appendix C, "Programming the Serializer,".

XCTR[3:0]	Definition
0	Corresponding output pin = VSS
1	Corresponding output pin = VDD

DEMOD_RST

QPSK Demodulator Software Reset **1**

The L64724 resets the internal datapath and the control modules for the QPSK Demodulator when the DEMOD_RST bit is set to 1. The L64724 also resets the demodulator processing unit and state machines to their initial states.The FEC Decoder module is not affected. The bit does not need to be cleared back to 0 to complete the reset. The L64724 issues a single reset pulse each

time the microprocessor writes a 1 to this bit. For additional details, see Section 3.10, “Reset Effect on Register Bits,” page 3-82.

DEMOD_RESET	Definition
0	No Reset
1	L64724 Issues a Demodulator Reset

FEC_RST **FEC Decoder Software Reset** **0**

The L64724 resets the internal datapath and control modules for the FEC portion of the device when the FEC_RST bit is set to 1. The L64724 also resets the FEC processing unit and state machines to their initial states. The demodulator module is not affected. The bit does not need to be cleared back to 0 to complete the reset. The L64724 issues a single reset pulse each time the microprocessor writes a 1 to this bit. For additional details, see Section 3.10, “Reset Effect on Register Bits.”

FEC_RST	Definition
0	No Reset
1	L64724 Issues an FEC Reset

3.6.43 Reserved (Group 4: APR 56 to 58)

Read/Write: R **Reset Value: 0x00**

APR	D7 D0
56	Reserved = 0x00
57	Reserved - 0x00
58	Reserved = 0x14

Reserved **Reserved Bits** **[7:0]**

The Reserved bits are for internal use only. The APR 56 and 57 bits return a value of 0x00 when read, and APR 58 returns a value of 0x14 when read.

3.6.44 Serial Interface to Tuner, Data, and Control (Group 4: APR 59 to 62)

These registers are used to communicate on a serial bus to the tuner using the XCTR[3:0] output pins. Both the host microprocessor and the on-chip microcontroller can write to the registers.

A 390 KHz SCLK for the serial protocol is generated on-chip by dividing the crystal clock (assumed to be 15 MHz) by 38. The SCLK signal is output on the XCTR[1] pin. SDATA for the serial protocol is output on the XCTR[0] pin.

When the Serial_C bit is a 1, a 3-wire protocol is used to transmit the serialized data on XCTR[2:0], with XCTR[2] acting as the ENABLE signal.

Read/Write: R/W

APR	D7	D6	D5	D4	D1	D0
59	Serial Transmission Start Data, TXSD[6:0]					Reserved
60	Serial Transmission Data, STXD[7:0]					
61	Serial Transmission End Data, TXED[7:0]					
62	Serial_B	Serial_C[1:0]		SPI_M[3:0]		Serial_A

TXSD[6:0] Serial Transmission Start Data [7:1]
When the APR 59 register is written, the on-chip serializer module generates the START condition on the SCLK (XCTR[1]) and SDATA (XCTR[0]) pins, serializes and transmits the address in TXSD[7:1] (MSB first), and appends a R/W bit of 0 to indicate a write cycle to the tuner.

STXD[7:0] Serial Transmission Data [7:0]
When the APR 60 register is written, the STXD[7:0] data is serialized and transmitted as the next data byte. The first bit sent serially is the MSB, bit 7. This register is buffered by the serializer so that a second 8-bit data byte can be loaded into STXD before waiting for the previous byte to be serialized. For a detailed description of the cycles, please refer to Appendix C “Programming the Serializer.”

TXED[7:0] **Serial Transmission End Data** **[7:0]**
When the APR 61 register is written, the TXED[7:0] bits are serialized and transmitted as the last serial data byte, and a STOP condition is generated on the SDATA (XCTR[0]) and SCLK (XCTR[1]) pins.

Serial_B **Serial Transmission Control Bit B** **7**
The Serial_B bit indicates whether the host microprocessor or on-chip microcontroller controls the XCTR[2:0] pins. When the bit is 1, the on-chip microcontroller controls the XCTR[2:0] pins. When the bit is 0, the host microprocessor controls the pins.

Serial_C[1:0] **Serial Transmission Control Bit C** **[6:5]**
The Serial_C[1:0] bits control whether the data is serialized with a serial 2-wire or 3-wire protocol. These bits are used to serialize data, as shown in the table below:

Serial_C[1:0]		Selected Function
0	0	Serial 2-Wire Interface
0	1	3-wire interface, ENABLE HIGH for all valid data
1	0	3-wire interface, ENABLE HIGH for 1 clock cycle at the start of data transfer
1	1	3-wire interface, ENABLE HIGH for 1 clock cycle at the end of data transfer

For more details, see Appendix C “Programming the Serializer.”

SPI_M[3:0] **SPI_M** **[4:1]**
The SPI_M[3:0] bits contain the value of the denominator for the Viterbi Code rate.

Serial_A **Serial Transmission Control Bit A** **0**
The Serial_A bit indicates whether the output pins XCTR_OUT[3:0] are to be controlled directly as programmed in the Group 4 APR 55 register “External Control Output Bits,” XCTR[3:0], or by the serializer module with data from the TXSD, STXD, and TXED registers. When the bit is 0 (the default), it indicates that control is as dictated by XCTR[3:0].

3.6.45 FMODE, SPI_CLK_AND, SPI_MODE_A_B, and SPI_N (Group 4: APR 63)

This register is used to configure the SPI Interface.

APR	D7	D6	D5	D4	D3	D0
63	FMODE	SPI_CLK_AND	SPI_MODE_A_B	Reserved	SPI_N[3:0]	

FMODE **BCLK Format** **7**

When the FMODE bit is 1, the descrambler byte clock signal (BCLKOUT) is enabled during the Reed-Solomon check bytes. When the bit is 0, the BCLKOUT signal is disabled during check bytes. Enabling SPI (by setting the SPI_On_Off bit to 1) automatically takes care of setting the proper values for the FMODE bit. The SPI_On_Off bit is located in Group 4, APR 31.

SPI_CLK_AND

SPI_Clock AND'ing **6**

When the SPI_CLK_AND bit is 1, the SPI Byte Clock is logically AND'ed with the DVALIDOUT signal.

SPI_MODE_A_B

SPI Mode Select5

The SPI_MODE_A_B bit selects between SPI Mode A (similar to SPI specification mode 2), and SPI Mode B (similar to SPI specification mode 3). When the bit is 0, Mode A is selected. When the bit is 1, Mode B is selected.

Reserved **Reserved** **4**

This bit is reserved for LSI Logic and must be cleared to 0.

SPI_N **SPI_N** **[3:0]**

The SPI_N[3:0] bits contain the numerator of the Viterbi Code rate.

3.6.46 SPI_Gain[9:0] (Group 4: APR 64 and 65)

This register sets the gain of the SPI Byte Clock generation loop.

Read/Write: R/W

APR	D7	D2	D1	D0
64	SPI_Gain[7:0]			

APR	D15	D10	D9	D8
65	Reserved		SPI_Gain[9:8]	

The SPI_Gain[9:0] value is used to control the loop gain in the SPI Byte Clock generation module. Typical values are 100 for high data rates (no decimation and decimation by 2), 50 for decimation by 4, 25 for decimation by 8, and 10 for decimation by 16.

3.6.47 SPI_Bias (Group 4: APR 66, 67, and 68)

This register sets the bias of the SPI Byte Clock generation loop.

Read/Write: R/W

APR	D7	D0
66	SPI_Bias[7:0]	

APR	D15	D8
67	SPI_Bias[15:8]	

APR	D23	D22	D16
68	Reserved	SPI_Bias[22:16]	

This 23-bit value is determined by Equation 3.9. The value must be rounded to the closest integer.

Equation 3.9

$$Bias = \frac{2^{24} \cdot VCR \cdot F_{symbol}}{F_{sample}}$$

The terms in Equation 3.9 have the following meanings:

Bias = SPI_Bias[22:0]

VCR = Viterbi Code Rate

F_{symbol} = Symbol Clock Frequency

F_{sample} = Sampling Clock Frequency

3.6.48 Timing Lock Detector Threshold (Group 4: APR 69)

This register contains the control bits for the Timing Lock Detector Threshold.

Read/Write: R/W

APR	D7	D0
69	Timing Lock Detector Threshold, CLK_LC_THSL[7:0]	

CLK_LC_THSL[7:0]

Timing Lock Detector Threshold Select [7:0]

Program these bits to select the threshold values for the timing lock detector mechanism.

3.7 Group 5: Self-Tuning Microcontroller Registers

Group 5 contains the memory space for instructions and configuration for the microprogrammed controller (uC). The registers can be accessed through the chip-level serial or parallel interface[1].

Note: These registers are write-only and the internal scratch pad registers are not visible to the host microprocessor.

Table 3.6 shows the addresses and fields of the Group 5 registers.

Table 3.6 Group 5 Register Map

APR	D7	D6	D5	D4	D3	D2	D1	D0
0	uC-Instruction 0 [7:0]							
1	Unused				uC Instruction 0 [11:8]			
(Sheet 1 of 2)								

1. Serial Mode is the recommended interface mode. LSI Logic does not recommend parallel mode for new designs.

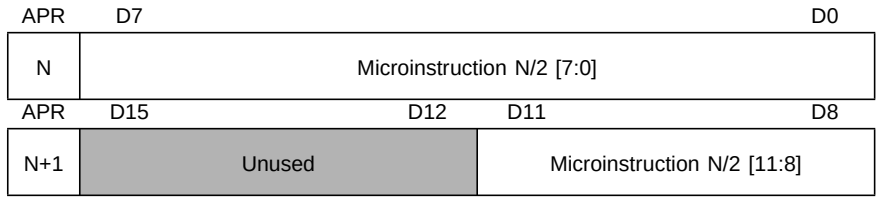
Table 3.6 Group 5 Register Map (Cont.)

APR	D7	D6	D5	D4	D3	D2	D1	D0
2	uC-Instruction 1 [7:0]							
3	Unused				uC Instruction 1 [11:8]			
. . .								
510	uC-Instruction 255 [7:0]							
511	Unused				uC Instruction 255 [11:8]			
512	Reserved							
513	Reserved							
514	Reserved							
515	Reserved							
516	Reserved							
517	Reserved							
518	Reserved							
519	Reserved							
520	uC Configuration [4:0]					Arbitra-tion_On	Reset_ Mode	Micro_ Enable
(Sheet 2 of 2)								

3.7.1 Microcontroller Instructions (Group 5: 0 to 511)

The first 512 locations in group 5 (0–511) are occupied by microinstructions for the Demodulator Control Module. Each 12-bit microinstruction is distributed over two address locations of the APR.

Read/Write: W



The value of N ranges from 0 to 510.

3.7.2 Reserved (Group 5: APR 512 to 519)

APR 512 to 519 are reserved for LSI Logic internal use only. They must be cleared to 0.

Read/Write: W **Reset Value: 0x00**

APR	D7 D0
512	Reserved
513	Reserved
514	Reserved
515	Reserved
516	Reserved
517	Reserved
518	Reserved
519	Reserved

3.7.3 Microcontrol Enable and Configuration (Group 5:APR 520)

APR 520 contains the enable and configuration mechanism for the microcontroller.

Read/Write: W **Reset Value: 0x00**

APR	D7	D3	D2	D1	D0
520	uC Configuration [4:0]		Arbitration _On	Reset_ Mode	Micro_ Enable

uC Configuration[4:0]

Microcontrol Configuration **[7:3]**

When a particular bit in the uC Configuration field is set to 1 or 0, it can be used to enable or disable, respectively, portions of the flow chart implemented in the microcontroller program. See Section B.1, “L64724 QPSK Demodulator Acquisition and Debugging Tips,” page B-1, for a sample flowchart.

Arbitration_On

Arbitration On **2**

When the Arbitration_On bit is 1, host microprocessor accesses to the L64724 status and configuration registers (Groups 0 to 5) are allowed while the on-chip uC is running. The host can thus disable the uC by writing into the Micro_Enable bit while the uC is running.

When the Arbitration_On bit is 0, host uP accesses to the L64724 status and configuration registers (Groups 0 to 5) are not allowed while the on-chip uC is running. The host can then disable the uC when it is running only by writing into Group 7 (A[2:0] = 0b111). For more details, see the Group 7 registers description.

Reset_Mode **Reset Mode** **1**

When the Reset_Mode bit is 1, the uC does not reset its instruction pointer to 0 when disabled while running, and resumes at the instruction it was last decoding when enabled again.

When the bit is 0, the uC resets its instruction pointer to 0 on being disabled. It also resets all internal scratch pad registers, uC_status registers (Group 3, APR 17 to 21), and associated interrupt bits.

Micro_Enable

Demodulator Micro Control Enable **0**

When the Micro_Enable bit is 1, the L64724 internal microcontroller for the demodulator section starts operation. In this mode, the demodulator acquires synchronization for carrier and symbol timing without the intervention of the external microprocessor. When the bit is 0, the microcontrol unit in the demodulator is disabled and the acquisition operation must be performed through the serial or parallel microprocessor interface[1].

Micro_ Enable	Definition
0	Microcontroller disabled. Acquisition through Microprocessor Interface.
1	Microcontroller enabled. Automatic internal demodulator acquisition.

3.8 Group 6: Reserved (Internal Use Only)

3.9 Group 7: Arbiter Control Register

Group 7 contains the memory space for internal control of the microcontroller/microprocessor arbitration module. APR 0 contains the Microcontroller Disable mechanism.

Read/Write: R **Reset Value: 0x00**

APR	D7	D0
0	Microcontroller Disable	

Microcontroller Disable **[7:0]**

A write operation to Group 7 disables the on-chip microcontroller when it is running. A Group 7 write can be used if the microcontroller/host microprocessor arbitration register is disabled, which means that host

1. Serial Mode is the recommended interface mode. LSI Logic does not recommend parallel mode for new designs.

microprocessor write operations to Groups 0 to 6 are disallowed while the on-chip microcontroller is enabled.

The operation can be described as follows: at power-up the Micro_Enable (Group 5, APR 520) bit is cleared to 0. The external microprocessor loads register Groups 2 and 4, then loads the micro instructions into Group 5. At this point, the Micro_Enable bit in Group 5 is set to 1.

If the uC Configuration[2] bit is cleared to 0 (indicating that arbitration is turned off), further host microprocessor writes to the uC Configuration and Micro_Enable bits in Group 5 are not allowed while the on-chip microcontroller is running. The host microprocessor then shuts off the on-chip microcontroller by writing to Group 7.

If the uC Configuration[2] bit is set to 1 (indicating that arbitration is turned on), further host microprocessor writes to all register groups are allowed, and the host microprocessor can disable the microcontroller by writing either to Group 7 or to the Micro_Enable bit in Group 5.

3.10 Reset Effect on Register Bits

This section contains a summary table showing how various reset operations affect the L64724 register bits. The following reset operation abbreviations appear in the table:

- HR–Hardware reset through the L64724 RESET pin.
- SF–Software reset for the FEC module (FEC_RST bit).
- SD–Software reset for the Demodulator module (DEMOD_RST bit)
- UR–Microcontroller reset based on the falling edge of the Micro_Enable bit (Group 5, APR 520), with the Reset Mode bit (Group 5, APR 520) cleared to 0.
- NR–Not affected by any reset.

Table 3.7 Reset Map

Group	APR	Name	D7	D6	D5	D4	D3	D2	D1	D0
0	0	APR0	NR (all bits)							
1	0	APR1	NR (all bits)							
2	0	SMR/ STS	HR, SF (all bits)							
	1		HR, SD (all bits)							
	2		HR, SD (all bits)							
	3		HR, UR (all bits)							
3	0–5	STATUS	HR, SF for all bits of APR 0–5							
	6		HR, SD	NR	Not Used					NR
	7–10		HR, SD (all bits)							
	11		HR, SF	HR, UR	HR, SD			HR, SF		
	12		Not Used		NR	NR	NR	NR	NR	NR
	13		Not Used		NR	NR	NR	NR	NR	NR
	14		Not Used			NR	NR	HR, SF		
	15		HR, SF (all bits)							
	16		HR, SF (all bits)							
	17		UR (all bits)							
	18									
	19									
	20									
	21									
	22		HR, SD (all bits)							
	23		Not Used				HR, SD (all bits)			

(Sheet 1 of 2)

Table 3.7 Reset Map (Cont.)

Group	APR	Name	D7	D6	D5	D4	D3	D2	D1	D0
4	0–69	CONFIG	NR (all bits)							
5	0–511	MICRO CONTROL	NR (all bits)							
	512–519		HR (all bits)							
	520		HR							HR or Group 7 access
6	Reserved									
7	HR (all bits)									
(Sheet 2 of 2)										

3.11 Internal Data Path Reset Effects

Hardware reset through the L64724 RESET pin (HR) and Software reset for the Demodulator module (SD) affect the Demodulator. HR and Software reset for the FEC module (SR) affect the FEC module.

Chapter 4
Channel Interfaces and Data Control

The L64724 interface supports two independent interfaces for incoming channel data and for decoded output data. Both interfaces are used simultaneously. The input interface transfers data from an external device to the L64724's internal ADC module. The output interface transfers data from the L64724 to the next processing device, typically an MPEG-2 transport demultiplexer such as the LSI Logic L64007/8. This chapter contains the following sections:

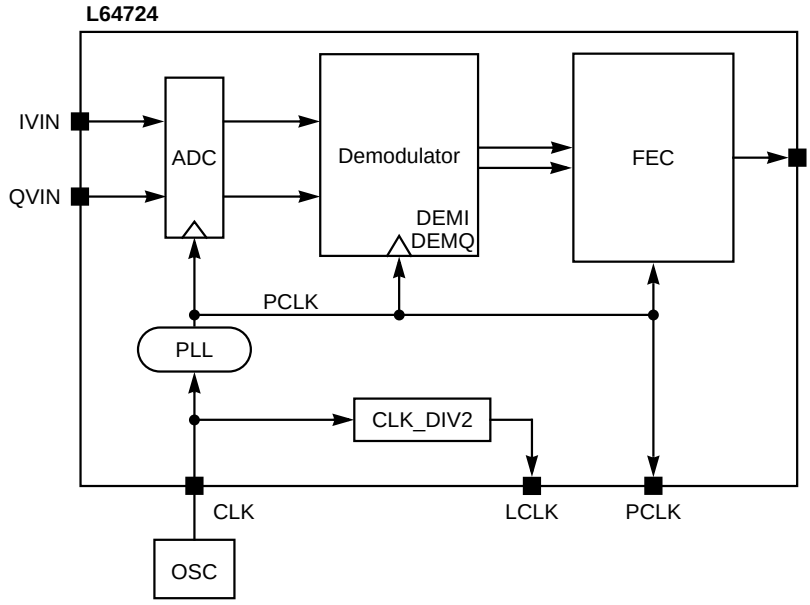
- Section 4.1, "Data Control and Clocking Schemes"
- Section 4.2, "PLL Clock Generation"
- Section 4.3, "Data Path Input Interface"
- Section 4.4, "Data Output Interface"

4.1 Data Control and Clocking Schemes

The L64724 uses the CLK input clock signal to accommodate a number of possible configurations in a channel decoding system. An external crystal oscillator generates the CLK signal. An on-chip PLL derives the PCLK sampling signal from the CLK signal. The PCLK signal operates the ADC, demodulator, and FEC modules. LCLK is generated by dividing the CLK signal by the CLK_DIV parameter.

Note that due to the demodulator architecture chosen, the output data stream always exhibits a certain degree of burstiness.

Figure 4.1 L64724 Clocking: Internal PLL



4.2 PLL Clock Generation

The data control and clocking schemes presented in Section 4.1, “Data Control and Clocking Schemes,” page 4-2, outline the requirements for the generation of the external CLK signal required by the L64724. The internal PLL generates the appropriate internal clock signal (PCLK) to operate the ADC, demodulator, and FEC modules. The following clock naming conventions are used in this section:

- CLK–Input Clock supplied to L64724
- PCLK–Sampling clock used to operate the ADC, demodulator, and FEC modules. The on-chip PLL derives the PCLK signal from the CLK signal.
- LCLK–Clock generated by dividing the CLK input signal by the CLK_DIV2 value.

The L64724 contains a clock synthesizer to derive PCLK from CLK. PCLK operates in the range of up to 90 MHz (see Figure 4.2). A common scenario calls for the connection of a 15 or 60 MHz external signal to the CLK pin as the basis for the internal PLL clock generation. It is also possible to reuse the 4 MHz tuner crystal for L64724 clock generation purposes.

The PLL can be configured to handle clock ratios for all data rates up to 45 Mbaud. The following registers must be set to derive the appropriate clock frequencies:

- PLL_T[4:0] (Group 4, APR 2)
- PLL_N[5:0] (Group 4, APR 0)
- PLL_S[5:0] (Group 4, APR 1)
- PLL_M[1:0] (Group 4, APR 3)

LCLK is derived from CLK as shown in Equation 4.1.

Equation 4.1

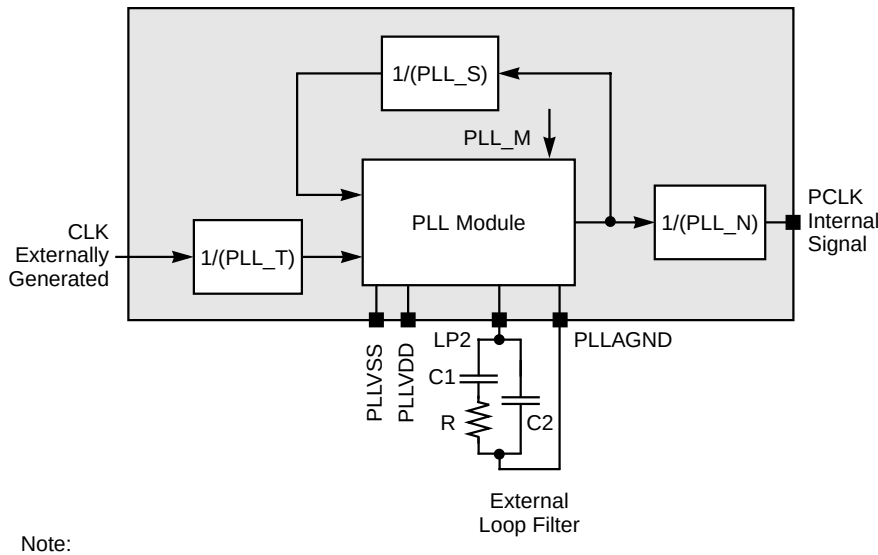
$$LCLK = \frac{CLK}{CLKDIV2}$$

The appropriate PCLK frequency is derived from CLK based on the symbol rate of the underlying data stream and the Viterbi decoder rate chosen. Due to the presence of an interpolator within the demodulator module, PCLK will be slightly higher in frequency than the average sampling rate for the demodulated symbol stream.

Based on the assumption that a 15 MHz external clock is available and that the system data rate is chosen at 26 Mbaud, a sample calculation for the L64724 clocking scheme is given in the following steps:

1. Determine the minimum PCLK required. Based on the data rate of 26 MBaud, a PCLK frequency of at least 52 MHz must be generated.
2. Determine PLL_T, PLL_S, PLL_M and PLL_N from Table 4.1 for the CLK rate of 15 MHz. One acceptable set of values, for example, is PLL_S = 14, PLL_N = 1, PLL_T = 4, and PLL_M = 1.

Figure 4.2 PLL Clock Synthesis



Note:
- R = 200 Ω
- C1 = 10 nF
- C2 = 20 pF

The example values for PLL_S, PLL_N, PLL_T, and PLL_M to cover the frequency range from 2 to 90 MHz for PCLK based on a 15 MHz external source and a 4 MHz source are tabulated in Table 4.1 and Table 4.2. The formula used for these tables is shown in Equation 4.2.

Equation 4.2

$$Fpclk = Fxtal \times \frac{PLL\_S}{PLL\_N \times PLL\_T}$$

The PLL_M value selects the minimum and maximum VCO range.

Table 4.1 Parameters for Crystal Clock (CLK) = 15 MHz

PLL_S [5:0]	PLL_N [5:0]	PLL_T [4:0]	PLL_M [1:0]	VCO (min)	VCO (max)	PCLK
12	1	2	3	70	90	90.00
58	1	10	3	70	90	87.00
46	1	8	3	70	90	86.25
34	1	6	3	70	85	85.00
56	1	10	3	70	85	84.00
22	1	4	3	70	85	82.50
54	1	10	3	70	85	81.00
32	1	6	3	70	85	80.00
42	1	8	3	70	85	78.75
62	1	12	3	70	85	77.50
10	1	2	3	70	85	75.00
58	1	12	3	70	85	72.50
38	1	8	3	70	85	71.25
28	1	6	2	60	70	70.00
46	1	10	2	60	70	69.00
18	1	4	2	60	70	67.50

(Sheet 1 of 4)

Table 4.1 Parameters for Crystal Clock (CLK) = 15 MHz (Cont.)

PLL_S [5:0]	PLL_N [5:0]	PLL_T [4:0]	PLL_M [1:0]	VCO (min)	VCO (max)	PCLK
44	1	10	2	60	70	66.00
26	1	6	2	60	70	65.00
34	1	8	2	60	70	63.75
50	1	12	2	60	70	62.50
4	1	1	1	50	60	60.00
46	1	12	1	50	60	57.50
30	1	8	1	50	60	56.25
22	1	6	1	50	60	55.00
36	1	10	1	50	60	54.00
14	1	4	1	50	60	52.50
48	1	14	1	50	60	51.43
20	1	6	0	40	50	50.00
26	1	8	0	40	50	48.75
38	1	12	0	40	50	47.50
6	1	2	0	40	50	45.00
34	1	12	0	40	50	42.50
22	1	8	0	40	50	41.25
38	1	14	0	40	50	40.71
42	2	8	3	70	85	39.38
62	2	12	3	70	85	38.75
10	2	2	3	70	85	37.50
58	2	12	3	70	85	36.25
38	2	8	3	70	85	35.62

(Sheet 2 of 4)

Table 4.1 Parameters for Crystal Clock (CLK) = 15 MHz (Cont.)

PLL_S [5:0]	PLL_N [5:0]	PLL_T [4:0]	PLL_M [1:0]	VCO (min)	VCO (max)	PCLK
46	2	10	2	60	70	34.50
18	2	4	2	60	70	33.75
26	2	6	2	60	70	32.50
34	2	8	2	60	70	31.88
4	2	1	1	50	60	30.00
46	2	12	1	50	60	28.75
22	2	6	1	50	60	27.50
14	2	4	1	50	60	26.25
48	2	14	1	50	60	25.71
26	2	8	0	40	50	24.38
38	2	12	0	40	50	23.75
6	2	2	0	40	50	22.50
34	2	12	0	40	50	21.25
22	2	8	0	40	50	20.62
42	4	8	3	70	85	19.69
10	4	2	3	70	85	18.75
38	4	8	3	70	85	17.81
18	4	4	2	60	70	16.88
34	4	8	2	60	70	15.94
46	4	12	1	50	60	14.38
22	4	6	1	50	60	13.75
62	6	12	3	70	85	12.92
38	4	12	0	40	50	11.88

(Sheet 3 of 4)

Table 4.1 Parameters for Crystal Clock (CLK) = 15 MHz (Cont.)

PLL_S [5:0]	PLL_N [5:0]	PLL_T [4:0]	PLL_M [1:0]	VCO (min)	VCO (max)	PCLK
26	6	6	2	60	70	10.83
42	8	8	3	70	85	9.84
38	8	8	3	70	85	8.91
34	8	8	2	60	70	7.97
46	10	10	2	60	70	6.90
38	8	12	0	40	50	5.94
46	14	10	2	60	70	4.93
34	16	8	2	60	70	3.98
62	26	12	3	70	85	2.98
18	34	4	2	60	70	1.99
38	48	12	0	40	50	0.99

(Sheet 4 of 4)

Table 4.2 Parameters for Crystal Clock (CLK) = 4 MHz

PLL_S [5:0]	PLL_N [5:0]	PLL_T [4:0]	PLL_M [1:0]	VCO (min)	VCO (max)	PCLK
45	1	2	3	70	90	90.00
22	1	1	3	70	90	88.00
43	1	2	3	70	90	86.00
42	1	2	3	70	90	84.00
41	1	2	3	70	90	82.00
20	1	1	3	70	90	80.00
39	1	2	3	70	90	78.00

(Sheet 1 of 4)

Table 4.2 Parameters for Crystal Clock (CLK) = 4 MHz (Cont.)

PLL_S [5:0]	PLL_N [5:0]	PLL_T [4:0]	PLL_M [1:0]	VCO (min)	VCO (max)	PCLK
38	1	2	3	70	90	76.00
37	1	2	3	70	90	74.00
18	1	1	3	70	90	72.00
35	1	2	2	60	70	70.00
34	1	2	2	60	70	68.00
33	1	2	2	60	70	66.00
16	1	1	2	60	70	64.00
31	1	2	2	60	70	62.00
30	1	2	1	50	60	60.00
29	1	2	1	50	60	58.00
14	1	1	1	50	60	56.00
27	1	2	1	50	60	54.00
26	1	2	1	50	60	52.00
25	1	2	0	40	50	50.00
12	1	1	0	40	50	48.00
23	1	2	0	40	50	46.00
45	2	2	3	70	90	45.00
22	1	2	0	40	50	44.00
43	2	2	3	70	90	43.00
42	2	2	3	70	90	42.00
41	2	2	3	70	90	41.00
10	1	1	0	40	50	40.00
39	2	2	3	70	90	39.00

(Sheet 2 of 4)

Table 4.2 Parameters for Crystal Clock (CLK) = 4 MHz (Cont.)

PLL_S [5:0]	PLL_N [5:0]	PLL_T [4:0]	PLL_M [1:0]	VCO (min)	VCO (max)	PCLK
38	2	2	3	70	90	38.00
37	2	2	3	70	90	37.00
18	2	1	3	70	90	36.00
35	2	2	2	60	70	35.00
34	2	2	2	60	70	34.00
33	2	2	2	60	70	33.00
16	2	1	2	60	70	32.00
31	2	2	2	60	70	31.00
30	2	2	1	50	60	30.00
29	2	2	1	50	60	29.00
14	2	1	1	50	60	28.00
27	2	2	1	50	60	27.00
26	2	2	1	50	60	26.00
25	2	2	0	40	50	25.00
12	2	1	0	40	50	24.00
23	2	2	0	40	50	23.00
22	2	2	0	40	50	22.00
42	4	2	3	70	90	21.00
10	2	1	0	40	50	20.00
38	4	2	3	70	90	19.00
18	4	1	3	70	90	18.00
34	4	2	2	60	70	17.00
16	4	1	2	60	70	16.00

(Sheet 3 of 4)

Table 4.2 Parameters for Crystal Clock (CLK) = 4 MHz (Cont.)

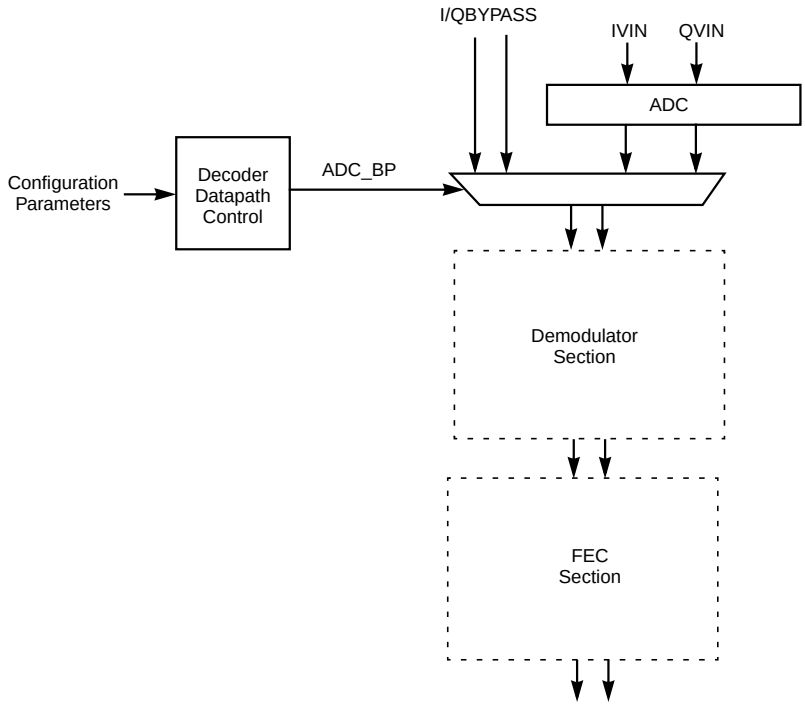
PLL_S [5:0]	PLL_N [5:0]	PLL_T [4:0]	PLL_M [1:0]	VCO (min)	VCO (max)	PCLK
30	4	2	1	50	60	15.00
22	6	1	3	70	90	14.67
20	6	1	3	70	90	13.33
38	6	2	3	70	90	12.67
34	6	2	2	60	70	11.33
16	6	1	2	60	70	10.67
38	8	2	3	70	90	9.50
22	10	1	3	70	90	8.80
38	10	2	3	70	90	7.60
34	10	2	2	60	70	6.80
20	14	1	3	70	90	5.71
22	18	1	3	70	90	4.89
42	22	2	3	70	90	3.82
22	30	1	3	70	90	2.93
22	46	1	3	70	90	1.91
14	58	1	1	50	60	0.97

(Sheet 4 of 4)

4.3 Data Path Input Interface

The L64724 provides a mechanism to select the input data path configurations. Figure 4.3 shows the internal blocks in the decoding pipeline.

Figure 4.3 L64724 Functional Blocks in the Decoding Pipeline



The user can select one of two datapath options:

- No ADC Bypass
- Bypass ADC

To select an input configuration, the external microcontroller must set the input selector ADC_BP (Group 4, APR 55, bit 7) to enable the appropriate functional blocks. See the description for ADC_BP in Chapter 3 for details.

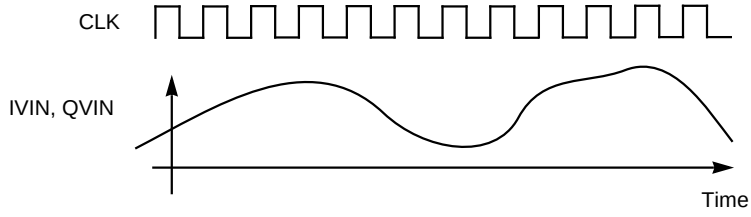
Table 4.3 Input Configuration

ADC_BP (APR 55, bit 7)	Input Mode Chosen
0	ADC, Demod and FEC sections active
1	Demod and FEC sections active, ADC bypassed

4.3.1 ADC, Demodulator, and FEC Active

You can supply data to the ADC modules and the subsequent demodulator and FEC sections by clearing the ADC_BP bit to 0. Figure 4.4 shows the channel analog data input signals IVIN and QVIN as well as the input signal CLK used in this input configuration.

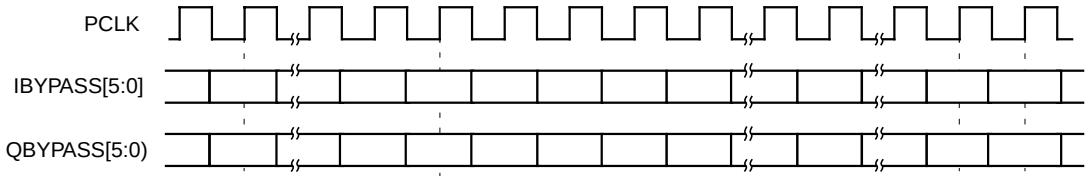
Figure 4.4 CLK and Analog Inputs for Channel Data Input



4.3.2 ADC Bypassed with Demodulator and FEC Active

Setting the ADC_BP bit to 1 bypasses the ADC and supplies data directly to the demodulator section. Figure 4.5 shows the channel digital input signals IBYPASS[5:0] and QBYPASS[5:0] as well as the PLL-generated signal PCLK used in this input configuration.

Figure 4.5 CLK and Digital Inputs for ADC Bypass Mode



4.4 Data Output Interface

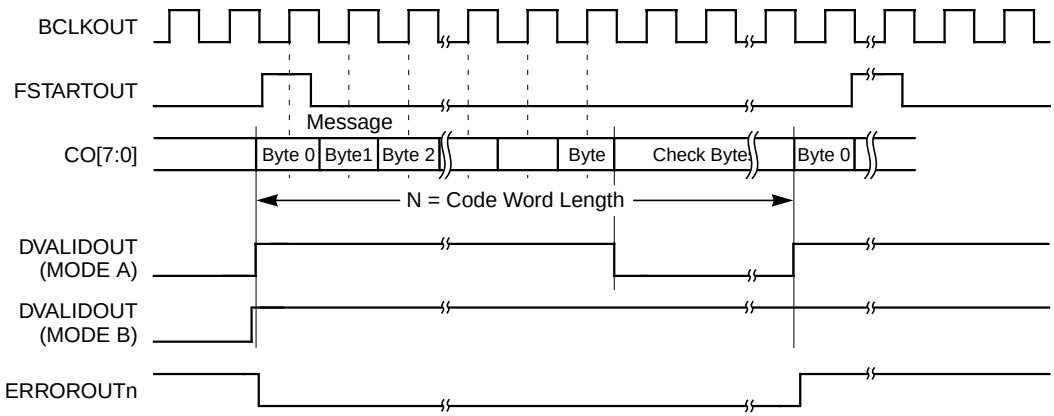
The L64724 provides a mechanism to observe different outputs of the decoding pipeline. This feature simplifies performance characterization and system diagnostics tasks. Figure 4.3 shows the functional blocks in the decoding pipeline.

The user can observe the outputs from the Descrambler and the parallel interface module through the CO[7:0], DVALIDOUT, ERROROUTn, FSTARTOUT, and BCLKOUT output signals. To select an output, the external microcontroller must set the following output selector bits in Group 4: SPI_On_Off, SPI_MODE_A_B, SPI_CLK_AND, and OF. These bits enable the appropriate functionality, as shown in Table 4.4 and Figure 4.6.

Table 4.4 Output Selection

SPI_On_Off	SPI_MODE_A_B	SPI_CLK_AND	OF	Functionality chosen
0	X	X	0	Descrambler Serial Output;
0	X	X	1	Descrambler Parallel Output (BCLKOUT is a data strobe)
1	0	0	X	Descrambler Parallel Output (Mode A)
1	0	1	X	Descrambler Parallel Output (Mode A, BCLKOUT AND'ed with DVALIDOUT
1	1	0	X	Descrambler Parallel Output (Mode B)
1	1	1	X	Descrambler Parallel Output (Mode B, BCLKOUT AND'ed with DVALIDOUT)

Figure 4.6 Parallel Output Interface Waveforms



4.4.1 Parallel Output Interface (SPI_On_Off = 1)[1]

You can observe the output of the entire decoding pipeline in parallel format. Two main modes exist, determined by the SPI_On_Off configuration bit in Group 4, APR 31, D5.

When the SPI_On_Off bit is set to 1, the parallel output interface outputs data on CO[7:0] in formats that are similar to the specifications for the Synchronous Parallel Interface (SPI). The parallel outputs are available in two modes, Mode A and Mode B. In Mode A, which is similar to mode 2 of SPI, the DVALIDOUT signal is HIGH only during the data bytes and goes LOW during the RS check bytes. In Mode B, which is similar to the SPI mode 3, the DVALIDOUT signal always stays HIGH.

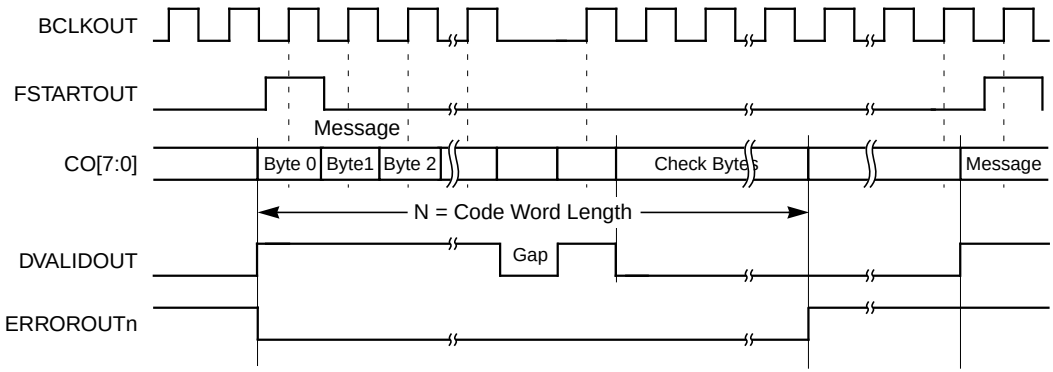
The FSTARTOUT strobe signal overlaps the first data byte. When the SPI_On_Off bit is HIGH, an internal clock generation scheme guarantees exactly 204 byte clock cycles per packet on the BCLKOUT pin as required for the DVB frame format. This ensures that the data stream is devoid of any gaps within a packet boundary and also between packet boundaries. The data is available on the CO[7:0] pins as a continuous flow. The L64724 asserts the BCLKOUT signal in the middle of the decoded data bytes, so the device that receives the output from the L64724 can latch data at the BCLKOUT rate instead of at the PCLK rate.

1. Serial Mode is the recommended interface mode. LSI Logic does not recommend parallel mode for new designs.

4.4.2 Parallel Output Interface (SPI_On_Off = 0)

When the SPI_On_Off bit is 0 and the OF bit is 1, the L64724 outputs one new data byte on the CO[7:0] pins every eight PCLK cycles, as shown in Figure 4.7.

Figure 4.7 Descrambler Parallel Output Waveforms



The FSTARTOUT signal strobe overlaps the first data byte. The L64724 provides the BCLKOUT signal as an additional strobe that has one rising and one falling edge per valid CO[7:0] data byte. The L64724 asserts the BCLKOUT signal in the middle of the decoded data bytes, so the device that receives the output from the L64724 can latch data at the BCLKOUT rate instead of at the PCLK rate.

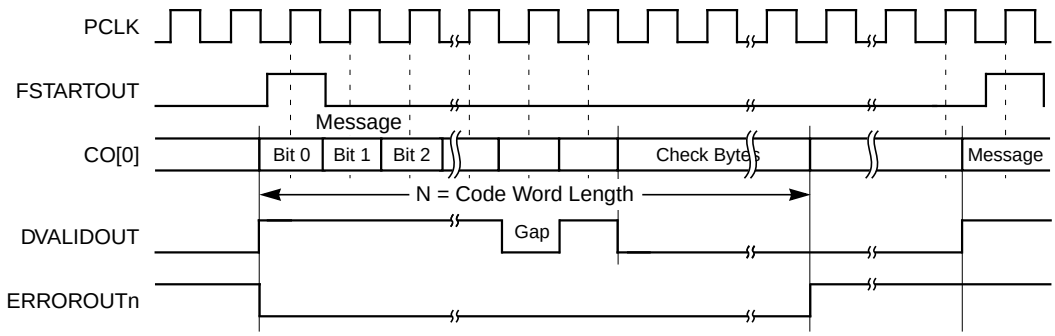
Note that due to the use of a constant sampling frequency and the internal demodulator architecture, the output data stream in the parallel output interface mode contains gaps (when DVALIDOUT is LOW.) The distribution and position in time of the gaps are governed mainly by the ratio of sampling frequency and symbol rate chosen. Gaps can occur at any time in the output data stream.

4.4.3 Serial Output Interface

To observe the output of the entire decoding pipeline in serial format, clear the SPI_On_Off and OF configuration bits to 0.

When the OF bit (Group 4, APR 17) is 0 (Serial Channel Output Mode), the L64724 outputs data bit serially on the CO[0] pin, as shown in Figure 4.8.

Figure 4.8 Descrambler Serial Output Waveforms



The L64724 outputs one new data bit each PCLK cycle. The L64724 asserts the FSTARTOUT signal for one cycle. The FSTARTOUT signal overlaps the first message bit of a Reed-Solomon code word. In the serial output mode, the L64724 chronologically orders the data. The MSB is the oldest output and the LSB is the newest output.

Note that due to the use of a constant sampling frequency and the internal demodulator architecture, the output data stream in this mode contains gaps (when DVALIDOUT is LOW.) The distribution and position in time of the gaps are governed mainly by the ratio of sampling frequency and symbol rate chosen. Gaps can occur at any time in the output data stream.

Chapter 5
Demodulator Module Functional Description

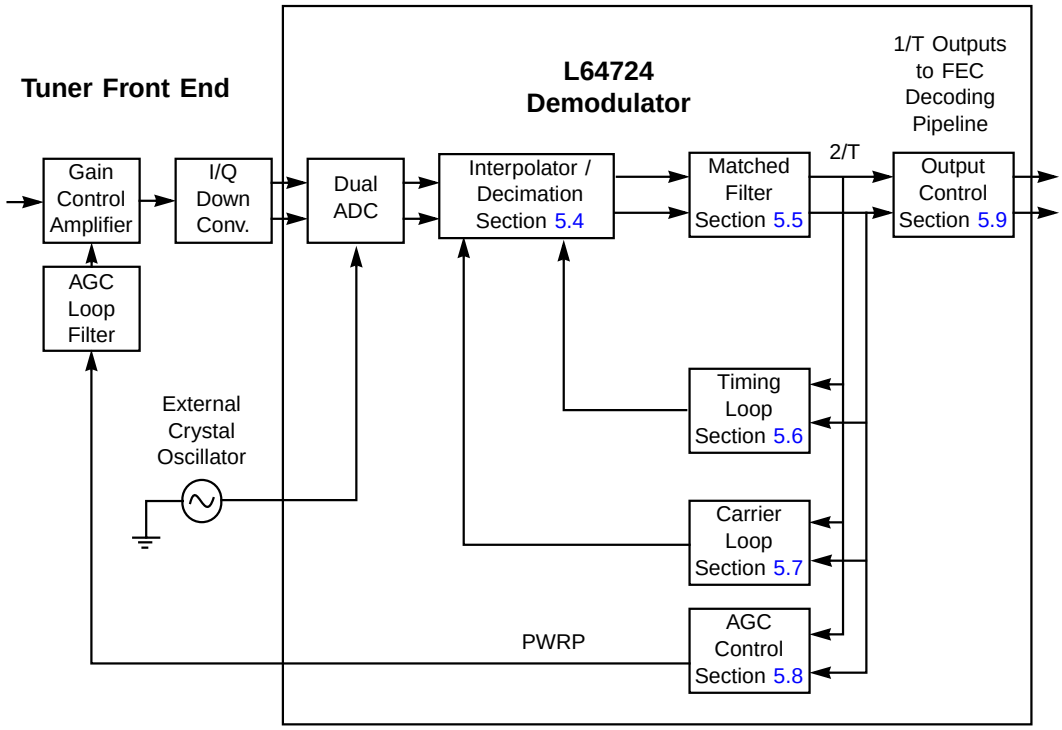
This chapter describes the function of the L64724 BPSK/QPSK Demodulator module and contains the following sections:

- Section 5.1, “Overview”
- Section 5.2, “Analog to Digital Conversion”
- Section 5.3, “DC Offset Compensation and Coupling to ADC Output”
- Section 5.4, “Decimation Filters”
- Section 5.5, “Matched Filter”
- Section 5.6, “Timing Clock Recovery”
- Section 5.7, “Carrier Recovery Loop”
- Section 5.8, “Automatic Gain Control (AGC)”
- Section 5.9, “Output Control”
- Section 5.10, “External Controls”

5.1 Overview

The Demodulator Module connects to the satellite receiver circuitry in the set-top box to recover the modulated MPEG-2 transport stream. Figure 5.1 shows the connections between the BPSK/QPSK Demodulator and its associated circuitry.

Figure 5.1 Demodulator Module and Associated Circuitry

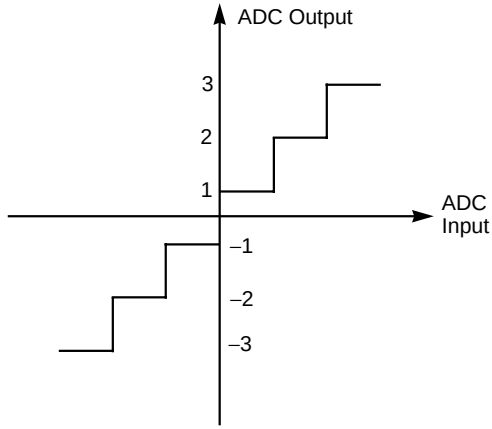


5.2 Analog to Digital Conversion

The L64724 incorporates two ADCs at the front end to receive the incoming analog I and Q data streams. The sampling clock to the ADC is generated by an on-chip PLL module. An externally applied signal on the CLK pin drives the PLL. For a detailed description of the PLL, see Chapter 4, "Channel Interfaces and Data Control."

The internal ADC produces six-bit samples that digitize the analog data streams into 64 discrete values, as shown in Figure 5.2.

Figure 5.2 Input Quantization



5.3 DC Offset Compensation and Coupling to ADC Output

The L64724 provides for an internal suppression of DC offsets on the I and Q channels.

The suppression feature is particularly useful when using an integrated front end that does not provide DC offset compensation pins and that introduces small offsets. DC offset compensation is controlled with the DC_Offset_On_Off[1:0] bits (see Group 4, APR 23). The DC offset compensation can be accomplished with or without noise feedback, whichever best optimizes BER. Noise feedback essentially shapes the quantization error spectrum.

Back end DC offset compensation (after the matched filter) is also provided and can be used if necessary. To enable this function, set the INT_DC bit to 1 (Group 4, APR 25).

5.4 Decimation Filters

The L64724 implements decimation filters on each I and Q branch. The following decimation ratios can be selected through the DF_RATIO parameter (Group 4, APR 19): 1, 1/2, 1/4, 1/8 and 1/16. These two filters enable the ADC to operate at an oversampling ratio of N > 2. The filters operate at the ADC sampling rate and generate down-sampled I and Q streams from the sampled I and Q inputs. The decimation and the sampling rate are configured to provide the highest possible number of samples per symbol with the tightest decimation filter available. The procedure is outlined in Table 5.1 and the results are shown in Table 5.2.

Table 5.1 Decimation Procedure

Rs Threshold (MS/s[1])	DF_RATIO	DF_SELECT	DF_GAIN	Group 4, Register 19 Setting		Fs (MHz)
				Binary	Hex	
45 to 44.5	1	0	1	10000100	0x84	91.5 (N = 1, S = 61, T = 10, M = 3
44.5 to 30	1	0	1	10000100	0x84	See footnote[2]
30 to 15	1	1	1	00000100	0x04	See footnote
15 to 7.5	2	2	2	00101000	0x28	See footnote
7.5 to 3.75	4	3	4	01010001	0x51	See footnote
3.75 to 1	8	4	8	01111010	0x7A	See footnote

1. Megasymbols per second (MS/s)
2. For Rs <= 44.5 MS/s, calculate the sampling rate as follows: from the set of valid sampling frequency values, (30, 35, 40 ..., 85, 90), select the lower, closest value to 4 * DF_RATIO * Rs/(1 + alpha), where alpha is the “corner” margin (1%).

Table 5.2 Decimation Results

Rb (MS/s)	Sampling Frequency (MHz)	DF_RATIO	Samples per Symbol	DF_FILTER	DF_GAIN
45	91.5	1	2.033	0	1
44.5	90	1	2.022	0	1
44	90	1	2.045	0	1
43	90	1	2.093	0	1
42	90	1	2.143	0	1
41	90	1	2.195	0	1
40	90	1	2.250	0	1
39	90	1	2.308	0	1
38	90	1	2.368	0	1
37	90	1	2.432	0	1
36	90	1	2.500	0	1
35	90	1	2.571	0	1
34	90	1	2.647	0	1
33	90	1	2.727	0	1
32	90	1	2.813	0	1
31	90	1	2.903	0	1
30	90	1	3 000	1	1
29	90	1	3.103	1	1
28	90	1	3.214	1	1
27	90	1	3.333	1	1
26	90	1	3.462	1	1
25	90	1	3.600	1	1
24	90	1	3.750	1	1
23	90	1	3.913	1	1
22.7250	85	1	3.740	1	1
21.4625	80	1	3.727	1	1
20.2000	75	1	3.713	1	1
18.9375	70	1	3.696	1	1
17.6750	65	1	3.678	1	1
16.4125	60	1	3.656	1	1
15.1500	55	1	3.630	1	1

(Sheet 1 of 3)

Table 5.2 Decimation Results (Cont.)

Rb (MS/s)	Sampling Frequency (MHz)	DF_RATIO	Samples per Symbol	DF_FILTER	DF_GAIN
15	90	2	6.000	2	2
14	90	2	6.429	2	2
13	90	2	6.923	2	2
12	90	2	7.500	2	2
11.3625	85	2	7.481	2	2
10.7313	80	2	7.455	2	2
10.1000	75	2	7.426	2	2
9.4688	70	2	7.393	2	2
8.8375	65	2	7.355	2	2
8.2063	60	2	7.312	2	2
7.5750	55	2	7.261	2	2
7.5	90	4	12.000	3	4
7	90	4	12.857	3	4
6	90	4	15.000	3	4
5.6813	85	4	14.961	3	4
5.3656	80	4	14.910	3	4
5.0500	75	4	14.851	3	4
4.7344	70	4	14.785	3	4
4.4188	65	4	14.710	3	4
4.1031	60	4	14.623	3	4
3.7875	55	4	14.521	3	4
3.75	90	8	24.000	4	8
3	90	8	30.000	4	8
2.8406	85	8	29.923	4	8
2.6828	80	8	29.819	4	8
2.5250	75	8	29.703	4	8
2.3672	70	8	29.571	4	8
2.2094	65	8	29.420	4	8
2.0516	60	8	29.246	4	8
1.8938	55	8	29.043	4	8

(Sheet 2 of 3)

Table 5.2 Decimation Results (Cont.)

Rb (MS/s)	Sampling Frequency (MHz)	DF_RATIO	Samples per Symbol	DF_FILTER	DF_GAIN
1.7359	50	8	28.803	4	8
1.5781	45	8	28.515	4	8
1.4203	40	8	28.163	4	8
1.2625	35	8	27.723	4	8
1.1047	30	8	27.157	4	8
1	30	8	30.000	4	8
(Sheet 3 of 3)					

5.5 Matched Filter

The L64724 implements a matched filter with selectable roll-off factor on the I and Q branches according to the DVB standard and DSS specifications, respectively (square root raised cosine shape with roll-off B = 0.35 or 0.20). The roll-off factor is selected through the configuration bit MF_20_35 (Group 4, APR 20, bit 0). The filter operates at a constant input rate of 2/T. The roll-off factor is configured as shown in Table 5.3.

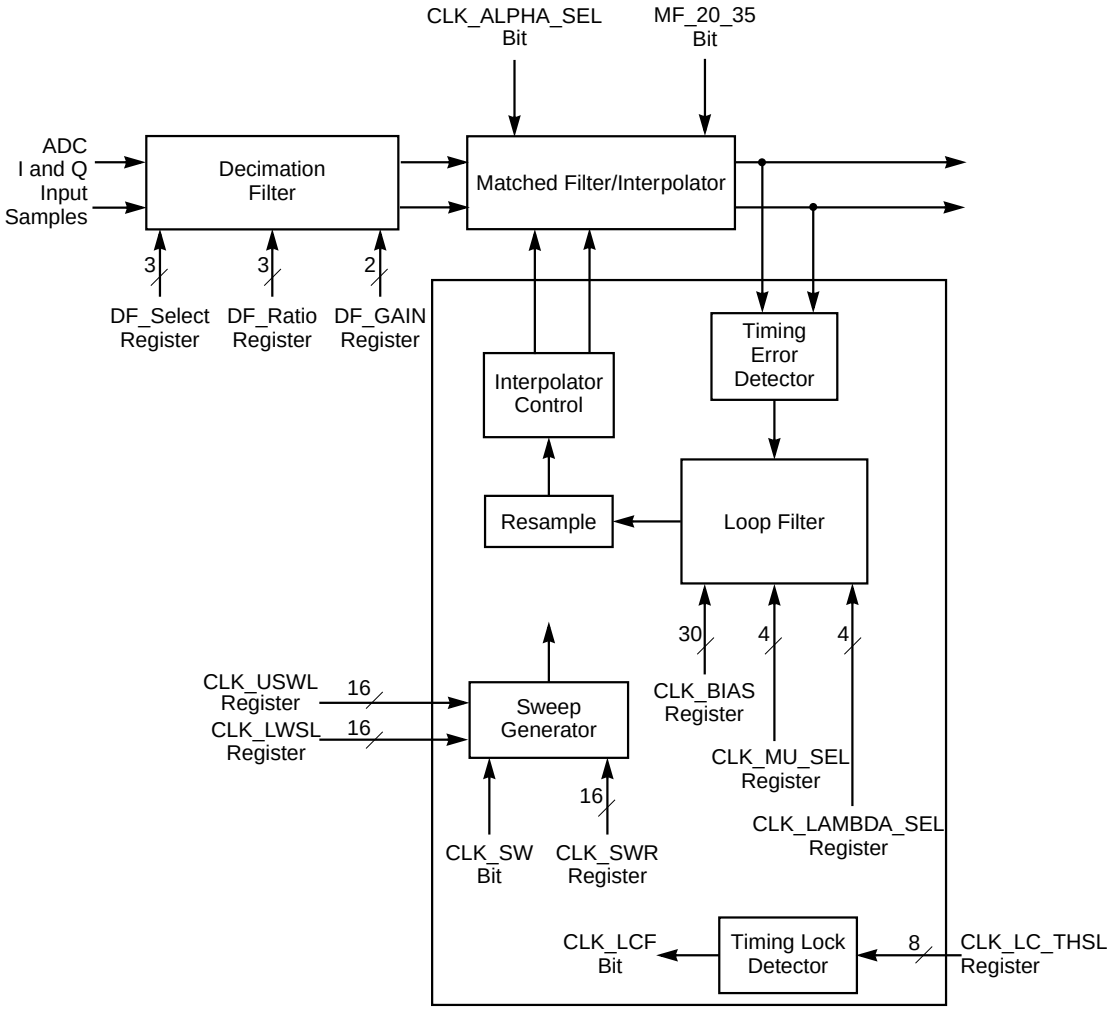
Table 5.3 Roll-Off Factor

MF_20_35	Roll-Off Factor
0	0.20 (DSS)
1	0.35 (DVB)

5.6 Timing Clock Recovery

Figure 5.3 illustrates the Timing Clock Recovery Loop. The L64724 Clock Synchronizer is implemented as an all-digital on-chip module requiring no external circuitry. The Clock Synchronizer generates the loop control signals for an internal NCO and interpolator from the L64724 decimation filter output samples. The main elements in the timing recovery loop are the interpolators for the I and Q components and the timing error detector.

Figure 5.3 Clock Recovery Loop



5.6.1 Clock Acquisition and Tracking Modes

The Clock Recovery Loop operates in two modes:

- Clock Acquisition
- Tracking

In both modes, the Clock Recovery Loop takes its input from the Timing Error Detector (TED).

The internal digital loop filter determines the loop characteristics using parameters CLK_MU_SEL, CLK_LAMBDA_SEL, and CLK_BIAS as well as the gains of the Timing Error Detector and NCO modules.

The CLK_MU_SEL and CLK_LAMBDA_SEL parameters are computed according to Equation 5.1, Equation 5.2, and Equation 5.3.

Equation 5.1 Timing Loop Phase Detector Gain

$$K_{dtim} = 0.0388$$

Equation 5.2 Symbol Time

$$T = \frac{1}{Fb}$$

Equation 5.3 Oversampling Ratio

$$L_{tim} = \frac{Fs}{Fb}\left(\frac{1}{DF\_RATIO}\right)$$

Fs is the sampling frequency, Fb is the baud rate, and DF_RATIO is the decimation filter downsampling ratio, which can be 1, 2, 4, 8, or 16.

Based on the intermediate values τ_a and τ_b, given in Equation 5.4 and Equation 5.5, the values for CLK_MU_SEL and CLK_LAMBDA_SEL are computed in Equation 5.6 and Equation 5.7. The damping factor (ζ) is normally 1.0. The natural frequency (ω_n) of the loop is in radians/sec.

Equation 5.4

$$\tau_a = \frac{\omega_n^2 T^2}{K_{dtim} L_{tim}}$$

Equation 5.5

$$\tau_b = \frac{2\zeta\omega_n T_b}{K_{dtim} L_{tim}}$$

Equation 5.6 CLK_MU_SEL

$$CLK\_MU\_SEL = log_2(\tau_a 2^{28})$$

Equation 5.7 CLK_LAMBDA_SEL

$$CLK\_LAMBDA\_SEL = log_2(\tau_b 2^{16})$$

During timing acquisition, the internal sweep mechanism can be used. To vary the sweep rate, change the value in the CLK_SWR register (Group 4, APR 43 and 44). To start the sweep generator, set the CLK_SW bit (Group 4, APR 53) to 1.

Equation 5.8 gives the suggested value for the timing loop bandwidth.

Equation 5.8

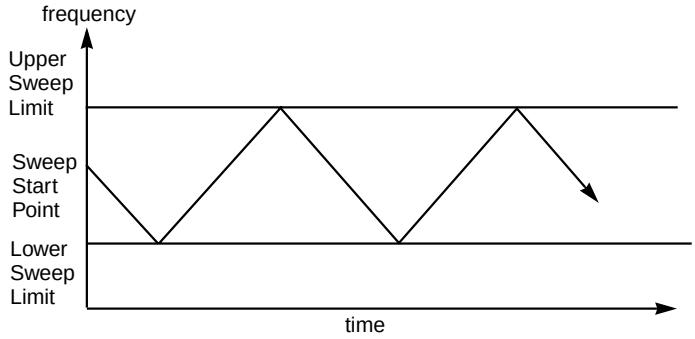
$$timing\_\mathrm{bw}(\omega_n) = 2\pi \times \frac{Rb[MSps]}{10} \quad [\mathrm{Krad/s}]$$

The parameter timing_bw refers to the natural frequency ω_n. Rs is the symbol rate (Rb = 1/Tb). Substitute the value of ω_n from Equation 5.8 into the above equations for τ_a and τ_b.

5.6.1.1 Timing Loop Sweep Limits

The CLK_USWL (Group 4, APR 45 and 46) and CAR_LSWL[15:0] (Group 4, APR 47 and 48) registers set the upper and lower timing loop sweep limits, respectively. Figure 5.4 shows the timing loop sweep operation.

Figure 5.4 Timing Loop Sweep Operation



5.6.1.2 Timing Loop Sweep Equations and Timing Loop Bias

The equations for the sweep rate and sweep limit are given below in Equation 5.9 and Equation 5.10. *Sweeprate* indicates the desired sweep rate in Hz/sec and DF_RATIO is the decimation filter down sampling ratio, which can be 1, 2, 4, 8 or 16. T is the symbol time and Fs is the sampling (A/D) frequency.

Equation 5.9 CLK_SWR

$$CLK\_SWR = \frac{2^{42} \times sweeprate \times Tb}{Fs \times \frac{1}{DF\_Ratio}}$$

Choose CLK_USWL or CLK_LSWL as given in Equation 5.10. *Sweeplimit* indicates the upper desired sweep limit in Hz for CLK_USWL and it indicates the lower limit for CLK_LSWL.

Equation 5.10 CLK_USWL

$$CLK\_XSWL = \frac{2^{24} \times sweeplimit}{Fs \times \frac{1}{DF\_Ratio}}$$

Note that X stands for either U or L. Also, you must set the appropriate sweeplimit.

Choose CLK_BIAS according to Equation 5.11.

Equation 5.11 CLK_BIAS

$$CLK\_BIAS = 2^{27} \times \frac{Fs}{Fb}\left(\frac{1}{DF\_RATIO}\right)$$

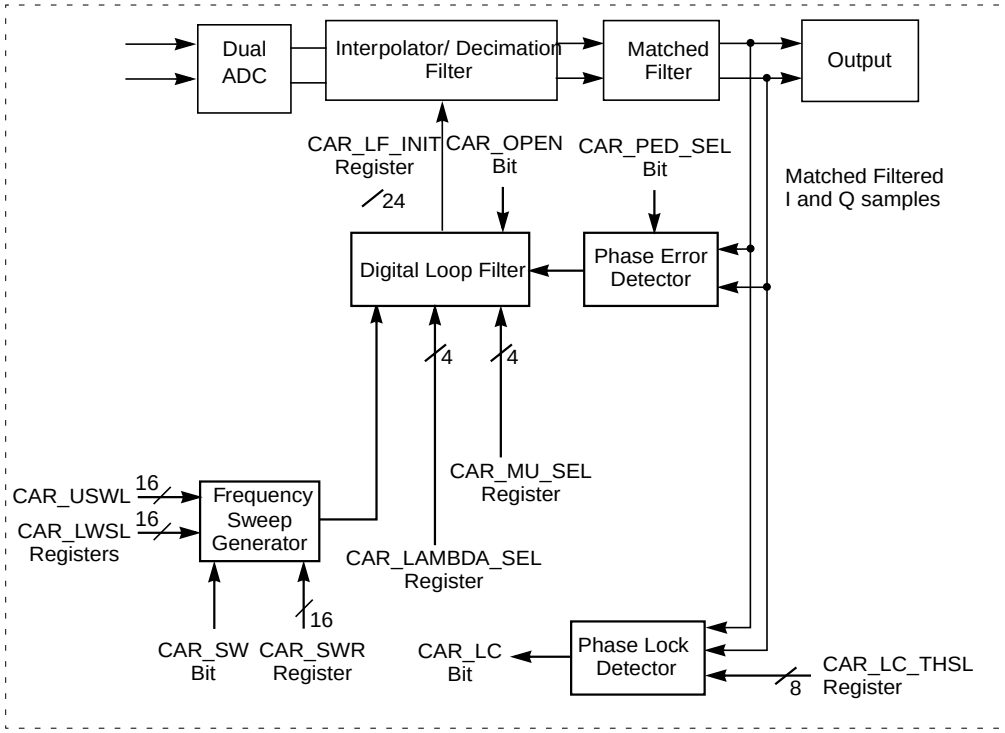
where Fs = sampling frequency, and Fb = baud rate.

5.7 Carrier Recovery Loop

Figure 5.5 illustrates the L64724 Carrier Recovery Loop. This circuit consists of the following main functional elements:

- Phase error detector
- Digital loop filter
- Phase lock detector
- Frequency sweep generator
- Frequency lock detector

Figure 5.5 Carrier Recovery Loop



Because the outputs of off-the-shelf tuners for DVB satellite receivers have a large frequency uncertainty (a common order of magnitude is ± 5 MHz), the L64724 Carrier Synchronizer includes a frequency sweep generator for signal acquisition.

The L64724 implements the entire carrier recovery loop digitally.

5.7.1 Carrier Acquisition

During carrier acquisition, the internal frequency sweep generator searches for the correct frequency. To vary the sweep rate, change the value in the CAR_SWR register (Group 4, APR 32, 33). To start the sweep generator, set the CAR_SW bit (Group 4, APR 41) to 1.

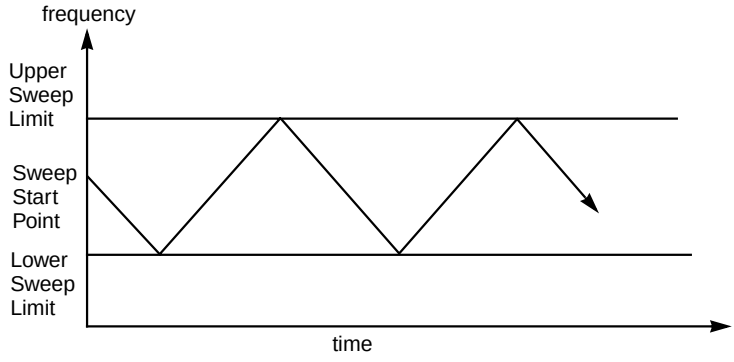
5.7.1.1 Frequency Sweep Limits

The CAR_USWL (Group 4, APR 34, 35) and CAR_LSWL (Group 4, APR 36, 37) registers set the upper and lower limits, respectively, of the frequency sweep.

5.7.1.2 Frequency Sweep

In the case shown in Figure 5.6, both the CAR_USWL (Group 4, APR 34, 35) and CAR_LSWL (Group 4, APR 36, 37) registers must be set. The state of the CAR_SWP_SWAP (Group 4, APR 41) bit controls the sweep direction. Even though the Carrier Synchronizer controls the frequency sweep rate based on the value in the CAR_SWR register (Group 4, APR 32, 33), the microcontroller can monitor the sweep direction itself.

Figure 5.6 Frequency Sweeping



If the CAR_AUTO_SWP (Group 4, APR 41) bit is used, the sweep waveform is similar to that shown in Figure 5.6, where the sweep direction changes once the upper or lower limit is reached.

5.7.1.3 Frequency Sweep Rate

The Carrier Synchronizer determines the frequency sweep rate based on the value in the CAR_SWR register. Set the value in the 16-bit CAR_SWR register based on Equation 5.12.

Equation 5.12

$$Sweep\_Rate = \left(\frac{CAR\_SWR \cdot Fs}{T \times 2^{33}} \right)$$

5.7.1.4 CAR_SWR

The suggested value for CAR_SWR can be derived by calculating the value for *sweep_rate* as shown in Equation 5.14 and substituting it in Equation 5.13.

Equation 5.13

$$CAR\_SWR = \frac{2^{34} \times sweeprate \times Tb}{Fs}$$

Equation 5.14

slow_sweep_rate[MHz/s] = N x Rs[MS/s]
fast_sweep_rate[MHz/s] = M x Rs[MS/s]

Rs is the symbol rate and M and N are as shown in the following table.

Rs (MS/s)	M	N
45 to 15	32	8
15 to 7.5	8	2
7.5 to 3.75	8	1
3.75 to 2	8	1
2 to 1	4	1

To provide reliable acquisition at any signal-to-noise ratio, the microcontroller uses two sweep rates. The fast rate pulls the loop out of

false locks. The parameters in the above table might have to be adjusted at very low rates (< 2 MS/s) for optimal performance, depending on the tuner.

Choose CAR_LSWL and CAR_USWL as given below. *Sweeplimit* indicates the upper desired sweep limit in Hz for CAR_USWL and it indicates the lower limit for CAR_LSWL.

Equation 5.15

$$CAR\_XSWL = \frac{2^{16} \times sweeplimit}{Fs}$$

In order to initialize the carrier frequency deviation to any desired value, use the CAR_LF_INIT register from Group 3. In Equation 5.16, *freqdeviation* is the desired frequency deviation in Hz and Fs is the sampling (A/D) frequency. Calculate CAR_LF_INIT as shown in Equation 5.16.

Equation 5.16

$$CAR\_LF\_INIT = \frac{2^{24} \times freqdeviation}{Fs}$$

The carrier frequency deviation can be read back from CAR_NCOF in Group 3, APR 7, 8, and 9. Equation 5.17 is the equation for frequency deviation.

Equation 5.17

$$frequencydeviation\ (Hz) = \frac{Fs \times CAR\_NCOF}{2^{24}}$$

5.7.1.5 Phase Lock Detection

When the carrier frequency is close enough to the frequency of the incoming wave, the carrier signal lies in the pull-in range of the phase-locked-loop. When the loop is phase locked, the phase lock detector sets the CAR_LC bit (Group 3, APR 11) to 1. To stop the sweep, the microprocessor must then set the CAR_SW bit (Group 4, APR 41) to 0.

The phase lock detector uses a internal threshold and an estimation period, which are programmable using the CAR_LC_THSL register (Group 4, APR 29).

The FP_LOCK_LEN bit (Group 4, APR 54) selects between a long and short estimation period. For operation at low E_b/N_o (less than 10 dB), the long period should be selected (FP_LOCK_LEN = 0). A typical value of CAR_LC_THSL is then 31.

For operation at higher E_b/N_o (10 dB or higher), the short period can be selected, which provides for a faster lock detection. In this case, a typical value for CAR_LC_THSL is 72.

5.7.1.6 False Locks

The microcontroller must take particular care to handle a false lock condition correctly. A false lock occurs when phase lock has been detected but the correct central frequency has not yet been reached. This situation occurs in QPSK for frequency offsets that are multiples of 1/4 T, where T is the QPSK symbol duration, and also at other offsets dictated by the discrete nature of the carrier recovery loop. Offsets that are not multiples of 1/4 T are hard to predict.

5.7.2 Carrier Phase Tracking

The following subsections give a detailed description of the phase error estimator and the carrier recovery loop characteristics.

5.7.2.1 Phase Error Estimator

In QPSK mode (the QB bit in Group 4, APR 2 is 0), the phase error detector implements two error estimators:

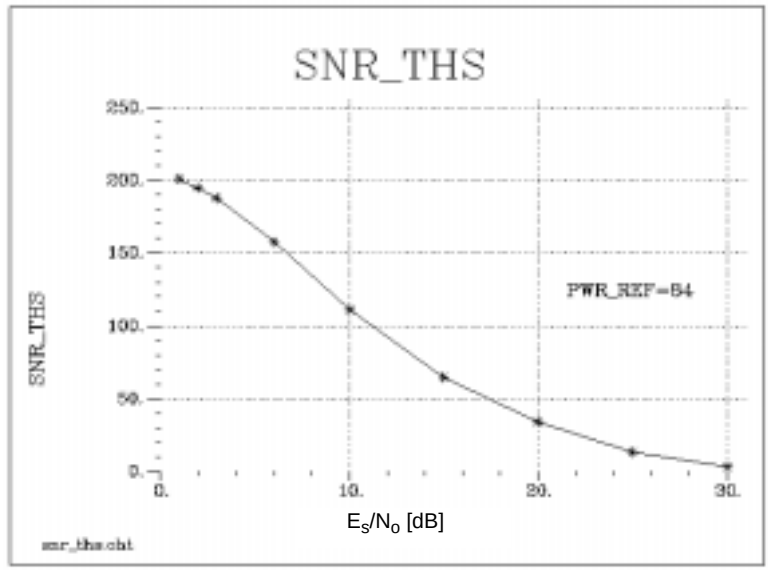
- Nondata Aided Maximum Likelihood (NDAML)
- Decision Directed Maximum Likelihood (DDML)

The microcontroller selects the estimator using the CAR_PED_SEL bit (Group 4, APR 41). When the CAR_PED_SEL is 0, the DDML estimator is used. When the bit is 1, the NDAML estimator is used.

In BPSK mode (the QB bit is 1 in Group 4, APR 2), the phase error detector implements a single DDML estimator.

The phase detector uses two gain values depending on the signal to noise ratio. The SNR is internally estimated and compared to the SNR_THS[7:0] 8-bit threshold (Group 4, APR 27). The plot in Figure 5.7 shows the relationship between the SNR_THS[7:0] parameter and the actual E_S/N_0 (symbol energy to noise power density) seen in-circuit. A value of 100 is recommended for SNR_THS[7:0]. The value of 100 corresponds to an actual E_S/N_0 of 11 dB. The result of the comparison of the estimated SNR to the threshold is stored in the Demod_SNR bit (Group 3, APR 6, bit 7). A 12-bit value for this SNR estimate is available from SNR[11:0] in Group 3, APR 22 and 23.

Figure 5.7 SNR Threshold vs. E_S/N_0



5.7.2.2 Loop Characteristics

To set the parameters of the carrier recovery loop (natural frequency and damping factor), the user must select the values the microprocessor writes into the CAR_MU_SEL and CAR_LAMBDA_SEL (Group 4, APR 28) registers.

Figure 5.8 Carrier Loop Filter Parameters

The values of CAR_MU_SEL and CAR_LAMBDA_SEL are computed according to Equation 5.18, Equation 5.19, and Equation 5.20.

Equation 5.18 Carrier Loop Phase Detector Gain

$$K_{dcar} = \frac{K_{digital} 0.78}{32}$$

$K_{digital}$ is a function of SNR (see Table 5.4 on page 5-19).

Equation 5.19 Symbol Time

$$T_b = \frac{1}{Fb}$$

Equation 5.20 Oversampling Ratio

$$L_{car} = \frac{Fs}{Fb}$$

Fs is the sampling frequency and Fb is the baud rate

Based on the intermediate values τ_a and τ_b, which are calculated in Equation 5.21 and Equation 5.22, CAR_MU_SEL and CAR_LAMBDA_SEL are computed as shown in Equation 5.23 and Equation 5.24. The damping factor (ζ) is normally 1.0. The natural frequency (ω_n) of the loop is in radians/sec.

Equation 5.21

$$\tau_a = \frac{\omega_n^2 (T_b)^2}{K_{dcar} L_{car}}$$

Equation 5.22

$$\tau_b = \frac{2\zeta\omega_n T_b}{K_{dcar} L_{car}}$$

Equation 5.23

$$CAR\_MU\_SEL = log_2(\tau_a 2^{25})$$

Equation 5.24

$$CAR\_LAMBDA\_SEL = log_2(\tau_b 2^{16})$$

K_{dcar} (or $K_{digital}$) is the Carrier Loop Phase Detector Gain. It is a function of SNR as well as the mode (DDML or NDAML). Table 5.4 presents the gains of the two phase detectors as a function of SNR.

Table 5.4 PED Gain For Carrier Loop

SNR (dB)	$K_{digital}$ DDML	$K_{digital}$ NDAML
1	4.26	4.39
2	5.91	6.19
3	8.36	8.16
4	11.65	10.66
5	14.76	13.59
6	16.77	16.78
7	19.25	20.18
8	20.74	23.39
9	23.00	26.67
10	24.39	29.58
12	25.39	34.38
14	25.61	37.82
16	25.89	40.26
18	26.02	41.75
20	26.10	42.71
25	26.10	43.34

The suggested value for ω_n is shown in Equation 5.25.

Equation 5.25 Suggested Values for ω_n

$$\text{carrier\_bw}(\omega_n) = 2\pi \times Rb[MS/s]$$

The value of ω_n from Equation 5.25 can be substituted in the carrier loop equations, Equation 5.21 and Equation 5.22, for τ_a and τ_b. Here carrier_bw refers to the natural frequency ω_n. Rs (1/T) is the symbol rate.

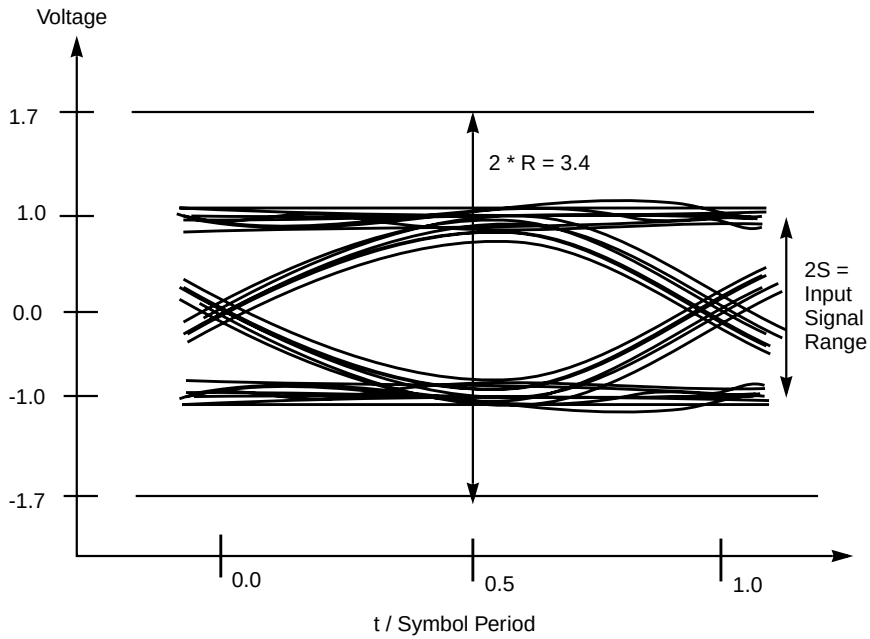
5.8 Automatic Gain Control (AGC)

This section describes the L64724 automatic gain control (AGC) function.

5.8.1 ADC Range and Power Reference

When the PWR_REF register (Group 4, APR 24) is set to the recommended value of 84, the AGC sets the ratio of the signal range to the ADC range to 1:1.7 (see Figure 5.9.)

Figure 5.9 Eye Pattern and ADC Range



Assuming that the signal power at the input of the ADC is normalized to 1 V^2, the range of the signal (2S) is 2 V (the noise-free level of the I and Q signals). The value of PWR_REF is computed from Equation 5.26.

Equation 5.26

$$PWR\_REF = min\left\{84, 84 \cdot \frac{\left[1 + \left(\frac{E_s}{N_o}\right)^{-1}\right] \cdot DF\_GAIN^2}{1 + \left(\frac{N_I}{P_s}\right) + \left(\frac{E_s}{N_o}\right)^{-1} \cdot \left(\frac{W_s}{R}\right)}\right\}$$

E_S is the signal energy, N_I is the interference power, P_S is the signal power of the desired channel, W_S is the bandwidth of the SAW, and R is the baud rate.

5.8.2 Power Control Loop

The L64724 measures the signal power at the output of the matched filter and compares the measured value to an expected value that the microcontroller has written into the PWR_REF register.

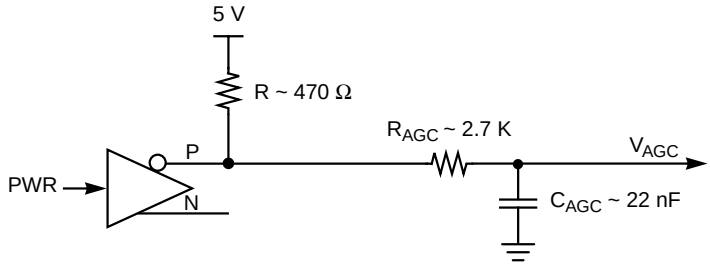
The microcontroller can adjust the power loop bandwidth using the PWR_BW[1:0] bits (Group 4, APR 25). The loop bandwidth is proportional to the value of PWR_BW[1:0] and proportional to the symbol rate. Set the PWR_BW bits according to Table 5.5.

Table 5.5 PWR_BW as a Function of Symbol Rate

PWR_BW[1:0]	Symbol Rate (MHz)
0b00	20–45
0b01	10–20
0b10	5–10
0b11	2–5

The power control signal drives the Sigma-Delta modulated output PWRP. Use the PWRP output to drive an external passive RC filter that feeds the gain control stage (see Figure 5.10.)

Figure 5.10 AGC Loop Control



The *R* and *C* values for the passive low-pass filter should meet the requirements of Equation 5.27.

Equation 5.27

$$R_{AGC}C_{AGC} \cong 64\ \mu s$$

5.8.3 Power Level

The L64724 stores the AGC loop control voltage in the PWR_LVL[7:0] register (Group 3, APR 10), where the microcontroller can monitor it. The relationship between the loop voltage V_{AGC} and the PWR_LVL register is shown in Equation 5.28.

Equation 5.28

$$V_{AGC} = \frac{\text{PWR\_LVL}}{256} \times V_{REF}$$

The PWRP pin uses an open drain buffer that allows you to apply an external V_{REF} voltage of 5 V even if the L64724 is powered at 3.3 V.

5.9 Output Control

Because the output of the matched filter is quantized to four bits for the subsequent Viterbi decoder, the L64724 Output Control properly adjusts the level of the output signals.

The microcontroller can adjust the level of the demodulated DEMI and DEMQ output signals using the SCALE register (Group 4, APR 26). The SCALE register multiplies the results of the matched filter before it is truncated to the 4-bit outputs.

When the PWR_REF register (Group 4, APR 24) is set to its recommended value of 84, the value of the SCALE[7:0] bits should be set to 158.

5.9.1 Eye Pattern and Soft Decision Thresholds

The useful part of the matched filter output signal is clipped for a larger value of SCALE.

Because the power control loop automatically reduces the eye amplitude for increasing noise, the DEMI and DEMQ signals include additional headroom for resolving noise.

Equation 5.29 and Equation 5.30 relate SCALE and PWR_REF.

Equation 5.29 SCALE and PWR_REF Relationship for QPSK Systems

$$\text{SCALE} = \frac{2047 \cdot \sqrt{1 + \left(\frac{E_s}{N_o}\right)^{-1}}}{\sqrt{2 \cdot \text{PWR\_REF}}}$$

Equation 5.30 SCALE and PWR_REF Relationship for BPSK Systems

$$\text{SCALE} = \frac{2047 \cdot \sqrt{1 + \left(\frac{E_s}{N_o}\right)^{-1}}}{2\sqrt{\text{PWR\_REF}}}$$

5.10 External Controls

External controls have been added in order to simplify the design of the analog front end, to reduce the amount of external circuitry, and to make the board layout as simple as possible.

Five external control bits are available on the L64724. Four of these bits (XCTR_OUT[3:0]) are output signals, and one (XCTR_IN) is an input signal. The controls can be used to setup or to read parameters from other components on the board (such as the RF front end and the tuner) using only the L64724 microprocessor interface.

The four output controls use pins XCTR_OUT[3:0], which are programmed by setting their respective bits in the XCTR[3:0] register

(Group 4, APR 55). The XCTR[i] register drives the XCTR_OUT[i] pin—that is, programming the XCTR[i] register to 0 deasserts pin XCTR_OUT[i] to a zero-volt level, and programming the XCTR[i] register to 1 asserts pin XCTR_OUT[i] to a 3.3 volt level.

The input control is sensed on the XCTR_IN pin. The logic level applied to this pin is read using the XCTR_IN bit (Group 3, APR 6).

Chapter 6
Decoding Pipeline Synchronization

This chapter describes the configurable synchronization circuit that aligns the decoding pipeline outputs to the overall frame structure of the L64724. The decoding pipeline consists of the Viterbi Decoder, Deinterleaver, Reed-Solomon (RS) Decoder, and the Descrambler. This chapter contains the following sections:

- Section 6.1, “Synchronization Scheme”
- Section 6.2, “Viterbi Decoder Synchronization”
- Section 6.3, “Reed-Solomon Deinterleaver Synchronization”
- Section 6.4, “Descrambler Synchronization”

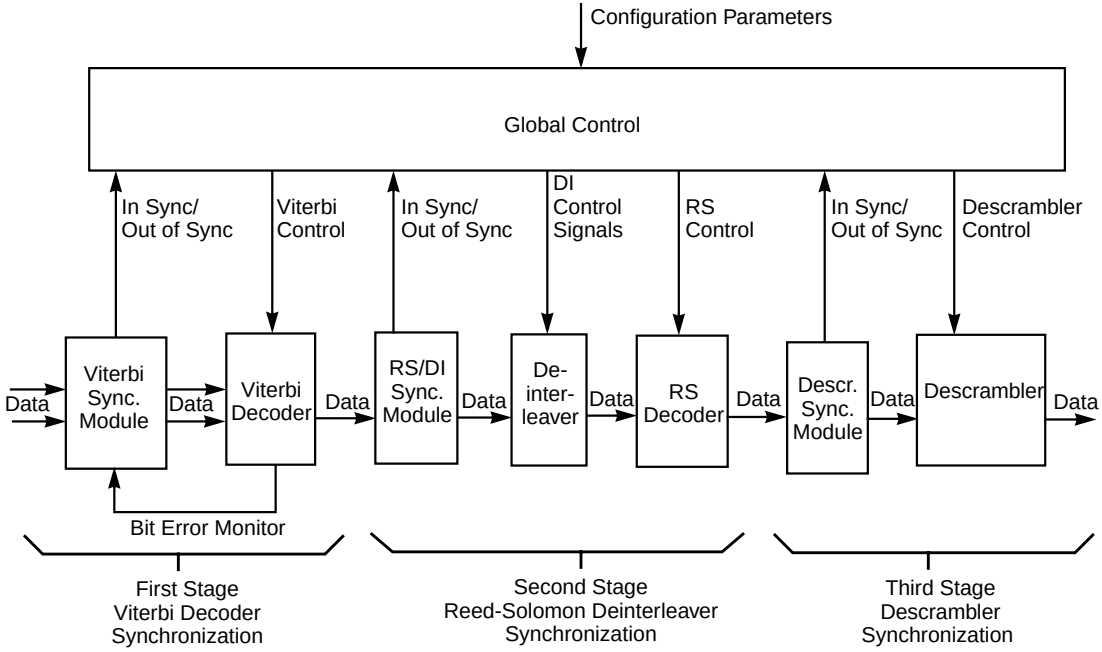
6.1 Synchronization Scheme

The L64724 FEC synchronization scheme is accomplished in three stages:

- The first synchronization stage uses output statistics from the Viterbi Decoder module.
- The second stage identifies a synchronization word.
- The third stage identifies an inverted synchronization word.

A global control module generates the control signals for the Viterbi, Descrambler, Deinterleaver, and RS Decoder modules. The global control module handles the appropriate sequencing of the synchronization signals for determining in- and out-of-synchronization. The input to the FEC portion of the L64724 is two symbols generated by the demodulator portion. The maximum information rate is 90 Mbits/s. Figure 6.1 shows the organization of the synchronization module.

Figure 6.1 Synchronization Module

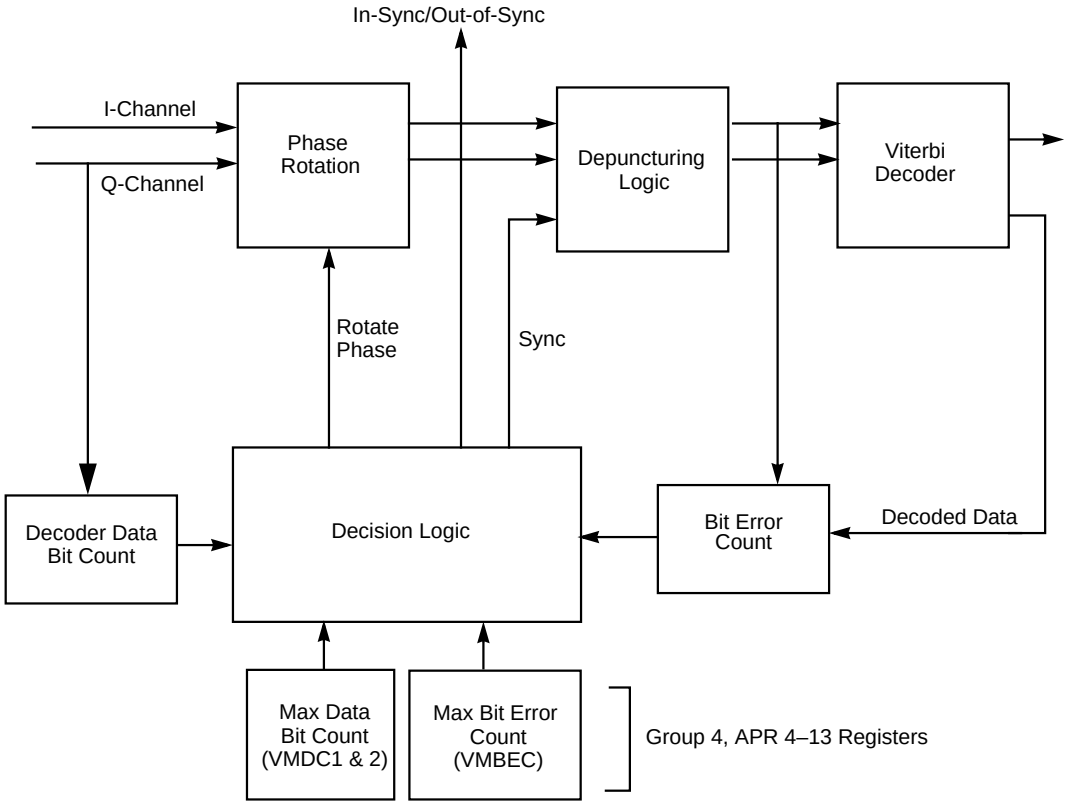


6.2 Viterbi Decoder Synchronization

This section describes the first stage of the Synchronization module, which performs Viterbi Decoder synchronization.

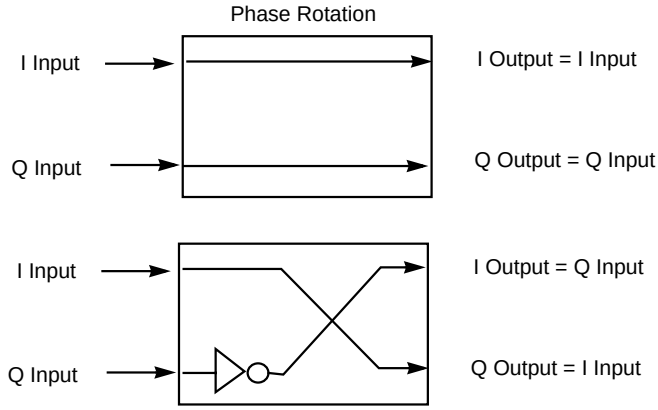
In the first stage, the decoder observes the valid data symbols and bit errors in the decoded data stream to determine the in- or out-of-synchronization condition. The Viterbi Max Data Bit Count Registers (VMDC1 in Group 4, APR 4, and VMDC2 in Group 4, APR 5–7) set the number of valid data bits at the output of the Viterbi Decoder over which the decoder counts channel symbol errors. During that interval, whenever the bit error count is above the value specified in the Viterbi Max Data Bit Error Count Register (Group 4, APR 8–13,) the synchronization logic flags an out-of-synchronization condition. Figure 6.2 shows the Viterbi Decoder synchronization.

Figure 6.2 Viterbi Decoder Synchronization



The decoder then proceeds to adjust either the phase in the phase rotation module or the data stream alignment in the depuncturing logic. The 180 degree rotation is removed in the Reed-Solomon decoder synchronization stage (see Section 6.3, “Reed-Solomon Deinterleaver Synchronization,” page 6-8.) Figure 6.3 outlines the operations performed during phase rotation.

Figure 6.3 Phase Rotation for Synchronization



This first synchronization stage does not inspect the data stream for specific synchronization patterns, nor does it remove any portions of the data stream. Once the Viterbi Decoder module has reached synchronization, the Deinterleaver and Reed-Solomon blocks in the data pipeline each require their own synchronization procedures.

The data bit count and bit error count threshold values are VMDC1 (Group 4, APR 4) and VMBEC (Group 4, APR 8–13.) To assist you in the proper selection of the ratio (VMBEC/VMDC1) of the threshold values, Figure 6.4 through Figure 6.9 show the plots of the Channel Symbol Error Rate vs. SNR for all the code rates that the L64724 supports. The upper curve in each graph represents the out-of-synchronization condition, and the lower curve represents the in-synchronization condition.

Figure 6.4 Channel Symbol Error Rate vs. SNR for Rate = 1/2 Code

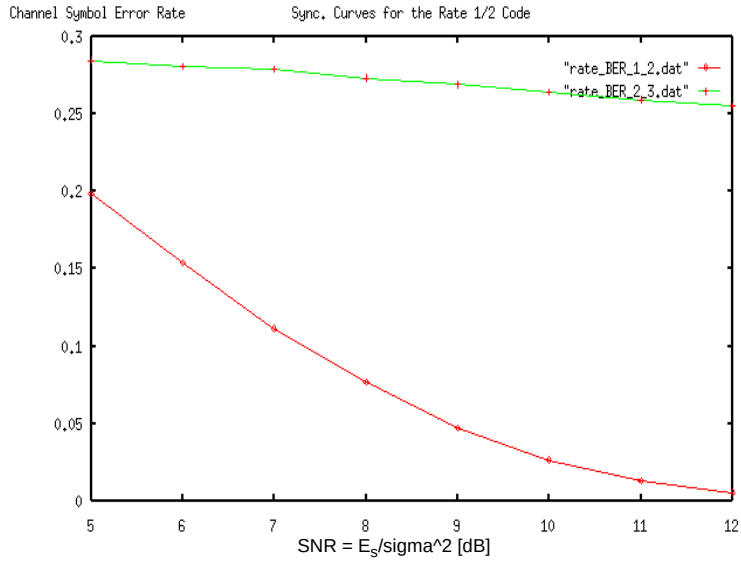


Figure 6.5 Channel Symbol Error Rate vs. SNR for Rate = 2/3 Code

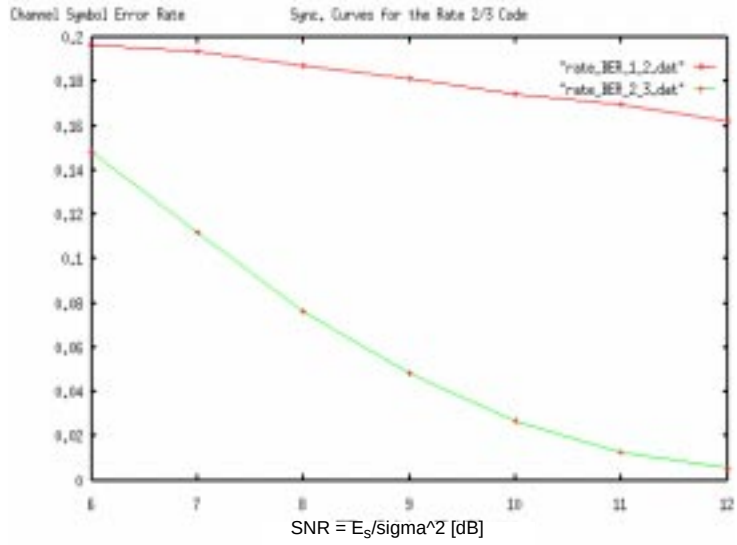


Figure 6.6 Channel Symbol Error Rate vs. SNR for Rate = 3/4 Code

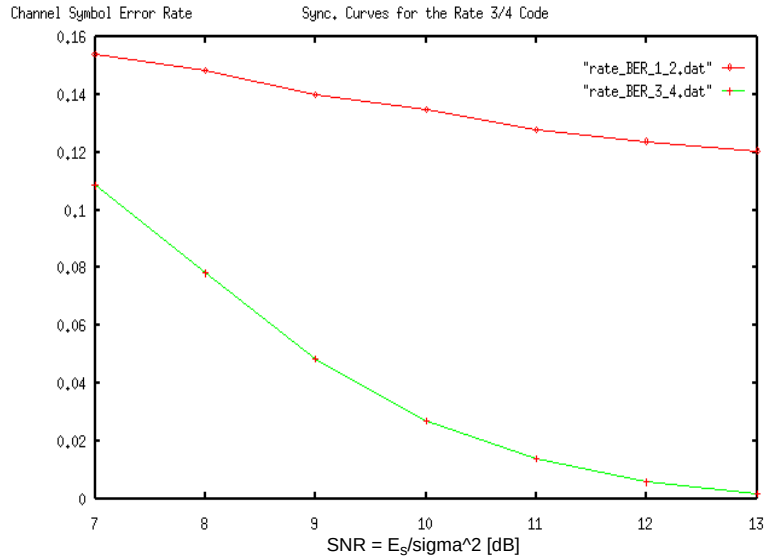


Figure 6.7 Channel Symbol Error Rate vs. SNR for Rate = 5/6 Code

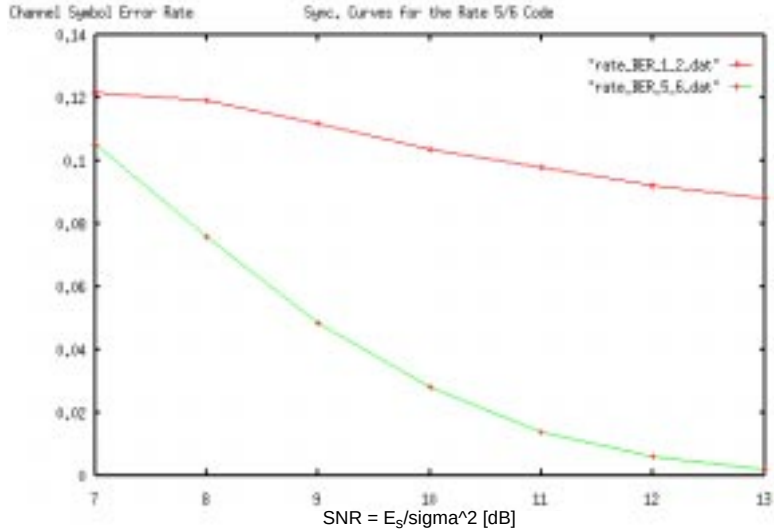


Figure 6.8 Channel Symbol Error Rate vs. SNR for Rate = 6/7 Code

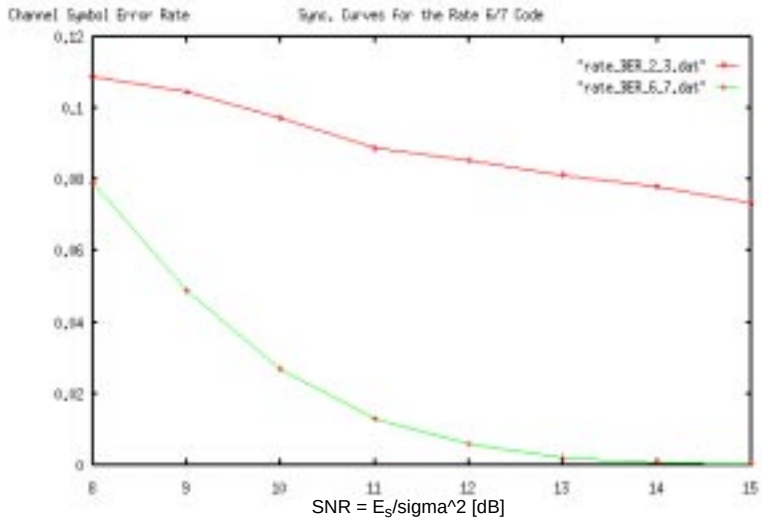
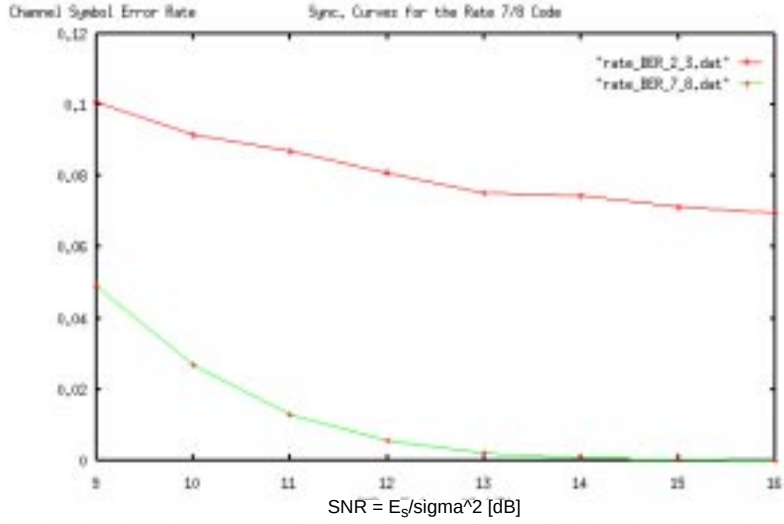


Figure 6.9 Channel Symbol Error Rate vs. SNR for Rate = 7/8 Code



You must select a value for the ratio VMBEC/VMDC1 that is between the in-synchronization and the out-of-synchronization curves. For example, for a rate equal to 1/2 code, a value of 0.24 for VMBEC/VMDC1 establishes a valid decision threshold over the entire E_b/N_o range shown.

Equation 6.1 shows the computation of Channel Symbol Error Rate as a function of VMBEC and VMDC1.

Equation 6.1

$$\text{Channel Symbol Error Rate} = \frac{128\,VMBEC + 32}{256\,VMDC1}$$

6.3 Reed-Solomon Deinterleaver Synchronization

This section describes the second synchronization stage, which performs Reed-Solomon Deinterleaver synchronization. In the second synchronization stage, the decoder searches the data stream for a predefined sync word to determine the in-sync or out-of-sync condition. Figure 6.10 illustrates the Reed-Solomon Deinterleaver synchronization module, which is designed to allow synchronization for DVB (Digital Video Broadcast) as well as for DSS (Digital Satellite Systems) compliant systems.

Figure 6.10 Reed-Solomon, Deinterleaver Synchronization

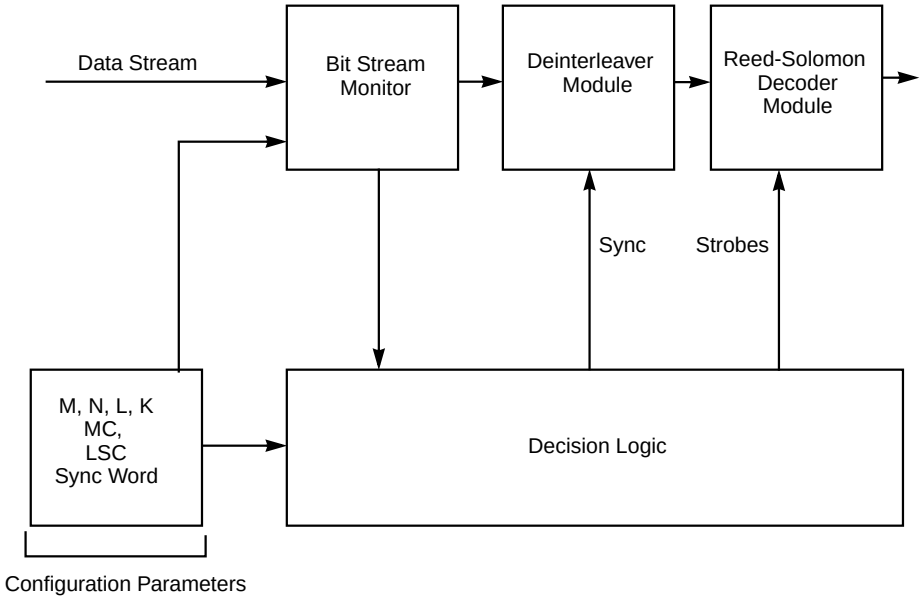
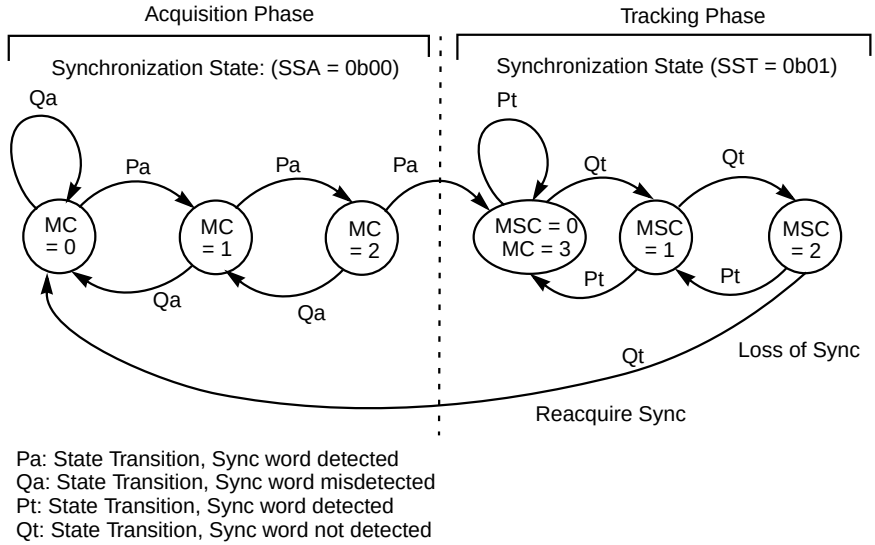


Figure 6.11 shows an example state diagram that outlines how the decoder determines synchronization, tracking, and loss of synchronization in the Reed-Solomon synchronization stage.

Figure 6.11 Synchronization, Tracking, and Loss of Sync for Three Missed Sync Words



The parameters in Figure 6.11 are defined as follows:

Parameter	Description
MC	Match counter—number of sync word matches found so far during the acquisition phase
MSC	Mismatch counter—number of sync word mismatches found so far during the tracking phase
Pa, Pt	Pa and Pt are functions of L, which is defined as the maximum number of mismatching bits allowed to declare a match when comparing M bits in the data stream to the reference sync word during tracking phase (L = 0, 1, or 2).

You can configure some of the parameters in the state diagram for the acquisition and tracking phase. For example, you can set the SSA parameter (Group 4, APR 16) to allow for three, four, five, or six sync words before the decoder declares itself to be in synchronization. You can also set the SST parameter (Group 4, APR 16) to allow for two, three, four, or five misdetected sync words before the decoder declares a loss of synchronization. Figure 6.12 and Figure 6.13 show the minimum and maximum number of states that you can select for acquisition and tracking modes.

Figure 6.12 Minimum and Maximum Number of States in the Acquisition Phase

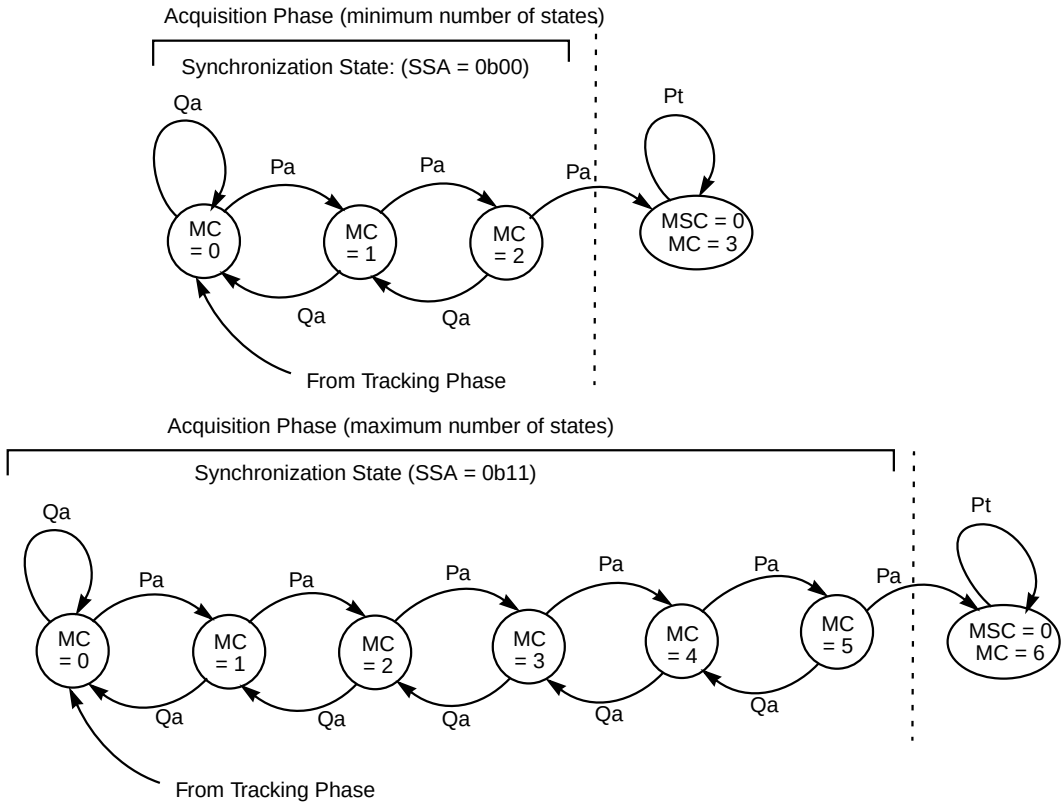
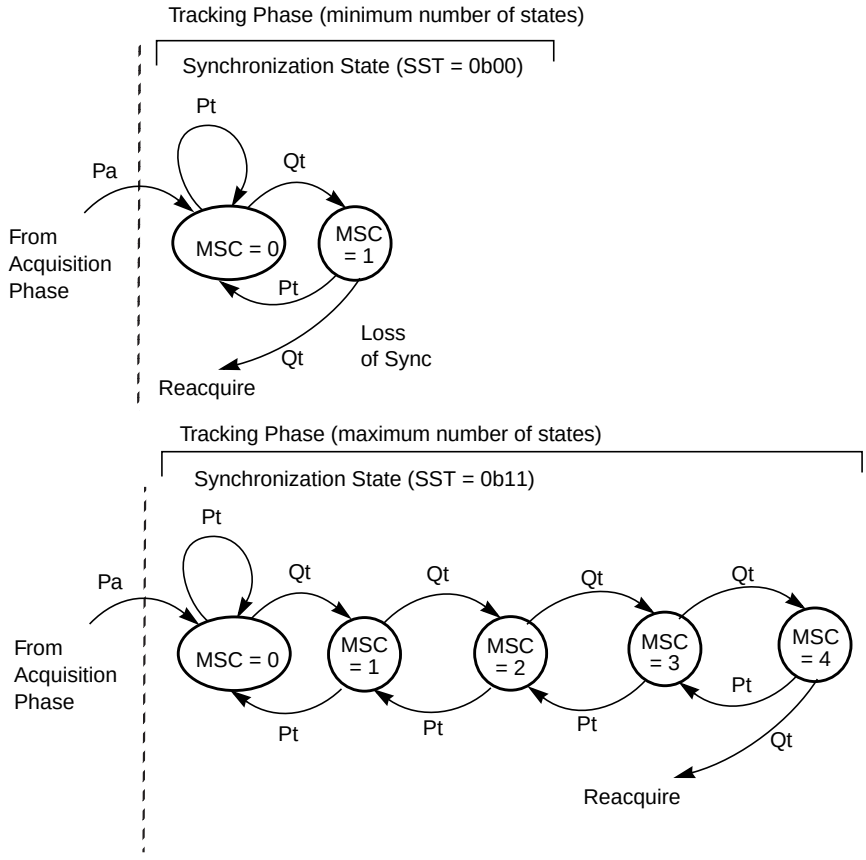
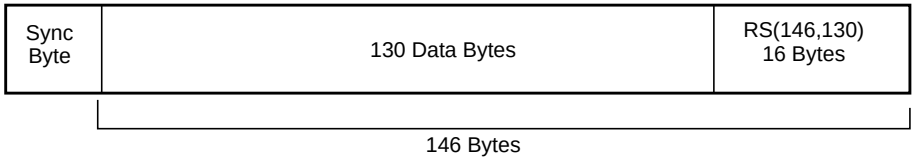


Figure 6.13 Minimum and Maximum Number of States in the Tracking Phase



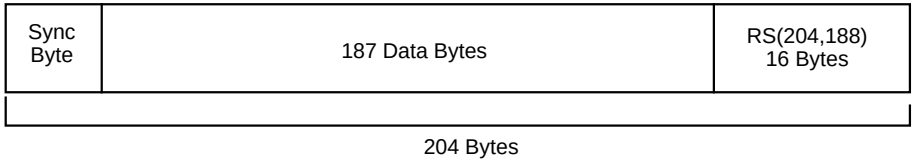
The data structure for DSS systems is shown in Figure 6.14. A DSS packet consists of 146 bytes, including 130 data bytes and 16 redundancy bytes. A synchronization byte precedes every Reed-Solomon block, but is added after the Reed-Solomon encoding and interleaving operations have been performed. The sync byte is removed in the bit stream monitor and is not supplied to the Deinterleaver and Reed-Solomon Decoder modules.

Figure 6.14 DSS Packet



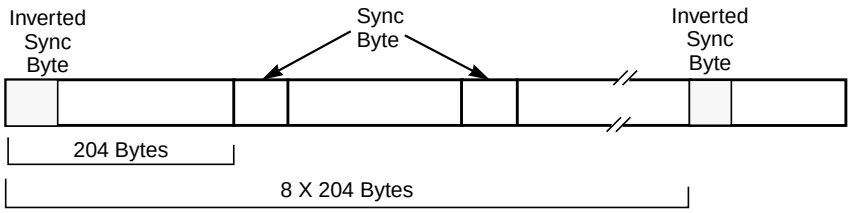
An MPEG-2 RS(204,188) protected transport packet consists of 204 bytes, including 1 sync byte, 187 data bytes, and 16 redundancy bytes. Figure 6.15 shows the data format of the MPEG-2 Transport Packet.

Figure 6.15 MPEG-2 Transport Packet



In the DVB data structure, one out of every eight synchronization words in the data stream is mod 2 complemented. Figure 6.16 shows the data format of the L64724 transport packet.

Figure 6.16 L64724 Transport Packet



Given a bit stream that consists of a sequence of the packets shown in Figure 6.16, the second synchronization stage searches for the predefined sync byte.

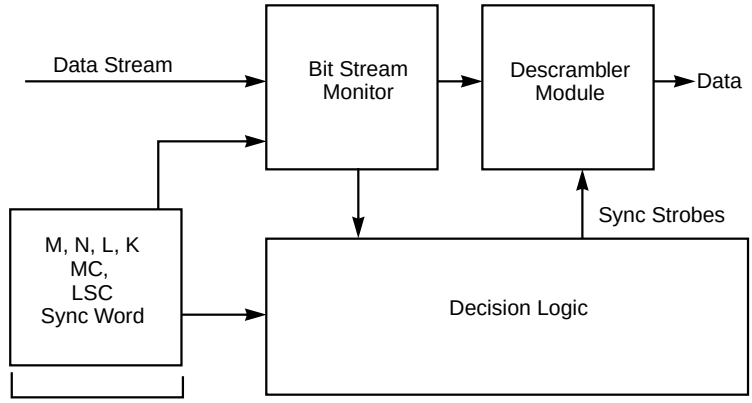
In addition to providing the proper data alignment for the Deinterleaver and Reed-Solomon Decoder modules, the second synchronization stage (Reed-Solomon Deinterleaver Synchronization) resolves the 180-degree phase uncertainty that the upstream demodulator may have introduced. The first (Viterbi) synchronization stage is not able to detect a phase uncertainty error.

6.4 Descrambler Synchronization

This section describes the third-stage synchronization, which performs Descrambler synchronization. Figure 6.17 illustrates the Descrambler synchronization process. The Descrambler module is only active in DVB systems and is not used for DSS systems.

The L64724 restarts the Descrambler every 8N byte times. The L64724 aligns this restart with the complemented synchronization word that is present in the data stream once every eight Reed-Solomon code words (once every 8 N bytes.)

Figure 6.17 Descrambler Synchronization



For third-stage synchronization, the L64724 uses an approach very similar to that of the second synchronization stage during the acquisition phase to ensure proper data alignment.

Note that in this stage, any noninverted corrupted sync bytes found in the tracking phase are replaced with the original predefined noninverted sync byte.

Chapter 7
The FEC Decoder Pipeline

This chapter discusses the FEC Decoder Pipeline. The decoder pipeline consists of four modules that are connected in a logical sequence. This chapter discusses the four modules in the pipeline in the following sections:

- Section 7.1, “Viterbi Decoder Module”
- Section 7.2, “Deinterleaver Module”
- Section 7.3, “Reed-Solomon Decoder”
- Section 7.4, “Descrambler Module Architecture and Operation”
- Section 7.5, “FEC Module Software Reset”

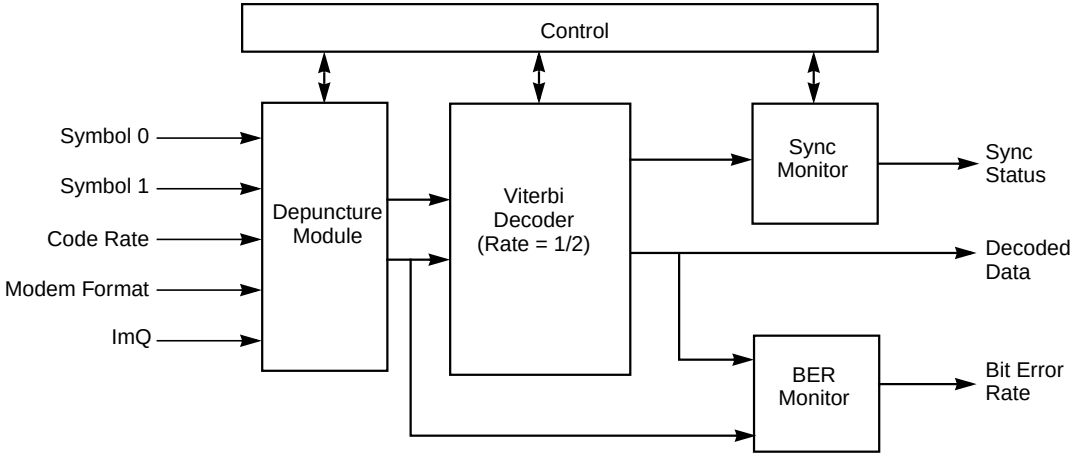
7.1 Viterbi Decoder Module

The Viterbi Decoder contains the following major modules:

- A Depuncture Module for code rates other than 1/2
- A 1/2 code rate Viterbi Decoder that computes the serial output data stream given two sets of soft decision data input streams
- A Synchronization Monitor to provide information on acquisition or loss of synchronization
- A Bit Error Rate (BER) Monitor

The block diagram in Figure 7.1 shows the Viterbi Decoder.

Figure 7.1 Viterbi Decoder Block Diagram



7.1.1 Features

The Viterbi decoder module has the following features:

- A Viterbi Decoder with a basic rate of 1/2
- Compliant with European Digital Video Broadcast (DVB-S)
- Depuncturing for code rates of 2/3, 3/4, 5/6, 6/7 and 7/8
- Compliant with DVB and DSS channel coding specifications
- Programmable Viterbi code rates of 1/2, 2/3, 3/4, 5/6, 6/7, 7/8
- Auto code rate, phase inversion, synchronization for Viterbi decoder with programmable threshold
- Auto-rate acquisition over the DVB and DSS code range
- Rate detection over the DVB code range
- Constraint length of 7
- Synchronization monitor
- Decoded BER monitor
- Maximal Likelihood (ML) decoding algorithm
- 5.2 dB coding gain for rate 1/2 (no erased input) code at BER of 10^{-5}
- Generating Polynomial 171 (Octal) and 133 (Octal)

7.1.2 Punctured Codes

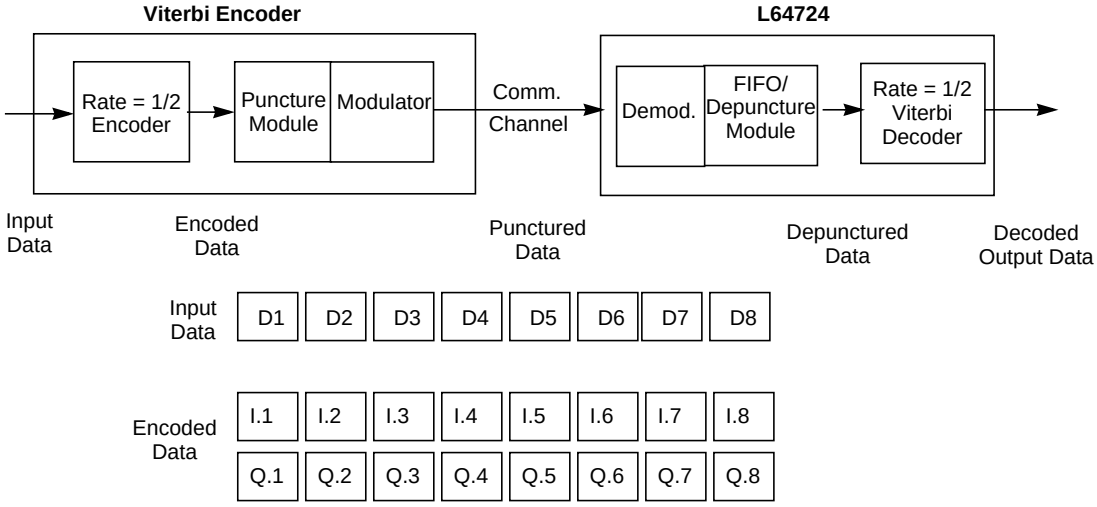
The L64724 supports not only the basic rate equal to 1/2 decoding operations, but also code rates equal to 2/3, 3/4, 5/6, 6/7 and 7/8. The code rate and underlying depuncture scheme chosen dictates the proper sequence of symbols on the DEM_I and DEM_Q inputs. Table 7.1 shows the puncture patterns for various code rates.

Table 7.1 Puncture Patterns for Various Code Rates

Code Rate	Puncture Pattern	
1/2	DEM_I: DEM_Q:	1 1
2/3	DEM_I: DEM_Q:	1 0 1 1
3/4	DEM_I: DEM_Q:	1 0 1 1 1 0
5/6	DEM_I: DEM_Q:	1 0 1 0 1 1 1 0 1 0
6/7	DEM_I: DEM_Q:	1 0 0 1 0 1 1 1 1 0 1 0
7/8	DEM_I: DEM_Q:	1 0 0 0 1 0 1 1 1 1 1 0 1 0

Figure 7.2 shows a block diagram of the puncturing and depuncturing process for a rate 1/2 encoder. For each data bit D*n*, the upstream encoder generates two corresponding encoded data symbols, I.*n* and Q.*n.* By deleting or *puncturing* some of the encoded data symbols, the puncturing process allows a rate 1/2 encoder to generate codes of higher rates. The L64724's depuncturing module allows its rate 1/2 decoder to decode data transmitted at higher code rates. Figure 7.3 illustrates the puncture patterns for different code rates.

Figure 7.2 Puncturing and Depuncturing Block Diagram



The L64724 receives the encoded data symbols in QPSK or BPSK format on the IVIN and QVIN signals. The L64724 receives these symbols in the order shown on the right of L64724 Input Data in Figure 7.2. The depuncturing module handles the reordering and the insertion of erasures into the received symbol stream before the rate equal to 1/2 Viterbi decoder module starts decoding.

Figure 7.3 Puncture Pattern for Different Code Rates

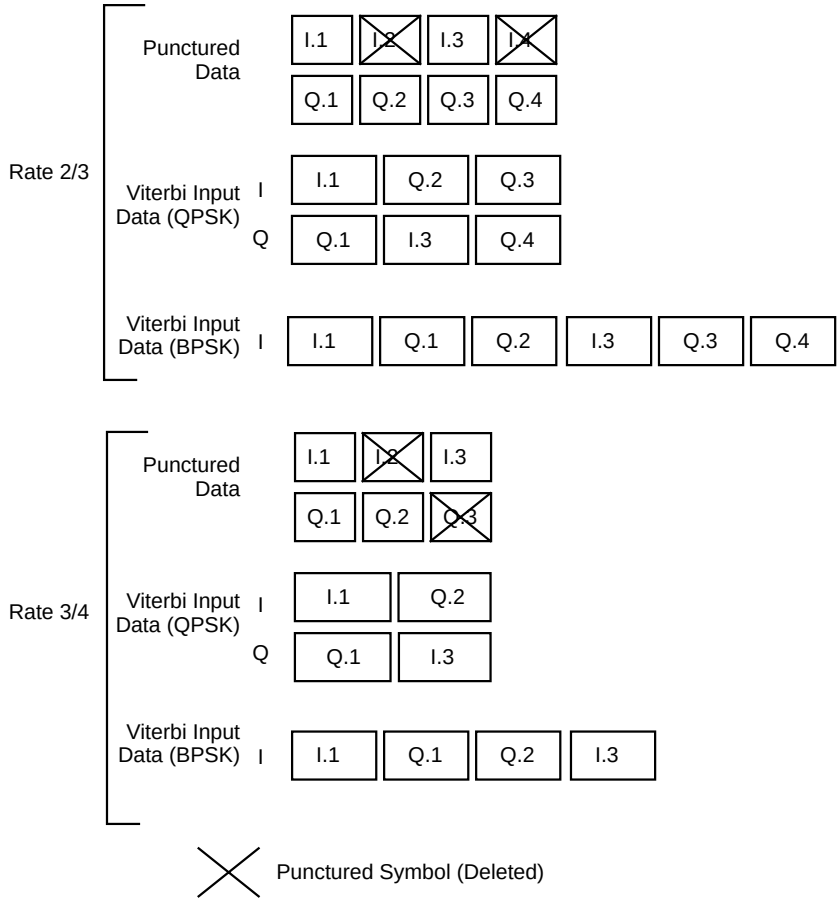
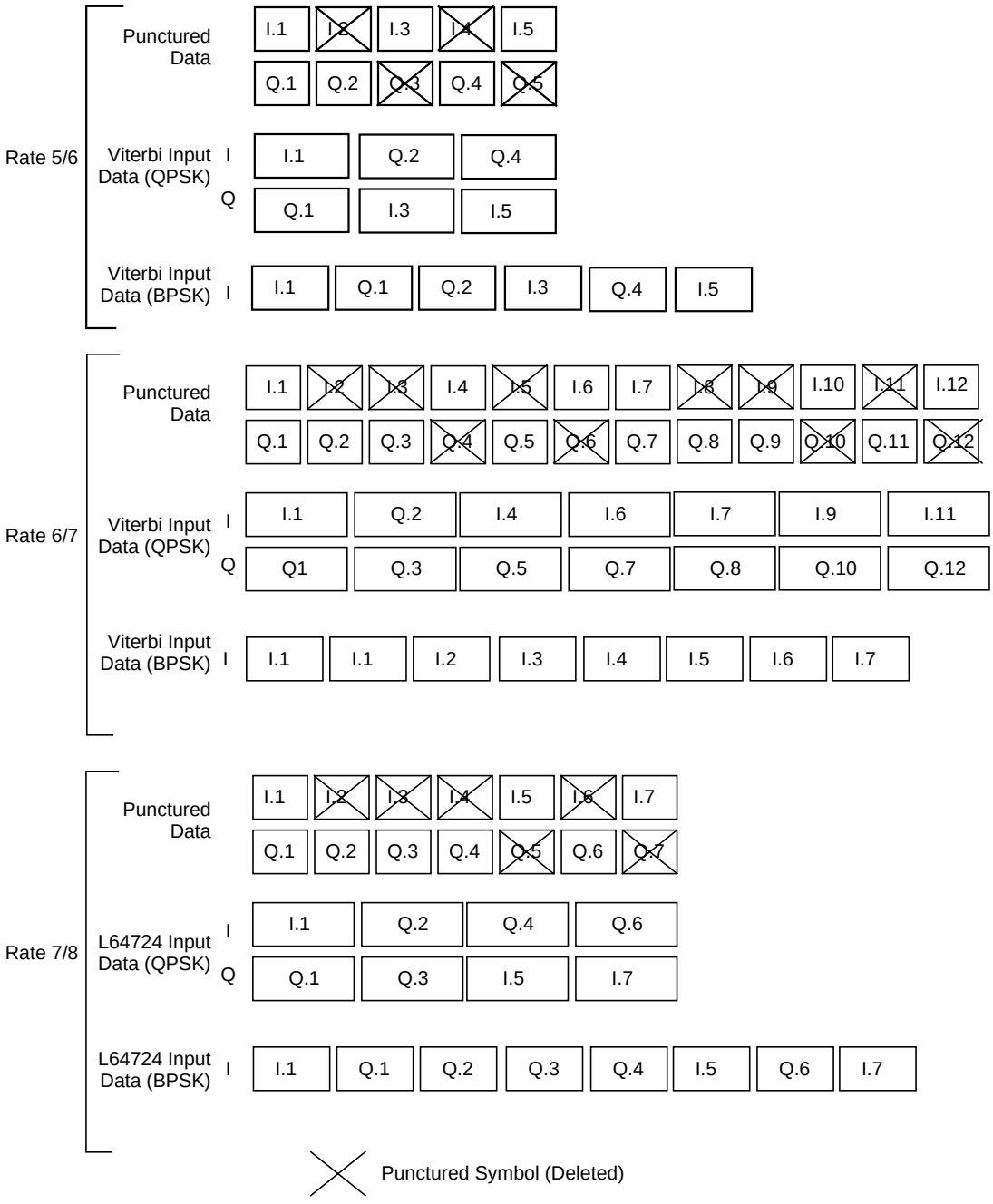


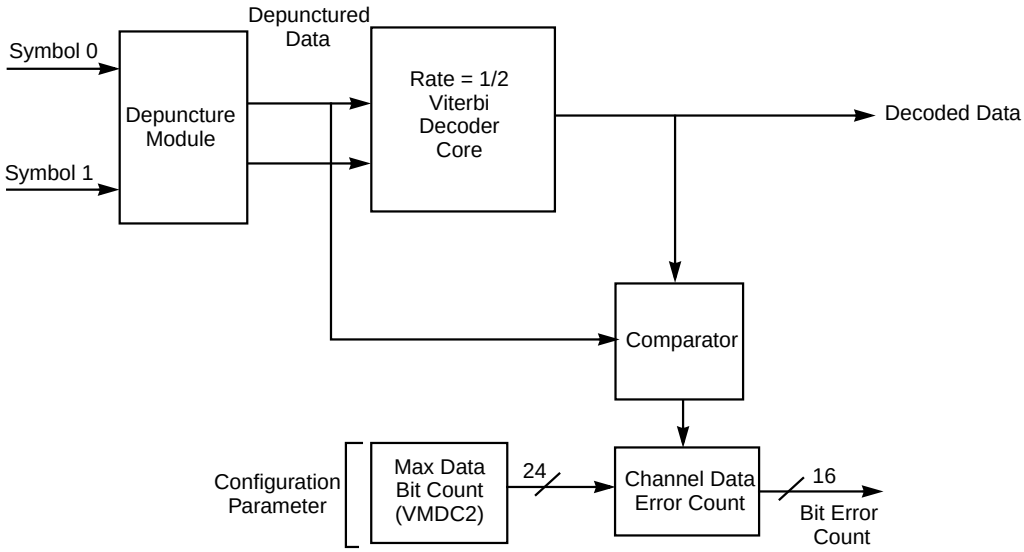
Figure 7.3 Puncture Pattern for Different Code Rates (Cont.)



7.1.3 Viterbi BER Monitor

A performance monitor for the channel BER is built into the L64724. The monitor compares an appropriately delayed version of the incoming channel data stream to the re-encoded Viterbi decoder output data stream to find occurrences of bit errors. Figure 7.4 is a block diagram of the Viterbi bit error detection circuit.

Figure 7.4 Block Diagram of Viterbi Bit Error Detection Circuit



The decoder processes the bit error events further to produce a measure of the actual channel bit error rate. The register VMDC2 (Group 4, APR 5–7) specifies the number of channel bits (and therefore the time period), divided by four, over which the decoder counts the number of occurring channel bit errors. Refer to Section 3.6.6, “Viterbi Max Data Bit Count 2 (Group 4: APR 5, 6, and 7),” page 3-42, for a description of VMDC2.

The channel data error counter accumulates the errors internally and updates the Viterbi Bit Error Rate Count (VBERC, Group 3, APR 4:5) once at the end of the period specified by VMDC2. You can read the value of the VBERC using the microcontroller interface. VBERC contains the number of errors divided by four. In addition, the L64724 sets the VBER flag in the System Status Register (Group 2.) The VBER flag indicates that the decoder has reached the period specified by VMDC2.

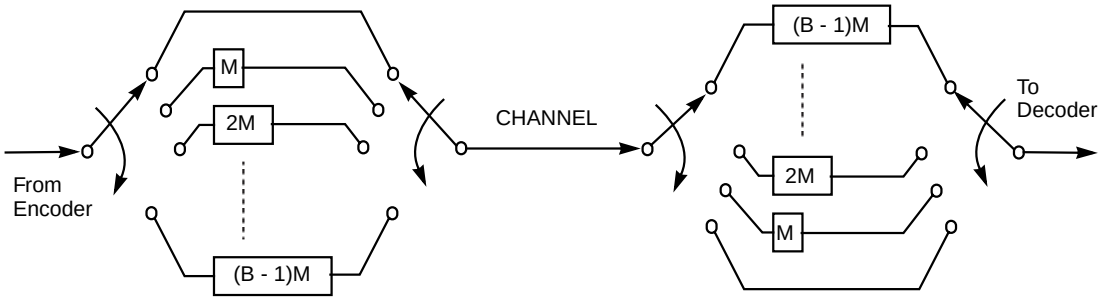
The decoder asserts INTn if the corresponding interrupt enable bit, VBER_IE, is set in the System Mode Register (Group 2.) Refer to Section 3.4, “Group 2: System Mode and System Status Registers,” page 3-9, for details.

The BER curves to assist in the proper selection of the ratio of the threshold values VMDC1 and VBERC are shown in Section 6.2, “Viterbi Decoder Synchronization,” page 6-2.

7.2 Deinterleaver Module

Figure 7.5 shows the interleaving/deinterleaving operation for the DVB mode.

Figure 7.5 Interleaving/Deinterleaving Operation for DVB



The Interleaver is a device that rearranges the ordering of a sequence of symbols in a deterministic manner. A (B, N) Periodic Interleaver has the following characteristics:

- The minimum separation at the Interleaver output is B symbols for any two symbols that are separated by less than N symbols at the Interleaver input.
- If the channel inserts any burst of less than B errors, single errors occur at the Deinterleaver output.

This scheme is also known as a convolutional Interleaver/Deinterleaver.

The L64724 Deinterleaver module performs periodic deinterleaving. The user must specify two parameters: B, the desired interleaving depth, and M, defined as

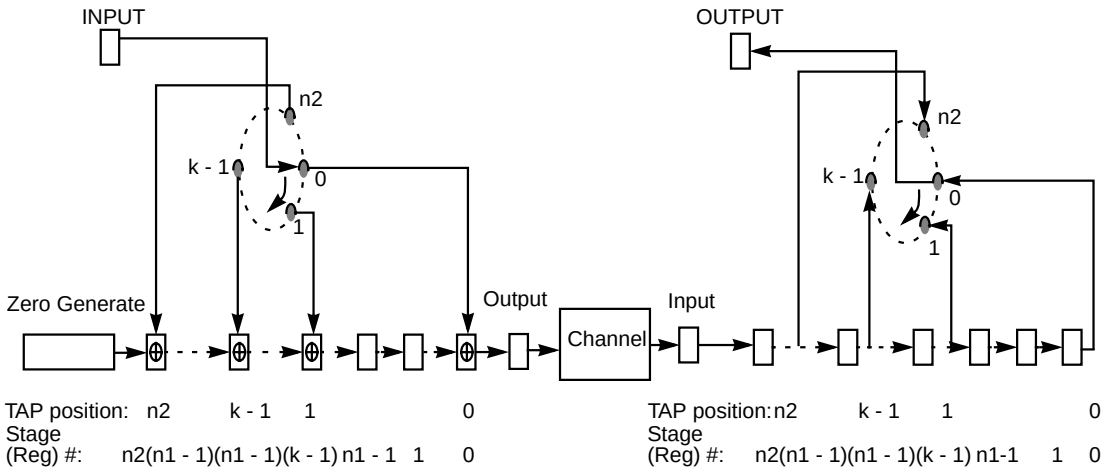
$$M = \left\lceil \frac{N}{B} \right\rceil \quad .$$

The L64724 Deinterleaver for DVB features are as follows:

- Convolutional deinterleaving
- Maximum block length of 204 bytes
- Deinterleaving depth of 12

Figure 7.6 shows the interleaving/deinterleaving operation for the DSS mode.

Figure 7.6 Interleaving/Deinterleaving Operation for DSS



Ramsey Type II Interleaver/Deinterleaver

The L64724 uses a Ramsey Type II Periodic Deinterleaver for DSS deinterleaving. A (B, N) Periodic Deinterleaver has the following characteristics:

- The minimum separation at the interleaver output is B symbols for any two symbols that are separated by less than N symbols at the interleaver input.
- Any burst of b < B errors inserted by the channel results in single errors at the deinterleaver output.

The L64724 Deinterleaver for DSS has the following features:

- Periodic deinterleaving
- Maximum block length of 146 bytes
- Deinterleaving depth of 13

7.3 Reed-Solomon Decoder

The Reed Solomon Decoder is a Forward Error Correction (FEC) unit that looks at the check bytes that are appended to the data stream and either corrects any errors that it finds in the data stream or asserts the ERROROUTn pin when it cannot correct the data.

7.3.1 Terms and Concepts

Error Correction Code (ECC) devices have a specific lexicon associated with their ability to correct transmission messages. This section defines the terms used for variables in the Reed-Solomon module. The terms are used throughout this document.

R **Check Bytes**
The encoder generates and appends check bytes to the incoming message according to the Reed-Solomon error correction encoding. The decoder uses check bytes to locate and correct errors caused by transmission. The system designer specifies the size of the check byte field within the limitations. There are 16 check bytes for both DSS/DVB modes.

d **Detection Power**
Detection power specifies the maximum number of detectable errors. Detection power has a minimum value of $\left\lfloor \frac{R}{2} \right\rfloor$ and a maximum value of R.

K **Message Length**
The message contains multiple bytes. The size of the message varies, depending on the code word length and the check bytes used, where K = N – R.

m **Symbol Size**
A data transfer contains multiple symbols. The symbol size, m, is 8 bits.

N **Codeword Length**
The variable N is the sum of the number of message bytes and the number of check bytes (K + R). The value of N is 204 for DVB; 147 for DSS (includes the MPEG sync bit).

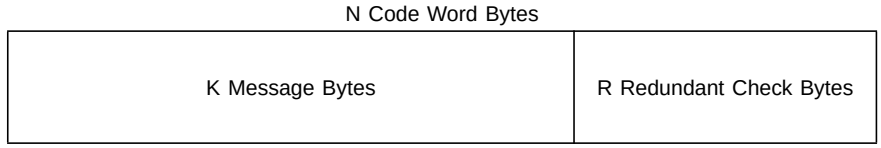
T **Number of Error Corrections**
This variable is the maximum number of error corrections performed by the decoder. The value of T is 8.

7.3.1.1 Forward Error Correction (FEC)

FEC requires an encoder that appends redundant check bytes to a message before transmission. The check bytes, with an indeterminate number of bits, are referred to as symbols. The message symbols followed by redundant check symbols are called code words. The check symbols are redundant in the sense that they are derived from the message and are appended to the message. Check symbols are also referred to as “redundant check bytes,” and sometimes as “correction bytes.”

Figure 7.7 illustrates a code word. Explanatory text follows the figure.

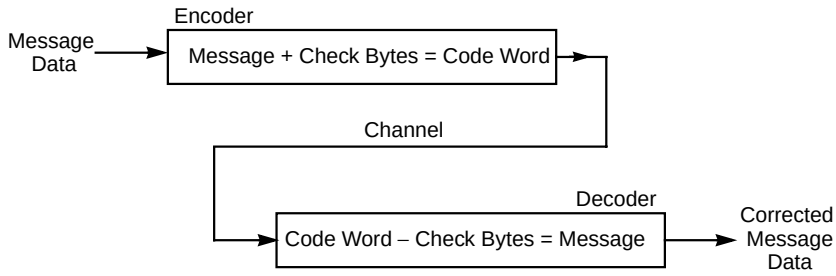
Figure 7.7 Code Word Structure



A code word is a block of N bytes that includes K message symbols and N – K check bytes (R.) The check bytes or symbols are some fraction of the message symbols. A large number of check symbols allows the decoder to correct a large number of transmission errors.

The redundant check symbols in a message allow a decoder at the receiving end of a transmission line to detect transmission errors and reconstruct the original message content. Figure 7.8 shows a block diagram of the basic encoder and decoder functions in a transmission system.

Figure 7.8 FEC Data Path



After generating a code word, the encoder transmits it through a low cost channel to a decoder. The decoder compares the bit stream in the message data to the encoding in the check bytes to detect transmission errors. The original message can be precisely reconstructed from the check symbols, as long as the number of symbol errors in the code word is less than or equal to R/2.

7.3.1.2 Reed-Solomon ERROR Correction Codes

Reed-Solomon (RS) error correction codes are systematic and operate on bytes rather than single-bit data streams. They are especially good in burst error applications The importance of RS codes is illustrated by their adoption as international and domestic standards in various areas of

applications. The codes are expressed by convention as two numbers, the first indicating the total codeword length (N), and the second indicating the number of message bytes (K). The difference between these two numbers (N – K) is the number of check bytes. A (255, 233) RS code, for instance, with 8-bit bytes, was adopted as part of the standard for space missions by both the European Space Agency and NASA. The compact disc digital-audio system uses a combination of a (32, 28) RS code and a (28, 24) RS code. The MIL-STD-2179/ANSI X3B.6 media exchange standard uses a (161, 153) RS code and a (128, 118) RS code for high-density magnetic recording.

The L64724 uses the following generator polynomial for RS codes:

$$\prod_{i=0}^{R-1} (x + \alpha^i)$$

where α is a root of the binary primitive polynomial:

$$x^8 + x^4 + x^3 + x^2 + 1$$

A data byte (d_7, d_6, ... d_1, d_0) is identified with the element $d_7\alpha^7 + d_6\alpha^6 + ... + d_1\alpha + d_0$ in GF(256), the finite field with 256 elements.

The error correcting power of an RS code is related to the number of redundant check symbols in its code words. In general, an RS code with two T check symbols per code word can correct up to *T* byte errors per code word. Higher redundancy allows more errors to be corrected

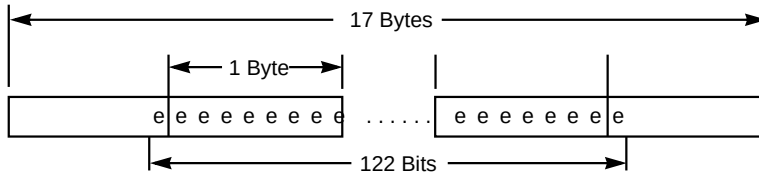
The remainder of this section describes the process of correcting transmission errors with Reed-Solomon codes.

7.3.1.3 Error Handling and Correction

A bit error occurs when a transmitted zero is received as a one or vice versa. A byte error occurs when one or more bits in the byte have errors. For example, a byte with only one bit error is counted as one byte error, and a byte with m bit errors (all bits are inverted) is also counted as one byte error. As long as a code word has no more than T = $\lfloor (R)/2 \rfloor$ byte errors, the RS Decoder corrects all errors. When a code word has more than T = $\lfloor (R)/2 \rfloor$ byte errors, the RS decoder detects the presence of excessive errors and asserts the ERROROUTn signal to notify the user.

Assume that the byte size is 8, the redundant check parameter is 32, and a 122-bit burst error is input to the RS decoder. The RS decoder can correct up to T = 16 byte errors. A 122-bit burst can be divided into 17 bytes as shown in Figure 7.9, where each *e* represents a one bit error. Because the redundancy is 32, the decoder corrects up to 16 byte errors. Because the 122-bit burst corrupts 17 consecutive bytes, the maximum guaranteed correctable burst length in this example is 121 bits.

Figure 7.9 122-Bit Burst Example



7.3.2 Features

- Flag for corrected errors
- Complies with CCITT-recommended CCIR723 standard for digital TV transmission
- DVB/DSS compliant
- Decoder channel output counts for uncorrected data and error vector data
- ERROROUTn signal flags uncorrectable errors
- (204, 188) Reed-Solomon Code Format for DVB
- (146, 130) Reed-Solomon Code Format for DSS

7.3.3 Performance Analysis

The performance of the code against independent random byte errors can be computed by the equation:

Equation 7.1

$$q = \sum_{i=T+1}^{N} \frac{i}{N}\binom{N}{i} p^i (1-p)^{N-i}$$

where:

N = Code word length in bytes

p = Input byte error rate

T = Number of errors to correct

q = Output byte error rate

$\binom{N}{i}$ = Binomial coefficient that represents the number of ways of choosing i items from a collection of N distinct items

When more than T byte errors occur in a code word, the RS decoders usually detect the presence of excessive errors and raise the uncorrectable error flag to notify the user. However, there is a small probability that the erroneous decoded code word remains undetected. The undetected erroneous code word rate is:

$$\frac{1}{T!}\left(\frac{N}{2^m-1}\right)^T \sum_{i=T+1}^{N} \binom{N}{i} p^i (1-p)^{N-i}$$

7.4 Descrambler Module Architecture and Operation

Figure 7.10 shows a block diagram of the Descrambler. The Descrambler performs two functions:

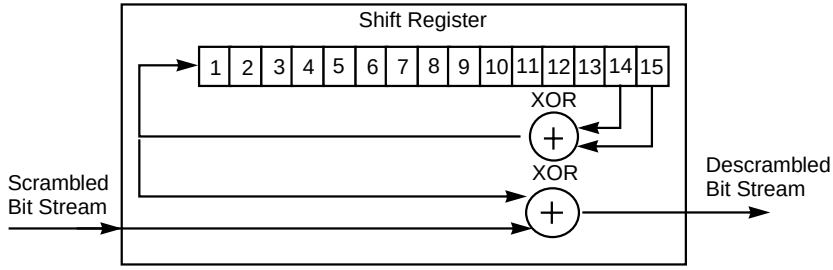
- Generates a pseudorandom binary sequence (PRBS) that modifies the incoming data stream
- Properly aligns data with the PRBS

Note: The Descrambler module is used only in the DVB mode of operation.

7.4.1 PRBS Generation

The block diagram of Figure 7.10 shows the operation of the PRBS.

Figure 7.10 Descrambler Block Diagram



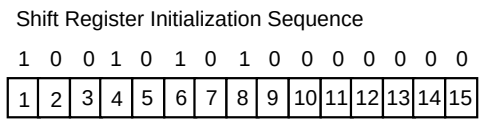
The following generator polynomial produces the pseudorandom bit sequence in the Descrambler:

$$1 + x^{14} + x^{15}$$

7.4.2 Data Alignment With PRBS

The 15-bit shift register is initialized with a specific value, as shown in Figure 7.11.

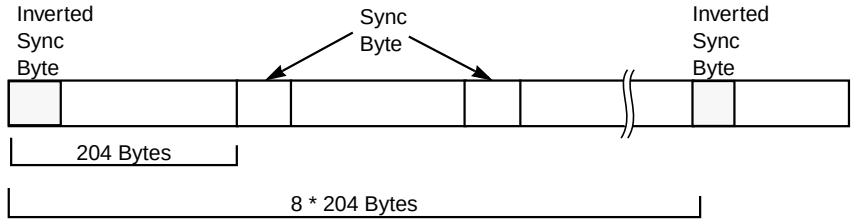
Figure 7.11 15-Bit Shift Register Initialization



The encoder inverts every eighth MPEG transport sync word (0x47) to generate a sync word (0xB8) that the decoder then uses to align the Descrambler with the incoming data stream. The first bit of the PRBS is applied to the first data bit following the inverted MPEG sync byte.

During the following seven noninverted MPEG sync words, the L64724 operates the Descrambler sequence generator, but does not modify the data stream. The L64724 resets the Descrambler after every inverted MPEG sync word (see Figure 7.12).

Figure 7.12 Inverted Sync Words in Descrambler



7.5 FEC Module Software Reset

The L64724 resets the internal datapath and control modules for the FEC portion of the device when the FEC_RST bit (Group 4, APR 55) is set to one. The Demodulator Module is not affected. You do not need to clear the bit back to zero to complete the reset. The L64724 issues a single reset pulse each time the microcontroller writes a one to the FEC_RST bit. When the FEC_RST bit is set, the L64724 resets the FEC processing unit and state machines to their initial states. The following operations occur when the FEC_RST bit is set to one:

- Internal datapath and control modules reset
- Group 4 registers unaffected by reset
- Group 3 UEC and CEC counters reset
- DVALIDOUT pin set LOW
- FSTARTOUT pin set LOW
- ERROROUTn pin set HIGH

Chapter 8
L64724 Specifications

This chapter provides the specifications for the L64724 Satellite Decoder from LSI Logic. The L64724 is implemented in 3.3-volt HCMOS.

This chapter contains the following sections:

- Section 8.1, “Electrical Requirements”
- Section 8.2, “AC Timing”
- Section 8.3, “L64724 Packaging”

All specifications are preliminary and subject to change.

8.1 Electrical Requirements

This section specifies the electrical requirements for the L64724 device. Four tables list electrical data in the following categories:

- Absolute Maximum Ratings — Table 8.1
- Recommended Operating Conditions — Table 8.2
- Capacitance — Table 8.3
- DC Characteristics — Table 8.4
- Pin Description Summary — Table 8.5

Table 8.1 L64724 Absolute Maximum Rating (Referenced to V_{SS})

Symbol	Parameter	Limits[1]	Unit
V_{DD}	DC Supply Voltage	–0.3 to + 3.9	V
V_{IN}	LVTTL Input Voltage	–1.0 to V_{DD} + 0.3	V
V_{IN}	5 V Compatible Input Voltage	–1.0 to 6.5	V
I_{IN}	DC Input Current	10	mA
T_{STG}	Storage Temperature Range (Plastic)	–40 to + 125	°C

1. Note that the ratings in this table are those beyond which permanent device damage is likely to occur. These values should not be used as the limits for normal device operation.

Table 8.2 L64724 Recommended Operating Conditions

Symbol	Parameter	Limits[1]	Unit
V_{DD}	DC Supply Voltage	+3.0 to 3.6	V

1. For normal device operation, adhere to the limits in this table. Sustained operation of a device at conditions exceeding these values, even if they are within the absolute maximum rating limits, may result in permanent device damage or impaired device reliability. Device functionality to stated DC and AC limits is not guaranteed if conditions exceed recommended operating conditions. Contact LSI Logic for the package thermal impedance information for this chip.

Table 8.3 L64724 Capacitance

Symbol	Parameter[1]	Max	Units
C_{IN}	Input Capacitance	5	pF
C_{OUT}	Output Capacitance	5	pF

1. Measurement conditions are V_{IN} = 3.3 V, T_A = 25 ˚C, and clock frequency = 1 MHz.

Table 8.4 lists the DC characteristics of the L64724.

Table 8.4 DC Characteristics of the L64724

Symbol	Parameter[1]	Condition[2]	Min	Typ	Max	Unit
V_{DD}	Supply Voltage	–	3.0	3.3	3.6	V
V_{IL}	Input Voltage LOW	–	V_{SS} – 0.5	–	0.8	V
V_{IH}	Input Voltage HIGH	LVTTL Com/Ind/Mil Temp Range	2.0	–	V_{DD} + 0.3	V
		5-volt Compatible	2.0	–	5.5	V
V_T	Switching Threshold	–	–	1.4	2.0	V
I_{IL}	Input Current Leakage	V_{DD} = Max, V_{IN} = V_{DD} or V_{SS}	–10	±1	10	mA
I_{IPU}	Input Current Leakage w/Pullup	V_{IN} = V_{SS}	–62	– 215	–384	mA
I_{IPD}	Input Current Leakage w/Pulldown	V_{IN} = V_{DD}	–62	– 215	–384	mA
V_{OH}	Output Voltage HIGH	I_{OH} = –1.0, –2.0, –4.0, –6.0, –8.0, –12.0 mA	2.4	–	V_{DD}	V
V_{OL}	Output Voltage LOW	I_{OH} = 1.0, 2.0, 4.0, 6.0, 8.0, 12.0 mA	–	0.2	0.4	V
I_{OZ}	3-state Output Leakage Current	V_{DD} = Max, V_{OUT} = V_{SS} or 3.5 V	–10	±1	10	µA
I_{OSP4}	Current P-Channel Output Short Circuit (4-mA Output Buffers)[3]	V_{OUT} = V_{DD} V_{OUT} = V_{SS}	–	–	140 –40	mA
I_{OSP6}	Current P-Channel Output Short Circuit (4-mA Output Buffers)[3]	V_{OUT} = V_{DD} V_{OUT} = V_{SS}	–	–	210 –60	mA
I_{DD}	Quiescent Supply Current	V_{IN} = V_{DD} or V_{SS}	–	–	2	mA

1. To identify an input with an internal pullup or pulldown resistor or an output's drive strength, see Table 8.5.
2. Specified at VDD = 3.3 V ± 5% at ambient temperature over the specified range.
3. Not more than one output may be shorted at time for a maximum duration on one second.

Table 8.5 L64724 Pin Description Summary

Mnemonic	Description	Type
A[2:0]	Address	TTL Input with pulldown[1]
ADCVDDI/Q	ADC Power	Input
ADCVSSI/Q	ADC Analog Ground	Input
ADCVREFI/Q	ADC Reference	Input
ADCVREFNI/Q	ADC Reference	Input
ASn	Address Strobe	TTL Input with pullup[1]
BCLKOUT	Byte Clock Out	Output
CLK	IVIN/QVIN Input Clock	TTL Input
CO[7:0]	Channel Data Out	3-State Output
COEn	Channel Output Enable	TTL Input with pullup[1]
CSn	Chip Select	TTL Input with pullup[1]
D[7:0]	Data	Bidirectional TTL
DTACK/POL	Data Acknowledge/Wait Polarity	Open Drain Output
DTACKn/WAIT	Data Acknowledge/Wait	Open Drain Output
DVALIDOUT	Valid Data Out	CMOS Output
ERROROUTn	Error Detection Flag	3-State Output
FSTARTOUT	Frame Start Output	Output
HOST_MODE	Serial or Parallel Interface Select[2]	Input
IBIAS	Current Bias I	Input
IBYPASS[5:0]	I Channel Data	TTL Inputs
IDDTN	Test Pin	Input
INTn	Interrupt	Open Drain Output
IVIN	I Channel Data	Input
LP2	Input to VCO	Input

(Sheet 1 of 2)

Table 8.5 L64724 Pin Description Summary (Cont.)

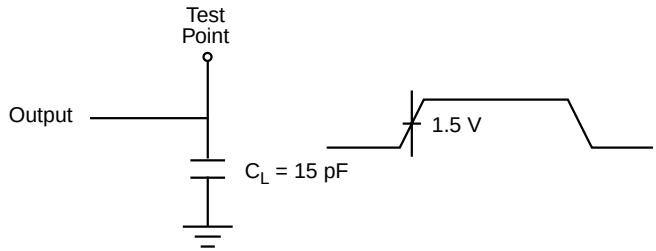
Mnemonic	Description	Type
LCLK	Decimated Clock Output	Output
PCLK	PLL Clock Output	Output
PLLVDD	PLL Power	Input
PLLVSS	PLL Ground	Input
PLLAGND	PLL Analog Ground	Input
PWRP	Power Control	Open Drain Output
QBYPASS[5:0]	Q Channel Data	TTL Inputs
QVIN	Q Channel Data	Input
READ/WRITE	Read/Write Strobe	TTL Input with pullup[1]
RESET	Reset	TTL Input
VDD	Digital Power Supply	Input
VSS	Digital Ground	Input
XCTR_IN	Control Input	CMOS Input
XCTR_OUT[3:0]	External Controls	CMOS Outputs
XOIN	Crystal Oscillator In	CMOS Input
XOOUT	Crystal Oscillator Out	CMOS Output
(Sheet 2 of 2)		

1. Do not use pullup or pulldown signals for active edge timing.
2. Serial Mode is the recommended interface mode. LSI Logic does not recommend parallel mode for new designs.

8.2 AC Timing

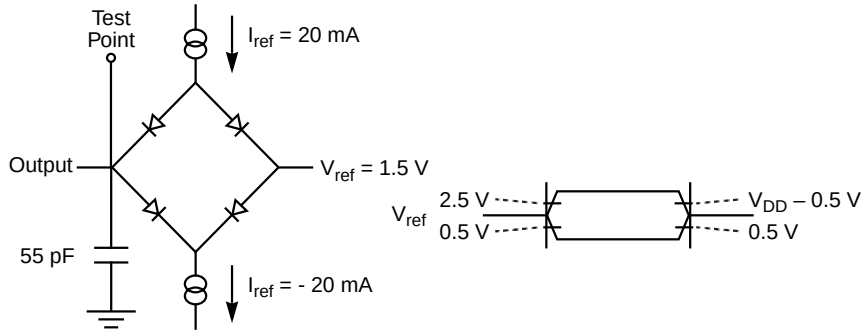
This section presents AC timing information of the L64724. During AC testing, HIGH inputs are driven to 3.0 V and LOW inputs are driven at 0 V. For transitions between HIGH, LOW, and invalid states, timing measurements are made at 1.5 V, as shown in Figure 8.1.

Figure 8.1 AC Test Load and Waveform for Standard Outputs



For 3-state outputs, timing measurements are made from the point at which the output turns ON or OFF. An output is ON when its voltage is greater than 1/2 V_{DD} or less than 0.5 V. An output is OFF when its voltage is less than V_{DD} – 0.5 V or greater than 0.5 V, as shown in Figure 8.2.

Figure 8.2 AC Test Load and Waveforms for 3-State Outputs



The timing parameters shown in Figures 8.3 through 8.7, refer to the numbers in column 1 of Tables 8.6 through 8.9.

Figure 8.3 L64724 Synchronous AC Timing

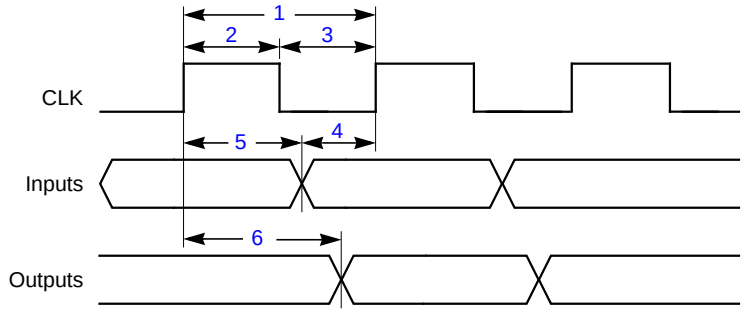


Figure 8.4 L64724 RESET Timing Diagram

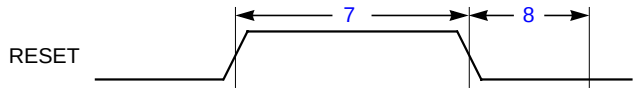


Figure 8.5 L64724 Bus 3-State Delay Timing

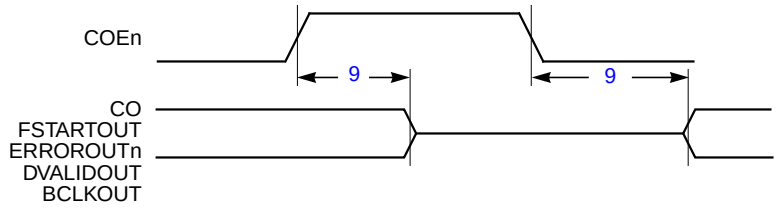


Figure 8.6 L64724 Decoder Read Cycle

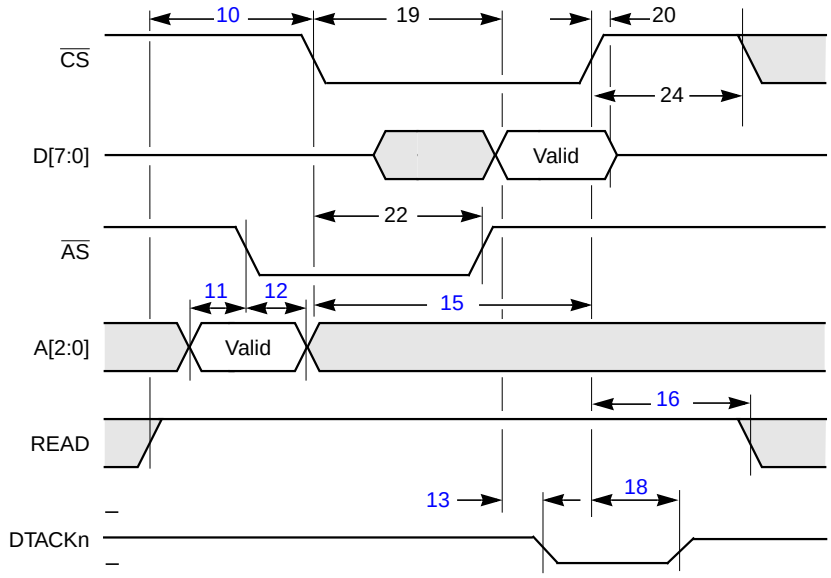


Figure 8.7 L64724 Decoder Write Cycle

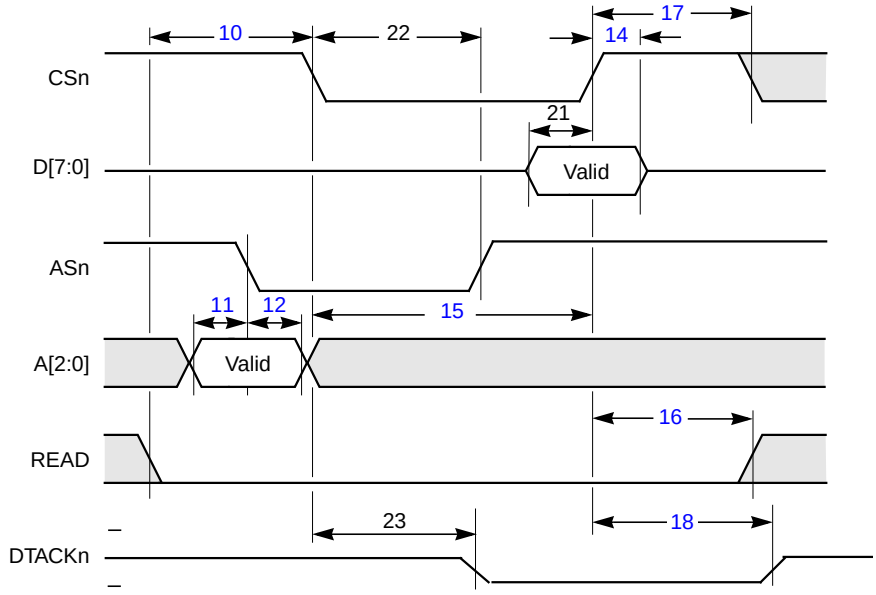


Table 8.8 shows the timing parameters valid for operation with the internal microcontroller disabled. Table 8.9 shows the timing for the microcontroller enabled. All parameters in the timing tables apply for T_A = 0 °C to 70 °C and a capacitive load of 15 pF.

Table 8.6 L64724-75 AC Timing Parameters with Microcontroller Disabled

Parameter		Description	Register Groups	75 MHz		Unit
				Min	Max	
1	t_{CYCLE}	Clock Cycle for CLK	–	13.3	–	ns
2	t_{PWH}	Clock Pulse Width HIGH	–	6.0	7.3	ns
3	t_{PWL}	Clock Pulse Width LOW	–	6.0	7.3	ns
4	t_S	Input Setup time to CLK	–	0	–	ns
5	t_H	Input Hold to CLK	–	4	–	ns
6	t_{OD}	Output Delay from CLK	–	–	9	ns
7	t_{RWH}	RESET Pulse Width HIGH	–	3	–	CLK Cycles[1]
8	t_{WK}	Wake-Up Time	–	280	–	CLK Cycles[1]
9	T_{DLY}	Delay from COEn	–	–	15.0	ns
10	t_{SURCS}	READ Setup Before CSn LOW	–	0.0	–	ns
11	t_{SUA}	A[2:0] Setup Before ASn LOW	–	15.0	–	ns
12	t_{HLDA}	A[2:0] Hold After ASn LOW	Groups 0, 1, 4 Groups 2, 3	0.0 0	–	ns CLK cycles[1]
13	t_{DCSDTL}	Data Valid to DTACKn/WAIT LOW	Groups 0, 1, 4 Groups 2, 3	–	15.0 1	ns CLK Cycles[1]
14	t_{HLDD}	Write Data Hold After CSn HIGH	–	0.0	–	ns

(Sheet 1 of 2)

Table 8.6 L64724-75 AC Timing Parameters with Microcontroller Disabled (Cont.)

Parameter		Description	Register Groups	75 MHz		Unit
				Min	Max	
15	t_{CYCLE_CS}	Minimum CSn Width	Groups 0, 1, 4 Groups 2, 3	45.0 5	–	ns CLK Cycles[1]
16	t_{HLDRCS}	READ Hold After CSn HIGH	–	0.0	–	ns
17	t_{WRREC}	Write Recovery Time	Groups 0, 1, 4 Groups 2, 3	30.0 3	–	ns CLK Cycles[1]
18	t_{DCSDTH}	CSn High to DTACKn/WAIT HIGH	Groups 0, 1, 4 Groups 2, 3	–	28.0 28.0	ns ns
19	t_{DELD}	CSn LOW to Data Valid	Groups 0, 1, 4 Groups 2, 3	17.0	30.0 4	ns CLK Cycles[1]
20	t_{DELLZ}	CSn HIGH to Data 3-State	Groups 0-,4	14.0	24.0	ns
21	t_{SUD}	Data Setup Before CSn Change	–	15.0	–	ns
22	t_{HLDW}	ASn Hold after CSn LOW	Groups 0,1,4 Groups 2,3	10.0 2	–	ns CLK Cycles[1]
23	t_{DELDTL}	CSn LOW to DTACKn/WAIT LOW	Groups 0, 1, 4 Groups 2, 3	–	45 5	ns CLK Cycles[1]
24	t_{RDREC}	Read Recovery Time	Groups 0, 1, 4 Groups 2, 3	30.0 5	–	ns CLK Cycles[1]

(Sheet 2 of 2)

1. Guaranteed by design.

Table 8.7 L64724-75 AC Timing Parameters with Microcontroller Enabled

Parameter		Description	Register Groups	75 MHz		Unit
				Min	Max	
1	t_{CYCLE}	Clock Cycle for CLK	–	13.3	–	ns
2	t_{PWH}	Clock Pulse Width HIGH	–	6.0	7.3	ns
3	t_{PWL}	Clock Pulse Width LOW	–	6.0	7.3	ns
4	t_S	Input Setup time to CLK	–	0	–	ns
5	t_H	Input Hold to CLK	–	4	–	ns
6	t_{OD}	Output Delay from CLK	–	–	9	ns
7	t_{RWH}	Reset Pulse Width HIGH	–	3	–	CLK Cycles[1]
8	t_{WK}	Wake-Up Time	–	280	–	CLK Cycles[1]
9	T_{DLY}	Delay from COEn	–	–	15.0	ns
10	t_{SURCS}	READ Setup Before CSn LOW	–	0.0	–	ns
11	t_{SUA}	A[2:0] Setup Before ASn LOW	–	15.0	–	ns
12	t_{HLDA}	A[2:0] Hold After ASn LOW	Groups 0–4	0.0	–	ns
13	t_{DCSDTL}	Data Valid to DTACKn/WAIT LOW	Groups 0–4	–	7 ns + 1 cycle	ns CLK Cycles[1]
14	t_{HLDD}	Write Data Hold After CSn HIGH	–	0.0	–	ns
15	t_{CYCLE_CS}	Minimum CSn Width	Groups 0–4	31	–	CLK Cycles[1]
16	t_{HLDRCS}	READ Hold After CSn HIGH	–	0.0	–	ns
17	t_{WRREC}	Write Recovery Time	Groups 0–4	5	–	CLK Cycles[1]
18	t_{DCSDTH}	CSn HIGH to DTACKn/WAIT HIGH	Groups 0–4	–	28.0	ns
19	t_{DELD}	CSn LOW to Data Valid	Groups 0–4	17.0	28	CLK Cycles[1]
20	t_{DELLZ}	CSn HIGH to Data 3-State	Groups 0–4	14.0	24.0	ns
21	t_{SUD}	Data Setup Before CSn Change	–	15.0	–	ns
22	t_{HLDW}	ASn Hold after CSn LOW	Groups 0–4	2	–	CLK Cycles[1]

(Sheet 1 of 2)

Table 8.7 L64724-75 AC Timing Parameters with Microcontroller Enabled (Cont.)

Parameter		Description	Register Groups	75 MHz		Unit
				Min	Max	
23	t_{DELDTL}	CSn LOW to DTACKn/WAIT LOW	Groups 0–4	–	30	CLK Cycles[1]
24	t_{RDREC}	Read Recovery Time	Groups 0–4	5	–	CLK Cycles[1]
(Sheet 2 of 2)						

1. Guaranteed by design.

Table 8.8 L64724-90 AC Timing Parameters with Microcontroller Disabled

Parameter		Description	Groups [1]	90 MHz		Unit
				Min	Max	
1	t_{CYCLE}	Clock Cycle for PCLK	–	11.1	–	ns
2	t_{PWH}	Clock Pulse Width HIGH	–	5.25	6.1	ns
3	t_{PWL}	Clock Pulse Width LOW	–	5.25	6.1	ns
4	t_S	Input Setup time to CLK	–	0	–	ns
5	t_H	Input Hold to CLK	–	4	–	ns
6	t_{OD}	Output Delay from CLK	–	–	9	ns
7	t_{RWH}	Reset Pulse Width HIGH	–	3	–	CLK Cycles[2]
8	t_{WK}	Wake-Up Time	–	280	–	CLK Cycles[2]
9	TDLY	Delay from COEn	–	–	15.0	ns
10	tSURCS	READ Setup Before CSn LOW	–	0.0	–	ns
11	tSUA	A[2:0] Setup Before ASn LOW	–	15.0	–	ns
12	tHLDA	A[2:0] Hold After ASn LOW	Groups 0, 1, 4 Groups 2, 3	0.0 0	–	ns CLK cycles[2]
13	tDCSDTL	Data Valid to DTACKn/WAIT LOW	Groups 0, 1, 4 Groups 2, 3	–	15.0 1	ns CLK Cycles[2]
(Sheet 1 of 2)						

Table 8.8 L64724-90 AC Timing Parameters with Microcontroller Disabled (Cont.)

Parameter		Description	Groups [1]	90 MHz		Unit
				Min	Max	
14	tHLDD	Write Data Hold After CSn HIGH	–	0.0	–	ns
15	tCYCLE_CS	Minimum CSn Width	Groups 0, 1, 4 Groups 2, 3	45.0 5	–	ns CLK Cycles[2]
16	tHLDRCS	READ Hold After CSn HIGH	–	0.0	–	ns
17	tWRREC	Write Recovery Time	Groups 0, 1, 4 Groups 2, 3	30.0 3	–	ns CLK Cycles[2]
18	tDCSDTH	CSn HIGH to DTACKn/WAIT HIGH	Groups 0-4	–	28.0	ns
19	t_{DELD}	CSn LOW to Data Valid	Groups 0, 1, 4 Groups 2, 3	17.0	30.0 4	ns CLK Cycles[2]
20	t_{DELLZ}	CSn HIGH to Data 3-State	Groups 0-4	14.0	24.0	ns
21	t_{SUD}	Data Setup Before CSn Change	–	15.0	–	ns
22	t_{HLDW}	ASn Hold after CSn LOW	Groups 0, 1, 4 Groups 2, 3	10.0 2	–	ns CLK Cycles[2]
23	t_{DELDTL}	CSn LOW to DTACKn/WAIT LOW	Groups 0, 1, 4 Groups 2, 3	–	45 5	ns CLK Cycles[2]
24	t_{RDREC}	Read Recovery Time	Groups 0, 1, 4 Groups 2, 3	30.0 5	–	ns CLK Cycles[2]

(Sheet 2 of 2)

1. The groups referred to are the register groups.
2. Guaranteed by design.

Table 8.9 L64724-90 AC Timing Parameters with Microcontroller Enabled

Parameter		Description	Groups [1]	90 MHz		Unit
				Min	Max	
1	t_{CYCLE}	Clock Cycle for PCLK	–	11.1	–	ns
2	t_{PWH}	Clock Pulse Width HIGH	–	5.25	6.1	ns
3	t_{PWL}	Clock Pulse Width LOW	–	5.25	6.1	ns
4	t_{S}	Input Setup time to CLK	–	0	–	ns
5	t_{H}	Input Hold to CLK	–	4	–	ns
6	t_{OD}	Output Delay from CLK	–	–	9	ns
7	t_{RWH}	Reset Pulse Width HIGH	–	3	–	CLK Cycles[2]
8	t_{WK}	Wake-Up Time	–	280	–	CLK Cycles[2]
9	T_{DLY}	Delay from COEn	–	–	15.0	ns
10	t_{SURCS}	READ Setup Before CSn LOW	–	0.0	–	ns
11	t_{SUA}	A[2:0] Setup Before ASn LOW	–	15.0	–	ns
12	t_{HLDA}	A[2:0] Hold After ASn LOW	Groups 0–4	0.0	–	ns
13	t_{DCSDTL}	Data Valid to DTACKn/WAIT LOW	Groups 0–4	–	7 ns + 1 cycle	ns CLK Cycles[2]
14	t_{HLDD}	Write Data Hold After CSn HIGH	–	0.0	–	ns
15	t_{CYCLE_CS}	Minimum CSn Width	Groups 0–4	31	–	CLK Cycles[2]
16	t_{HLDRCS}	READ Hold After CSn HIGH	–	0.0	–	ns
17	t_{WRREC}	Write Recovery Time	Groups 0–4	5	–	CLK Cycles[2]
18	t_{DCSDTH}	CSn HIGH to DTACKn/WAIT HIGH	Groups 0–4	–	28.0	ns

(Sheet 1 of 2)

Table 8.9 L64724-90 AC Timing Parameters with Microcontroller Enabled (Cont.)

Parameter		Description	Groups [1]	90 MHz		Unit
				Min	Max	
19	t_{DELD}	CSn LOW to Data Valid	Groups 0–4	17.0	28	CLK Cycles[2]
20	t_{DELLZ}	CSn HIGH to Data 3-State	Groups 0–4	14.0	24.0	ns
21	t_{SUD}	Data Setup Before CSn Change	–	15.0	–	ns
22	t_{HLDW}	ASn Hold after CSn LOW	Groups 0–4	2	–	CLK Cycles[2]
23	t_{DELDTL}	CSn Low to DTACKn/WAIT LOW	Groups 0–4	–	30	CLK Cycles[2]
24	t_{RDREC}	Read Recovery Time	Groups 0–4	5	–	CLK Cycles[2]
(Sheet 2 of 2)						

1. The groups referred to are the register groups.
2. Guaranteed by design.

8.3 L64724 Packaging

The L64724-75 is available in a 100-pin PQFP package. The L64724-90 is available in a 100-pin MQFP package. Table 8.10 lists ordering information for the L64724.

Table 8.10 L64724 Ordering Information

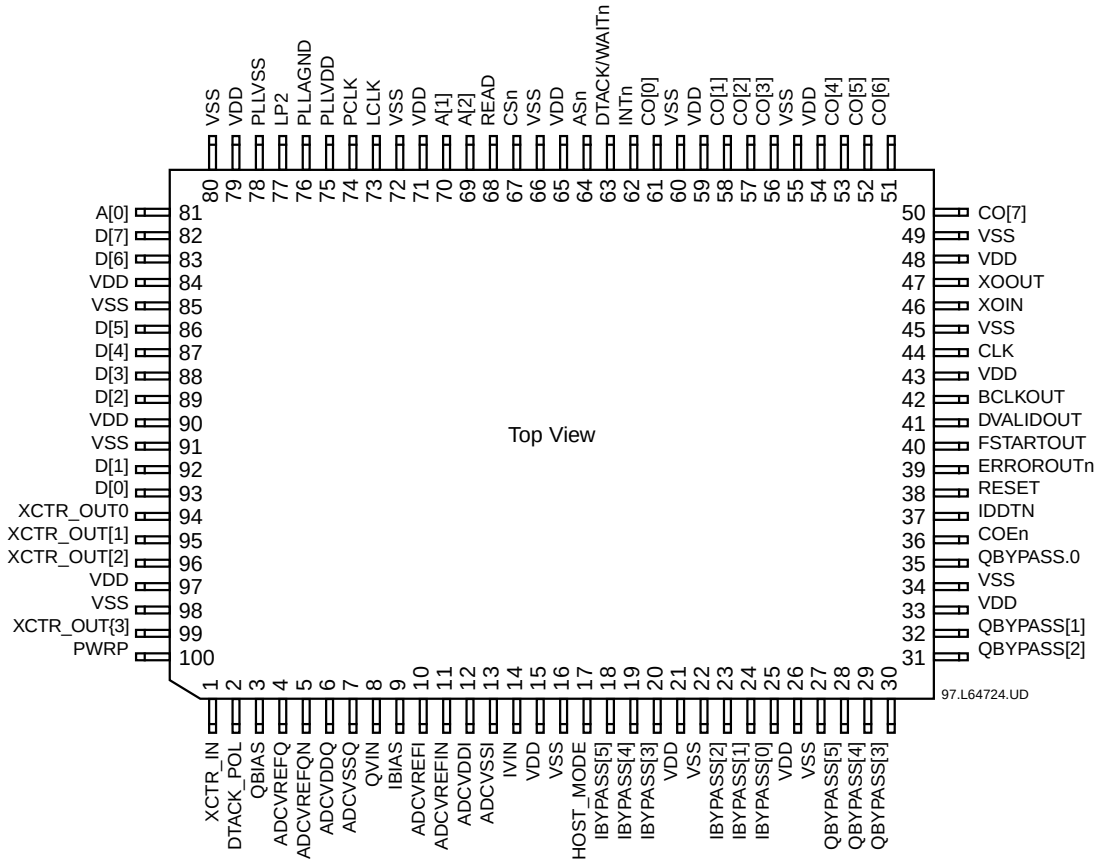
Order Number	Clock Frequency (MHz)	Package Type	Operating Range
65035A2-002	75	100-pin PQFP	Commercial
65035A1-004	90	100-pin MQFP	Commercial

The tables and figures that follow provide a pinout and a mechanical drawing for the package.

8.3.1 L64724 Pinout

Figure 8.8 gives the pinout for the 100-pin PQFP/MQFP L64724 package.

Figure 8.8 100-Pin PQFP/MQFP Pinout



8.3.2 Mechanical Drawings

Figure 8.9 is a mechanical drawing for the 100-pin PQFP/MQFP L64724-75 package.

Note: The L64724-75 is available in a PQFP package and can be used for applications that implement data rates of up to 31 Mbaud and sampling frequencies of up to 75 MHz. For applications that require higher data rates, with sampling frequencies up to 90 MHz, the L64724-90 is available in an MQFP package.

Figure 8.9 100-Pin PQFP/MQFP Mechanical Drawing

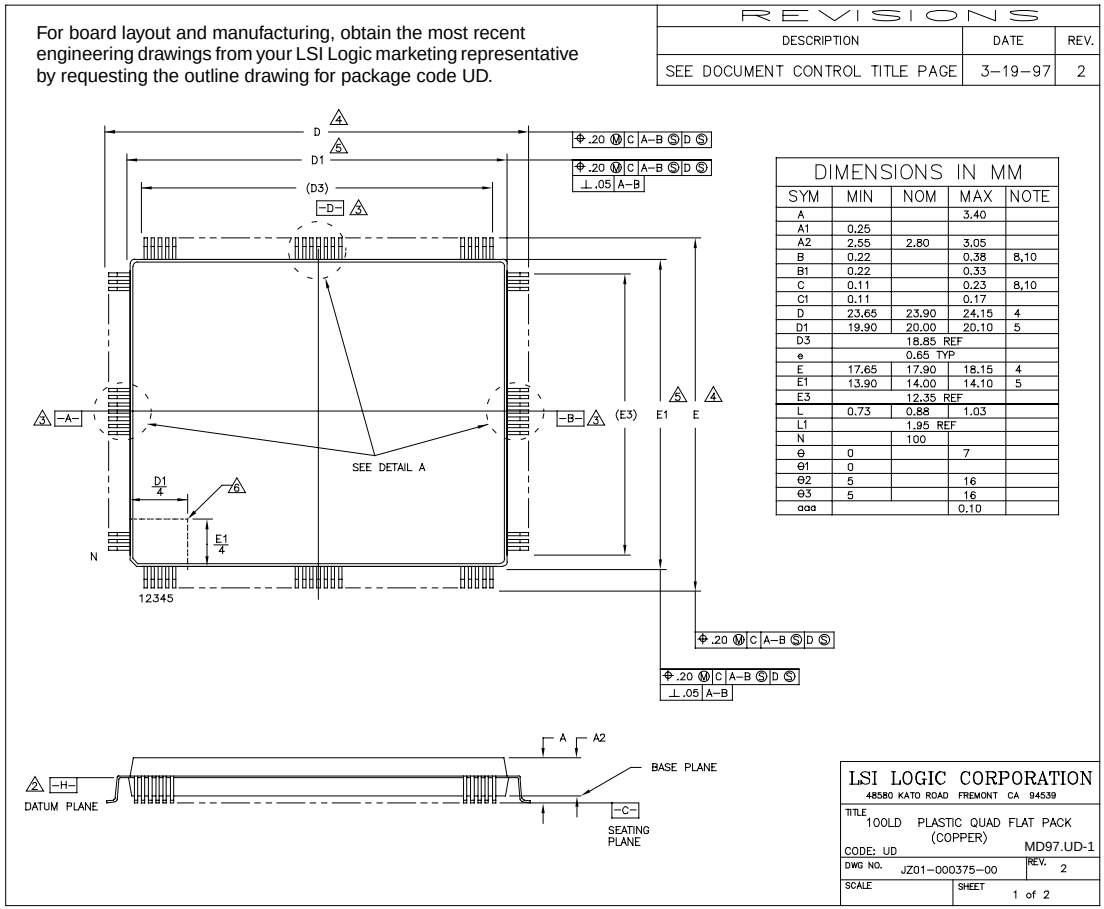
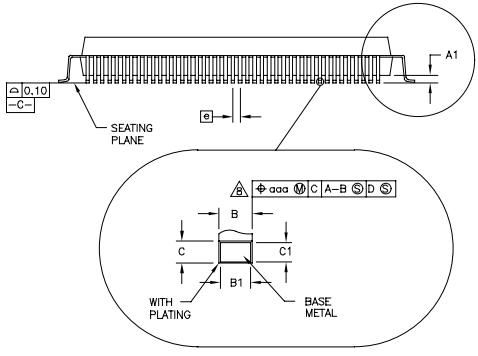
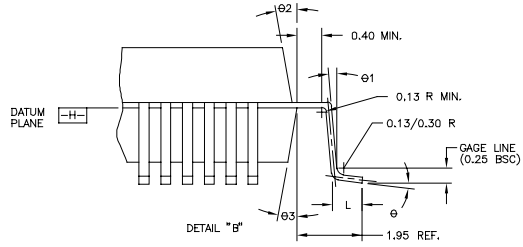


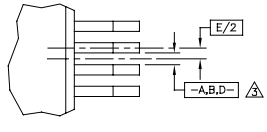
Figure 8.9 100-Pin PQFP/MQFP Mechanical Drawing (Cont.)



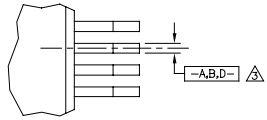


NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1982.
2. DATUM PLANE –H– IS LOCATED AT THE MOLD PARTING LINE AND IS COINCIDENT WITH THE BOTTOM OF THE LEADS WHERE THE LEAD EXITS THE PLASTIC BODY.
3. DATUMS A–B AND –D– TO BE DETERMINED AT DATUM PLANE –H–.
4. TO BE DETERMINED AT SEATING PLANE –C–.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .25mm/.010" PER SIDE. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –H–.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. CONTROLLING DIMENSION: MILLIMETER.
8. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .08mm/.003" TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACING BETWEEN ADJACENT LEADS TO BE 0.10mm.
9. MARKING AREA MUST BE FREE FROM PACKAGE SURFACE PROTRUSION OR INTRUSION.
10. PLATING THICKNESS INCLUDED, PLATING THICKNESS TO BE 0.005mm MINIMUM, 0.020mm MAXIMUM.



EVEN LEAD SIDES



ODD LEAD SIDES

DETAIL "A"

For board layout and manufacturing, obtain the most recent engineering drawings from your LSI Logic marketing representative by requesting the outline drawing for package code UD.

LSI LOGIC CORPORATION	
48580 KATO ROAD FREMONT CA 94539	
TITLE: 100LD PLASTIC QUAD FLAT PACK (COPPER)	MD97.UD-2
CODE: UD	
DWG NO. JZ01–000375–00	REV. 2
SCALE	SHEET 2 of 2

Appendix A
Programming the L64724 Using the Serial Bus Protocol

This appendix discusses how to program the L64724 internal registers and data tables in Serial Host Interface mode. This chapter is intended primarily for system programmers who are developing software drivers using the serial bus.

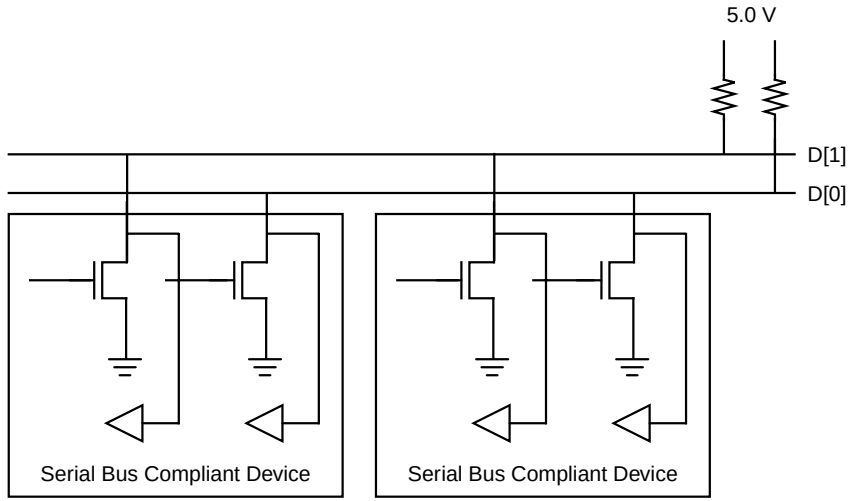
This chapter contains the following sections:

- Section A.1, “Serial Bus Protocol Overview”
- Section A.2, “Programming the Slave Address Using the Serial Bus Interface”
- Section A.3, “Write Cycle Using the Serial Bus Interface”
- Section A.4, “Read Cycle Using the Serial Bus Interface”

A.1 Serial Bus Protocol Overview

The multimaster serial bus interface has two signal lines—D[1] (Serial Data) and D[0] (Serial Clock)—that are connected to the bus as shown in Figure A.1. External pullup resistors are required to hold the bus HIGH when the bus is not in operation.

Figure A.1 Serial Bus Architecture



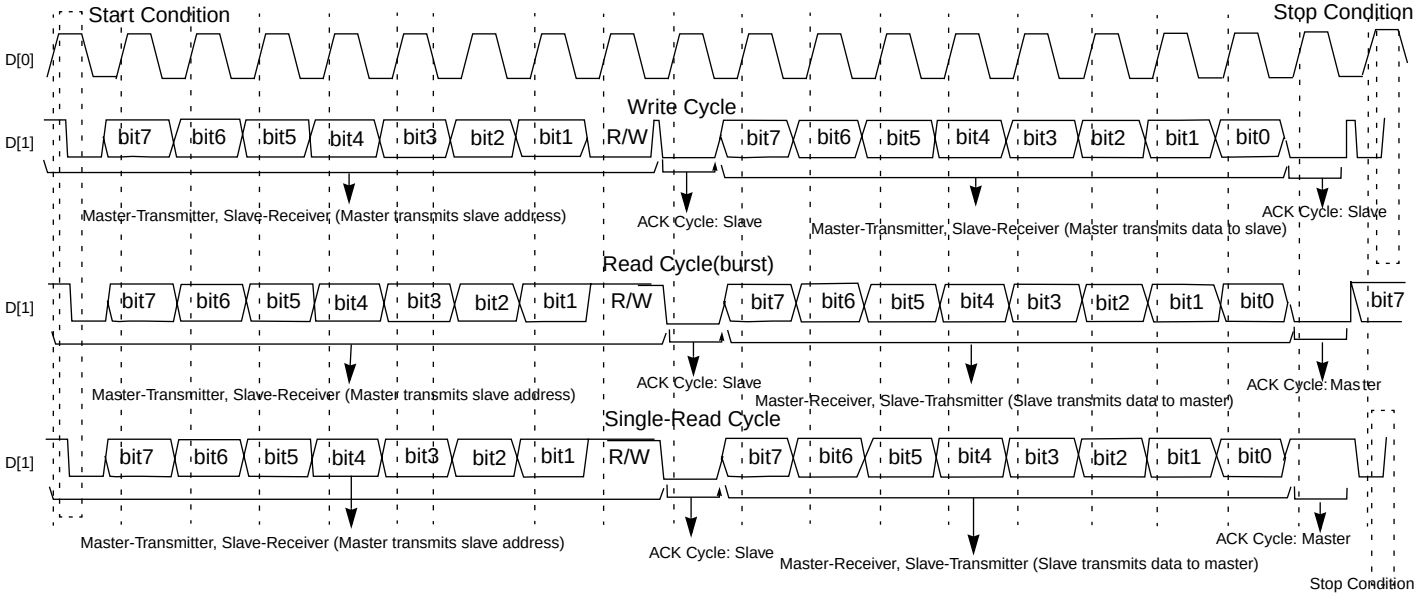
Serial Host Interface mode is selected when the HOST_MODE input pin is deasserted (LOW). In Serial Host Interface mode, data is transferred on the D[1] pin, synchronized to a serial clock that is input on the LSB of the Host Data Bus, D[0]. The serial data clock can have a maximum frequency of 400 kHz. The Host Data Bus pins D[3:2] are used to input the two LSBs of the slave address, which the serial bus protocol requires. The slave address definition is shown below:

Figure A.2 7-Bit Slave Address for the L64724 Serial Bus

0	0	0	1	1	D[3]	D[2]

The bus master always generates the clock and cycle start and stop conditions. Figure A.3 gives an overview of the Read and Write cycles using the Serial Bus Protocol.

Figure A.3 Serial Bus Write/Read Cycle Overview



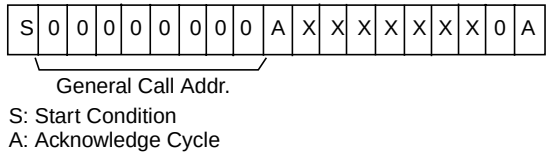
Start Condition: The master (drives D[0]) indicates the start of a cycle by pulling D[1] LOW when D[0] is HIGH.
Stop Condition: The master (drives D[0]) indicates the end of a cycle by releasing D[1] HIGH when D[0] is HIGH.
Data Transfer: All data changes on the D[1] line occur only when clock is LOW, except for the special cases outlined above to indicate Start/Stop cycles.
Acknowledge: The receiver always generates the acknowledge. In the case of a single read, the master-receiver does not generate an ACK so that it can generate the Stop condition (as indicated above).

A.2 Programming the Slave Address Using the Serial Bus Interface

A general call address operation on the serial bus is indicated when the master generates a start condition followed by eight zeroes (see Figure A.4.) A general call address operation addresses every device on the serial bus. Any device that requires information to be supplied through this general call structure should acknowledge the cycle (see Figure A.3.)

The second byte, when set to 0b00000110, indicates a reset and a hardware write of the programmable part of the slave address. The L64724 must read the D[3:2] pins, which form the two LSBs of the slave address. The D[3:2] pins are unused when the serial interface is in use, and can be hardwired to any of the four possible combinations.

Figure A.4 General Call Structure



S: Start Condition
A: Acknowledge Cycle

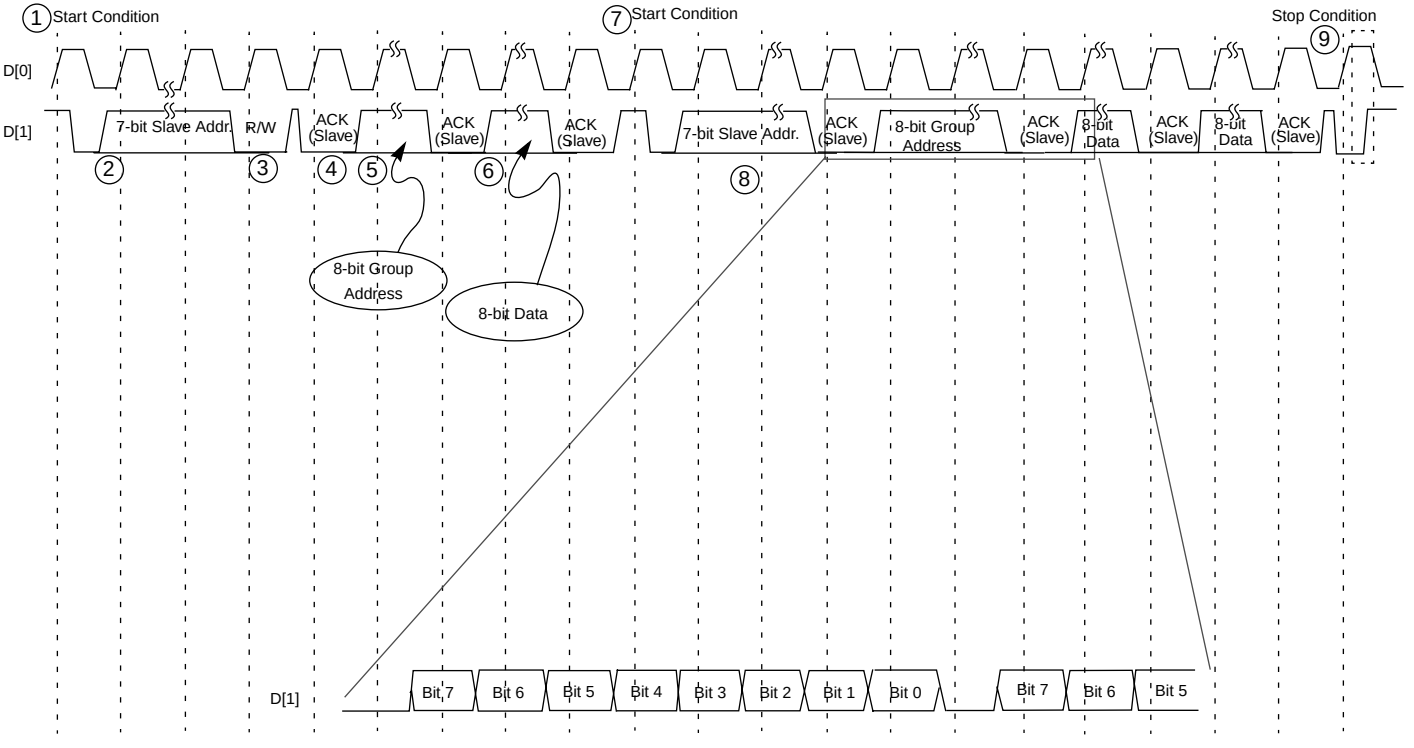
A.3 Write Cycle Using the Serial Bus Interface

Refer to Figure A.5 for a burst or a single write cycle. The following steps must take place for a write cycle:

1. The master starts the cycle with the start condition.
2. The master transmits the 7-bit slave address.
3. The master transmits the eighth bit (R/W) cleared to 0 to indicate a write cycle.
4. The addressed slave acknowledges the reception of the slave address by deasserting D[1] (LOW) in the ACK cycle.
5. The master sends the 8-bit Group 0 address (0x0) to indicate that the APR is to be loaded. Group 0 is accessed only to load the APR.

6. The master sends the 8-bit data, which initializes the Address Pointer register (APR0/1).
7. The master generates another start condition.
8. The master repeats steps 2–7 to address the appropriate group and write one or more data bytes.
9. The master issues a stop condition to terminate the cycle.

Figure A.5 Burst Write or Single Write to Slave (Master-Transmitter, Slave-Receiver)



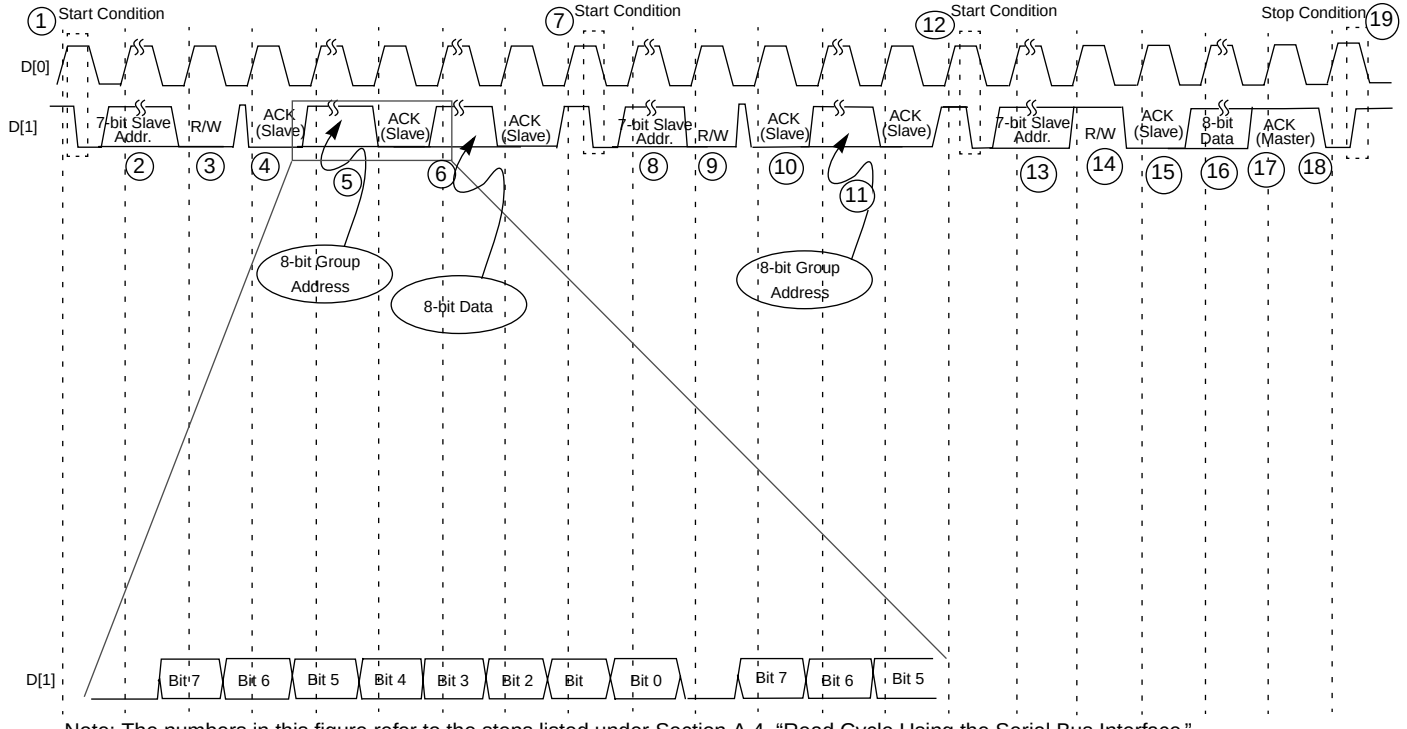
Note: The numbers in this figure refer to the steps listed under Section A.3, “Write Cycle Using the Serial Bus Interface.”

A.4 Read Cycle Using the Serial Bus Interface

Please refer to Figure A.6 for a burst or a single read cycle. The following steps must take place for a read cycle:

1. The master starts the cycle by issuing a start condition.
2. The master transmits the 7-bit slave address.
3. The master sets the R/W bit = 0 to indicate a write cycle.
4. The addressed slave acknowledges the reception of the slave address by driving D[1] LOW in the ACK cycle.
5. The Master sends the 8-bit Group 0 address (0x0) to indicate that the APR is to be loaded. Group 0 is accessed only to load the APR.
6. The master then sends the 8-bit data. This data is used to initialize the base pointer (APR0/1).
7. The master does a repeat start condition.
8. The master transmits the 7-bit slave address.
9. The master sets the R/W bit = 0 to indicate a write cycle.
10. The addressed slave acknowledges the reception by driving D[1] LOW in the ACK cycle.
11. The master transmits the number of the group that it wishes to read (which is acknowledged by the slave).
12. The master issues another start condition.
13. The master transmits the 7-bit slave address.
14. The master sets the R/W bit = 1 to indicate a read cycle.
15. The slave drives D[1] LOW to acknowledge.
16. The slave starts transmitting the data, MSB first.
17. The master has to provide the acknowledge by driving D[1] LOW during the ACK cycle.
18. In the case of a single read, the master does not drive D[1] LOW during the ACK cycle after reception of the first byte. The slave responds to this by relinquishing control of the bus and waiting for the master to issue a stop condition. For burst reads, the master drives D[1] LOW for each byte it receives during the ACK cycle, except for the last byte.
19. The master terminates the cycle by issuing a stop condition.

Figure A.6 Burst Read or Single Read Cycle from Slave



Note: The numbers in this figure refer to the steps listed under Section A.4, “Read Cycle Using the Serial Bus Interface.”

Appendix B
L64724 Application Notes

This appendix provides updated information on the use of the LSI Logic L64724 Satellite Receiver in a typical application. It contains the following sections:

- Section B.1, "L64724 QPSK Demodulator Acquisition and Debugging Tips," describes how to program and monitor the L64724's AGC, Clock Synchronization, and Carrier Synchronization loops.
- Section B.2, "Demodulator Configuration Tips," gives useful hints on selecting crucial parameters such as Sampling frequency, Decimation filter configuration, and Loop Bandwidths.
- Section B.3, "QPSK Demodulator and FEC Configuration Example: High Data Rates," shows an example of how the demodulator and FEC portion of the L64724 can be programmed for high data rates.
- Section B.4, "QPSK Demodulator and FEC Configuration Example: Low Data Rates," shows an example of how the demodulator and FEC portion of the L64724 can be programmed for low data rates where the oversampling ratio is greater than four.

Also, refer to the *L64724 Satellite Receiver Evaluation Board User's Guide,* which gives a good description of board related issues and demodulator and FEC programming guidelines.

B.1 L64724 QPSK Demodulator Acquisition and Debugging Tips

This section presents a debugging procedure to follow in case the L64724 QPSK demodulator fails to lock.

B.1.1 Automatic Gain Control (AGC) Loop

The AGC loop must lock first. When the AGC loop is closed, the signal level at the analog-to-digital converter (ADC) input is 0.588 (1/1.7) times the ADC range, assuming the PWR_REF register (Group 4, APR 24) is set to its correct value and DF_GAIN = 1.

A simple test that you can perform is to change the power of the transmitted signal and observe the I or Q channels with an oscilloscope just before the ADC input. Make sure that the peak-to-peak signal range is about 1/1.7 of the peak-to-peak ADC range. Also check that the AGC can keep the signal level fixed, even when the transmitted power is changed. Observe that the AGC voltage at the loop output is changing with the changes in the transmitted power. You may need to toggle the PWRP bit (Group 4, APR 54) to switch the polarity of the PWRP output.

The parameters in the following subsections are related to the AGC loop.

B.1.1.1 Group 4, APR 21—Set to 0x00

Clear the PLL_BP bit to 0 to enable the internal PLL to generate the A/D clock. Clear the CLK_DIV1[4:0] bits to 0 because the internal PLL is used. Set Group 4, APR 21 to 0x00.

B.1.1.2 Group 4, APR 21–23—Set to 0x00

Set Group 4 APR 21 and 23 to 0x00, because the CLK_DIV bits are unused when the internal PLL has been selected.

B.1.1.3 Group 4, APR 24

The PWR_REF[7:0] parameter controls the signal level at the input of the ADC. It should be set to the value given in Equation 5.26, on page 5-21.

B.1.1.4 Group 3, APR 10

The PWR_LVL[7:0] field is proportional to the mean value of the AGC level. With an AGC amplification range of 0 dB to – 40 dB, Table B.1 shows the corresponding PWR_LVL settings and amplification levels.

Table B.1 PWR_LVL Register Setting

PWR_LVL Setting	Amplification (dB)
0	0
128	–20
255	–40

B.1.1.5 Group 4, APR 26

The SCALE[7:0] parameter controls the internal signals DEMI and DEMQ. It does not affect the loop itself, but it is related to PWR_REF by Equation B.1.

Equation B.1

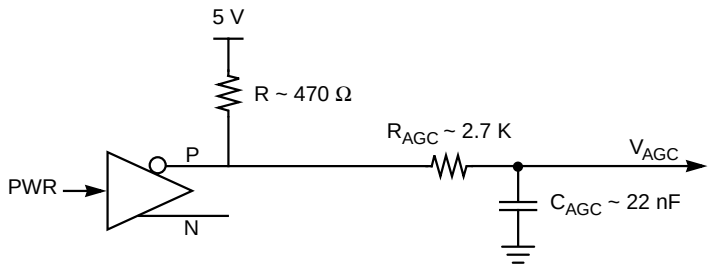
$$SCALE = \frac{2047 \cdot \sqrt{1 + \left(\frac{E_s}{N_o}\right)^{-1}}}{\sqrt{2 \cdot PWR - REF}}$$

If PWR_REF = 84, SCALE = 186 (for E_S/N_0 = 4 dB).

B.1.1.6 PWRP Pin

Connect the L64724 PWRP output pin to 5 volts using a 470-ohm pullup resistor. The PWRP pin is then connected to an RC loop filter with a time constant of ~60 microseconds. Figure B.1 shows how to connect the PWRP pin to the AGC circuit.

Figure B.1 AGC Loop Control



For more information on the AGC loop, see Section 5.8, “Automatic Gain Control (AGC),” page 5-20.

B.1.2 Clock Loop

Set the loop bandwidth according to Equation 5.8, on page 5-10. The CLK_LCF status bit (Group 3, APR 11, bit 3) indicates whether the clock loop is locked.

B.1.3 Carrier Loop

The following steps show how to set up the carrier loop.

1. Set the CAR_SW bit to 1 the and CAR_OPEN bit to 0 in the Carrier Loop Configuration register (Group 4, APR 41). These bit settings force the sweep to begin. Auto sweep can be selected to sweep between upper and lower sweep limits.
2. Change the upper and lower sweep limits registers (CAR_USWL and CAR_LSWL in Group 4, APR 34–37) and observe CAR_NCOF (Group 3, APR 7).
3. Change the value in the Carrier Sweep Rate register (CAR_SWR in Group 4, APR 32 and 33). If the sweep rate is fast, you may not be able to turn the sweep off fast enough through manual intervention, the microcontroller will have to do this in real time.

B.1.4 QPSK Demodulator Debugging Summary

The following steps summarize how to debug the QPSK Demodulator portion of a system that includes the L64724.

1. Ensure that the AGC loop functions properly.
2. Ensure that the clock loop is locked.
3. Set the CAR_SW and CAR_OPEN bits in the Carrier Loop Configuration register to 0b01. The loop should now lock or at least slow down near the center of the frequency range.
4. If the carrier still does not lock, check the CAR_SWP parameter and recalculate the loop constant values if needed. Each one of these parameters affects the behavior of the loop.
5. If the carrier seems to lock and stops sweeping, check the Carrier and FEC Synchronization Status register (Group 3, APR 11) for the status. All flags should be set to 1 when the carrier and clock are locked.

6. If all of the flags in the Carrier and FEC Synchronization Status register are set to 1, clear the CAR_SW bit in the Carrier Loop Configuration register to 0b0. The sweep turns off.

B.2 Demodulator Configuration Tips

The following tips help in configuring the demodulator registers. Refer to the *L64724 Satellite Receiver Evaluation Board User's Guide.* The acquisition process is controlled by the L64724 microcontroller.

For the equations given in the following subsections, the relationship shown in Equation B.2 holds.

Equation B.2

$$B_L = \frac{\zeta\omega_n}{2}\left(1 + \frac{1}{4\zeta^2}\right)$$

B_L is the loop bandwidth, ω_n is the natural frequency, and ζ is the damping factor.

B.2.1 CAR_BW (Carrier Loop Bandwidth)

Set the carrier loop bandwidth according to Equation B.3.

Equation B.3 CAR_BW

carrier_bw (KHz) = Rs(MSps)

B.2.2 CAR_SWR (Carrier Sweep Rate)

To provide reliable acquisition at any signal-to-noise ratio, the microcontroller uses two sweep rates. The fast rate pulls the loop out of false locks. The parameters in the above table might have to be adjusted at very low rates (< 2 MSps) for optimal performance, depending on the tuner.

The sweep rate equations are shown in Equation B.4.

Equation B.4

slow_sweep_rate[MHz/s] = N x Rs[MS/s]
fast_sweep_rate[MHz/s] = M x Rs[MS/s]

Rs is the symbol rate and M and N are as shown in the following table.

Rs (MS/s)[1]	M	N
45 to 15	32	8
15 to 7.5	8	2
7.5 to 3.75	8	1
3.75 to 2	8	1
2 to 1	4	1

1. Megasamples per second.

B.2.3 SYM_BW (Timing Loop Bandwidth)

Equation B.5 describes the timing loop bandwidth.

Equation B.5

symbol_bw (KHz) = Rs(MS/s) /10

B.2.4 SYM_SWR (Timing Loop Sweep Rate)

Equation B.6 describes the timing loop sweep rate.

Equation B.6

symbol_sweep_rate (KHz/s) = 0.1 * slow_sweep_rate (MHz/s)

B.2.5 Decimation Control

The decimation and the sampling rate are configured to provide the highest possible number of samples per symbol with the tightest decimation filter available. The procedure is outlined in Table B.2 and the results are shown in Table B.3.

Table B.2 Decimation Procedure

Rs Threshold (MS/s)[1]	DF_RATIO	DF_SELECT	DF_GAIN	Group 4, Register 19 Setting		Fs (MHz)
				Binary	Hex	
45 to 44.5	1	0	1	10000100	0x84	91.5 (N = 1, S = 61, T = 10, M = 3
44.5 to 30	1	0	1	10000100	0x84	See footnote[2]
30 to 15	1	1	1	00000100	0x04	See footnote
15 to 7.5	2	2	2	00101000	0x28	See footnote
7.5 to 3.75	4	3	4	01010001	0x51	See footnote
3.75 to 1	8	4	8	01111010	0x7A	See footnote

1. Megasamples per second (MS/s)
2. For Rs <= 44.5 MSps, calculate the sampling rate as follows: from the set of valid sampling frequency values, (30, 35, 40 ..., 85, 90), select the lower, closest value to 4 * DF_RATIO * Rs/(1 + alpha), where alpha is the “corner” margin (1%).

Table B.3 Decimation Results

Rs (MS/s)[1]	Sampling Frequency (MHz)	DF_RATIO	Samples per Symbol	DF_FILTER	DF_GAIN
45	91.5	1	2.033	0	1
44.5	90	1	2.022	0	1
44	90	1	2.045	0	1
43	90	1	2.093	0	1
42	90	1	2.143	0	1
41	90	1	2.195	0	1

(Sheet 1 of 3)

Table B.3 Decimation Results (Cont.)

Rs (MS/s)[1]	Sampling Frequency (MHz)	DF_RATIO	Samples per Symbol	DF_FILTER	DF_GAIN
40	90	1	2.250	0	1
39	90	1	2.308	0	1
38	90	1	2.368	0	1
37	90	1	2.432	0	1
36	90	1	2.500	0	1
35	90	1	2.571	0	1
34	90	1	2.647	0	1
33	90	1	2.727	0	1
32	90	1	2.813	0	1
31	90	1	2.903	0	1
30	90	1	3 000	1	1
29	90	1	3.103	1	1
28	90	1	3.214	1	1
27	90	1	3.333	1	1
26	90	1	3.462	1	1
25	90	1	3.600	1	1
24	90	1	3.750	1	1
23	90	1	3.913	1	1
22.7250	85	1	3.740	1	1
21.4625	80	1	3.727	1	1
20.2000	75	1	3.713	1	1
18.9375	70	1	3.696	1	1
17.6750	65	1	3.678	1	1
16.4125	60	1	3.656	1	1
15.1500	55	1	3.630	1	1
15	90	2	6.000	2	2
14	90	2	6.429	2	2
13	90	2	6.923	2	2
12	90	2	7.500	2	2
11.3625	85	2	7.481	2	2
10.7313	80	2	7.455	2	2
10.1000	75	2	7.426	2	2

(Sheet 2 of 3)

Table B.3 Decimation Results (Cont.)

Rs (MS/s)[1]	Sampling Frequency (MHz)	DF_RATIO	Samples per Symbol	DF_FILTER	DF_GAIN
9.4688	70	2	7.393	2	2
8.8375	65	2	7.355	2	2
8.2063	60	2	7.312	2	2
7.5750	55	2	7.261	2	2
7.5	90	4	12.000	3	4
7	90	4	12.857	3	4
6	90	4	15.000	3	4
5.6813	85	4	14.961	3	4
5.3656	80	4	14.910	3	4
5.0500	75	4	14.851	3	4
4.7344	70	4	14.785	3	4
4.4188	65	4	14.710	3	4
4.1031	60	4	14.623	3	4
3.7875	55	4	14.521	3	4
3.75	90	8	24.000	4	8
3	90	8	30.000	4	8
2.8406	85	8	29.923	4	8
2.6828	80	8	29.819	4	8
2.5250	75	8	29.703	4	8
2.3672	70	8	29.571	4	8
2.2094	65	8	29.420	4	8
2.0516	60	8	29.246	4	8
1.8938	55	8	29.043	4	8
1.7359	50	8	28.803	4	8
1.5781	45	8	28.515	4	8
1.4203	40	8	28.163	4	8
1.2625	35	8	27.723	4	8
1.1047	30	8	27.157	4	8
1	30	8	30.000	4	8

(Sheet 3 of 3)

1. Megasamples per second

B.3 QPSK Demodulator and FEC Configuration Example: High Data Rates

This section gives an example of how to use the microcontroller interface of the L64724 to configure the QPSK Demodulator and FEC section for high data rates. No decimation or decimation filtering is performed. The configuration in the example is optimized for fixed rate operation with the following parameters:

Parameter	Value
Transmission Rate	42.6 Mbit/s (21.3 Mbaud)
ADC Sampling Frequency	50 MHz
Xtal OSC	15.00 MHz
ADC	Input: 1.0 V p-to-p
DC offset control	Used after A/D, not after Nyquist filter.
Viterbi Rate	1/2
E_b/N_o	4.0 dB
Model	DVB

The registers for this example are configured as shown in the following subsections. See Table B.8, on page B-26, for a summary of the register settings.

Group 4, APR 0 – Set to 0x81.

Set bit D7 to 1 and clear bit D6 to 0. Based on Section 4.2, set the PLL_N[5:0] bits (D5 to D0) to 0x01.

Group 4, APR 1 – Set to 0x14.

Clear bits D7 and D6 to 0. Based on section 4.2, set PLL_S[5:0] (D5 to D0) to 0x14.

Group 4, APR 2 – Set to 0x06.

Set the IMQ bit (D7) to either 0 or 1, clear the DVB_DSS bit (D6) and the QB bit (D5) to 0. Based on Table 4.2, set PLL_T[4:0] (D4 to D0) to 0x06.

Group 4, APR 3 – Set to 0x18.

Clear the Viterbi Code Rate[2:0] bits (D7 to D5) to 0 for rate 1/2, set the TEI bit (D4) to 1, set the SYNC2_MOD bit (D3) to 1, clear bit D2 to 0, and based on Section 4.3, clear the PLL_M[1:0] bits (D1 to D0) to 0.

Group 4, APR 4 – Set to 0x40.

Since the Viterbi code rate is 1/2, based on the graph shown in Figure 6.4, for a E_b/N_o = 4.0 (E_s/sigma^2 = 7.0), a choice of 0.24 for VMBEC/VMDC1 establishes a valid decision threshold over the entire SNR range. Equation B.7 shows the relationship between VMBEC and VMDC1.

Equation B.7

$$0.24 = \frac{128\,VMBEC + 32}{256\,VMDC1}$$

Choosing VMDC1[7:0] = 64 (0x40) yields a value of 30 (0x1E) for VMBEC[7:0].

Group 4, APR 5–7 – Set to 0x0F0000.

The VMDC2[23:0] bits select a second window. The VMDC2[23:0] value controls the window size over which Viterbi errors are counted. The VMDC2[23:0] value is used for calculating the BER, not for the auto-synchronization that is controlled by the VMDC1[7:0] bits. In this example, choose a window size of 3.932 x 10^6 bits = VMDC2[23:0] x 4, which is approximately equal to 0x0F0000

Set Group 4, APR 5 to 0x00, set Group 4, APR 6 to 0x00, and set Group 4, APR 7 to 0x0F.

Group 4, APR 8 – Set to 0x1E.

Equation B.7 yields a value for VMBEC[7:0] of 30 (0x1E.)

Group 4, APR 9, 10, 11, 12, 13 – Set all these registers to 0x00.

Group 4, APR 14 – Set to 0x47.

The DVB Synchronization Word[7:0] value is 0x47.

Group 4, APR 15 – Set to 0x00.

Clear D7 to 0. Clear the Auto Rate bit (D6) to 0 to obtain a code rate from the Viterbi Code Rate. Clear the D5 and D4 bits to 0. Clear the IMQ_EN bit (D3) to 0 for IMQ to be determined by APR 2 bit 7. Clear the DI_Bypass bit (D2) to 0 to enable the deinterleaver, and clear the L[1:0] bits (D1and D0) to 0 to select zero mismatching bits.

Group 4, APR 16 – Set to 0x00.

Clear the D7 and D6 bits to 0. Clear the SSS[1:0] bits (D5 and D4) to 0 to observe Viterbi decoder sync. Clear the SSA[1:0] bits (D3 and D2) to 0 to set the number of sync words to acquire to three. Clear the SST[1:0] bits (D1 and D0) to 0 to set the number of missed sync words until loss of lock is equal to two.

Group 4, APR 17 – Set to 0x00.

Clear D7 and D6 to 0. Clear the OF bit (D5) to 0 for serial mode and clear the OS[4:0] bits (D4 to D0) to 0 to observe the descrambler output.

Group 4, APR 18 – Set to 0x00.

Write any value to this register to reset the PLL module.

Group 4, APR 19 – Set to 0x84.

Select the register bits according to the following table.

Bits	Setting	Parameter	Meaning
D7 to D5	0b100	DF_SELECT [2:0]	No Decimation filter selected.
D4 to D3	0b00	DF_GAIN[1:0]	DF Gain = 1 (No decimation filter used).
D2 to D0	0b100	DF_RATIO[2:0]	No decimation implemented.

A DF gain of one is chosen because no decimation filter was used.

Group 4, APR 20 – Set to 0x01.

Clear bits D7 through D5 to 0. Clear the PD bit (D4) to 0 for normal operation. Clear bits D3 to D1 to 0. Set the MF_20_35 bit (D0) to 1 for a matched filter roll-off factor of 0.35.

Group 4, APR 21 – Set to 0x00.

Clear the PCLK_INV bit (D7) to 0 for a non-inverted PCLK output. Clear the PLL_BP bit (D6) to 0 to enable the internal PLL to generate the A/D clock. Clear the LCLK_OFF bit (D5) to 0 to turn off the LCLK signal. Clear the CLK_DIV1[4:0] bits (D4 to D0) to 0 because the internal PLL is used.

Group 4, APR 22 – Set to 0x00.

Set APR register 22 to 0x00, because the CLK_DIV2[7:0] bits are unused when the internal PLL has been selected.

Group 4, APR 23 – Set to 0xC0.

Set the DC_Offset_On_Off[1] bit (D7) to 1 to cause the DC offset compensation after the ADC to be activated. Set the DC_Offset_On_Off[0] bit (D6) to 1 to cause the noise feedback to the compensation circuit to be selected. Clear the D5 bit to 0. Clear the CLK_DIV2[12:8] bits (D4 to D0) to 0, because the CLK_DIV2[12:8] bits are unused when the internal PLL has been selected.

Group 4, APR 24 – Set to 0x54.

Set the PWR_REF[7:0] bits to 0x54. See Section 5.8.1, “ADC Range and Power Reference,” page 5-20, for more details.

Group 4, APR 25 – Set to 0x00.

Clear the D7 to D3 bits to 0. Clear the INT_DC bit (D2) to 0 to disable internal DC offset compensation after the matched filter and clear the PWR_BW[1:0] bits (D1 and D0) PWR_BW to 0 (see Section 5.8.2, “Power Control Loop,” page 5-21.)

Group 4, APR 26 – Set to 0xBA.

Use Equation B.8 to calculate the value of SCALE[7:0].

Equation B.8

$$SCALE = \frac{2047 \cdot \sqrt{1 + \left(\frac{E_s}{N_o}\right)^{-1}}}{\sqrt{2 \cdot PWR\_REF}}$$

$$SCALE = \frac{2047 \cdot \sqrt{1 + (2.51)^{-1}}}{\sqrt{2 \cdot 84}} = 186 \text{ (0xBA)}$$

Group 4, APR 27 – Set to 0x64.

This register is set to a signal-to-noise threshold value dependent on the value of the PWR_REF[7:0] value. The SNR_THS[7:0] bits contain a threshold value that indicates a good or bad signal-to-noise ratio. Set the SNR_THS[7:0] value to 100 (0x64.)

Group 4, APR 28 – Set to 0xAA.

This register defines the loop bandwidths for a particular baud rate (in the equations that follow, the symbol T represents the baud period). A good approximation to the equivalent noise bandwidth is given in Equation B.9 (for high data rates). The damping factor (ζ) is chosen as 1.0. K_{dcar} = $K_{digital}$ x 0.78/32.0. $K_{digital}$ is chosen from Table 5.4, on page 5-19. For a SNR of 4dB, $K_{digital}$ = 10, with the result that K_{dcar} = 0.24. Using these values, we get L_{car} = Fs/Fb = 50e6/21.3e6 = 2.34.

Equation B.9

$$B_L = 0.003125 \times BaudRate$$

$$B_L = \frac{\zeta\omega_n}{2}\left(1 + \frac{1}{4\zeta^2}\right)$$

For a baud rate of 21.3 Mbaud we can choose B_L = 66 Krad/s and therefore ω_n = 106 Krad/s.

The loop equations are calculated as shown in Equation B.10 and Equation B.11.

Equation B.10

$$\tau_a = \frac{\omega_n^2 T^2}{K_{dcar} L_{car}} \times 2\pi$$

Equation B.11

$$\tau_b = \frac{2\zeta\omega_n T}{K_{dcar} L_{car}} \times 2\pi$$

The values of τ_a and τ_b are used to calculate CAR_MU_SEL[3:0] and CAR_LAMBDA_SEL[3:0] registers in Group 4.

We can now calculate τ_a and τ_b as shown in Equation B.12 and Equation B.13.

Equation B.12

$$\tau_a = \frac{(106 \times 10^3)^2\left(\frac{1}{21.3 \times 10^6}\right)^2}{0.24 \times 2.34} = 44 \times 10^{-6}$$

Equation B.13

$$\tau_b = \frac{2 \times 106 \times 10^3 \times \frac{1}{21.3 \times 10^6}}{0.24 \times 2.34} = 17.7 \times 10^{-3}$$

CAR_MU_SEL[3:0] and CAR_LAMBDA_SEL[3:0] are defined in Equation B.14 and Equation B.15.

Equation B.14

$$CAR\_MU\_SEL = log_2(t_a \times 2^{25}) = log_2(44e\text{-}6 \times 2^{25}) = 10 = 0xA$$

Equation B.15

$$CAR\_LAMBDA\_SEL = log_2(t_b \times 2^{16}) = log_2\{17.7\text{-}6 \times 2^{16}\} = 10 = 0xA$$

Program the four LSBs of APR 28 with 0xA and the four MSBs of APR 28 with 0xA.

Group 4, APR 29 – Set to 0x1F.

The recommended value for CAR_LC_THSL[7:0] is 31 (0x1F) when FP_LOCK_LEN (Group 4, APR 54) is set to 0. Otherwise, set it according to the following table:

FP_LOCK_LEN	CAR_LC_THSL[7:0]	
0	31	Low E_b/N_o
1	72	High E_b/N_o

Group 4, APR 30 – Set to 0x00.

Group 4, APR 31 – Set to 0x20.

Set the RS Bit/Byte Select bit (D7) as needed to select the Reed-Solomon bit or byte error count for Group 3 APR 0 and 1. Set the Errorout_Invert bit (D6) as needed to control the polarity of the ERROROUTn signal. Set the SPI_On_Off bit (D5) to 1. Clear bits D4 through D0 to 0.

Group 4, APR 32–33 – Set to 0x6AE.

The value for the sweep rate, CAR_SWR[15:0], is set according to Equation B.16, Equation B.17 and Equation B.18.

Equation B.16

$$fast\_sweeprate = 32 * 21.6\ (MS/s) = 691.2\ (MS/s)$$

Equation B.17

$$CAR\_SWR = \frac{2^{37} \times fast\_sweeprate \times T}{Fs \times 16} \times 2$$

Equation B.18

$$CAR\_SWR = \frac{2^{37} \times 691.2 \times 10^{6} \times \frac{1}{21.3 \times 10^{6}}}{50.0 \times 10^{6} \times 16} \times 2 = 11,150 \quad (2B8E)$$

Set Group 4, APR 33 to 0x2B and APR 32 to 0x8E.

Group 4, APR 34–35 – Set to 0x3334.

The value for the upper sweep limit, CAR_USWL[15:0], is set as explained in the following paragraphs. It should be noted that the upper sweep limit is an approximate value but the approximation to the real sweep limit is accurate enough. Assume that the upper sweep limit needed is + 5 MHz. The maximum sweep limit achievable is ± 0.5 x Fs. Calculate CAR_USWL[15:0] as shown in Equation B.19 and Equation B.20.

Equation B.19

$$CAR\_USWL = \frac{2^{37} \times sweeplimit}{Fs \times 2^{21}}$$

Equation B.20

$$CAR\_USWL = \frac{2^{37} \times 5 \times 10^{6}}{50.0 \times 10^{6} \times 2^{21}} = 6554_{(0x199A)}$$

Set Group 4 APR 35 to 0x19 and APR 34 to 0x9A.

Group 4, APR 36–37 – Set to 0xCCCC.

The value for the lower sweep limit, CAR_LSWL[15:0], is set as explained in the following paragraphs. It should be noted that the lower sweep limit is an approximate value but the approximation to the real sweep limit is accurate enough. Assume that the lower sweep limit needed is – 5 MHz. Calculate CAR_LSWL[15:0] as shown in Equation B.21 and Equation B.22.

Equation B.21

$$CAR\_LSWL = \frac{2^{37} \times sweeplimit}{Fs \times 2^{21}}$$

Equation B.22

$$\text{CAR\_LSWL} = \frac{2^{37} \times -5 \times 10^{6}}{50.0 \times 10^{6} \times 2^{21}} = -6554 \quad (0xE666)$$

Set Group 4, APR 37 to 0xE6 and APR 36 to 0x66.

Group 4, APR 38–40 – Set to 0x51EB8.

The value for CAR_LF_INIT[23:0] is in accordance with Equation B.23.

Equation B.23

$$\text{CAR\_LF\_INIT} = \frac{2^{37} \times freqdeviation}{2^{13} \times Fs}$$

Assuming an initial carrier frequency deviation of + .1 MHz is required, the value for CAR_LF_INIT[23:0] is given in Equation B.24.

Equation B.24

$$\text{CAR\_LF\_INIT} = \frac{2^{37} \times 1 \times 10^{6}}{2^{13} \times 50 \times 10^{6}} = 335554 \quad (0x51EB8)$$

Set Group 4, APR 40 to 0x05, APR 39 to 0x1E, and APR 38 to 0xB8.

Group 4, APR 41 – Set to 0x65.

Set the bits in the Carrier Loop Control 1 register as shown in Table B.4.

Table B.4 Carrier Loop Control 1 Register Bits

Bits	Setting	Acronym	Meaning
D7	0	CAR_SWP_SWAP	Not significant when auto sweep is on
D6	1	CAR_ERROR_SWAP	Carrier phase error detector output inverted
D5	1	CAR_AUTO_SWP	Carrier auto sweep on
D4	0	Reserved	–
D3	0	Reserved	–
D2	1	CAR_PED_SEL	Choose NDAML phase error detector
D1	0	CAR_OPEN	Carrier loop operates normally
D0	1	CAR_SW	Carrier sweep on

If the carrier is locked but the constellation is rotated by 45 degrees, reverse the polarity of bit 6 (CAR_ERROR_SWAP).

Group 4, APR 42 – Set to 0xAA.

This register defines the loop bandwidths for a particular baud rate. A good approximation to the equivalent noise bandwidth is given in Equation B.25.

Equation B.25

$$B_L = 0.0003125 \times BaudRate$$

$$B_L = \frac{\zeta \omega_n}{2}\left(1 + \frac{1}{4\zeta^2}\right)$$

For a baud rate of 21.3 Mbaud we can choose B_L = 6.6 Krad/s and therefore ω_n = 10.6 Krad/s.

The loop equations are calculated as shown in Equation B.26 and Equation B.27.

Equation B.26

$$\tau_a = \frac{\omega_n^2 T^2}{K_{tim} L_{tim}} \times 2\pi$$

Equation B.27

$$\tau_b = \frac{2\zeta\omega_n T}{K_{tim} L_{tim}} \times 2\pi$$

The damping factor (ζ) is chosen as 1.0, and K_{tim} = 0.0388. Using these values we get L_{tim} = Fs x decimation_ratio/Fb = 50e6 x 1/21.3e6 = 2.34. We can now calculate τ_a and τ_b as shown in Equation B.28 and Equation B.29.

Equation B.28

$$\tau_a = \frac{(10.6 \times 10^3)^2 \left(\frac{1}{21.3 \times 10^6}\right)^2}{0.0388 \times 2.34} = 3 \times 10^{-6}$$

Equation B.29

$$\tau_b = \frac{2 \times 10.6 \times 10^3 \times \frac{1}{21.3 \times 10^6}}{0.0388 \times 2.34} = 11 \times 10^{-3}$$

CLK_MU_SEL[3:0] and CLK_LAMBDA_SEL[3:0] are defined in Equation B.31 and Equation B.32.

Equation B.30

$$CAR\_MU\_SEL = log_2((\tau_a \times 2^{28}) = log_2(3e\text{-}6 \times 2^{28}) = 10 = 0xA$$

Equation B.31

$$CAR\_LAMBDA\_SEL = log_2(\tau_b \times 2^{16}) = log_2\{11e\text{-}3 \times 2^{16}\} = 10 = 0xA$$

Program the four LSBs of APR 42 with 0xA and the four MSBs of APR 42 with 0xA.

Note: Group 4, APR 43–48, contain sweep parameters that need to be programmed only if clock sweep is required. These parameters have meaning only when the CLK_SW bit (bit D0 of Group 4, APR 53) is set to a 1.

Group 4, APR 43–44 – Set to 0x0FA0.

The value for the clock sweep rate, CLK_SWR[15:0], is set according to Equation B.32, assuming a clock sweep rate of 1 MHz/s.

Equation B.32

$$\text{CLK\_SWR} = \frac{2^{45} \times sweeprate \times T}{Fs \times \frac{1}{\text{DF\_Ratio}} \times 16} \times 2$$

$$\text{CLK\_SWR} = \frac{2^{45} \times 1 \times 10^{6} \times \frac{1}{21.3 \times 10^{6}} \times 2}{50.0 \times 10^{6} \times 1 \times 16} = 4000 \ (0\text{xFA0})$$

Set Group 4 APR 44 to 0x0F and APR 43 to 0xA0.

Group 4, APR 45–46 – Set to 0x0600.

The value for the upper sweep limit, CLK_USWL[15:0], is set as explained in the following paragraphs. It should be noted that the upper sweep limit is an approximate value but the approximation to the real sweep limit is accurate enough. Assume that the upper sweep limit needed is +10 kHz. CLK_USWL[15:0] is calculated as shown in Equation B.33.

Equation B.33

$$\text{CLK\_USWL} = \frac{2^{45} \times sweeplimit}{Fs \times \frac{1}{\text{DF\_RATIO}} \times 2^{22}} \times 2$$

$$\text{CLK\_USWL} = \frac{2^{45} \times 10 \times 10^{3}}{50.0 \times 10^{6} \times 1 \times 2^{22}} = 1536 \ (0\text{x}0600)$$

Set Group 4, APR 46 to 0x06 and APR 45 to 0x00.

Group 4, APR 47–48 – Set to 0xFA00.

The value for the lower clock sweep limit, CLK_LSWL[15:0], is set as explained in the following paragraphs. It should be noted that the lower sweep limit is an approximate value, but the approximation to the real sweep limit is accurate enough. Assume that the lower sweep limit needed is –10 kHz. The CLK_LSWL[15:0] value is calculated as shown in Equation B.34.

Equation B.34

$$\text{CLK\_LSWL} = \frac{2^{45} \times -10 \times 10^{3}}{50.0 \times 10^{6} \times 1 \times 2^{22}} \times 2 = -1536 \ (0\text{xFA00})$$

Set Group 4, APR 48 to 0xFA and APR 47 to 0x00.

Group 4, APR 49–52 – Set to 0x12C78301.

Choose CLK_BIAS[30:0] according to Equation B.35.

Equation B.35

$$\text{CLK\_BIAS} = \frac{Fs \times \frac{1}{\text{DF\_RATIO}} \times 2^{28}}{2 \times Fb}$$

$$\text{CLK\_BIAS} = \frac{50.0 \times 10^{6} \times 1 \times 2^{28}}{2 \times 21.3 \times 10^{6}} = 315065089 \quad (0x12C7.8301)$$

Fs = sampling frequency at the A/D and Fb is the baud rate.

Set Group 4, APR 52 to 0x12, APR 51 to 0xC7, APR 50 to 83, and APR 49 to 01.

Group 4, APR 53 – Set to 0x38.

Set the bits in the Clock Loop Configuration register (APR 53) as shown in Table B.5.

Table B.5 Clock Loop Configuration Register Bits

Bits	Setting	Acronym	Meaning
D7	0	CLK_SWP_SWAP	Not significant when auto sweep is on or when sweep is off
D6	0	CLK_ERROR_SWAP	Timing error detector output not inverted
D5	1	CLK_AUTO_SWP	Automatic internal sweep control
D4	1	Reserved	Ser this bit to 1
D3	1	AGC_CLK_SEL	Integrate over all samples
D2	0	Reserved	Clear this bit to 0
D1	0	CLK_OPEN	Enable the clock loop
D0	0	CLK_SW	Clock sweep off

Group 4, APR 54 – Set to 0x00.

Set the bits in the Demodulator Configuration register (APR 54) as shown in Table B.6.

Table B.6 Demodulator Configuration Register Bits

Bits	Setting	Acronym	Meaning
D7	0	SNR_EST	Enable SNR estimator
D6	0	PWRP_TRI	PWRP not 3-stated
D5	0	ADC_PD	A/D normal operation
D4	0	FP_LOCK_LEN	Normal (long) window for phase lock
D3	0	PWRP	PWRP pin in normal mode
D2 to D1	0b00	Reserved	Clear these bits to 0 for normal mode
D0	0	CLK_ALPHA_SEL	Alpha value = 0.43

Group 4, APR 55 – Set to 0x00.

Set the bits in the External Output Control Bits and Reset register (APR 55) as shown in Table B.7.

Table B.7 External Output Control Bits and Reset Register Bits

Bits	Setting	Acronym	Meaning
D7	0	ADC_BP	Enable ADCs
D6	0	OB_2C	Input is offset-binary format
D5 to D2	0b0000	XCTR[3:0]	Corresponding output pin = VSS
D1	0	DEMOD_RST	No reset for demodulator
D0	0	FEC_RST	No reset for FEC

Group 4, APR 56–57 - Set to 0x00.

Group 4, APR 58 – Set to 0x14.

Group 4, APR 59–61 – These registers are used to communicate on a serial bus to the tuner using the XCTR[3:0] output pins. Refer to Appendix C for details on programming the SPI interface.

Group 4, APR 62 – Set to user preference.

Set the bits in the Group 4, APR 62 register as shown in the following table.

Bits	Setting	Acronym	Meaning
D7	–	Serial_B	See Appendix C, Programming the Serializer, for more details.
D6 to D5	–	Serial_C[1:0]	See Appendix C, Programming the Serializer, for more details.
D4 to D1	0b0100	SPI_M[3:0]	Denominator of Viterbi Code Rate = 4 (rate = 3/4)
D0	–	Serial_A	See Appendix C, Programming the Serializer, for more details.

Group 4, APR 63 – Set to 0x63.

Clear the FMODE bit (D7) to 0. Set the SPI_CLK_AND bit (D6) to 1 to AND the SPI byte clock and the DVALIDOUT signal. Clear the SPI_MODE_A_B bit to 0 for Mode A. Set the SPI_N[3:0] bits to 0x03 because the Viterbi Code Rate is 3/4.

Group 4, APR 64–65 – Set to 0x3200.

Set the SPI_GAIN[9:0] to 50 (0x32) because the oversampling ratio (OR) is between 2 and 4.

OR	SPI Gain
2 to 4	50.0
4 to 8	35.0
8 to 16	15.0
Greater than 16	less than 10

Group 4, APR 66–68 – Set to 0x51CAC0.

Set the SPI_Bias[22:0] value as shown in Equation B.36.

Equation B.36

$$SPIBias = \frac{2^{24} \cdot VCR}{OR}$$

In the equation, VCR = 3/4 and OR = 50e6/21.3e6. The result is that SPIBias = 5,360,320 (0x51.CAC0.)

Set Group 4, APR 68 to 0x51, APR 67 to 0xCA, and APR 66 to 0xC0.

Group 4, APR 69 – Set to 0x4B.

Set the timing lock threshold (CLK_LC_THSL[7:0]) value at 75 (0x4B.)

Table B.8 gives the register values calculated for high data rates.

Table B.8 High Data Rate Register Values

APR [5:0]	D7	D6	D5	D4	D3	D2	D1	DO	HEX
0	Set to 1	Re-served	PLL_N[5:0]						81
1	Reserved		PLL_S[5:0]						14
2	IMQ	DVB_ DSS	QB	PLL_T[4:0]					6
3	Viterbi Code Rate[2:0]			TEI	SYNC2 _ MOD	Sync1 Over-ride	PLL_M[1:0]		18
4	Viterbi Max Data Bit Count, VMDC1[7:0]								40
5	Viterbi Max Data Bit Count 2, VMDC2[7:0], low byte								00
6	Viterbi Max Data Bit Count 2, VMDC2[15:8], middle byte								00
7	Viterbi Max Data Bit Count 2, VMDC2[23:16], high byte								0F
8	Viterbi Maximum Bit Error Count[7:0], Rate 1/2								1E
9	Viterbi Maximum Bit Error Count[7:0], Rate 2/3								00
10	Viterbi Maximum Bit Error Count[7:0], Rate 3/4								00
11	Viterbi Maximum Bit Error Count[7:0], Rate 5/6								00
12	Viterbi Maximum Bit Error Count[7:0], Rate 6/7								00
13	Viterbi Maximum Bit Error Count[7:0], Rate 7/8								00
14	Synchronization Word[7:0]								47
15	BER	Auto Rate	Reserved		IMQ_ EN	DI_ Bypass	L[1:0]		00
16	Reserved		Sync Status Select, SSS[1:0]		Sync States Acq, SSA [1:0]		Sync States Track, SST[1:0]		00
17	Reserved		OF	Output Selector, OS[4:0]					00
18	PLL_RESET								00

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Table B.8 High Data Rate Register Values (Cont.)

APR [5:0]	D7	D6	D5	D4	D3	D2	D1	DO	HEX
19	DF_Select[2:0]			DF_Gain[1:0]		DF_Ratio[2:0]			84
20	Reserved			PD	Reserved			MF_20_35	01
21	PCLK_INV	PLL_BP	LCLK_OFF	CLK_DIV1[4:0]					00
22	CLK_DIV2[7:0]								00
23	DC_Offset_On_Off [1:0]		Re-served	CLK_DIV2[12:8]					C0
24	PWR_REF[7:0]								54
25	Reserved					INT_DC	PWR_BW[1:0]		00
26	Scale factor for DEMI, DEMQ, SCALE[7:0]								BA
27	SNR Estimator Threshold, SNR_THS[7:0]								64
28	Carrier Loop Lambda, CAR_LAMBDA_SEL[3:0]				Carrier Loop Mu, CAR_MU_SEL[3:0]				AA
29	Carrier Phase Lock Detector Threshold, CAR_LC_THSL[7:0]								1F
30	Reserved								00
31	RS Bit/Byte Select	Errorout_ Invert	SPI_On_ Off	Reserved = 0					20
32	Carrier Sweep Rate, CAR_SWR[7:0]								8E
33	Carrier Sweep Rate, CAR_SWR[15:8]								2B
34	Carrier Upper Sweep Limit, CAR_USWL[7:0]								9A
35	Carrier Upper Sweep Limit, CAR_USWL[15:8]								19
36	Carrier Lower Sweep Limit, CAR_LSWL[7:0]								66
37	Carrier Lower Sweep Limit, CAR_LSWL[15:8]								E6
38	Carrier Loop Filter Initialization, CAR_LF_INIT[7:0]								B8
39	Carrier Loop Filter Initialization, CAR_LF_INIT[15:8]								1E

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Table B.8 High Data Rate Register Values (Cont.)

APR [5:0]	D7	D6	D5	D4	D3	D2	D1	DO	HEX
40	Carrier Loop Filter Initialization, CAR_LF_INIT[23:16]								05
41	CAR_ SWP_ SWAP	CAR_ ERROR_ SWAP	CAR_ AUTO_ SWP	Reserved		CAR_ PED_ SEL	CAR_ OPEN	CAR_ SW	65
42	Clock Loop Lambda, CLK_LAMBDA_SEL[3:0]				Clock Loop Mu, CLK_MU_SEL[3:0]				AA
43	Clock Sweep Rate, CLK_SWR[7:0]								A0
44	Clock Sweep Rate, CLK_SWR[15:8]								0F
45	Clock Upper Sweep Limit, CLK_USWL[7:0]								00
46	Clock Upper Sweep Limit, CLK_USWL[15:8]								06
47	Clock Lower Sweep Limit, CLK_LSWL[7:0]								00
48	Clock Lower Sweep Limit, CLK_LSWL[15:8]								FA
49	Clock Loop Bias, CLK_BIAS[7:0]]								01
50	Clock Loop Bias, CLK_BIAS[15:8]								83
51	Clock Loop Bias, CLK_BIAS[23:16]								C7
52	Reserved	Clock Loop Bias, CLK_BIAS[30:24]							12
53	CLK_ SWP_ SWAP	CLK_ ERROR_ SWAP	CLK_ AUTO_ SWP	Re- served	AGC_ CLK_ SEL	Re- served	CLK_ OPEN	CLK_ SW	38
54	SNR_EST	PWRP_ TRI	ADC_PD	FP_ LOCK_ LEN	PWRP	Reserved		CLK_ ALPHA_ SEL	00
55	ADC_BPS	OB_2C	External Control Output Bits, XCTR[3:0]				DEMOD _RST	FEC_ RST	00
56	Reserved								00
57	Reserved								00
58	Reserved								14

Table B.8 High Data Rate Register Values (Cont.)

APR [5:0]	D7	D6	D5	D4	D3	D2	D1	DO	HEX
59	Serial Transmission Start Data, TXSD[6:0]							Re-served	10
60	Serial Transmission Data, STXD[7:0]								00
61	Serial Transmission End Data, TXED[7:0]								00
62	Serial_B	Serial_C[1:0]		SPI_M[3:0]				Serial_A	—
63	FMODE	SPI_CLK _AND	SPI_ Mode_A _B	Re-served	SPI_N[3:0]				63
64	SPI_Gain[7:0](LSB)								32
65	Reserved						SPI_Gain[9:8]		00
66	SPI_Bias[7:0](LSB)								C0
67	SPI_Bias[15:8](MSB)								CA
68	Reserved	SPI_Bias[22:16]							51
69	Timing Lock Threshold, CLK_LC_THSL[7:0]								4B

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B.4 QPSK Demodulator and FEC Configuration Example: Low Data Rates

This section contains an example of how to configure the QPSK Demodulator section of the L64724 through its microcontroller interface. This example configuration is optimized for fixed rate operation with the following parameters:

Transmission Rate:	4.0 Mbit/s (2.0 Mbaud)
ADC Sampling Frequency	60 MHz
Xtal OSC	15.00 MHz
ADC	Input: 1.0 V p-to-p
DC Offset Control	Used
Viterbi Rate	1/2
E_b/N_o	4.0 dB
Model	DVB

The registers for this example are configured as shown in the following subsections. See Table B.14, on page B-45, for a summary of the register settings.

Group 4, APR 0 – Set to 0x81.

Set bit D7 to 1 and clear bit D6 to 0. Based on Section 4.2, set the PLL_N[5:0] field to 0x01 (PCLK = 60 MHz.)

Group 4, APR 1 – Set to 0x04.

Clear bits D7 and D6 to 0. Based on section 4.2, set the PLL_S[5:0] bits to 0x04 (PCLK = 60 MHz.)

Group 4, APR 2 – Set to 0x01.

Set the IMQ bit (D7) to either 1 or 0, clear the DVB_DSS bit (D6) bit to 0 for DVB, and clear the QB bit (D5) to 0 for QPSK. Based on Table 4.2, set the PLL_T[4:0] bits to 0x01.

Group 4, APR 3 – Set to 0x09.

Clear the VCR[2:0] bits (D7 to D5) to 0x00 for rate 1/2, the TEI bit (D4) to 0 or 1, set the SYNC2_MOD bit (D3) to 1, clear bit D2 to 0, and based on Section 4.2, set the PLL_M[1:0] bits to 0x01.

Group 4, APR 4 – Set to 0x40.

Since the Viterbi code rate is 1/2, based on the graph shown in Figure 6.4 for an E_b/N_o = 4.0 (E_s/sigma^2 = 7.0,) a choice of 0.24 for VMBEC/VMDC1 establishes a valid decision threshold over the entire SNR range. Equation B.37 shows the relationship between VMBEC and VMDC1.

Equation B.37

$$0.24 = \frac{128\,VMBEC + 32}{256\,VMDC1}$$

Choosing VMDC1[7:0] = 64 (0x40) yields a value of 30 (0x1E) for VMBEC[7:0].

Group 4, APR 5–7 – Set to 0x0F0000.

The VMDC2[23:0] bits select a second window. The VMDC2[23:0] bits control the window size over which Viterbi errors are counted and are used for calculating the BER, not for the auto-synchronization that is controlled by VMDC1. In this example, choose a window size of 3.932×10^6 bits = VMDC2[23:0] x 4. Other values may work as well.

Set Group 4, APR 7 to 0x0F, APR 6 to 0x00, and APR 5 to 0x00.

Group 4, APR 8 – Set to 0x1E.

Equation B.37 yields a value for VMBEC[7:0] of 30 or 0x1E.

Group 4, APR 9–13 – Set all these registers to 0x00.

Group 4, APR 14 – Set to 0x47.

The DVB Synchronization Word[7:0] value is 0x47.

Group 4, APR 15 – Set to 0x10.

Clear D7 to 0, clear the Auto Rate bit (D6) to 0 to obtain the code rate from the VCR, clear the D5 and D4 bits to 0, clear the IMQ_EN bit (D3) to 0 for IMQ to be determined by APR 2 bit 7, clear the Di_Bypass bit (D2) to 0 to enable the deinterleaver, and clear the L[1:0] bits (D1, D0) to 0x00 to select zero mismatching bits.

Group 4, APR 16 – Set to 0x00.

Clear D7 and D6 to 0, clear the SSS[1:0] bits (D5 and D4) to 0 to select Viterbi decoder sync, clear the SSA[1:0] bits D3 and D2 to 0x00 to set the number of sync words to acquire to three, and clear the SST[1:0] bits (D1 and D0) to 0 to set the number of missed sync words to loss of lock at two.

Group 4, APR 17 – Set to 0x00.

Clear the D7 and D6 bits to 0, clear the OF bit (D5) to 0 for serial channel output mode, and clear the OS[4:0] bits (D4 to D0) to 0 to observe the descrambler output.

Group 4, APR 18 – Set to 0x00.

Write any value to this register to reset the PLL module.

Group 4, APR 19 – Set to 0x7A.

Select the register bits according to the following table.

Bits	Setting	Parameter	Meaning
D7 to D5	0b011	DF_SELECT[2:0]	Select filter 4 (16-band filter)
D4 to D3	0b11	DF_GAIN[1:0]	DF_Gain = 8
D2 to D0	0b010	DF_RATIO[2:0]	Select decimation ratio = 8.

See Section 5.4, “Decimation Filters,” page 5-4, for more details.

Group 4, APR 20 – Set to 0x11.

Clear the D7 through D5 bits to 0, clear the PD bit (D4) to 0 for normal operation, clear the D5 through D1 bits to 0, and set the MF_20_35 bit (D0) to 1 for a matched filter roll-off factor of 0.35.

Group 4, APR 21 – Set to 0x00.

Clear the PCLK_INV bit (D7) to 0 for a noninverted PCLK output. Clear the PLL_BP bit (D6) to 0 to enable the internal PLL to generate the A/D clock. Clear the LCLK_OFF bit (D5) to 0 to turn off the LCLK signal. Clear the CLK_DIV1[4:0] bits (D4 to D0) to 0 because the internal PLL is used.

Group 4, APR 22 – Set to 0x00.

Set APR register 22 to 0x00, because the CLK_DIV2[7:0] bits are unused when the internal PLL has been selected.

Group 4, APR 23 – Set to 0xC0.

Set the DC_Offset_On_Off[1] bit (D7) to 1 to cause the DC offset compensation after the ADC to be activated. Set the DC_Offset_On_Off[0] bit (D6) to 1 to cause the noise feedback to the compensation circuit to be selected. Clear the D5 bit to 0. Clear the CLK_DIV2[12:8] bits (D4 to D0) to 0, because the CLK_DIV2[12:8] bits are unused when the internal PLL has been selected.

Group 4, APR 24 – Set to 0x54.

Set the PWR_REF[7:0] bits to 0x54. See Section 5.8.1, “ADC Range and Power Reference,” page 5-20, for more details.

Group 4, APR 25 – Set to 0x03.

Clear the D7 through D3 bits to 0, clear the INT_DC bit (D2) to 0 to disable internal DC offset compensation, and set the PWR_BW[1:0] bits to 0b11 according to section 5.8.2.

Group 4, APR 26 – Set to 0xBA.

Equation B.38 used to calculate the value of SCALE[7:0].

Equation B.38

$$SCALE = \frac{2047 \cdot \sqrt{1 + \left(\frac{E_s}{N_o}\right)^{-1}}}{\sqrt{2 \cdot PWR\_REF}}$$

$$SCALE = \frac{2047 \cdot \sqrt{1 + (2.51)^{-1}}}{\sqrt{2 \cdot 84}} = 186 \ (0xBA)$$

Group 4, APR 27 – Set to 0x64.

This register is set to a signal-to-noise threshold value dependent on the value of the PWR_REF[7:0] value. The SNR_THS[7:0] bits contain a threshold value that indicates a good or bad signal-to-noise ratio. Set the SNR_THS[7:0] value to 100 (0x64.)

Group 4, APR 28 – Set to 0x58.

This register defines the loop bandwidths for a particular baud rate. A good approximation to the equivalent noise bandwidth is given in Equation B.39 (for low data rates.)

Equation B.39

$$B_L = 0.003125 \times BaudRate$$

$$B_L = \frac{\zeta \omega_n}{2}\left(1 + \frac{1}{4\zeta^2}\right)$$

For a baud rate of 2.0 Mbaud we can choose B_L = 15.625 Krad/s and therefore ω_n = 25 Krad/s.

The loop equations are calculated as shown in Equation B.40 and Equation B.41.

Equation B.40

$$\tau_a = \frac{\omega_n^2 T^2}{K_{dcar} L_{car}}$$

Equation B.41

$$\tau_b = \frac{2\zeta\omega_n T}{K_{dcar} L_{car}}$$

The damping factor (ζ) is chosen as 1.0. $K_{dcar} = K_{digital} \times 0.78/32.0$. $K_{digital}$ is chosen from Table 5.4, on page 5-19. For a SNR of 4dB, $K_{digital} = 10$, with the result that $K_{dcar} = 0.24$. Using these values, we get $L_{car} = Fs/Fb = 60e6/2.0e6 = 30$. We can now calculate τ_a and τ_b as shown in Equation B.42 and Equation B.43.

Equation B.42

$$\tau_a = \frac{(25\times10^3)^2\left(\frac{1}{2.0\times10^6}\right)^2}{0.24\times30} = 1.24\times10^{-6}$$

Equation B.43

$$\tau_b = \frac{(2)\times25\times10^3\times\frac{1}{2.0\times10^6}}{0.24\times30} = 3.4\times10^{-3}$$

CAR_MU_SEL[3:0] and CAR_LAMBDA_SEL[3:0] are defined as shown in Equation B.45 and Equation B.46.

Equation B.44

$$CAR\_MU\_SEL = log_2((t_a\times2^{25}) = log_2(1.24e\text{-}6\times2^{25}) = 5 = 0x5$$

Equation B.45

$$CAR\_LAMBDA\_SEL = log_2(\tau_b\times2^{16}) = log_2\{3.4e\text{-}3\times2^{16}\} = 8 = 0x8$$

Program the four LSBs of APR 28 with 0x5 and the four MSBs of APR 28 with 0x8.

Group 4, APR 29 – Set to 0x1F.

The recommended value for CAR_LC_THSL[7:0] is 31 (0x1F) when FP_LOCK_LEN (Group 4, APR 54) is set to 0. Otherwise, set it according to the following table:

FP_LOCK_LEN	CAR_LC_THSL[7:0]	
0	31	Low E_b/N_o
1	72	High E_b/N_o

Group 4, APR 30 – Set to 0x00.

Group 4, APR 31 – Set to 0x20.

Set the RS Bit/Byte Select bit (D7) as needed to select the Reed-Solomon bit or byte error count for Group 3 APR 0 and 1. Set the Errorout_Invert bit (D6) as needed to control the polarity of the ERROROUTn signal. Set the SPI_On_Off bit (D5) to 1. Clear bits D4 through D0 to 0.

Group 4, APR 32–33 – Set to 0x11C.

The value for the sweep rate, CAR_SWR[15:0], is set according to Equation B.46 and Equation B.47. Assume a sweep rate of 2 MHz/s is required.

Equation B.46

$$\text{CAR\_SWR} = \frac{2^{37} \times sweeprate \times T}{Fs \times 16} \times 2$$

Equation B.47

$$\text{CAR\_SWR} = \frac{2^{37} \times 2 \times 10^6 \times \dfrac{1}{2.0 \times 10^6}}{60 \times 10^6 \times 16} \times 2 = 284 \qquad (0x11C)$$

Set Group 4, APR 33 to 0x01 and APR 32 to 0x1C.

Group 4, APR 34–35 – Set to 0x1110.

The value for the upper sweep limit, CAR_USWL[15:0], is set as explained in the following paragraphs. It should be noted that the upper sweep limit is an approximate value but the approximation to the real sweep limit is accurate enough. Assume that the upper sweep limit needed is + 2 MHz. Calculate CAR_USWL[15:0] as shown in Equation B.48 and Equation B.49.

Equation B.48

$$\text{CAR\_USWL} = \frac{2^{37} \times sweeplimit}{Fs \times 2^{21}}$$

Equation B.49

$$\text{CAR\_USWL} = \frac{2^{37} \times 2 \times 10^{6}}{60 \times 10^{6} \times 1 \times 2^{21}} = 2184 \quad (0x0888)$$

Set Group 4, APR 35 to 0x08 and APR 34 to 0x88.

Group 4, APR 36–37 – Set to 0xEEFD.

The value for the lower sweep limit, CAR_LSWL[15:0], is set as explained in the following paragraphs. It should be noted that the lower sweep limit is an approximate value but the approximation to the real sweep limit is accurate enough. Assume that the lower sweep limit needed is – 2 MHz. Calculate CAR_LSWL[15:0] as shown in Equation B.50 and Equation B.51.

Equation B.50

$$\text{CAR\_LSWL} = \frac{2^{37} \times sweeplimit}{Fs \times 2^{21}}$$

Equation B.51

$$\text{CAR\_LSWL} = \frac{2^{37} \times -2 \times 10^{6}}{60 \times 10^{6} \times 1 \times 2^{21}} = -2184 \quad (0xF778)$$

Set Group 4, APR 37 to0xF7 and APR 36 to 0x78.

Group 4, APR 38–40 – set to 0x006D39.

The value for CAR_LF_INIT[23:0] is in accordance with Equation B.52.

Equation B.52

$$CAR\_LF\_INIT = \frac{2^{37} \times freqdeviation}{2^{13} \times Fs}$$

Assuming an initial carrier frequency deviation of + .1 MHz is required, the value for CAR_LF_INIT[23:0] is given as shown in Equation B.53.

Equation B.53

$$CAR\_LF\_INIT = \frac{2^{37} \times 0.1 \times 10^{6}}{2^{13} \times 60 \times 10^{6}} = 27961 \quad (0x6D39)$$

Set Group 4, APR 40 to 0x00, APR 39 to 0x6D, and APR 38 to 0x39.

Group 4, APR 41 – Set to 0x65.

Set the bits in the Carrier Loop Configuration register as shown in Table B.9.

Table B.9 Carrier Loop Configuration Register Bits

Bits	Setting	Acronym	Meaning
D7	0	CAR_SWP_SWAP	Not significant when auto sweep is on
D6	1	CAR_ERROR_SWAP	Carrier phase error detector output inverted
D5	1	CAR_AUTO_SWP	Carrier auto sweep on
D4	0	Reserved	–
D3	0	Reserved	–
D2	1	CAR_PED_SEL	Choose NDAML phase error detector
D1	0	CAR_OPEN	Carrier loop operates normally
D0	1	CAR_SW	Carrier sweep on

If the carrier is locked but the constellation is rotated by 45 degrees, reverse the polarity of bit 6 (CAR_ERROR_SWAP).

Group 4, APR 42 – Set to 0x99.

This register defines the loop bandwidths for a particular baud rate. A good approximation to the equivalent noise bandwidth is given in Equation B.54.

Equation B.54

$$B_L = 0.0003125 \times BaudRate$$

$$B_L = \frac{\zeta\omega_n}{2}\left(1 + \frac{1}{4\zeta^2}\right)$$

For a baud rate of 21.3 Mbaud we can choose B_L = .625 Krad/s and therefore ω_n = 1 Krad/s.

The loop equations are calculated as shown in Equation B.55 and Equation B.56.

Equation B.55

$$\tau_a = \frac{\omega_n^2 T^2}{K_{tim} L_{tim}}$$

Equation B.56

$$\tau_b = \frac{2\zeta\omega_n T}{K_{tim} L_{tim}}$$

The damping factor (ζ) is chosen as 1.0, and K_{tim} = 0.0388. Using these values we get L_{tim} = Fs x decimation_ratio/Fb = 60e6 *(0.25)/2.0e6 = 3.75. We can now calculate τ_a and τ_b as shown in Equation B.57 and Equation B.58.

Equation B.57

$$\tau_a = \frac{(1 \times 10^3)^2\left(\frac{1}{2.0 \times 10^6}\right)^2}{0.0388 \times 3.75} = 0.171 \times 10^{-5}$$

Equation B.58

$$\tau_b = \frac{2 \times 1 \times 10^3 \times \frac{1}{2.0 \times 10^6}}{0.0388 \times 3.75} = 68.6 \times 10^{-4}$$

CLK_MU_SEL[3:0] and CLK_LAMBDA_SEL[3:0] are defined as shown in Equation B.59 and Equation B.60.

Equation B.59

$$CAR\_MU\_SEL = log_2(t_a \times 2^{28}) = log_2(0.171e\text{-}5 \times 2^{28}) = 9 = 0x9$$

Equation B.60

$$CAR\_LAMBDA\_SEL = log_2(\tau_b \times 2^{16}) = log_2(68.6\,e\text{-}4 \times 2^{16}) = 9 = 0x9$$

Program the four LSBs of APR 42 with 0x9 and the four MSBs of APR 42 with 0x9.

Note: Group 4, APR 43–48, contain sweep parameters that need to be programmed only if clock sweep is required. These parameters have meaning only when the CLK_SW bit (bit D0 of Group 4, APR 53) is set to a 1.

Group 4, APR 43–44 – Set to 0x28CC.

The value for the clock sweep rate, CLK_SWR[15:0], is set according to Equation B.61, assuming a clock sweep rate of 10 kHz/s.

Equation B.61

$$CLK\_SWR = \frac{2^{45} \times sweeprate \times T}{Fs \times \frac{1}{DF\_RATIO} \times 16} \times 2$$

$$CLK\_SWR = \frac{2^{45} \times 10 \times 10^3 \times \frac{1}{2.0 \times 10^6}}{60 \times 10^6 \times 0.125 \times 16} \times 2 = 10444 \ (0x28CC)$$

Set Group 4, APR 44 to 0x28 and APR 43 to 0xCC.

Group 4, APR 45–46 – Set to 0x0940.

The value for the upper sweep limit, CLK_USWL[15:0], is set as explained in the following paragraphs. It should be noted that the upper sweep limit is an approximate value but the approximation to the real sweep limit is accurate enough. Assume that the upper sweep limit needed is + 10 kHz. CLK_USWL[15:0] is calculated as shown in Equation B.62.

Equation B.62

$$\text{CLK\_USWL} = \frac{2^{45} \times sweeplimit}{Fs \times \frac{1}{\text{DF\_RATIO}} \times 2^{22}} \times 2$$

$$\text{CLK\_USWL} = \frac{2^{45} \times 10 \times 10^{3}}{60 \times 10^{6} \times 0.125 \times 2^{22}} \times 2 = 2368_{10} \quad (0x0940)$$

Set Group 4, APR 46 to 0x09 and APR 45 to 0x40.

Group 4, APR 47–48 – Set to 0xFBC0.

The value for the lower clock sweep limit, CLK_LSWL[15:0], is set as explained in the following paragraphs. It should be noted that the lower sweep limit is an approximate value, but the approximation to the real sweep limit is accurate enough. Assume that the lower sweep limit needed is – 10 kHz. The CLK_LSWL[15:0] value is calculated as shown in Equation B.63.

Equation B.63

$$\text{CLK\_LSWL} = \frac{2^{45} \times -10 \times 10^{3}}{60 \times 10^{6} \times 0.125 \times 2^{22}} \times 2 = -2368_{10} \quad (0xFBC0)$$

Set Group 4, APR 48 to 0xFB and APR 47 to 0xC0.

Group 4, APR 49–52 – Set to 0x1E000000.

Choose CLK_BIAS[30:0] according to Equation B.64.

Equation B.64

$$\text{CLK\_BIAS} = \frac{Fs \times \frac{1}{\text{DF\_RATIO}} \times 2^{28}}{2 \times Fb}$$

$$\text{CLK\_BIAS} = \frac{60 \times 10^{6} \times 0.125 \times 2^{28}}{2 \times 2.0 \times 10^{6}} = 503316480 \quad (0x1E00.0000)$$

Fs = sampling frequency at the A/D and Fb is the baud rate.

Set Group 4, APR 52 to 0x1E, APR 51 to 0x00, APR 50 to 00, and APR 49 to 00.

Group 4, APR 53 – Set to 0x38**.**

Set the bits in the Clock Loop Configuration register (APR 53) as shown in Table B.10.

Table B.10 Clock Loop Configuration Register Bits

Bits	Setting	Acronym	Meaning
D7	0	CLK_SWP_SWAP	Not significant when auto sweep is on or when sweep is off
D6	0	CLK_ERROR_SWAP	Timing error detector output not inverted
D5	1	CLK_AUTO_SWP	Automatic internal sweep control
D4	1	Reserved	Set this bit to 1
D3	1	AGC_CLK_SEL	Integrate over all samples
D2	0	Reserved	Clear this bit to 0
D1	0	CLK_OPEN	Enable the clock loop
D0	0	CLK_SW	Clock sweep off

Group 4, APR 54 – Set to 0x00.

Set the bits in the Demodulator Configuration register (APR 54) as shown in Table B.11.

Table B.11 Demodulator Configuration Register Bits

Bits	Setting	Acronym	Meaning
D7	0	SNR_EST	Enable SNR estimator
D6	0	PWRP_TRI	PWRP not 3-stated
D5	0	ADC_PD	A/D normal operation
D4	0	FP_LOCK_LEN	Normal (long) window for phase lock
D3	0	PWRP	PWRP pin in normal mode
D2 to D1	0b00	Reserved	Clear these bits to 0 for normal mode
D0	0	CLK_ALPHA_SEL	Alpha value = 0.43

Group 4, APR 55 – Set to 0x00.

Set the bits in the External Output Control Bits and Reset register (APR 55) as shown in Table B.12.

Table B.12 External Output Control Bits and Reset Register Bits

Bits	Setting	Acronym	Meaning
D7	0	ADC_BP	Enable ADCs
D6	0	OB_2C	Input is offset-binary format
D5 to D2	0b0000	XCTR[3:0]	Corresponding output pin = VSS
D1	0	DEMOD_RST	No reset for demodulator
D0	0	FEC_RST	No reset for FEC

Group 4, APR 56–57 - Set to 0x00.

Group 4, APR 58 - Set to 0x14.

Group 4, APR 59–61 – These registers are used to communicate on a serial bus to the tuner using the XCTR[3:0] output pins. Refer to Appendix C for details on programming the SPI interface.

Group 4, APR 62 – Set according to user preference.

Set the bits in the Group 4, APR 62 register as shown in Table B.13.

Table B.13 Group 4, APR 62 Register Bits

Bits	Setting	Acronym	Meaning
D7	–	Serial_B	Refer to Appendix C, Programming the Serializer, for more details.
D6 to D5	–	Serial_C[1:0]	Refer to Appendix C, Programming the Serializer, for more details.
D4 to D1	0b0100	SPI_M[3:0]	Denominator of Viterbi Code Rate = 4 (rate = 3/4)
D0	–	Serial_A	Refer to Appendix C, Programming the Serializer, for more details.

Group 4, APR 63 – Set to 0x63.

Clear the FMODE bit (D7) to 0. Set the SPI_CLK_AND bit (D6) to 1 to AND the SPI byte clock and the data valid signal. Set SPI_MODE_A_B to 0 for Mode A. Set SPI_N[3:0] to 3 since the Viterbi Code Rate is 3/4.

Group 4, APR 64–65 – Set to 0x0008.

Set the SPI_GAIN[9:0] to 8 because the oversampling ratio (OR) is 30.

OR	SPI Gain
2 to 4	50.0
4 to 8	35.0
8 to 16	15.0
Greater than 16	less than 10

Set Group 4, APR 65 to 0x08 and APR 64 to 0x00.

Group 4, APR 66–68 – Set to 0x066666.

Set the SPI_Bias[22:0] value as shown in Equation B.65.

Equation B.65

$$SPIBias = \frac{2^{24} \cdot VCR}{OR}$$

In the equation, VCR = 3/4 and OR = 60e6/2e6, so SPIBias = 419430 (0x06.6666).

Set Group 4, APR 68 to 0x06, APR 67 to 0x66, and APR 66 to 0x66.

Group 4, APR 69 – Set to 0x4B.

Set the timing lock threshold (CLK_LC_THSL[7:0]) value at 75 (0x4B.)

Table B.14 gives the register values calculated for low data rates.

Table B.14 Low Data Rate Register Values

APR [5:0]	D7	D6	D5	D4	D3	D2	D1	DO	HEX
0	Set to 1	Re-served	PLL_N[5:0]						81
1	Reserved		PLL_S[5:0]						04
2	IMQ	DVB_ DSS	QB	PLL_T[4:0]					01
3	Viterbi Code Rate[2:0]			TEI	SYNC2 _MOD	Reserved	PLL_M[1:0]		09
4	Viterbi Max Data Bit Count, VMDC1[7:0]								40
5	Viterbi Max Data Bit Count 2, VMDC2[7:0], low byte								00
6	Viterbi Max Data Bit Count 2, VMDC2[15:8], middle byte								00
7	Viterbi Max Data Bit Count 2, VMDC2[23:16], high byte								00
8	Viterbi Maximum Bit Error Count[7:0], Rate 1/2								1E
9	Viterbi Maximum Bit Error Count[7:0], Rate 2/3								00
10	Viterbi Maximum Bit Error Count[7:0], Rate 3/4								00
11	Viterbi Maximum Bit Error Count[7:0], Rate 5/6								00
12	Viterbi Maximum Bit Error Count[7:0], Rate 6/7								00
13	Viterbi Maximum Bit Error Count[7:0], Rate 7/8								00
14	Synchronization Word[7:0]								47

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Table B.14 Low Data Rate Register Values (Cont.)

APR [5:0]	D7	D6	D5	D4	D3	D2	D1	DO	HEX
15	Reserved	Auto Rate	Reserved		IMQ_ EN	DI_ Bypass	L[1:0]		10
16	Reserved		Sync Status Select, SSS[1:0]		Sync States Acq, SSA [1:0]		Sync States Track, SST[1:0]		00
17	Reserved		OF	Output Selector, OS[4:0]					00
18	PLL_RESET								00
19	DF_Select[2:0]			DF_Gain[1:0]		DF_Ratio[2:0]			7A
20	Reserved			PD	Reserved			MF_20_ 35	11
21	PCLK_ INV	PLL_BP	LCLK_ OFF	CLK_DIV1[4:0]					00
22	CLK_DIV2[7:0]								00
23	DC_Offset_On_Off [1:0]		Re- served	CLK_DIV2[12:8]					C0
24	PWR_REF[7:0]								54
25	Reserved					INT_DC	PWR_BW[1:0]		03
26	Scale factor for DEMI, DEMQ, SCALE[7:0]								BA
27	SNR Estimator Threshold, SNR_THS[7:0]								64
28	Carrier Loop Lambda, CAR_LAMBDA_SEL[3:0]				Carrier Loop Mu, CAR_MU_SEL[3:0]				58
29	Carrier Phase Lock Detector Threshold, CAR_LC_THSL[7:0]								1F
30	Reserved								00
31	RS Bit/Byte Select	Errorout _ Invert	SPI_On _Off	Reserved					20
32	Carrier Sweep Rate, CAR_SWR[7:0]								1C
33	Carrier Sweep Rate, CAR_SWR[15:8]								88
34	Carrier Upper Sweep Limit, CAR_USWL[7:0]								08

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Table B.14 Low Data Rate Register Values (Cont.)

APR [5:0]	D7	D6	D5	D4	D3	D2	D1	DO	HEX
35	Carrier Upper Sweep Limit, CAR_USWL[15:8]								78
36	Carrier Lower Sweep Limit, CAR_LSWL[7:0]								F7
37	Carrier Lower Sweep Limit, CAR_LSWL[15:8]								EE
38	Carrier Loop Filter Initialization, CAR_LF_INIT[7:0]								39
39	Carrier Loop Filter Initialization, CAR_LF_INIT[15:8]								6D
40	Carrier Loop Filter Initialization, CAR_LF_INIT[23:16]								00
41	CAR_ SWP_ SWAP	CAR_ ERROR _SWAP	CAR_ AUTO_ SWP	Reserved		CAR_ PED_ SEL	CAR_ OPEN	CAR_ SW	65
42	Clock Loop Lambda, CLK_LAMBDA_SEL[3:0]				Clock Loop Mu, CLK_MU_SEL[3:0]				99
43	Clock Sweep Rate, CLK_SWR[7:0]								CC
44	Clock Sweep Rate, CLK_SWR[15:8]								28
45	Clock Upper Sweep Limit, CLK_USWL[7:0]								40
46	Clock Upper Sweep Limit, CLK_USWL[15:8]								09
47	Clock Lower Sweep Limit, CLK_LSWL[7:0]								C0
48	Clock Lower Sweep Limit, CLK_LSWL[15:8]								FB
49	Clock Loop Bias, CLK_BIAS[7:0]]								00
50	Clock Loop Bias, CLK_BIAS[15:8]								00
51	Clock Loop Bias, CLK_BIAS[23:16]								00
52	Reserved	Clock Loop Bias, CLK_BIAS[30:24]							00
53	CLK_ SWP_ SWAP	CLK_ ERROR _SWAP	CLK_ AUTO_ SWP	Set to 1	AGC_ CLK_ SEL	Reserved	CLK_ OPEN	CLK_ SW	38
54	SNR_ EST	PWRP_ TRI	ADC_ PD	FP_ LOCK_ LEN	PWRP	Reserved		CLK_ ALPHA _SEL	00

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Table B.14 Low Data Rate Register Values (Cont.)

APR [5:0]	D7	D6	D5	D4	D3	D2	D1	DO	HEX
55	ADC_BP	OB_2C	External Control Output Bits, XCTR[3:0]				DE-MOD_ RST	FEC_ RST	00
56	Reserved								00
57	Reserved								00
58	Reserved								14
59	Serial Transmission Start Data, TXSD[6:0]							Re-served	10
60	Serial Transmission Data, STXD[7:0]								00
61	Serial Transmission End Data, TXED[7:0]								00
62	Serial_B	Serial_C[1:0]		SPI_M[3:0]				Serial_ A	—
63	FMODE	SPI_ CLK_ AND	SPI_ MODE_ A_B	Re-served	SPI_N[3:0]				63
64	SPI_Gain[7:0](LSB)								08
65	Reserved						SPI_Gain[9:8]		00
66	SPI_Bias[7:0](LSB)								66
67	SPI_Bias[15:8](MB)								66
68	Reserved	SPI_Bias[23:16]							06
69	Timing Lock Threshold CLK_LC_THSL[7:0]								4B

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Appendix C
Programming the Serializer

This appendix explains how to program the Serializer module and shows the signal waveforms corresponding to Serializer 2- and 3-wire operation. It contains the following sections:

- Section C.1, “Serializer Overview”
- Section C.2, “Serializer Interface Signals and Configuration Registers”
- Section C.3, “Programming for Serial Mode (2-Wire Compliant)”
- Section C.4, “Programming for 3-Wire Mode”

This chapter provides complete information on how to use the L64724 registers for Serializer operation, but does not provide information on how to program the registers for a specific application for the bits, which depends on the addressed slave device.

C.1 Serializer Overview

The Serializer implements a write-only interface for serial 2- or 3-wire compliant devices. A microprocessor or microcontroller writes to the Group 4 Address Pointer Registers (APR) 59–62 to control Serializer operation.

Note: APR 62 needs the applicable bits (Serial_A, Serial_B, and Serial_C) programmed before writing to APR 59–61.

In the case of a 2-wire compliant slave, the serializer may be used to perform writes to the slave as follows:

- Write to APR 59 (TXSD)—generates the START condition
- Write to APR 60 (STXD)—generates subsequent data

- Write to APR 61(TXED)—generates the last byte that is to be written, followed by a STOP condition

The method used to control the Serializer frees up the external microprocessor or the on-board microcontroller to perform other critical operations. Similarly, the Serializer may be used to implement the 3-wire interface in any of the three modes of the 3-wire interface (see Section C.4, “Programming for 3-Wire Mode,” page C-6.)

The pinouts and a detailed description of the operation of the serializer are outlined in the following sections.

C.2 Serializer Interface Signals and Configuration Registers

TXSD[6:0]

TXSD[6:0] provide the 7-bit slave address of the tuner chip and comes from Group 4, APR 59, of the microprocessor interface (uPI.) Bit 7 is the MSB of the slave address. The Serializer module serializes the slave address and outputs it on XCTR_OUT[1].

TXED[7:0]

The content of this register is the last data of the serial interface write cycle. It is an 8-bit value stored in Group 4, APR 61 of the uPI.

STXD[7:0]

This register holds the data that is serialized and sent out on the serial interface by the Serializer. This value comes from Group 4, APR 60 of the uPI, and is used when the uPI or the uC wants to write two or more data bytes to the tuner.

XCTR[2] (ENABLE)

XCTR[2] is a bit in the Group 4, APR 55 register that controls the ENABLE signal on the XCTR_OUT[2] pin within the 3-wire interface. When the ENABLE signal is HIGH, the data on the data bus is valid.

XCTR[1] (SCLK)

XCTR[1] is a bit in the Group 4, APR 55 register that controls the SCLK signal on the XCTR_OUT[1] pin. SCLK operates at a maximum of 394.74 kHz and is obtained from a divide by 38 counter operating at the rate of the crystal clock connected to the L64724. If the crystal is at 15 MHz, the SCLK signal is at 15 MHz divided by 38 (394.74 kHz.) For a 10 MHz crystal, SCLK is 263.16 kHz.

XCTR[0] (SDATA)

XCTR[0] is a bit in the Group 4, APR 55 register that controls the SDATA signal on the XCTR_OUT[0] pin. SDATA is the serial data output within the 3-wire interface.

Serial_A

The Serial_A bit indicates whether the output pins XCTR_OUT[2:0] are to be controlled directly as programmed in the Group 4 register External Control Output Bits, XCTR[2:0], or by the serializer module with data from the TXSD, STXD, and TXED registers. When the bit is 0 (the default), it indicates that control is as dictated by XCTR[2:0].

Serial_C[1:0]

Serial Transmission Control Bit C

The Serial_C[1:0] bits control whether a serial 2-wire or a 3-wire protocol is used to serialize data. The following table outlines the options:

Serial_C[1:0]		Selected Function
0	0	2-wire serial interface
0	1	3-wire interface, ENABLE HIGH for all valid data
1	0	3-wire interface, ENABLE HIGH for 1 clock cycle at the start of data transfer
1	1	3-wire interface, ENABLE HIGH for 1 clock cycle at the end of data transfer

C.3 Programming for Serial Mode (2-Wire Compliant)

To set the serializer in a mode to produce 2-wire compliant signals on the SDATA (XCTR_OUT[1]) and the SCLK (XCTR_OUT[0]) signal lines, the Serial_C register (Group 4, APR 62[6:5]) must be programmed to 0b00.

Note: Only writes to a 2-wire compliant slave can be accomplished using the Serializer—it does not perform read operations. Furthermore, the serializer assumes that the acknowledge signal is generated properly, every 9th SCLK cycle, by the slave that the Serializer is addressing.

Follow the steps outlined below to address the slave and perform subsequent write cycles to it.

C.3.1 Single Data Write

1. Write TXSD (7-bit slave address)
2. Wait (11 SCLK cycles)
3. Write TXED (8-bit data)

C.3.2 Two Data Writes

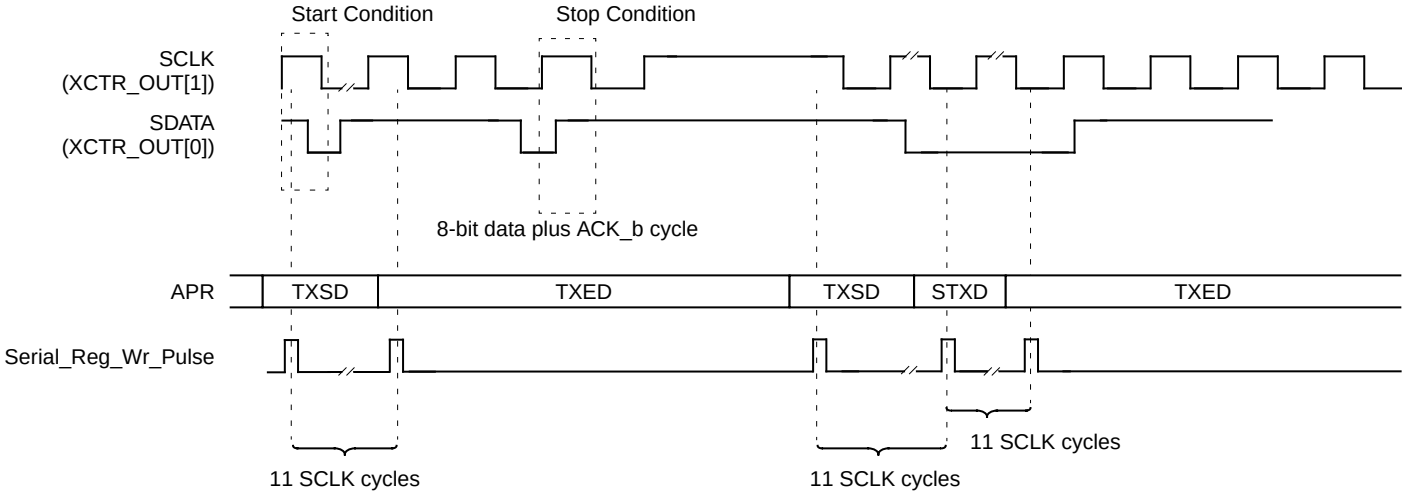
1. Write TXSD (7-bit slave address)
2. Wait (11 SCLK cycles)
3. Write STXD (8-bit data)
4. Wait (11 SCLK cycles)
5. Write TXED (8-bit data)

C.3.3 Multiple-Data Writes

```
1. Write TXSD (7-bit slave address)
2. Wait (11 SCLK cycles){
3. For (i =1; i < #data_bytes; i++)
          Write STXD (8-bit data)
          Wait (11 SCLK cycles)
   }
          Write TXED (8-bit data)
```

Figure C.1 shows the 2-wire Serializer operation.

Figure C.1 2-Wire Compliant Interface



C.4 Programming for 3-Wire Mode

To set the Serializer in a mode to produce 3-wire interface compliant signals on the SDATA (XCTR_OUT[1]), SCLK (XCTR_OUT[0]), and the ENABLE (XCTR_OUT[2]) signals, the Serial_C register (Group 4, APR 62[6:5]) must be programmed as shown in the table below:

Serial_C[1:0]		Selected Function
0	1	3-wire interface, ENABLE HIGH for all valid data
1	0	3-wire interface, ENABLE HIGH for 1 clock cycle at the start of data transfer
1	1	3-wire interface, ENABLE HIGH for 1 clock cycle at the end of data transfer

Note: Only writes to a 3-wire compliant slave can be accomplished using the Serializer—it does not perform read operations.

Follow the steps outlined below, written as pseudo-code, to address the slave and perform subsequent write cycles to it.

C.4.1 Single Data Write

```
1. Write TXED (8-bit data)
```

C.4.2 Two Data Writes

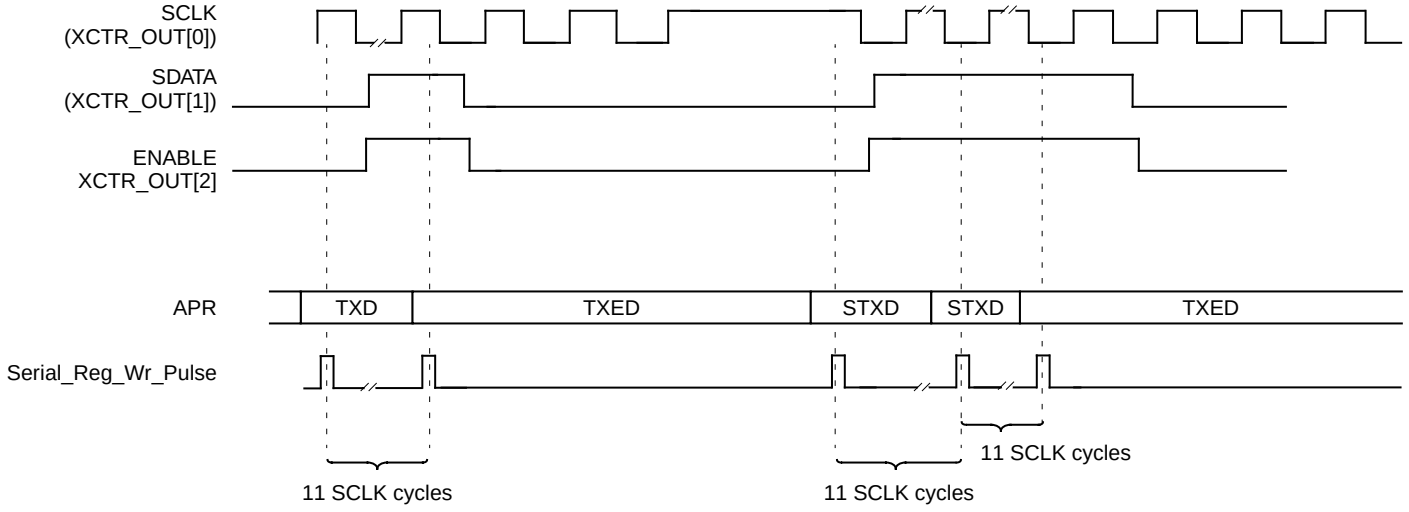
```
1. Write STXD (8-bit slave-address)
2. Wait (11 SCLK cycles)
3. Write TXED (8-bit data)
```

C.4.3 Multiple-Data Writes

```
1. Write STXD (8-bit data)
2. Wait (11 SCLK cycles){
3. for (i =1; i < #data_bytes; i++)
         Write STXD(8-bit data)
         Wait (11 SCLK cycles)
   }
   Write TXED(8-bit data)
```

Figure C.2 shows the 3-wire Serializer operation.

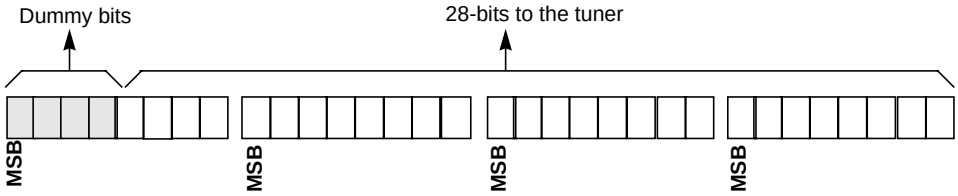
Figure C.2 3-Wire Interface



C.4.4 Example - Write 28 Bits of Data Using the 3-Wire Mode.

Data writes using the 3-wire interface are possible with a granularity of eight bits. To write data that is not divisible by eight, some “padding” of dummy data is necessary. For instance, if a 28-bit message is to be sent to the tuner, four 8-bit data bytes should be sent with the first high nibble (4 bits) being the dummy bits, followed by the 4 bits that are to be sent to the tuner. An illustration is shown below.

Figure C.3 28-Bit Write Using 3-Wire Mode



Appendix D
A/D Converters

This appendix discusses the analog-to-digital converters (ADCs) used in the L64724. The ADCs sample the signal from the I/Q downconverters at the appropriate oversampling rate and output a 6-bit sign-magnitude equivalent digital signal.

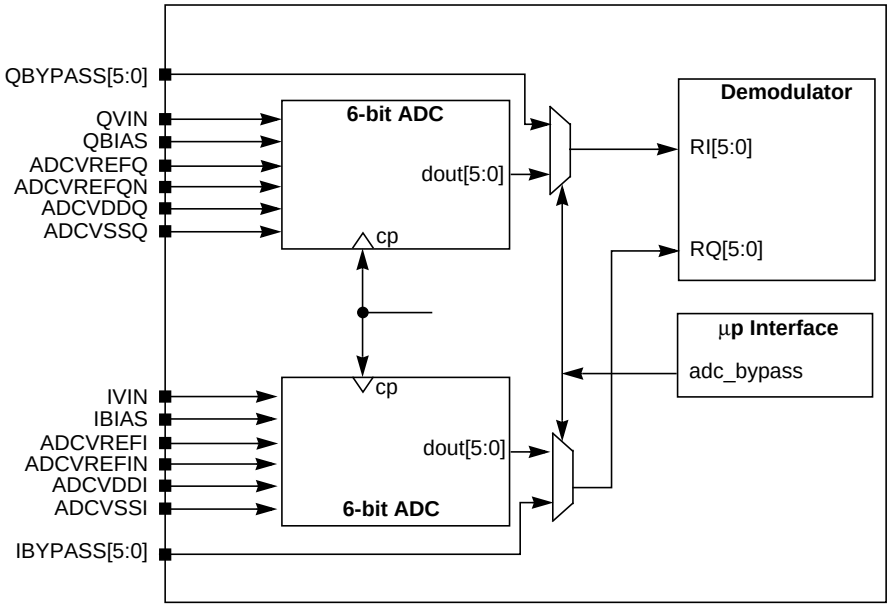
This chapter contains the following sections:

- Section D.1, “ADC Overview”
- Section D.2, “Board Level Interface”
- Section D.3, “DC Characteristics”
- Section D.4, “AC Characteristics”

D.1 ADC Overview

Two 6-bit flash ADCs generate the digitized data stream at the input of the demodulator. The interconnection of the ADCs with other modules and their connections with the L64724 I/O pins are shown in Figure D.1.

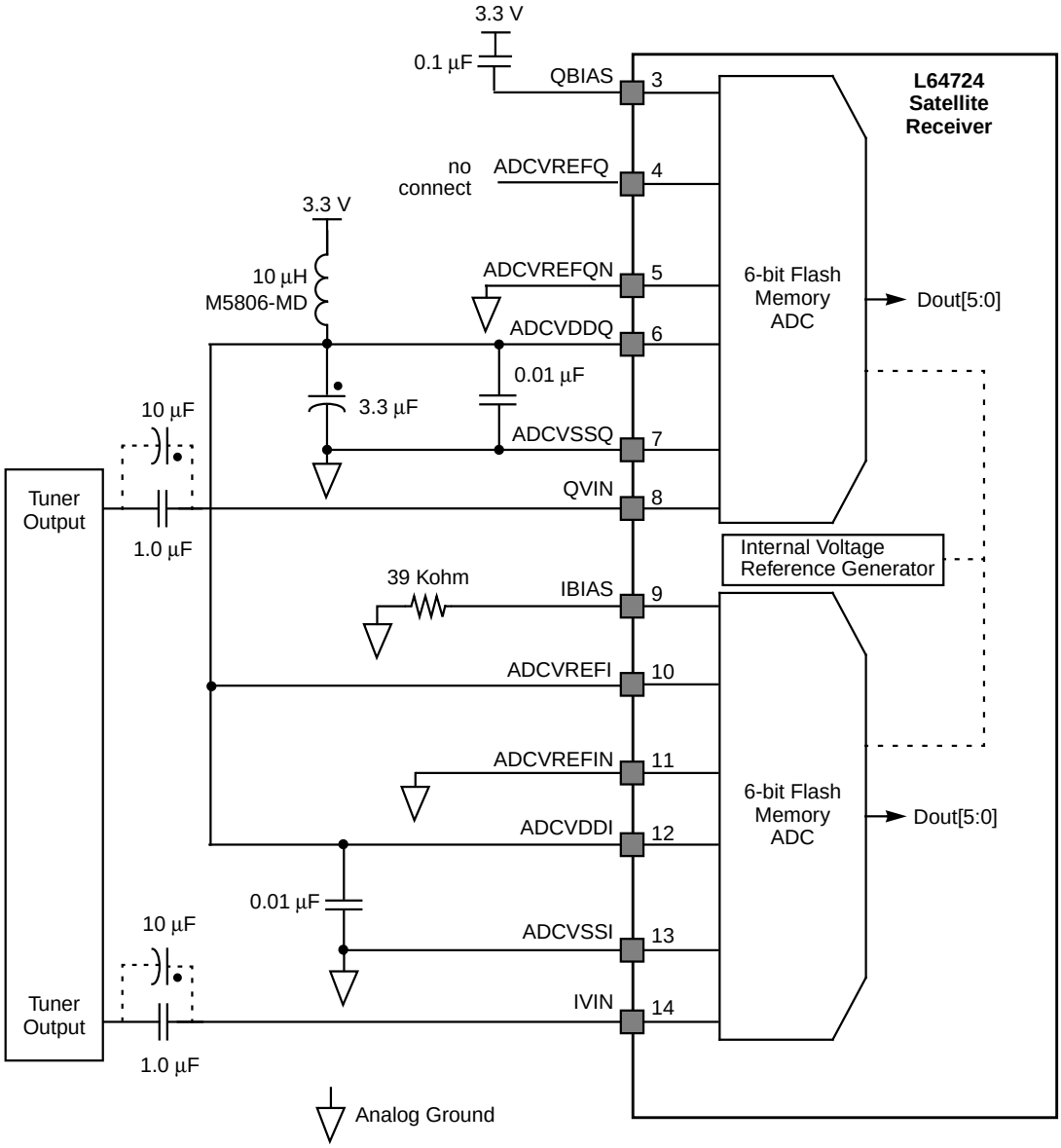
Figure D.1 ADC Connections for L64724



D.2 Board Level Interface

The ADCs require some additional circuitry at the board level. Figure D.2 shows sample circuitry that connects to the ADC-related pins on the L64724.

Figure D.2 ADC Board Level Interface



It is recommended that the filter components connected to the ADCVDDQ/ADCVSSQ and ADCVDDI/ADDVSSI pins be placed in close proximity to their respective pins.

D.2.1 Analog Input Impedance

The analog input (IVIN, QVIN) capacitance is specified to be typically 10 pF. No input resistance is specified because the input is connected to the gate of a FET or an array of FETs. The DC resistance for the input is very high (millions of ohms), only degraded by leakage current. However, due to the capacitance, the input impedance decreases with increase in input frequency. The source impedance should be kept as low as possible.

D.2.2 Analog Input Range

The recommended analog input range is from 0 to 1 V. The actual top of the range is set by the voltage at ADCVREFI (ADCVREFQ), which is recommended to be 1 V. The actual bottom of the range is the voltage at ADCVREFIN (ADCVREFQN), which is 0 V, or analog ground.

While it is possible to set up the Analog Input Range to be different from the 0 to 1 V range, be aware that if ADCVREFI (ADCVREFQ) is decreased from 1 V, the linearity of the A/D suffers. It is not recommended that the voltage be more than 10% above 1 V. The L64724 internally generates the DC offset for the Analog Input (IVIN, QVIN).

D.2.3 Reference Voltage

The L64724 internally generates the reference voltage for the dual ADCs.

D.2.4 External Bias Current

The external bias current is recommended to be 50 µA, which is the bias current for the array of differential pair FET comparators inside the A/D converter. The external resistor sinks the bias current.

D.3 DC Characteristics

Table D.1 shows the DC characteristics for the ADC modules.

Table D.1 DC Characteristics

Parameter	Min	Typ	Max	Units
Supply Voltage (VDD and AVDD)	2.97	3.3	3.63	V
Resolution		6		Bits
Analog Input Range	0		1	V
External Bias Current	–	50	–	µA
Differential Nonlinearity	–	1/2	–	LSB
Integral Nonlinearity	–	1/2	–	LSB
Analog Input Capacitance	–	10	–	pF
Ladder Resistance (Vref to Vrefn)	30	70	200	W

D.4 AC Characteristics

Table D.2 shows the AC characteristics for the ADC modules.

Table D.2 AC Characteristics

Parameter	Min	Typ	Max	Units
Clock Rate	–	–	90	MHz
Supply Current (from AVDD)	–	–	90	mA
Supply Current (from VDD)	–	–	4	mA

Appendix E
L64724 On-chip Microcontroller

This appendix describes the L64274 On-chip Microcontroller and contains the following sections:

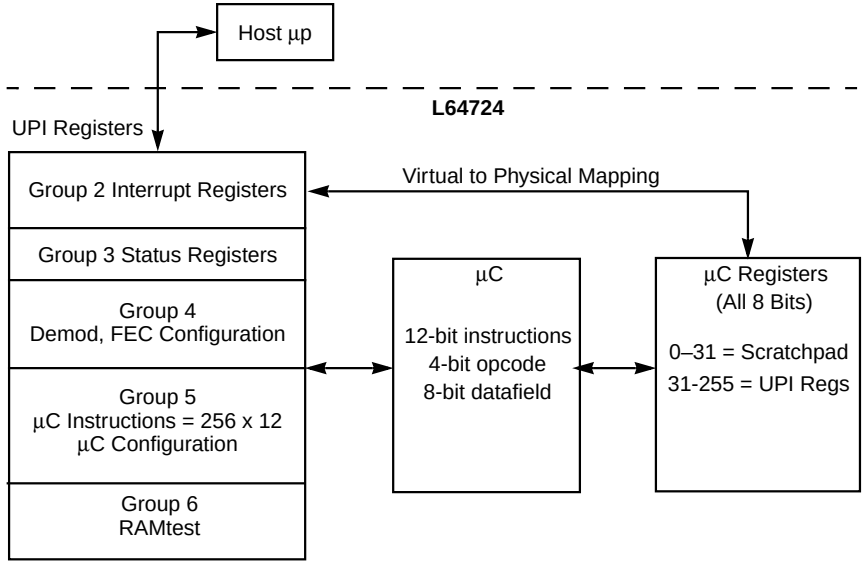
- Section E.1, “L64724 Microcontroller Instruction Set,” page E-2
- Section E.2, “Microcontroller Address Map,” page E-5

The features of the L64724 on-chip microcontroller are as follows:

- A 24-bit accumulator
- 12-bit instructions, with a 4-bit opcode and 8-bit datafield
- Code size of 256 instructions
- Memory size of 256 registers (8-bits each)

Figure E.1 shows how the L64724 uC and the host microprocessor access the L64724 Configuration and Status registers. For more details on L64724 registers, refer to Chapter 3, “L64724 Registers.”

Figure E.1 Registers Shared Between the Host uP and L64724 µC



E.1 L64724 Microcontroller Instruction Set

Table E.1 lists the instructions available in the µC.

Table E.1 L64724 µC Instruction Set

Mnemonic	Expansion	Opcode [11:8]	Datafield [7:0]	Description
CLA	Clear Acc	0000	xxxxxxxx	Set accumulator value to all zero
LDALI	Load Acc Low Immediate	0001	Immediate 8-bit data	Load immediate 8 bit data into accumulator's low byte (acc[7:0]). Other accumulator bytes do not change.
LDAMI	Load Acc Middle Immediate	0010	Immediate 8-bit data	Load immediate 8 bit data into accumulator's middle byte (acc[15:8]). Other accumulator bytes do not change.

(Sheet 1 of 3)

Table E.1 L64724 μC Instruction Set (Cont.)

Mnemonic	Expansion	Opcode [11:8]	Datafield [7:0]	Description
LDALR	Load Acc Low Register	0011	8-bit register address	Load 8 bit register value into accumulator's low byte. The register's address is given as immediate data in the command's data field.
SRBIT	Set/Reset Bit	0100	axxxxbcd	Set specified bit in accumulator's low byte to given value. a = value (0 or 1). bcd = bit position 000 = acc[0], 001 = acc[1], 010 = acc[2], 011 = acc[3], 100 = acc[4], 101 = acc[5], 110 = acc[6], 111 = acc[7].
ADDALR	Add Acc Low Register	0101	8-bit register address	Add 8-bit unsigned register value to accumulator's low byte. The added value is positioned opposite acc[7:0], with no sign extension. The register's address is given in the instruction's datafield.
ADDAMR	Add Acc Middle Register	0110	8-bit register address	Add 8 bit signed register value * 2^8 to accumulator[15:0]. The register address is given in the instruction's datafield. The register value is positioned opposite accumulator bits [15:8] after appropriate sign-extension (to 24 bits), and zero-padding.
SUBAMR	Subtract Acc Middle Register	0111	8-bit register address	Subtract 8 bit signed register value * 2^8 from accumulator. The register address is given in the instruction's datafield. The register value is positioned opposite accumulator bits [15:8] after appropriate sign-extension to 24 bits, and zero-padding.
STAR	Store Acc Register	1000	8-bit register address	Store accumulator's low byte - acc[7:0] in register whose address is given in the instruction's datafield.
WTCLKS	Wait Clock periods	1001	8-bit unsigned	Wait for specified number of clock periods before loading next instruction. The instruction will take the specified number of clock periods + 2 for execution.

(Sheet 2 of 3)

Table E.1 L64724 μC Instruction Set (Cont.)

Mnemonic	Expansion	Opcode [11:8]	Datafield [7:0]	Description
ASA	Arithmetic Shift Acc	1010	xxxxxabc	Arithmetic shift to accumulator value, according to bits abc in instruction's datafield. a = direction of shift 0 = left shift with zero padding 1 = right shift with sign extension bc = amount of shift 00 = 1-bit shift 01 = 2-bit shift 10 = 4-bit shift 11 = 8-bit shift The sign bit = acc(23) retains its value during all right and left arithmetic shifts.
DECLP	Decrement Loop Control Register	1011	xxxxxxab	Decrement specified scratch pad register dedicated for loop control. 00 = decrement LP0 01 = decrement LP1 10 = decrement LP2
BR	Branch	1100	Relative 8-bit instruction address in two's complement	Branch to the specified uC program line. The relative branching address is given in the instruction's data field. Jump to relative address + 1.
SKZ	Skip on Zero	1101	abcdefgh	Skip the next instruction if the result of applying the specified and-or mask on the accumulator's low byte results in a logical zero. acc[7:0] = acc[7:0], in other words, its value is not affected by the SKZ instruction.
SKNZ	Skip on Non-Zero	1110	abcdefgh	Skip the next instruction if the results of applying the specified mask on the accumulator's low byte results in non-zero. acc[7:0] = acc[7:0], i.e. its value is not affected by the SKNZ instruction
WTSYMBS	Wait valid demod symbols	1111	8-bit unsigned	Wait until timer count down completed, the timer counts valid demod symbols. Formula for number of clk cycles it takes for this instruction is to be included.

(Sheet 3 of 3)

E.2 Microcontroller Address Map

Table E.2 shows the µC to µP address mapping.

Table E.2 Microcontroller Address Map

	µC_ADD	µP_APR	D7	D6	D5	D4	D3	D2	D1	DO	R/W by µC
Scratch Pad[1]	0	N/A	Loop Control Register 0, LP0[7:0]								R/W
	1		Loop Control Register 1, LP1[7:0]								
	2		Loop Control Register 2, LP2[7:0]								
	3							Loop Control Register[2] status, lp_status[2:0]			
	4							Accumulator status, acc_status[3][2:0]			
	5		Scratch Pad Register 0, SP0[7:0]								
	6		Scratch Pad Register 1, SP1[7:0]								
	7		Scratch Pad Register 2, SP2[7:0]								
	8		Scratch Pad Register 3, SP3[7:0]								
	9		Scratch Pad Register 4, SP4[7:0]								
	10		Scratch Pad Register 5, SP5[7:0]								
	11		Scratch Pad Register 6, SP67:0]								
	12		Scratch Pad Register 7, SP7[7:0]								
	13		µC_Configuration, µC_CONFIG[7:0][4]								R
	..[5]										
Group 2	32	0	Group 2 System Status Register STS[7:0]								R
	33	1	Group 2 System Status Register STS[15:8]								R
	34	2	Group 2 System Status Register STS[[23;16]								R
	35[6]	3	Group 2 uC Interrupt Register, uC_I[7:0]								R/W
	..										
Group 3	64	0	Reed-Solomon Corrected Error Count low byte, CEC[7:0]								R
	65	1	Reed-Solomon Corrected Error Count high byte, CEC[15:8]								
	66	2	Reed-Solomon Uncorrected Error Count low byte, UEC[7:0]								
	67	3	Reed-Solomon Uncorrected Error Count high byte, UEC[15:0]								
	68	4	Viterbi Bit Error Rate Count low byte, VBERC[7:0]								

(Sheet 1 of 5)

Table E.2 Microcontroller Address Map (Cont.)

	µC_ADD	µP_APR	D7	D6	D5	D4	D3	D2	D1	DO	R/W by µC
Group 3 (Cont.)	69	5	Viterbi Bit Error Rate Count high byte, VBERC[15:8]								R/W
	70	6	Demod_SNR	XCTR_IN	Reserved						
	71	7	NCO Frequency Deviation, CAR_NCOF[7:0]								
	72	8	NCO Frequency Deviation, CAR_NCOF[15:8]								
	73	9	NCO Frequency Deviation, CAR_NCOF[23:16]								
	74	10	AGC Loop Voltage Meter, PWR_LVL[7:0]								
	75	11	S2_FL	uC Active	CAR_LCF	CAR_LC	CLK_LCF	S3	S2	S1	
	76	12	Reserved		RI Read Back, RI[5:0]						
	77	13	Reserved		RQ Read Back, RQ[5:0]						
	78	14	Reserved					Viterbi Code Rate[2:0]			
	79	15	Reed-Solomon False Lock Uncorrected Error Count low byte, UECFL[7:0]								
	80	16	Reed-Solomon False Lock Uncorrected Error Count high byte, UECFL[15:0]								
	81[7]	17	uC_Status_byte4 [7:0]								
	82	18	uC_Status_byte3 [7:0]								
	83	19	uC_Status_byte2 [7:0]								
	84	20	uC_Status_byte1 [7:0]								
	85	21	uC_Status_byte0 [7:0]								
	86	22	Demod SNR Estimate, SNR[7:0]								
	87	23	Reserved				Demod SNR Estimate, SNR[11:8]				
Group 4	128	0	en	tstn	PLL_N[5:0]						R/W
	129	1	iddtn	cnt_outl	PLL_S[5:0]						
	130	2	IMQ	DVB_DSS	QB	PLL_T[4:0]					
	131	3	Viterbi Code Rate[2:0]			TEI	SYNC2_MOD	Sync1 Override	PLL_M[1:0]		

(Sheet 2 of 5)

Table E.2 Microcontroller Address Map (Cont.)

	µC_ADD	µP_APR	D7	D6	D5	D4	D3	D2	D1	DO	R/W by µC
Group 4 (Cont.)	132	4	Viterbi Max Data Bit Count, VMDC1[7:0]								R/W
	133	5	Viterbi Max Data Bit Count 2, VMDC2[7:0], low byte								
	134	6	Viterbi Max Data Bit Count 2, VMDC2[15:8], middle byte								
	135	7	Viterbi Max Data Bit Count 2, VMDC2[23:16], high byte								
	136	8	Viterbi Maximum Bit Error Count[7:0], Rate 1/2								
	137	9	Viterbi Maximum Bit Error Count[7:0], Rate 2/3								
	138	10	Viterbi Maximum Bit Error Count[7:0], Rate 3/4								
	139	11	Viterbi Maximum Bit Error Count[7:0], Rate 5/6								
	140	12	Viterbi Maximum Bit Error Count[7:0], Rate 6/7								
	141	13	Viterbi Maximum Bit Error Count[7:0], Rate 7/8								
	142	14	Synchronization Word[7:0]								
	143	15	BER	Auto Rate	Ber_ Nor	New_ Ber	IMQ_ EN	DI_By pass	L[1:0]		
	144	16	BF	Sync2 Freeze	Sync Status Select, SSS[1:0]		Sync States Acq, SSA [1:0]		Sync States Track, SST[1:0]		
	145	17	Sync_ Step	Sync2 RST Enable	OF	Output Selector, OS[4:0]					
	146	18	PLL_RESET								
	147	19	DF_Select[2:0]			DF_Gain[1:0]		DF_Ratio[2:0]			
	148	20	Dem_ BP	ST1_ BP	RAM Test	PD				MF_ 20_35	
	149	21	PCLK_ INV	PLL_ BP	Res.	CLK_DIV1[4:0]					
	150	22	CLK_DIV2[7:0]								
	151	23	Reserved]			CLK_DIV2[12:8]					
	152	24	PWR_REF[7:0]								
	153	25	Reserved					INT_ DC	PWR_BW [1:0]		
	154	26	Scale factor for DEMI, DEMQ, SCALE[7:0]								
	155	27	SNR Estimator Threshold, SNR_THS[7:0]								
	156	28	Carrier Loop Lambda, CAR_LAMBDA_SEL[3:0]				Carrier Loop Mu, CAR_MU_SEL[3:0]				
	157	29	Carrier Phase Lock Detector Threshold, CAR_LC_THSL[7:0]								

(Sheet 3 of 5)

Table E.2 Microcontroller Address Map (Cont.)

	µC_ADD	µP_APR	D7	D6	D5	D4	D3	D2	D1	DO	R/W by µC
Group 4 (Cont.)	158	30	Carrier Frequency Lock Detector Threshold, CAR_LCF_THSL[7:0]								R/W
	159	31	Reserved			Carrier Frequency Lock Detector Threshold, CAR_LCF_THSL[12:8]					
	160	32	Carrier Sweep Rate, CAR_SWR[7:0]								
	161	33	Carrier Sweep Rate, CAR_SWR[15:8]								
	162	34	Carrier Upper Sweep Limit, CAR_USWL[7:0]								
	163	35	Carrier Upper Sweep Limit, CAR_USWL[15:8]								
	164	36	Carrier Lower Sweep Limit, CAR_LSWL[7:0]								
	165	37	Carrier Lower Sweep Limit, CAR_LSWL[15:8]								
	166	38	Carrier Loop Filter Initialization, CAR_LF_INIT[7:0]								
	167	39	Carrier Loop Filter Initialization, CAR_LF_INIT[15:8]								
	168	40	Carrier Loop Filter Initialization, CAR_LF_INIT[23:16]								
	169	41	CAR_ SWP_ SWAP	CAR_ ERROR _SWAP	CAR_ Auto_ SWP	AGC_ Input_ sel	Tim_ jit_flr_ en	CAR_ PE_ SEL	CAR_ Open	CAR_ SW	
	170	42	Clock Loop Lambda, CLK_LAMBDA_SEL[3:0]				Clock Loop Mu, CLK_MU_SEL[3:0]				
	171	43	Clock Sweep Rate, CLK_SWR[7:0]								
	172	44	Clock Sweep Rate, CLK_SWR[15:8]								
	173	45	Clock Upper Sweep Limit, CLK_USWL[7:0]								
	174	46	Clock Upper Sweep Limit, CLK_USWL[15:8]								
	175	47	Clock Lower Sweep Limit, CLK_LSWL[7:0]								
	176	48	Clock Lower Sweep Limit, CLK_LSWL[15:8]								
	177	49	Clock Loop Bias, CLK_BIAS[7:0]]								
	178	50	Clock Loop Bias, CLK_BIAS[15:8]								
	179	51	Clock Loop Bias, CLK_BIAS[23:16]								
	180	52	Res	Clock Loop Bias, CLK_BIAS[30:24]							
	181	53	CLK_ SWP_ SWAP	CLK_ ERROR _SWAP	CLK_ Auto_ SWP	CLK_LC_THSL [1:0]		CLK_ PE_ SEL	CLK_ Open	CLK_ SW	
	182	54	SNR_ EST	PWRP_ TRI	ADC_ PD	FP_ LOCK _LEN	PWRP	F_ Lock_ Test	TED_ Sym_ SWP	CLK_ ALPH A_ SEL	

(Sheet 4 of 5)

Table E.2 Microcontroller Address Map (Cont.)

	µC_ADD	µP_APR	D7	D6	D5	D4	D3	D2	D1	DO	R/W by µC
Group 4 (Cont.)	183	55	ADC_ BPS	OB_2C	External Control Output Bits, XCTR[3:0]				DEM OD_ RST	FEC_ RST	R/W
	184	56	Reed-Solomon Max Block Count[7:0]								
	185	57	RSUBC_Threshold[7:0]								
	186	58	ADC_ Test_ EN	ADC_ Test_ start	Res.	FIFO_Depth[4:0]					
	187	59	Serial Transmission Start Data, TXSD[6:0]							Res.	
	188	60	Serial Transmission Data, TXD[7:0]								
	189	61	Serial Transmission End Data, TXED[7:0]								
	190	62	Serial_ B	Serial_C[1:0]		Reserved				Serial _A	
	191										

(Sheet 5 of 5)

1. Scratch Pad registers reside physically within the µController module.
2. LP_status[i] = 1 if Loop control register LPi = 0.
3. Acc_status[2] = 1 if µC accumulator < 0, Acc_status[1] = 1 if µC accumulator >= 0, Acc_status[0] = 1 if µC accumulator = 0.
4. This register is mapped from Group 5 into µController scratchpad memory space so as to be readable by the microcode. Look at Chapter 3 of the L64724 Datasheet for more information.
5. The microcode assembler checks for accesses to unmapped addresses and writes to read-only addresses. It flags these instructions as illegal at assemble time.
6. This register resides physically within the µController module.
7. Registers 81-85 reside physically within the µController module.

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