



## ICs for Communications

Acoustic Echo Canceller

ACE

PSB 2170 Version 1.1

Data Sheet 01.98

<b>PSB 2170</b>		
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**1 Overview**

The PSB 2170 provides acoustic echo cancellation for analog and digital featurephones. The chip supports two IOM<sup>®</sup>-2 compatible channels and a dedicated interface to the PSB 4851 (dual codec). It is programmed by a simple four wire serial control interface. The PSB 2170 also supports a power down mode and provides interface pins to +5 V levels.

## Acoustic Echo Canceller PSB 2170

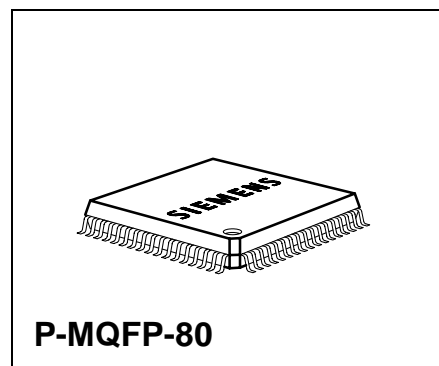
PSB 2170

Version 1.1

CMOS

### 1.1 Features

- Two modes of acoustic echo cancellation:
  - 20 dB ERLE @60 ms, <1 ms delay
  - 30 dB ERLE @70-200 ms, 38/43 ms delay
- Fast adaptation without learning tone
- Comfort noise generator
- Line echo cancellation without learning tone
- DMTF tone generation
- Flexible ringing generation
- Programmable side gain
- Transducer correction filters
- DTMF tone detector
- Call progress tone detector
- Caller ID decoder
- General purpose parallel port (16 bits)
- Independent gain for all channels
- Serial control interface for programming
- 3.3V power supply, 5V interface
- IOM<sup>®</sup>-2 interface
- Interface to PSB 4851
- Interface to Burst Mode Controllers



Type	Ordering Code	Package
PSB 2170		P-MQFP-80

1.2 Pin Configuration  
(top view)

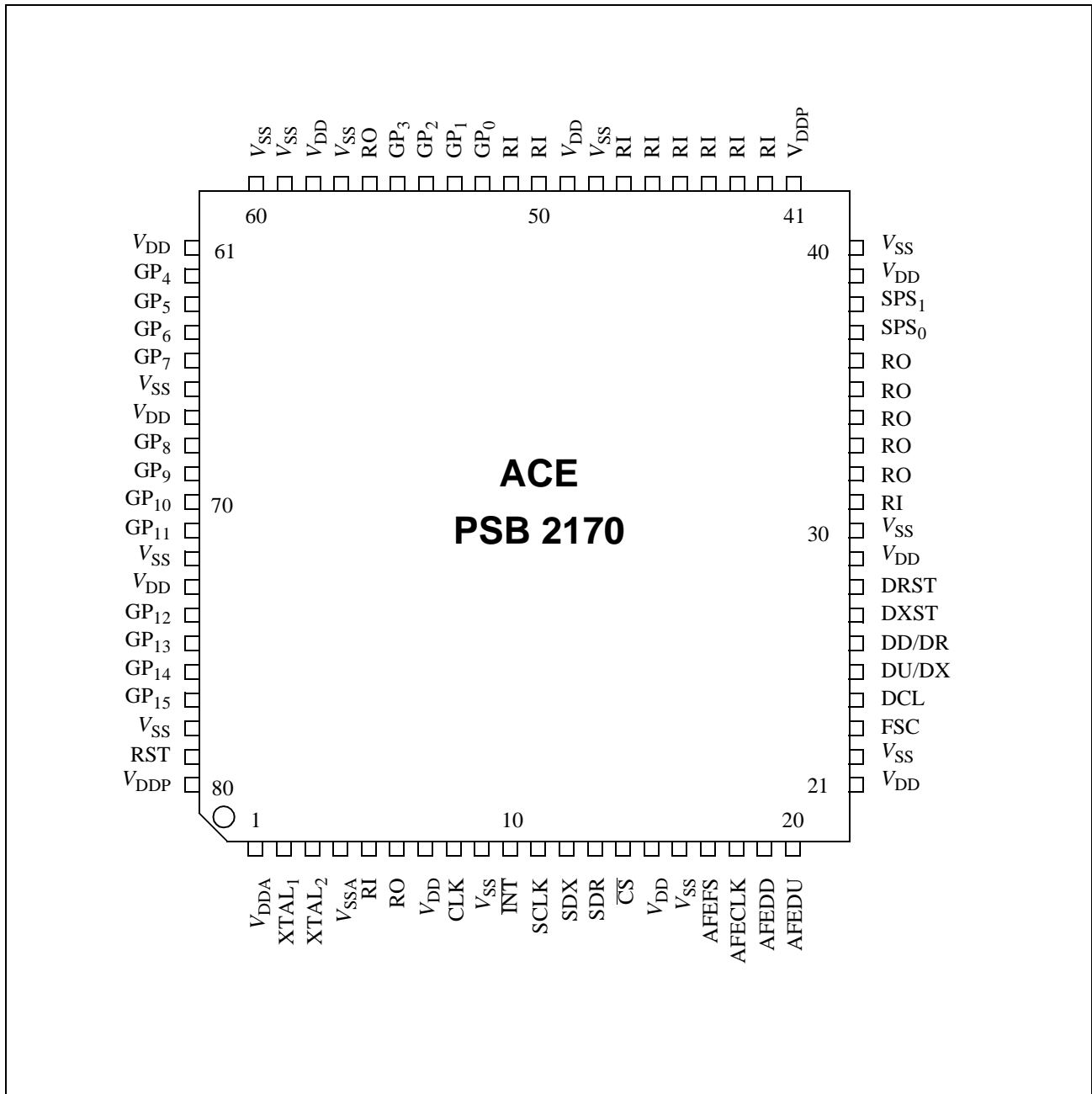


Figure 1 Pin Configuration

### 1.3 Pin Definitions and Functions

**Table 1 Pin Definitions and Functions**

Pin No. P-MQFP-80	Symbol	Dir.	Reset	Function
41, 80	$V_{DDP}$	-	-	<b>Power supply (5V <math>\pm</math>10 %)</b> Power supply for the interface.
7, 15, 21, 29, 39, 49, 58, 61, 67, 73	$V_{DD}$	-	-	<b>Power supply (3.3V <math>\pm</math>5 %)</b> Power supply for logic.
1	$V_{DDA}$	-	-	<b>Power supply (3.3V <math>\pm</math>5 %)</b> Power supply for clock generator.
4	$V_{SSA}$	-	-	<b>Power supply (0 V)</b> Power supply for clock generator.
9, 16, 22, 30, 40, 48, 57, 59, 60, 78, 66, 72	$V_{SS}$	-	-	<b>Power supply (0 V)</b> Ground for logic and interface.
17	AFEFS	O	L	<b>Analog Frontend Frame Sync:</b> 8 kHz frame synchronization signal for communication with the analog frontend.
18	AFECLK	O	L	<b>Analog Frontend Clock:</b> Clock signal for the analog frontend (6.912 MHz).
19	AFEDD	O	L	<b>Analog Frontend Data Downstream:</b> Data output to the analog frontend.
20	AFEDU	I	-	<b>Analog Frontend Data Upstream:</b> Data input from the analog frontend.
79	RST	I	-	<b>Reset:</b> Active high reset signal.
23	FSC	I	-	<b>Data Frame Synchronization:</b> 8 kHz frame synchronization signal (IOM <sup>®</sup> -2 and SSDI mode).
24	DCL	I	-	<b>Data Clock:</b> Data Clock of the serial data interface.

Table 1 Pin Definitions and Functions

26	DD/DR	I/OD I	-	<b>IOM<sup>®</sup>-2 Compatible Mode:</b> Receive data from IOM <sup>®</sup> -2 controlling device. <b>SSDI Mode:</b> Receive data of the strobed serial data interface.
25	DU/DX	I/OD O/ OD	-	<b>IOM<sup>®</sup>-2 Compatible Mode:</b> Transmit data to IOM <sup>®</sup> -2 controlling device. <b>SSDI Mode:</b> Transmit data of the strobed serial data interface.
27	DXST	O	L	<b>DX Strobe:</b> Strobe for DX in SSDI interface mode.
28	DRST	I	-	<b>DR Strobe:</b> Strobe for DR in SSDI interface mode.
14	$\overline{CS}$	I	-	<b>Chip Select:</b> Select signal of the serial control interface (SCI).
11	SCLK	I	-	<b>Serial Clock:</b> Clock signal of the serial control interface (SCI).
13	SDR	I	-	<b>Serial Data Receive:</b> Data input of the serial control interface (SCI).
12	SDX	O/ OD	H	<b>Serial Data Transmit:</b> Data Output of the serial control interface (SCI).
10	$\overline{INT}$	O/ OD	H	<b>Interrupt</b> New status available.
8	CLK	I	-	<b>Alternative AFCLK Source</b> 13,824 MHz
2 3	XTAL <sub>1</sub> XTAL <sub>2</sub>	I O	- Z	<b>Oscillator:</b> XTAL <sub>1</sub> : External clock or input of oscillator loop. XTAL <sub>2</sub> : output of oscillator loop for crystal.
37 38	SPS <sub>0</sub> SPS <sub>1</sub>	O O	L L	<b>Speakerphone State:</b> Current speakerphone unit state, general purpose outputs or status register output

Table 1 Pin Definitions and Functions

52	GP <sub>0</sub>	I/O	L <sup>1)</sup>	<b>General Purpose Parallel Port 0-15:</b> General purpose I/O.
53	GP <sub>1</sub>	I/O	L	
54	GP <sub>2</sub>	I/O	L	
55	GP <sub>3</sub>	I/O	L	
62	GP <sub>4</sub>	I/O	L	
63	GP <sub>5</sub>	I/O	L	
64	GP <sub>6</sub>	I/O	L	
65	GP <sub>7</sub>	I/O	L	
68	GP <sub>8</sub>	I/O	L	
69	GP <sub>9</sub>	I/O	L	
70	GP <sub>10</sub>	I/O	L	
71	GP <sub>11</sub>	I/O	L	
74	GP <sub>12</sub>	I/O	L	
75	GP <sub>13</sub>	I/O	L	
76	GP <sub>14</sub>	I/O	L	
77	GP <sub>15</sub>	I/O	L	
6, 32, 33, 34, 35, 36, 56	RO	O	-	<b>Reserved Output:</b> Do not connect.
5, 31, 42, 43, 44, 45, 46, 47, 50, 51	RI	I	-	<b>Reserved Input:</b> Connect to V <sub>SS</sub> .

<sup>1)</sup> These lines are driven low with 20 µA during reset.

1.4 Logic Symbol

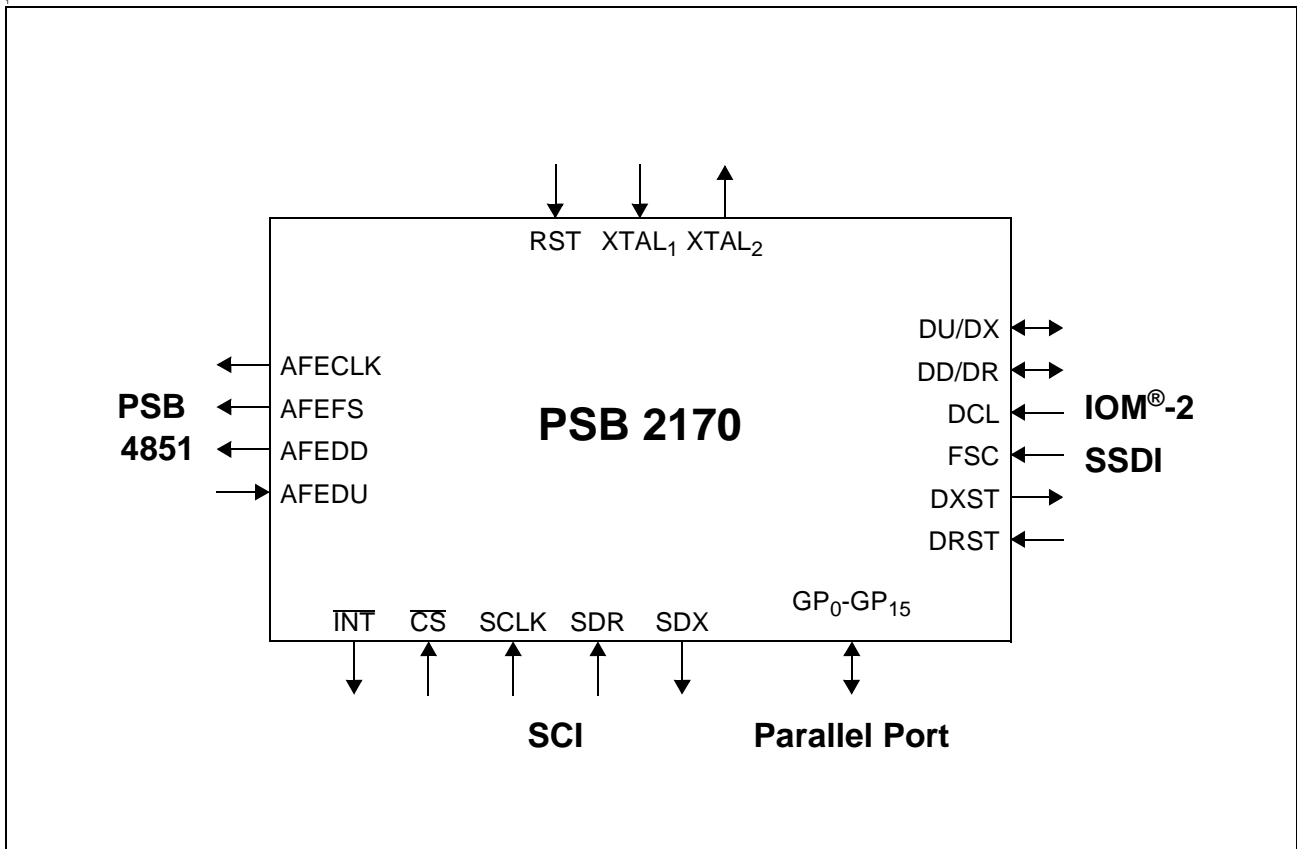


Figure 2 Logic Symbol

1.5 Functional Block Diagram

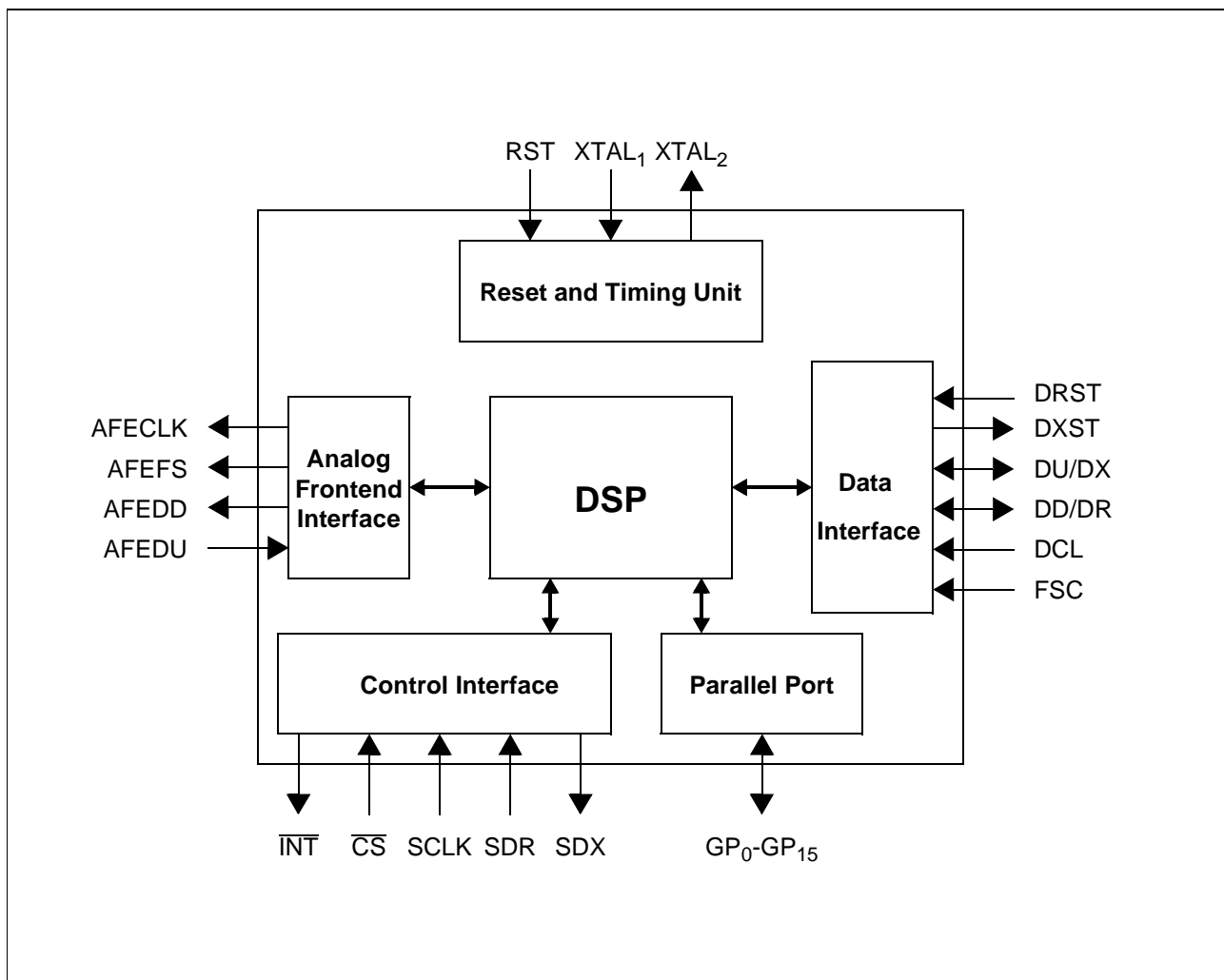


Figure 3 PSB 2170 - Block Diagram

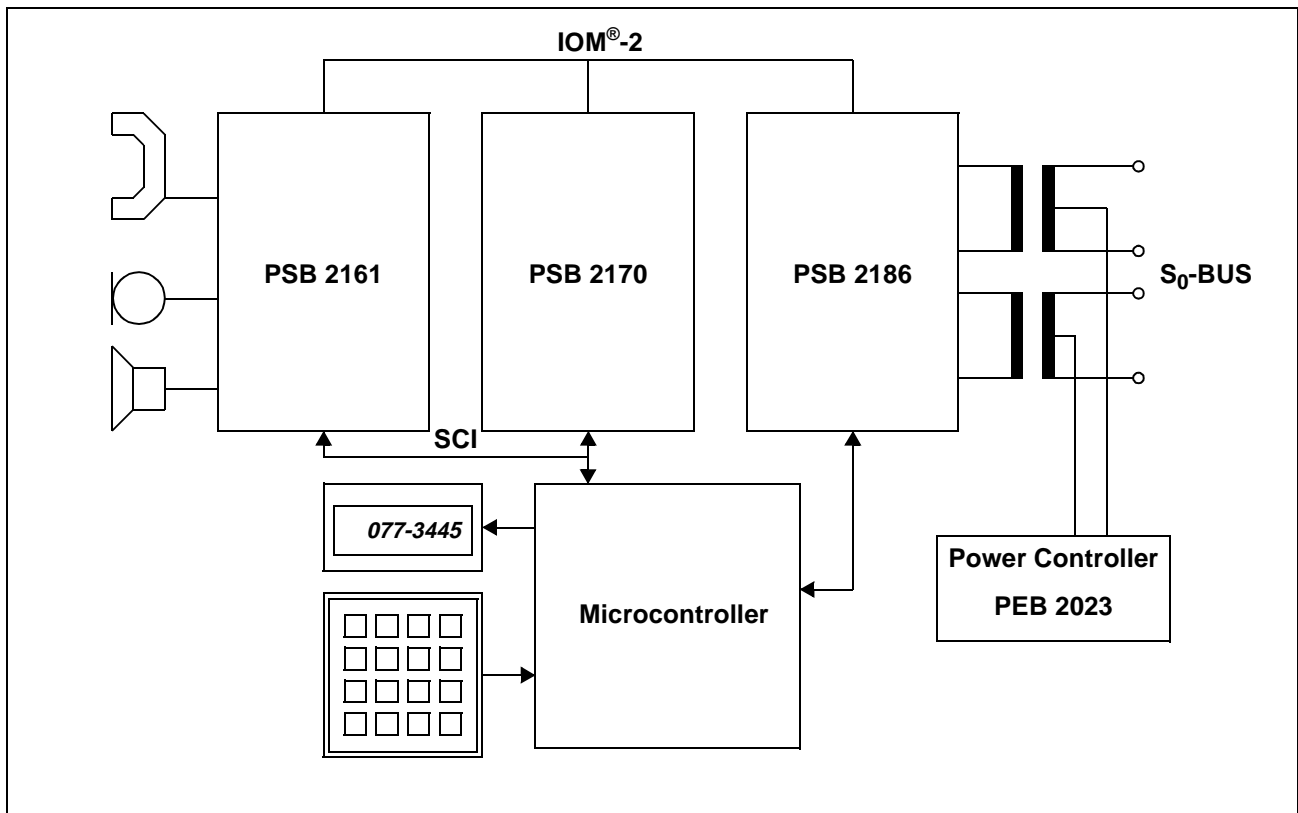


**1.6 System Integration**

The PSB 2170 provides a full duplex speakerphone in a variety of applications. Some examples are outlined below.

**1.6.1 Full Duplex Featurephone for ISDN Terminal**

Figure 4 shows an ISDN featurephone with the PSB 2170 providing a full duplex speakerphone.



**Figure 4 Full Duplex Featurephone for ISDN Terminal**

1.6.2 DECT Basestation with Full Duplex Featurephone

Figure 5 shows a DECT basestation with acoustic echo cancellation based on the PSB 2170. The full duplex featurephone can be switched to the basestation or a mobile handset dynamically. For programming the serial control interface (SCI) is used while voice data is transferred via the strobed serial data interface (SSDI).

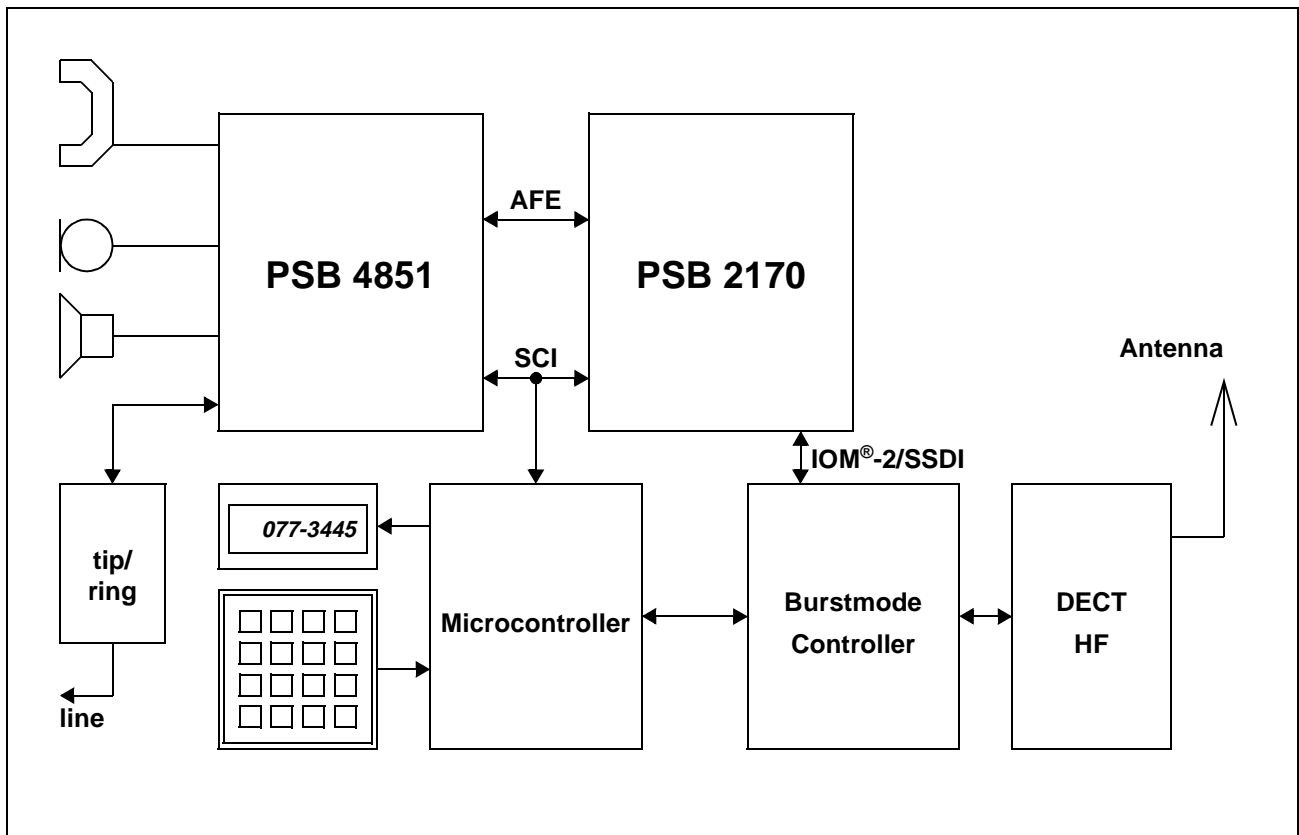


Figure 5 DECT Basestation with Full Duplex Speakerphone

1.6.3 H.320 Videophone with Full Duplex Speakerphone (3.4 KHz audio)

As shown in figure 6 the PSB 2170 can be used to provide a full duplex speakerphone solution for a videophone with 3.4 KHz bandwidth.

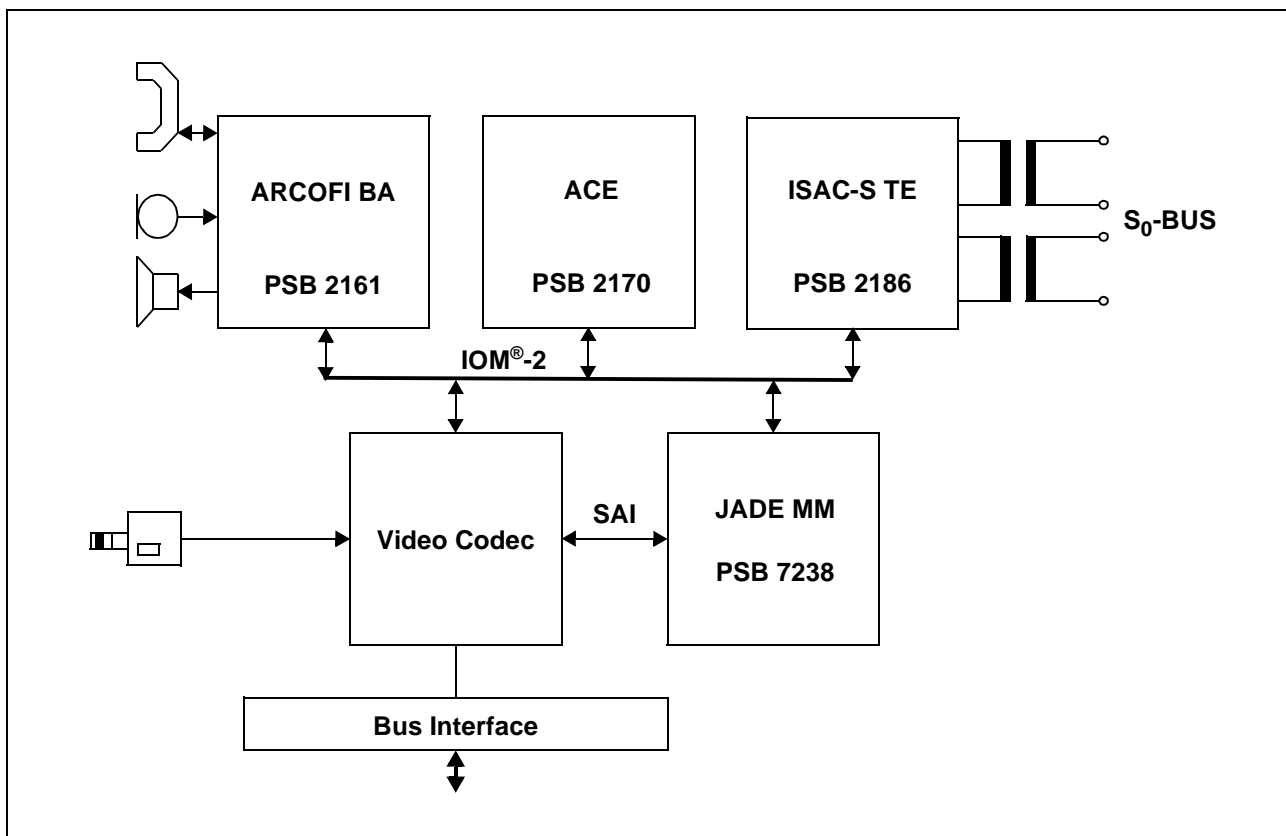


Figure 6 Videophone (ISDN, 3.4 KHz audio)

In transmit direction the ARCOFI BA (PSB 2161, analog frontend with 8 KHz sampling rate) in combination with the acoustic echo canceller (PSB 2170) provides the uncompressed audio data from the microphone via IOM-2. The IOM-2 timeslots could be assigned as shown in table 2.

Table 2 Time Slot Assignment for Videophone Application

Logical Connection	Bit Width	Physical Channel	Timeslot Name
2161 <-> 2170	16	IOM Channel 1	IC1/IC2
2170 <-> 7238	16	IOM Channel 2	IC3/IC4
Vid. Codec <-> 2186	2*8	IOM Channel 0	B1,B2

The data is compressed by the JADE (PSB 7280) or alternatively by the JADE MM (PSB 7238), multiplexed into the audio/video data stream by the video codec and sent to the line by the ISAC-S TE (PSB 2186). In receive direction the video codec demultiplexes

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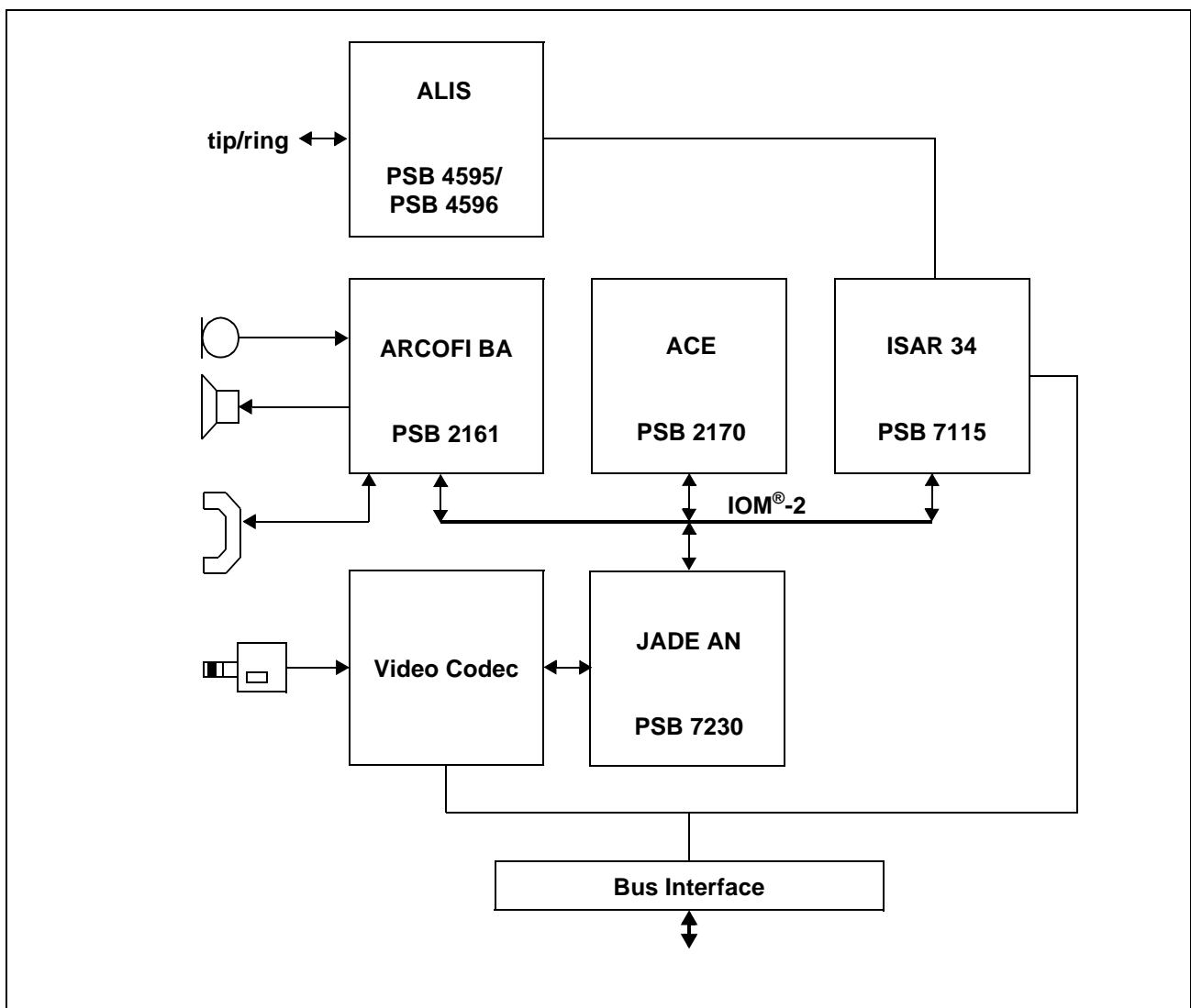
**Overview**

the compressed audio data from the data stream delivered by the ISAC-S TE (PSB 2186). If desired it also introduces a delay to achieve lip synchronization. The compressed data is sent to the JADE/JADE MM which in turn sends the audio data after decompression to the ACE (PSB 2170) which then sends the data to the ARCOFI BA (PSB 2161).

**1.6.4 H.324 Videophone with Full Duplex Speakerphone (3.4 KHz audio)**

For an analog videophone the PSB 2170 provides a full duplex speakerphone according to figure 7.

A discrete modem frontend (DAA, data access arrangement) is different depending on the country where the application shall be used. Thus, although cheap in terms of bill of material, a logistic overhead is necessary to address a world-wide market since several different versions have to be produced. A solution for this problem is also shown in figure 7 using the Siemens Analog Line Interface Solution (ALIS, PSB 4595/4596) chipset. With the ALIS the country specific requirements like DC characteristics and impedance matching can be met by simply programming registers.



**Figure 7 H.324 Videophone (3.4 KHz audio)**

In transmit direction the PSB 2161 (ARCOFI BA) provides the uncompressed audio data from the microphone to the acoustic echo canceller (PSB 2170). The acoustic echo

---

**Overview**

canceller provides the echo-free data to the audio compression device JADE AN (Joint Audio Decoder/Encoder for analog applications, PSB 7230). The data is then compressed by the JADE AN and multiplexed into the audio/video data stream by the video codec. The video codec in turn sends the combined data for modulation to the ISAR 34 (PSB 7115) by the  $\mu$ -controller. Finally the ISAR 34 sends the data to the ALIS (PSB 4595/4596) which passes it unmodified to the analog telephone line. In receive direction the same signal path is used in the other direction.

The ALIS chipset is a programmable solution for codec and DAA. It can be configured by software to meet the requirements of the different countries, thus offering one hardware solution for all countries. The potential separation is done by capacitors instead of transformers.

1.6.5 Videophone with External Line Interface

A videophone using an external line interface with the PSB 2170 providing a full duplex speakerphone is shown in figure 8.

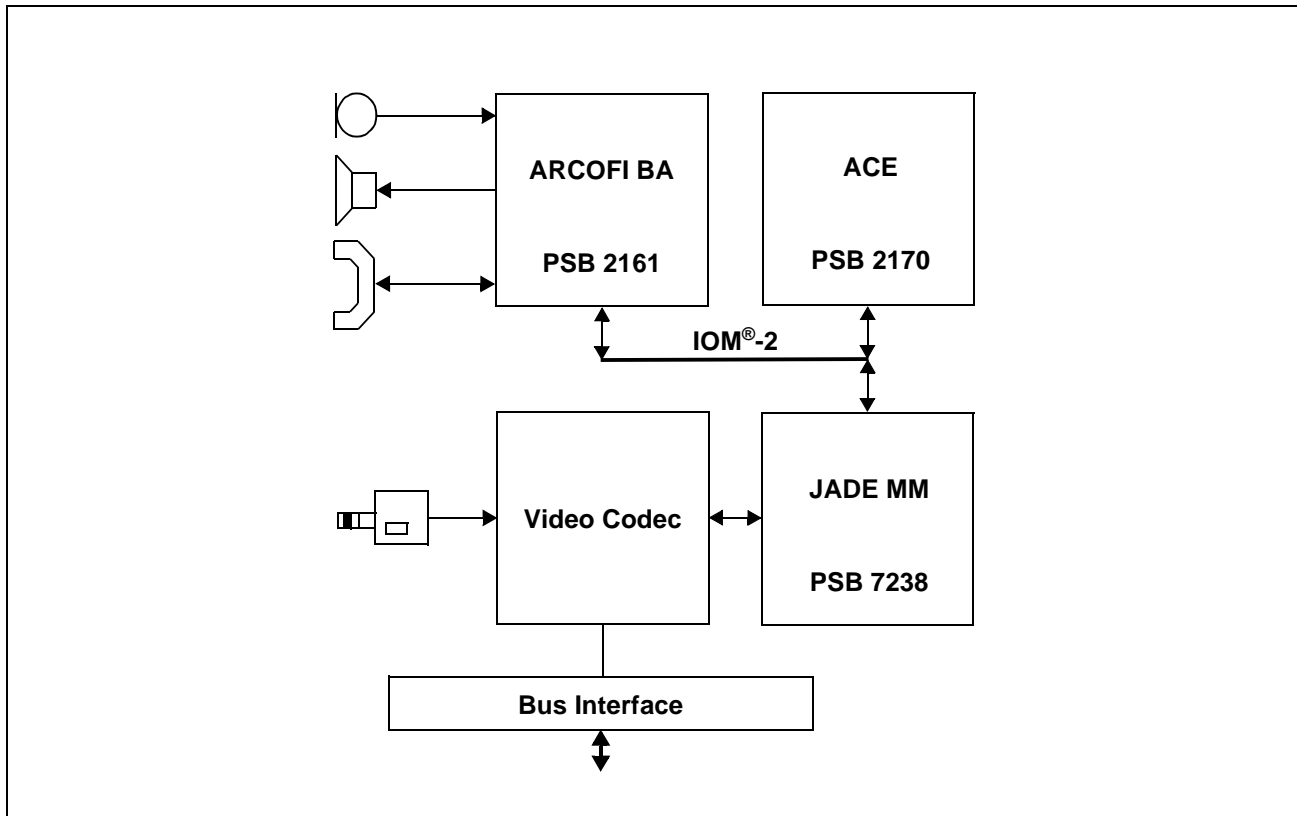


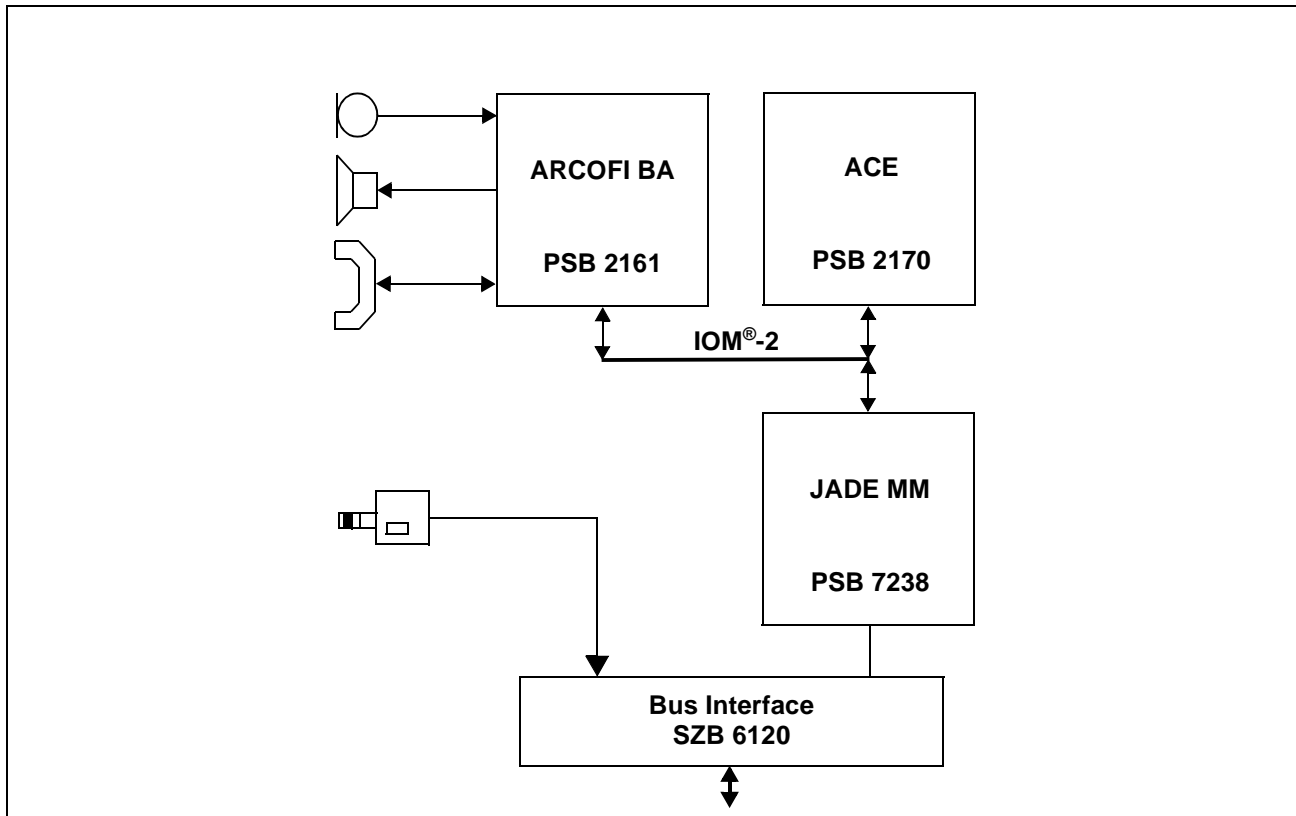
Figure 8 Videophone with External Line Interface (Hardware Video Codec)

In transmit direction the PSB 2161 (ARCOFI BA) provides the uncompressed audio data from the microphone to the acoustic echo canceller (PSB 2170). The acoustic echo canceller provides the echo-free data to the audio compression device JADE MM (PSB 7238). The JADE MM offers all necessary compression algorithms to cover H.320/323/324 applications, i.e. ITU-T G.711, G.722, G.723 and G.728. The compressed data is then multiplexed into the audio/video data stream by the video codec. The video codec in turn sends the combined data via the bus interface to a host unit (e.g. the CPU in a PC) which passes it to the line interface (e.g. ISAC-S TE for ISDN, V.34bis modem for POTS or an Ethernet adapter for LAN). In receive direction the same signal path is used in the other direction.

The off-board line interface offers the advantage of one videophone board applicable to different lines such as ISDN (H.320), LAN (H.323) or POTS (H.324, plain old telephone system) by just exchanging the line interface card and some control software on the PC.

### 1.6.6 Videophone with Software Video Compression

A videophone using software video compression with the PSB 2170 providing a full duplex speakerphone is shown in figure 8.



**Figure 9 Videophone with External Line Interface (Software Video Codec)**

In transmit direction the PSB 2161 (ARCOFI BA) provides the uncompressed audio data from the microphone to the acoustic echo canceller (PSB 2170). The acoustic echo canceller provides the echo-free data to the audio compression device JADE MM (PSB 7238). The JADE MM offers all necessary compression algorithms to cover H.320/323/324 applications, i.e. ITU-T G.711, G.722, G.723 and G.728. The compressed data is then transmitted to the host processor via the bus interface (e.g. using the Siemens PCI interface SZB 6120). The host processor also captures the uncompressed video data through the same bus interface and does the video compression and multiplexing by software. The multiplexed data stream is then passed to the corresponding line interface (e.g. ISAC-S TE for ISDN, V.34bis modem for POTS or an Ethernet adapter for LAN). In receive direction the same signal path is used in the other direction.

If only H.324 (POTS) videophones shall be supported, the JADE MM (PSB 7238) may be substituted by the JADE AN (PSB 7230), which offers only the ITU-T G.723.1 compression needed for H.324. A combi-design of JADE MM and JADE AN is also possible, thus offering both solutions by assembly options. See JADE AN data sheet for details.



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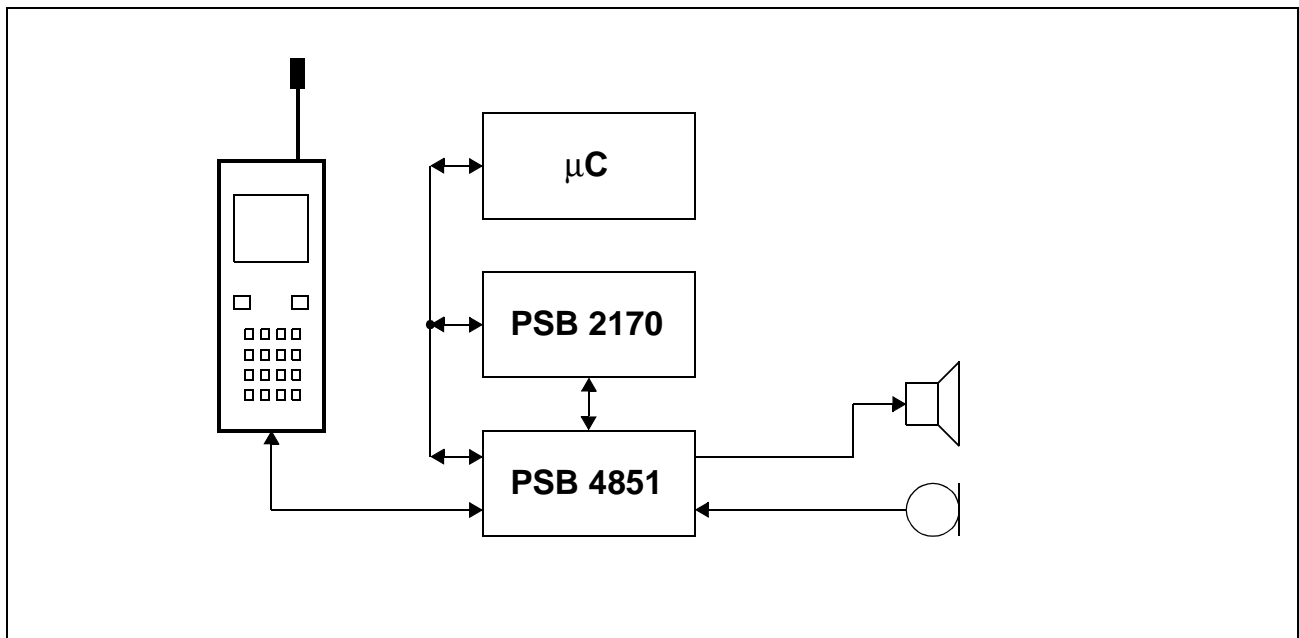
**Overview**

The off-board line interface offers the advantage of one videophone board applicable to different lines such as ISDN (H.320), LAN (H.323) or POTS (H.324, plain old telephone system) by just exchanging the line interface card and some control software on the PC. Due to the limited computational power of the host processor (e.g. Intel Pentium), the video quality using software compression usually does not reach the quality of a separate video processor. Nevertheless, if accepted by the customer this offers a very low cost solution for videoconferencing.

**1.6.7 Full Duplex Speakerphone in Car Environment**

The PSB 2170 has special provisions for operation in noisy environments like cars. In this application the PSB 2170 can monitor the background noise and insert similar noise into the transmitted signal when necessary. This feature, called comfort noise generation, reduces unpleasant noise modulation.

Figure shows an application where the PSB 2170 provides a full duplex speakerphone for a mobile communications unit in a car.



**Figure 10 Full Duplex Speakerphone in Car Environment**

The PSB 2170 receives (transmits) analog data from (to) the mobile communications unit via the first codec of the PSB 4851. The microphone and the loudspeaker of the mobile communications unit are muted. Instead of them the loudspeaker and microphone mounted in the car are used. They are connected directly to the second channel of the PSB 4851.

2 Functional Units

The PSB 2170 contains several functional units that can be connected to either of the two interfaces (PSB 4851 and SSDI/IOM®-2) as necessary. Figure 11 shows the functional units available within the PSB 2170.

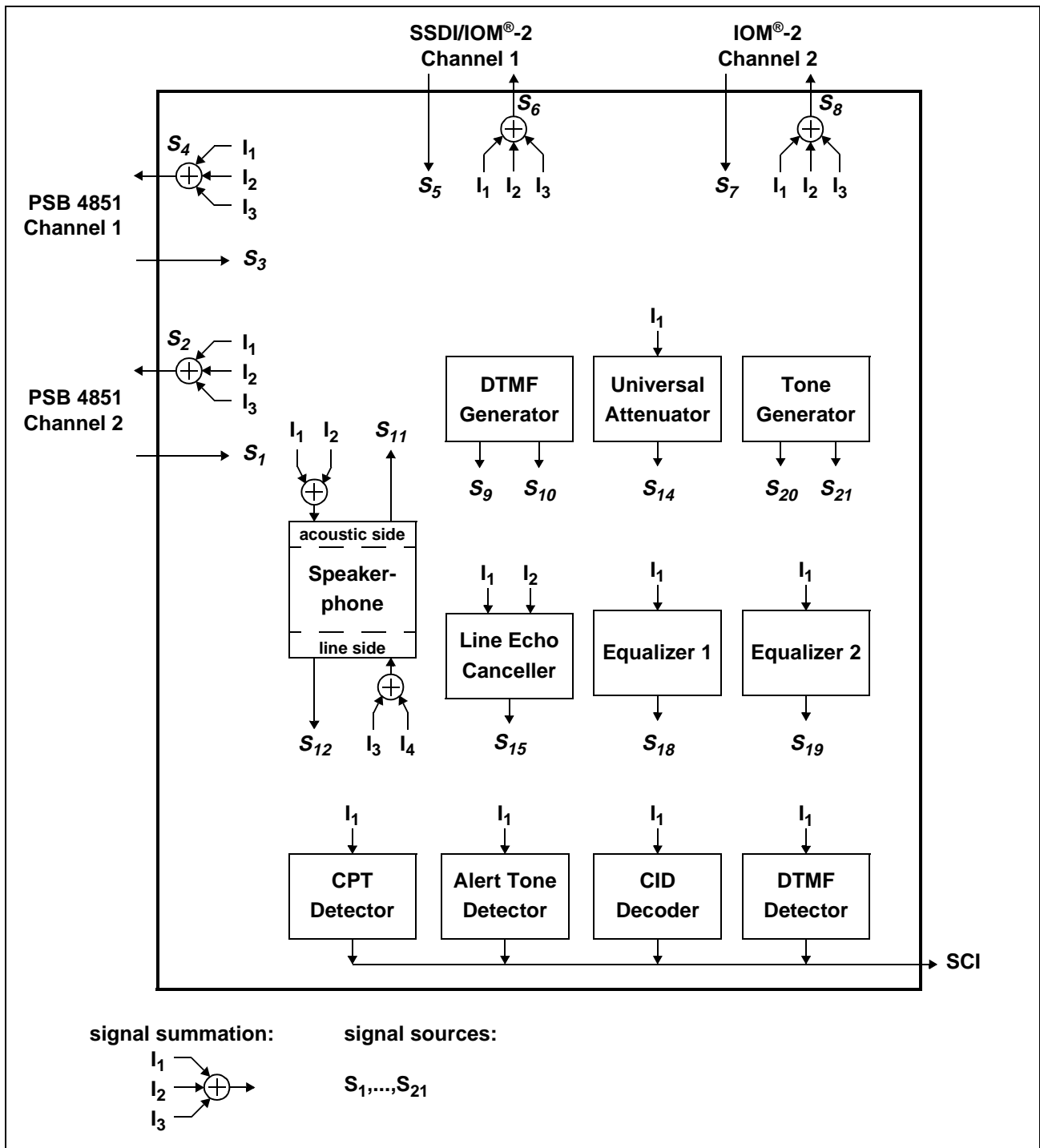


Figure 11 Functional Units - Overview

## Functional Units

Each unit has one or more signal inputs (denoted by I). Most units have at least one signal output (denoted by S). Any input I can be connected to any signal output S. In addition to the signals shown in figure 11 there is also the signal  $S_0$  (silence), which is useful at signal summation points. Table 3 lists the available signals within the PSB 2170 according to their reference points.

**Table 3 Signal Summary**

Signal	Description
$S_0$	Silence
$S_1$	Analog line input (Channel 1 of PSB 4851 interface)
$S_2$	Analog line output (Channel 1 of PSB 4851 interface)
$S_3$	Microphone input (Channel 2 of PSB 4851 interface)
$S_4$	Loudspeaker/Handset output (Channel 2 of PSB 4851 interface)
$S_5$	Serial interface input, Channel 1
$S_6$	Serial interface output, Channel 1
$S_7$	Serial interface input, Channel 2
$S_8$	Serial interface output, Channel 2
$S_9$	DTMF generator output
$S_{10}$	DTMF generator auxiliary output
$S_{11}$	Speakerphone output (acoustic side)
$S_{12}$	Speakerphone output (line side)
$S_{13}$	reserved
$S_{14}$	Universal attenuator output
$S_{15}$	Line echo canceller output
$S_{16}$	reserved
$S_{17}$	reserved
$S_{18}$	Equalizer 1 output
$S_{19}$	Equalizer 2 output
$S_{20}$	Tone generator output 1
$S_{21}$	Tone generator output 2

The following sections describe the functional units in detail.

Functional Description

2.1 Full Duplex Speakerphone

The speakerphone unit (figure 12) is attached to four signals (microphone, loudspeaker, line out and line in). The two input signals (microphone, line in) are preceded by a signal summation point.

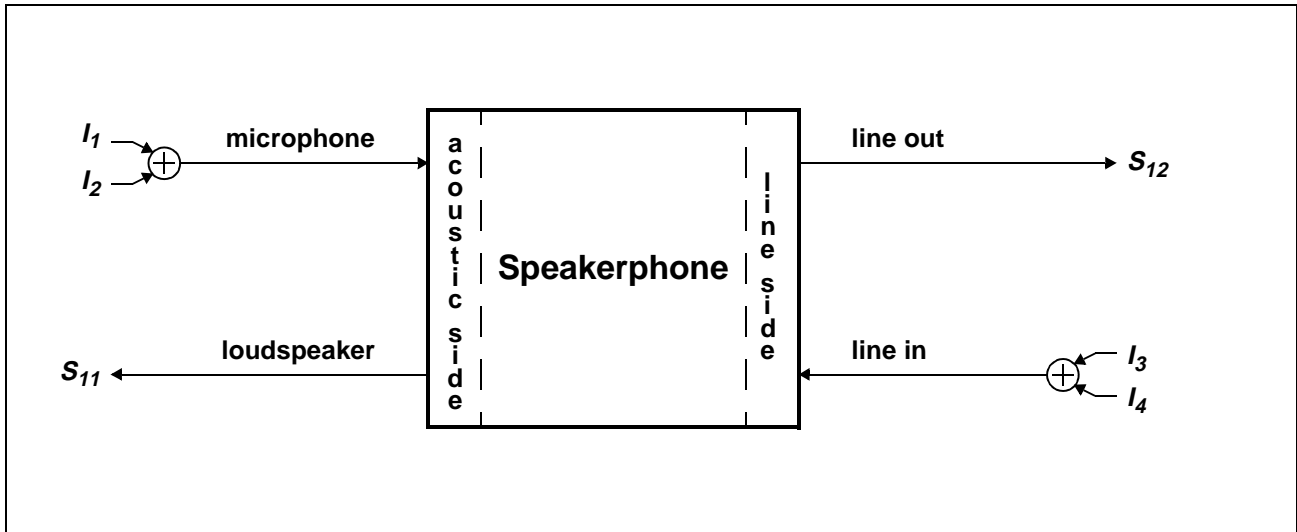


Figure 12 Speakerphone - Signal Connections

Internally, this unit can be divided into an echo cancellation unit and an echo suppression unit (figure 13). The echo cancellation unit provides the attenuation  $G_c$  while the echo suppression unit provides the attenuation  $G_s$ . The total attenuation ATT of the speakerphone is therefore  $ATT=G_c+G_s$ .

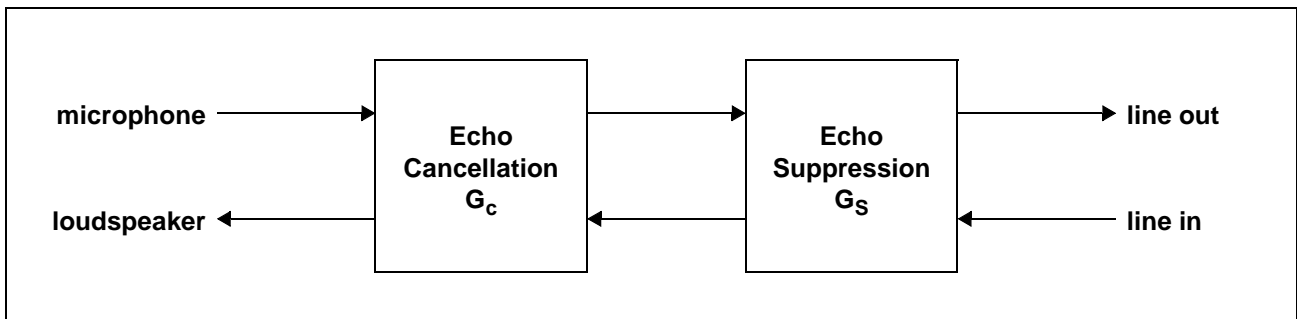


Figure 13 Speakerphone - Block Diagram

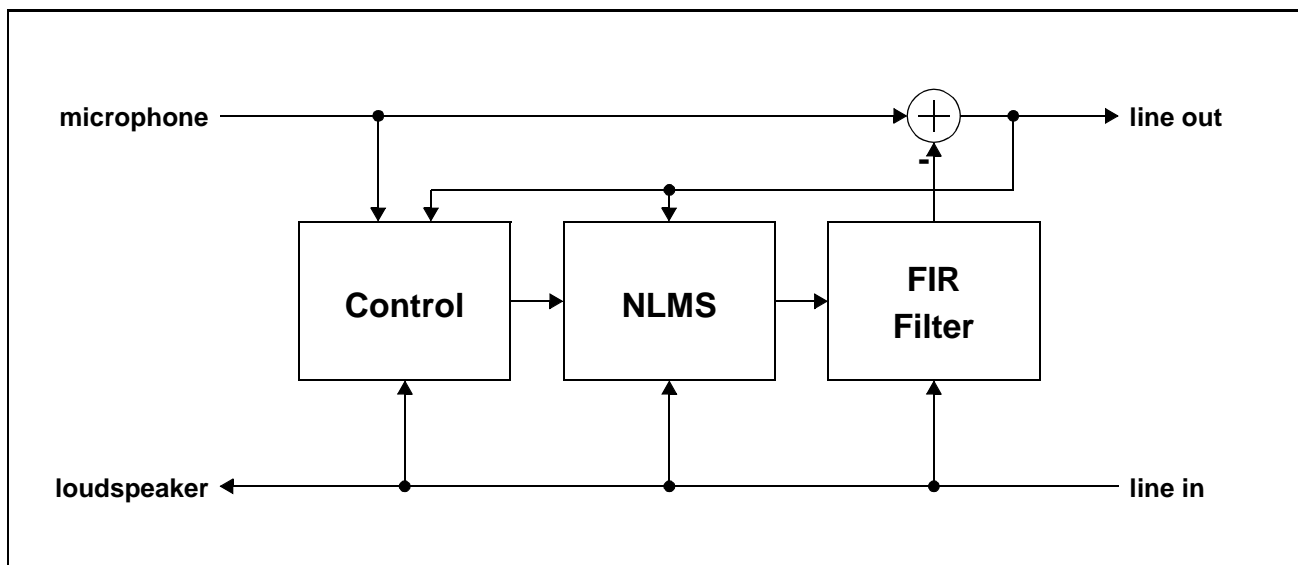
The echo suppression unit is used to provide additional attenuation if the echo cancellation unit cannot provide all of the required attenuation itself. The echo cancellation unit has two operating modes: fullband and subband mode. Table 4 shows the basic differences of the two modes.

**Table 4 Echo Cancellation Modes**

	fullband mode	subband mode
max. $G_c$	20 dB	30 dB
echo length	16-80 ms	>70_200 ms
delay	< 1 ms	38/43 ms

**2.1.1 Echo Cancellation (Fullband Mode)**

A simplified block diagram of the fullband echo cancellation unit is shown in figure 14.



**Figure 14 Echo Cancellation Unit (Fullband Mode) - Block Diagram**

The echo cancellation unit consists of an finite impulse response filter (FIR) that models the expected acoustic echo, an NLMS based adaptation unit and a control unit. The expected echo is subtracted from the actual input signal from the microphone. If the model is exact and the echo does not exceed the length of the filter, then the echo can be completely cancelled. However, even if this ideal state can be achieved for one given moment the acoustic echo usually changes over time. Therefore the NLMS unit continuously adapts the coefficients of the FIR filter. This adaptation process is steered by the control unit. As an example, the adaptation is inhibited as long as double talk is detected by the control unit. Furthermore the control unit informs the echo suppression unit about the achieved echo return loss.

Table 5 shows the registers associated with the echo cancellation unit in fullband mode.

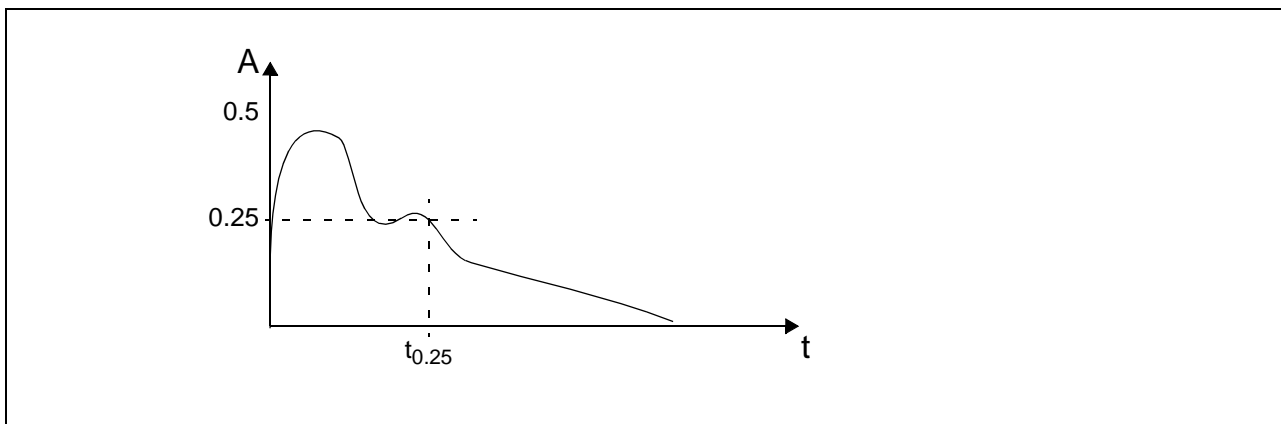
Functional Description

**Table 5 Echo Cancellation Unit Registers**

Register	# of Bits	Name	Comment
SAELEN	10	LEN	Length of FIR filter
SAEATT	15	ATT	Attenuation reduction during double-talk
SAEGS	3	GS	Global scale (all blocks)
SAEPS	3	AS	Partial scale (for blocks $\geq$ SAEPS2:FB)
SAEBL	3	FB	First block affected by partial scale

The length of the FIR filter can be varied from 127 to 639 taps (16 ms to 80 ms). The taps are grouped into blocks. Each block contains 64 taps.

The performance of the FIR filter can be enhanced by prescaling some or call of the coefficients of the FIR filter. A coefficient is prescaled by multiplying it by a constant. The advantage of prescaling is an enhanced precision and consequently an enhanced echo cancellation. The disadvantage is a reduced signal range. More precisely, if a coefficient at tap  $T_i$  is scaled by a factor  $C_i$  then the level of the echo (room impulse response) must not exceed  $Max/C_i$  (Max: Maximum PCM value). As an example figure shows a typical room impulse response.



**Figure 15 Echo Cancellation Unit - Typical Room Impulse Response**

First of all, the echo never exceeds 0.5 of the maximum value. Furthermore the echo never exceeds 0.25 of the maximum value after time  $t_{0.25}$ . Therefore all coefficients can be scaled by a factor of 2 and all coefficients for taps corresponding to times after  $t_{0.25}$  can be scaled a factor of 4.

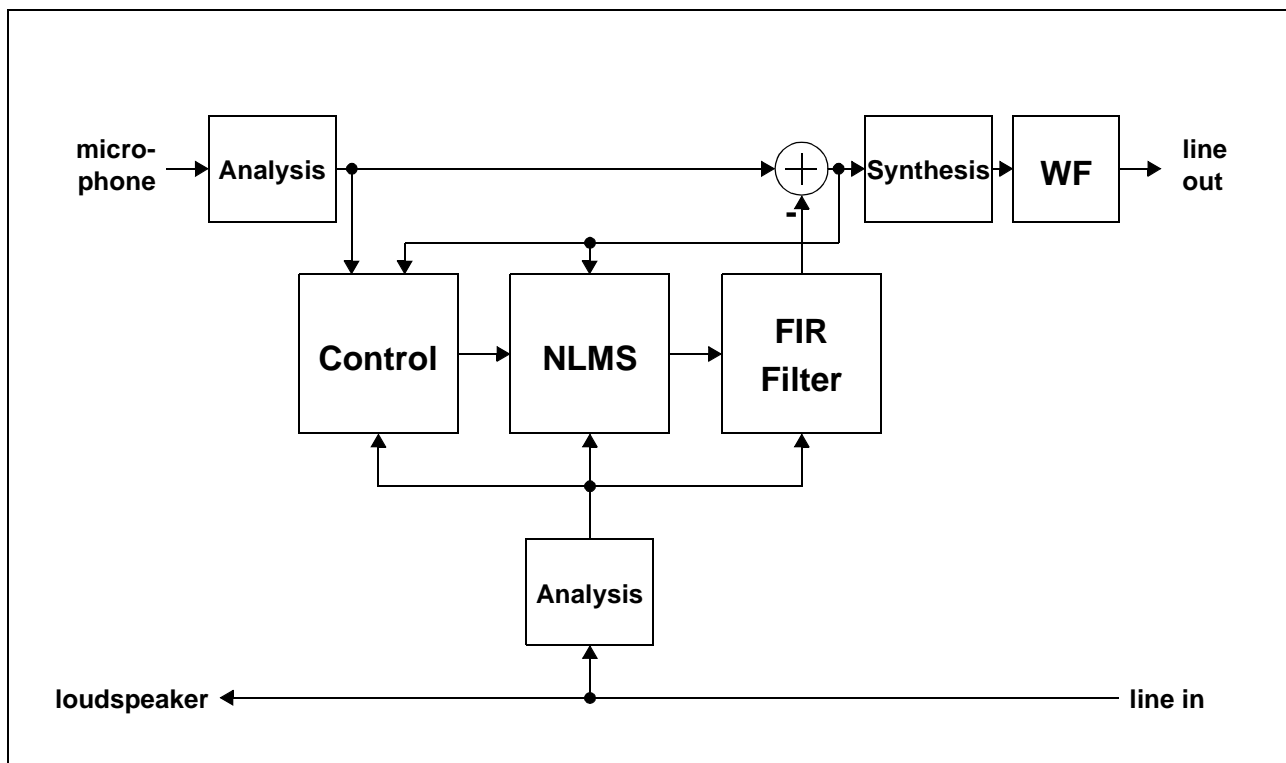
The echo cancellation unit provides three parameters for scaling coefficients. The first parameter (GS) determines a scale for all coefficients. The second parameter (FB) determines the first block for which an additional scale (PS) takes effect.

This feature can be used for different default settings like large or small rooms.

## Functional Description

## 2.1.2 Echo Cancellation (Subband Mode)

A simplified block diagram of the subband echo cancellation unit is shown in figure 16.



**Figure 16 Echo Cancellation Unit (Subband Mode) - Block Diagram**

With the exception of an additional (optional) Wiener filter the block diagram is identical to the fullband echo cancellation unit. The subband mode can be enabled in three different submodes. These submodes offer a trade-off between the maximum echo length and the functional units that can be run simultaneously (see chapter 3.6). All units that cannot be run simultaneously must be disabled before the subband echo cancellation unit can be enabled. After the subband echo cancellation unit is disabled, the parameters for the affected units must be rewritten by the microcontroller.

For the optional Wiener filter both the activation/deactivation time and the maximum attenuation can be programmed. If the Wiener filter is enabled, it is only active while there is no speech detected on the near side (microphone). The transition time from the inactive state to the active state (and vice versa) is determined by the parameter WFTIME.

Furthermore the maximum attenuation provided by the Wiener filter can be limited by the parameter WFLIMIT. As shown in figure 13 the total attenuation provided the speakerphone consists of the attenuation  $G_C$  (provided by the echo cancellation unit) and  $G_S$  (provided by the echo suppression unit). In subband mode the attenuation  $G_C$  is further split into  $G_A$  (provided by the adaptive filter) and  $G_W$  (provided by the Wiener filter).



## Functional Description

If  $G_A$  already exceeds WFLIMIT due to good adaptation then the Wiener filter is deactivated and  $G_C = G_A$ .

Otherwise WFLIMIT limits the attenuation  $G_W$  of the Wiener filter such that  $G_C = G_A + G_W$  never exceeds WFLIMIT.

Table 6 shows the registers associated with the subband echo cancellation unit.

**Table 6 Subband Mode Registers**

Register	# of Bits	Name	Comment
SCTL	2	EM	Echo cancellation mode (fullband, subband)
SCTL	1	EWFL	Wiener filter enable (subband only)
SAEWFT	15	TRTIME	Transition time of Wiener filter
SAEWFL	15	LIMIT	Wiener filter attenuation limit
SAEATT	15	ATT	Attenuation reduction during double-talk

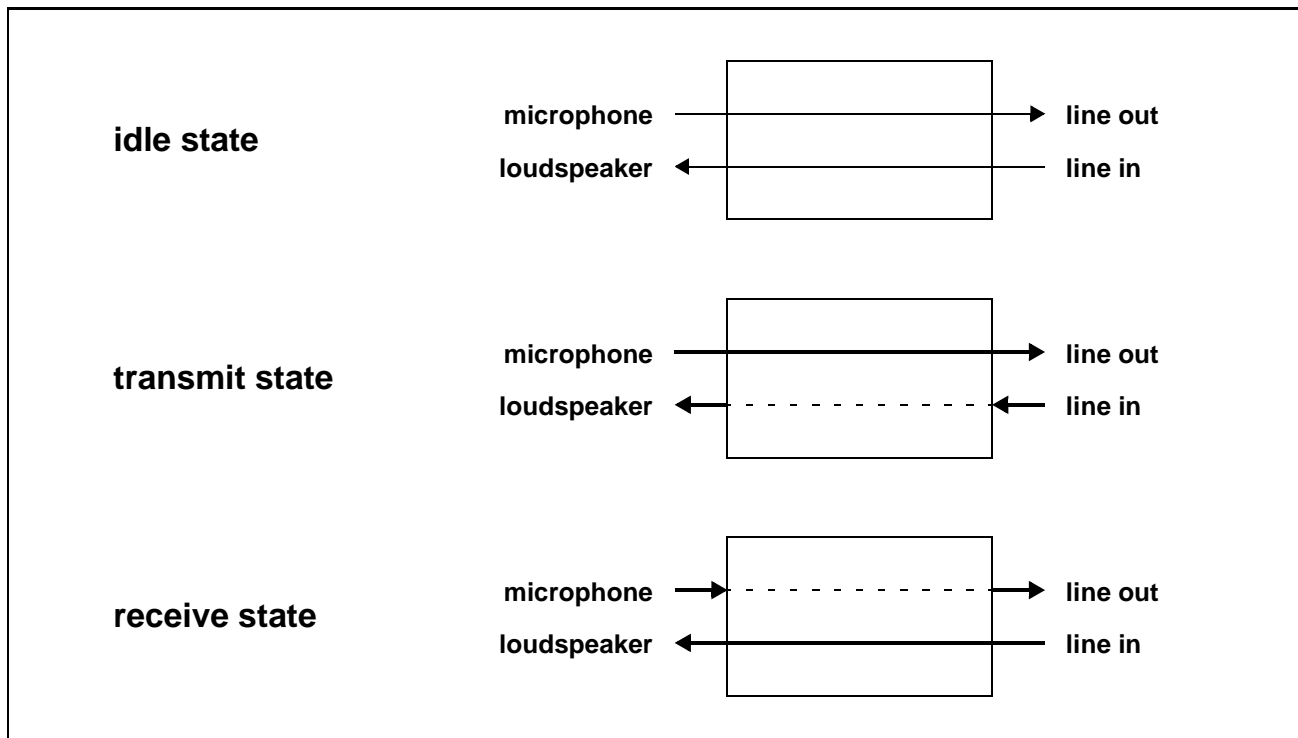
**Functional Description**

**2.1.3 Echo Suppression**

The echo suppression unit can be in one of three states:

- transmit state
- receive state
- idle state

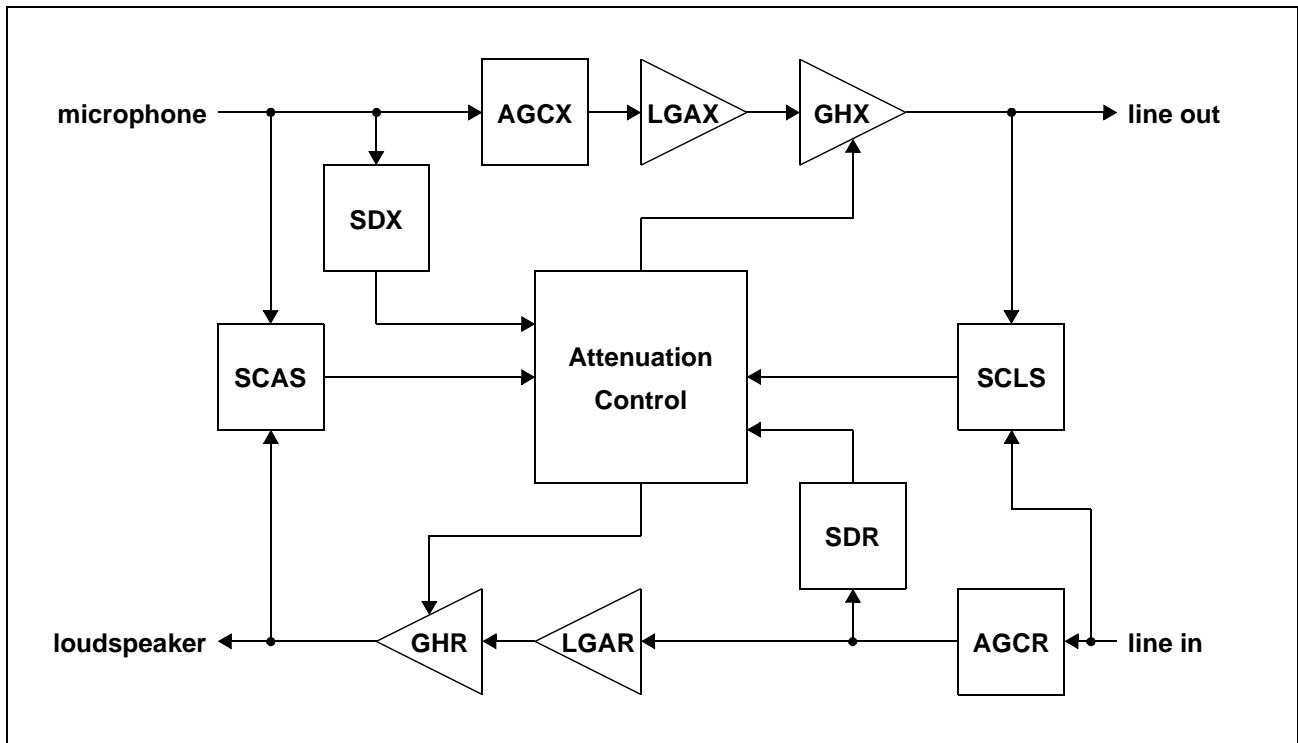
In transmit state the microphone signal drives the line output while the line input is attenuated. In receive state the loudspeaker signal is driven by the line input while the microphone signal is attenuated. In idle state both signal paths are active with evenly distributed attenuation.



**Figure 17 Echo Suppression Unit - States of Operation**

Functional Description

Figure18 shows the signal flow graph of the echo suppression unit in more detail.



**Figure 18 Echo Suppression Unit - Block Diagram**

State switching is controlled by the speech comparators (SCAS, SCL) and the speech detectors (SDX, SDR). The amplifiers (AGCX, AGCR, LGAX, LGAR) are used to achieve proper signal levels for each state. All blocks are programmable. Thus the telephone set can be optimized and adjusted to the particular geometrical and acoustical environment. The following sections discuss each block of the echo suppression unit in detail.

Functional Description

2.1.3.1 Speech Detector

For each signal source a speech detector (SDX, SDR) is available. The speech detectors are identical but can be programmed individually. Figure 19 shows the signal flow graph of a speech detector.

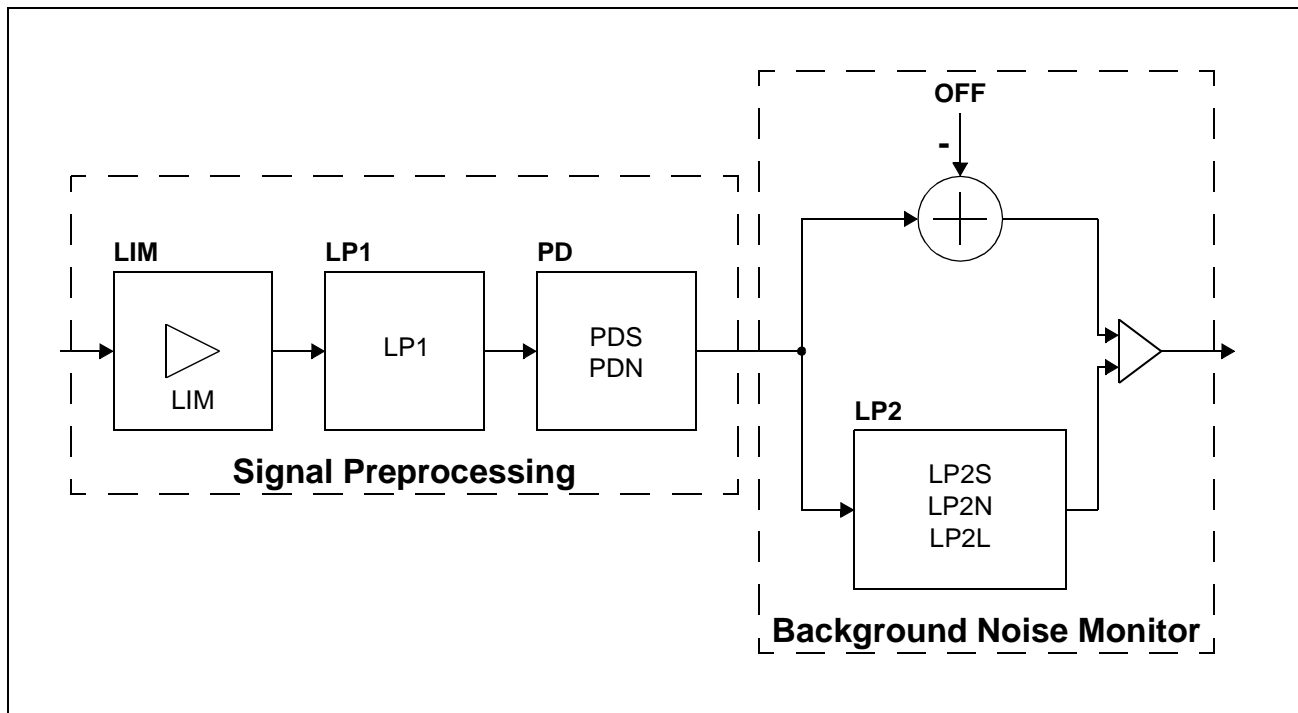


Figure 19 Speech Detector - Block Diagram

The first three units (LIM, LP1, PD) are used for preprocessing the signal while the actual speech detection is performed by the background noise monitor.

Background Noise Monitor

The tasks of the noise monitor are to differentiate voice signals from background noise, even if it exceeds the voice level, and to recognize voice signals without any delay. Therefore the Background Noise Monitor consists of the Low-Pass Filter 2 (LP2) and the offset in two separate branches. Basically it works on the burst-characteristic of the speech: voice signals consist of short peaks with high power (bursts). In contrast, background noise can be regarded approximately stationary from its average power.

Low-Pass Filter 2 provides different time constants for noise (non-detected speech) and speech. It determines the average of the noise reference level. In case of background noise the level at the output of LP2 is approximately the level of the input. As in the other branch an additional offset OFF is added to the signal, the comparator signals noise. At speech bursts the digital signals arriving at the comparator via the offset branch change faster than those via the LP2-branch. If the difference exceeds the offset OFF, the

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## Functional Description

comparator signals speech. Therefore the output of the background noise monitor is a digital signal indicating speech (1) or noise (0).

A small fade constant (LP2N) enables fast settling of LP2 to the average noise level after the end of speech recognition. However, a too small time constant for LP2N can cause rapid charging to such a high level that after recognizing speech the danger of an unwanted switching back to noise exists. It is recommended to choose a large rising constant (LP2S) so that speech itself charges the LP2 very slowly. Generally, it is not recommended to choose an infinite LP2S because then approaching the noise level is disabled. During continuous speech or tones the LP2 will be charged until the limitation LP2L is reached. Then the value of LP2 is frozen until a break discharges the LP2. This limitation permits transmission of continuous tones and "music on hold".

The offset stage represents the estimated difference between the speech signal and averaged noise.

### Signal Preprocessing

As described in the preceding chapter, the background noise monitor is able to discriminate between speech and noise. In very short speech pauses e.g. between two words, however, it changes immediately to non-speech, which is equal to noise. Therefore a peak detection is required in front of the Noise Monitor.

The main task of the Peak Detector (PD) is to bridge the very short speech pauses during a monolog so that this time constant has to be long. Furthermore, the speech bursts are stored so that a sure speech detection is guaranteed. But if no speech is recognized the noise low-pass LP2 must be charged faster to the average noise level. In addition, the noise edges are to be smoothed. Therefore two time constants are necessary. As the peak detector is very sensitive to spikes, the low-pass LP1 filters the incoming signal containing noise in a way that main spikes are eliminated. Due to the programmable time constant it is possible to refuse high-energy sibilants and noise edges.

To compress the speech signals in their amplitudes and to ease the detection of speech, the signals have to be companded logarithmically. Hereby, the speech detector should not be influenced by the system noise which is always present but should discriminate between speech and background noise. The limitation of the logarithmic amplifier can be programmed via the parameter LIM. LIM is related to the maximum PCM level. A signal exceeding the limitation defined by LIM is getting amplified logarithmically, while very smooth system noise below is neglected. It should be the level of the minimum system noise which is always existing; in the transmit path the noise generated by the telephone circuitry itself and in receive direction the level of the first bit which is stable without any speech signal at the receive path. Table 9 shows the parameters for the speech detector.

## Functional Description

Table 7 Speech Detector Parameters

Parameter	# of bytes	Range	Comment
LIM	1	0 to 95 dB	Limitation of log. amplifier
OFF	1	0 to 95 dB	Level offset up to detected noise
PDS	1	1 to 2000 ms	Peak decrement PD1 (speech)
PDN	1	1 to 2000 ms	Peak decrement PD1 (noise)
LP1	1	1 to 2000 ms	Time constant LP1
LP2S	1	2 to 250 s	Time constant LP2 (speech)
LP2N	1	1 to 2000 ms	Time constant LP2 (noise)
LP2L	1	0 to 95 dB	Maximum value of LP2

The input signal of the speech detector can be connected to either the input signal of the echo suppression unit (as shown for SDX) or the output of the associated AGC (as shown for SDR).

Functional Description

2.1.3.2 Speech Comparators (SC)

The echo suppression unit has two identical speech comparators (SCAS, SCLS). Each comparator can be programmed individually to accommodate the different system characteristics of the acoustic interface and the line interface. As SCAS and SCLS are identical, the following description holds for both SCAS and SCLS.

The SC has two input signals SX and SR, which map to microphone/loudspeaker for SCAS and line in/line out for SCLS.

In principle, the SC works according to the following equation:

$$\text{if } SX > SR + V \text{ then switch state}$$

Therefore, SCAS controls the switching to transmit state and SCLS controls the switching to receive state. Switching is done only if SX exceeds SR by at least the expected acoustic level enhancement V which is divided into two parts: G and GD. A block diagram of the SC is shown in figure 20.

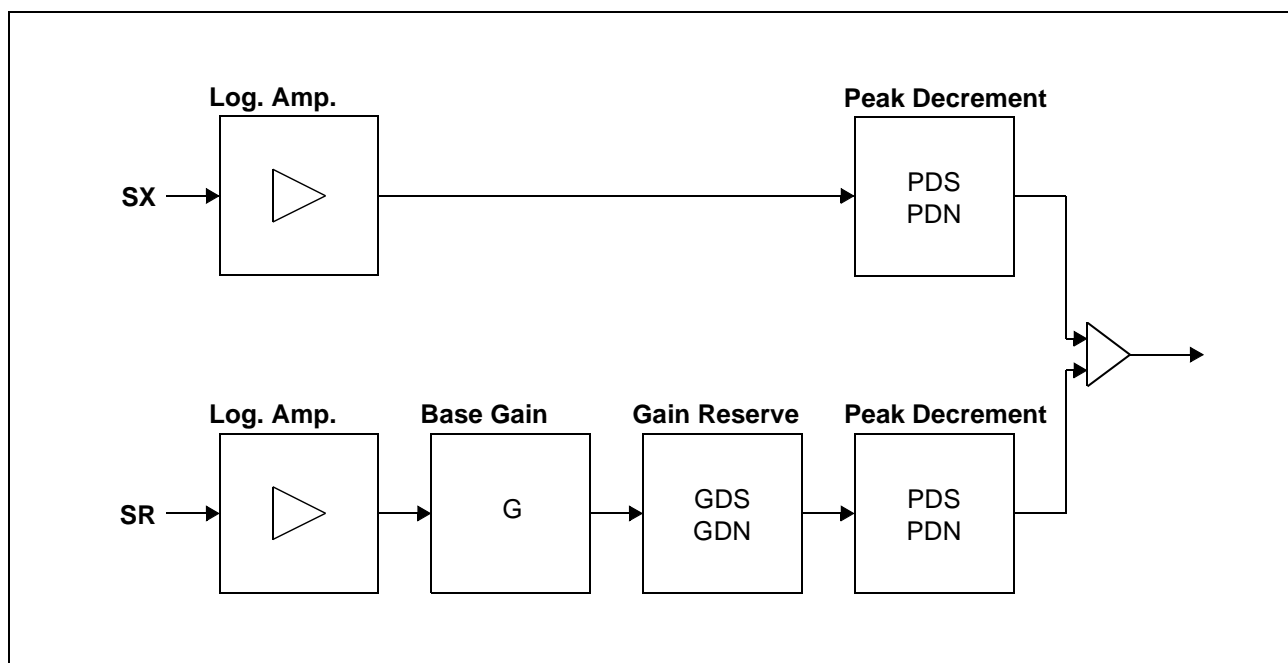


Figure 20 Speech Comparator - Block Diagram

At both inputs, logarithmic amplifiers compress the signal range. Hence after the required signal processing for controlling the acoustic echo, pure logarithmic levels on both paths are compared.

The main task of the comparator is to control the echo. The internal coupling due to the direct sound and mechanical resonances are covered by G. The external coupling, mainly caused by the acoustic feedback, is controlled by GD/PD.

Functional Description

The base gain (G) corresponds to the terminal couplings of the complete telephone: G is the measured or calculated level enhancement between both receive and transmit inputs of the SC.

To control the acoustic feedback two parameters are necessary: GD represents the actual reserve on the measured G. Together with the Peak Decrement (PD) it simulates the echo behavior at the acoustic side: After speech has ended there is a short time during which hard couplings through the mechanics and resonances and the direct echo are present. Till the end of that time ( $\Delta t$ ) the level enhancement V must be at least equal to G to prevent clipping caused by these internal couplings. Then, only the acoustic feedback is present. This coupling, however, is reduced by air attenuation. For this in general the longer the delay, the smaller the echo being valid. This echo behavior is featured by the decrement PD.

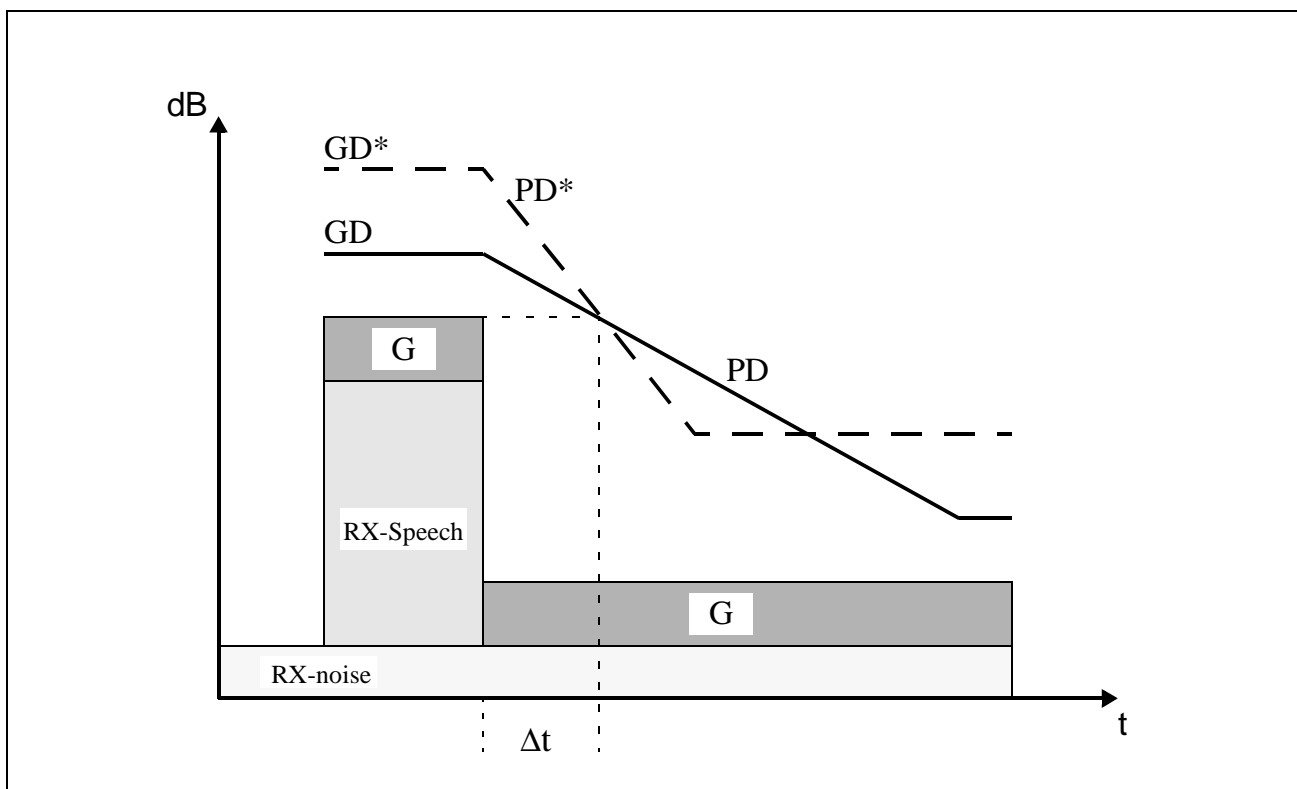


Figure 21 Speech Comparator - Interdependence of Parameters

According to figure 21, a compromise between the reserve GD and the decrement PD has to be made: a smaller reserve (GD) above the level enhancement G requires a longer time to decrease (PD). It is easy to overshoot the other side but the intercommunication is harder because after the end of the speech, the level of the estimated echo has to be exceeded. In contrary, with a higher reserve (GD\*) it is harder to overshoot continuous speech or tones, but it enables a faster intercommunication because of a stronger decrement (PD\*).



**Functional Description**

Two pairs of coefficients, GDS/PDS when speech is detected, and GDN/PDN in case of noise, offer a different echo handling for speech and non-speech.

With speech, even if very strong resonances are present, the performance will not be worsened by the high GDS needed. Only when speech is detected, a high reserve prevents clipping. A time period ET [ms] after speech end, the parameters of the comparator are switched to the “noise” values. If both sets of the parameters are equal, ET has no function.

**Table 8 Speech Comparator Parameters**

Parameter	# of bytes	Range	Comment
G	1	– 48 to + 48 dB	Base Gain
GDS	1	0 to 48 dB	Gain Reserve (Speech)
PDS	1	0.025 to 6 dB/ms	Peak Decrement (Speech)
GDN	1	0 to 48 dB	Gain Reserve (Noise)
PDN	1	0.025 to 6 dB/ms	Peak Decrement (Noise)
ET	1	0 to 992 ms	Time to Switch from speech to noise parameters

**2.1.3.3 Attenuation Control**

The attenuation control unit controls the attenuation stages GHX and GHR and performs state switching. The programmable attenuation ATT is completely switched to GHX (GHR) in receive state (transmit state). In idle state both GHX and GHR attenuate by ATT/2.

In addition, attenuation is also influenced by the automatic gain control stages (AGCX, AGCR).

State switching depends on the signals of one speech comparator and the corresponding speech detector. While each state is associated with the programmed attenuation, the time it takes to reach the steady-state attenuation after a state switch can be programmed ( $T_{SW}$ ).

If the current state is either transmit or receive and no speech on either side has been detected for time  $T_W$  then idle state is entered. To smoothen the transition, the attenuation is incremented (decremented) by DS until the evenly distribution ATT/2 for both GHX and GHR is reached.

Table 9 shows the parameters for the attenuation unit. Note that  $T_{SW}$  is dependant on the current attenuation by the formula  $T_{sw} = SW \times ATT$ .

## Functional Description

**Table 9 Attenuation Control Parameters**

Parameter	# of bytes	Range	Comment
TW	1	16 ms to 4 s	$T_W$ to return to idle state
ATT	1	0 to 95 dB	Attenuation for GHX and GHR
DS	1	0.6 to 680 ms/dB	Decay Speed (to idle state)
SW	1	0.0052 to 10 ms/dB	Decay Rate (used for $T_{SW}$ )

*Note: In addition, attenuation is also influenced by the Automatic Gain Control stages (AGCX, AGCR) in order to keep the total loop attenuation constant.*

**2.1.3.4 Echo Suppression Status Output**

The PSB 4860 can report the current state of the echo suppression unit to ease the optimization of the parameter set of the echo suppression unit. In this case the  $SPS_0$  and  $SPS_1$  pins are set according to table 10.

**Table 10 SPS Encoding**

$SPS_0$	$SPS_1$	Echo Suppression Unit State
0	0	no echo suppression operation
0	1	receive
1	0	transmit
1	1	idle

Furthermore the controller can read the current value of the SPS pins by reading register SPSCCTL.

**2.1.3.5 Loudhearing**

The speakerphone unit can also be used for controlled loudhearing. If enabled in loudhearing mode, the loudspeaker amplifier of the PSB 4851 (ALS) is used instead of GHR when appropriate to avoid oscillation. In order to enable this feature, the PSB 4851 must be programmed to allow ALS override. The ALS field within the AFE control register AFECTL defines the value sent to the PSB 4851 if attenuation is necessary.

**2.1.3.6 Automatic Gain Control**

The echo suppression unit has two identical automatic gain control units (AGCX, AGCR).

Operation of the AGC depends on a threshold level defined by the parameter COM (value relative to the maximum PCM-value). The regulation speed is controlled by

Functional Description

SPEEDH for signal amplitudes above the threshold and SPEEDL for amplitudes below. Usually SPEEDH will be chosen to be at least 10 times faster than SPEEDL. The bold line in Figure 22 depicts the steady-state output level of the AGC as a function of the input level.

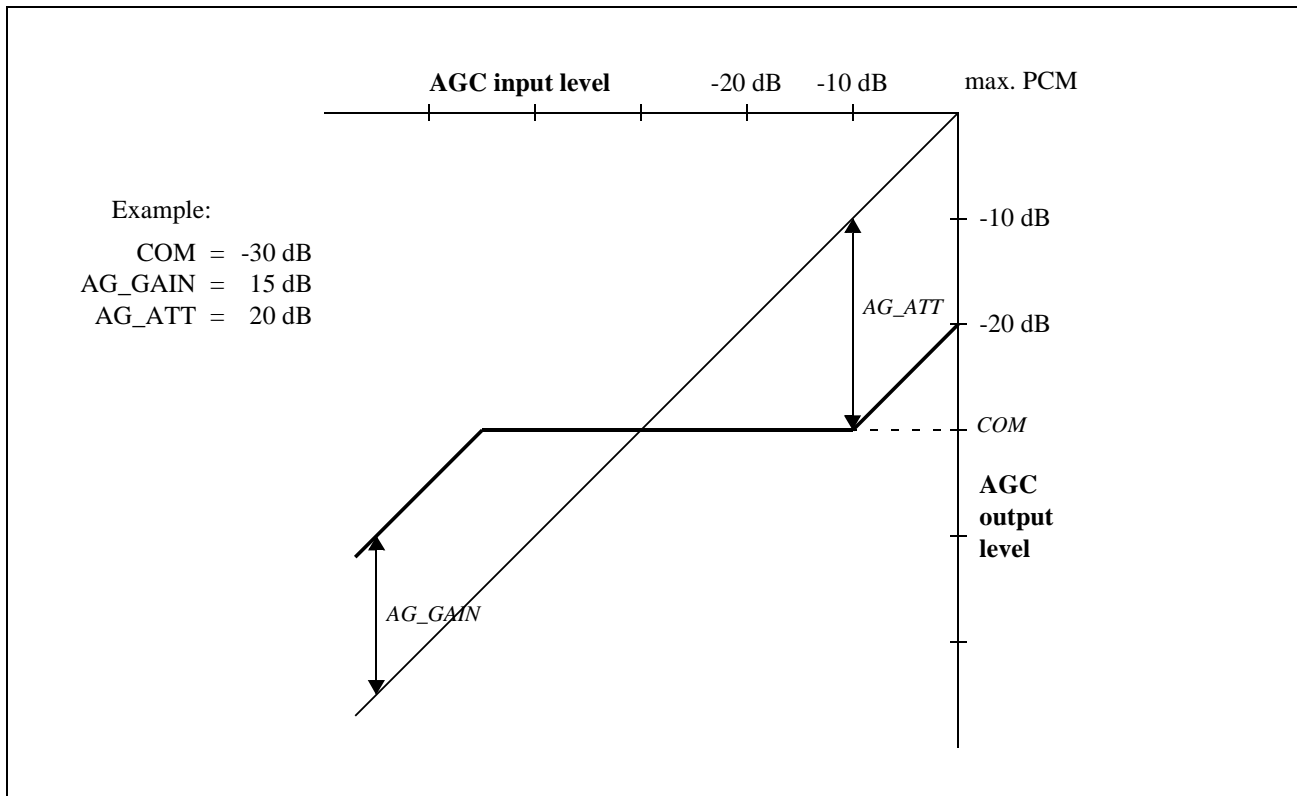


Figure 22 Echo Suppression Unit - Automatic Gain Control

For reasons of physiological acceptance the AGC gain is automatically reduced in case of continuous background noise (e.g. by ventilators). The reduction is programmed via the NOIS parameter. When the noise level exceeds the threshold determined by NOIS, the amplification will be reduced by the same amount the noise level is above the threshold. The current gain/attenuation of the AGC can be read at any time.

An additional low pass with time constant LPA is provided to avoid an immediate response of the AGC to very short signal bursts.

The AGCX is not working in the receive state. In this case the last gain setting is used. Regulation starts with this value as soon as receive state is left.

Likewise, AGCR is not working in transmit state. In this case the last gain setting is used. Regulation starts with this value as soon transmit state is left. When the AGC has been disabled the initial gain used immediately after enabling the AGC can be programmed. Table 11 shows the parameters of the AGC.

## Functional Description

**Table 11 Automatic Gain Control Parameters**

Parameter	# of Bytes	Range	Comment
AG_INIT	1	-95 dB to 95dB	Initial AGC gain/attenuation
COM	1	0 to – 95 dB	Compare level rel. to max. PCM-value
AG_ATT	1	0 to -95 dB	Attenuation range
AG_GAIN	1	0 to 95 dB	Gain range
AG_CUR	1	-95 dB to 95 dB	Current gain/attenuation
SPEEDL	1	0.25 to 62.5 dB/s	Change rate for lower levels
SPEEDH	1	0.25 to 62.5 dB/s	Change rate for higher levels
NOIS	1	0 to – 95 dB	Threshold for AGC-reduction by background noise
LPA	1	0.025 to 16 ms	AGC low pass time constant

**2.1.3.7 Fixed Gain**

Each signal path features an additional amplifier (LGAX, LGAR) that can be set to a fixed gain. These amplifiers should be used for the basic amplification in order to avoid saturation in the preceding stages. Table 12 shows the only parameter of this stage.

**Table 12 Fixed Gain Parameters**

Parameter	# of Bytes	Range	Comment
LGA	1	-12 dB to 12 dB	always active

**2.1.3.8 Mode Control**

Table 13 shows the registers used to determine the signal sources and the mode.

**Table 13 Speakerphone Registers**

Register	# of Bits	Name	Comment
SCTL	1	ENS	Echo suppression unit enable
SCTL	1	ENC	Echo cancellation unit enable
SCTL	1	MD	Speakerphone or loudhearing mode
SCTL	1	AGX	AGCX enable
SCTL	1	AGR	AGCR enable
SCTL	1	SDX	SDX input tap
SCTL	1	SDR	SDR input tap

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**Functional Description**

**Table 13 Speakerphone Registers**

AFECTL	4	ALS	ALS value for loudhearing
SSRC1	5	I1	Input signal 1 (microphone)
SSRC1	5	I2	Input signal 2 (microphone)
SSRC2	5	I3	Input signal 3 (line in)
SSRC2	5	I4	Input signal 4 (line in)

2.2 Operation in Noisy Environment

The full duplex speakerphone can be augmented by a comfort noise generator which can enhance the performance of the speakerphone in noisy environments. The purpose of the comfort noise is to reduce signal modulation when the echo suppression unit switches the attenuation. The principle of operation is as follows:

As long as the echo suppression unit is transmit state no additional noise is added to the outgoing signal. In this state there is already the natural noise transmitted to the line.

In addition the comfort noise generator estimates the noise at the microphone input when no speech is detected by either of the three speech detectors (SD, SDX, SDR).

Once the echo suppression unit switches to receive or idle state the comfort noise generator generates noise similar to the external noise and adds this noise to the outgoing signal. Figure 23 shows the integration of the comfort noise generator into the speakerphone.

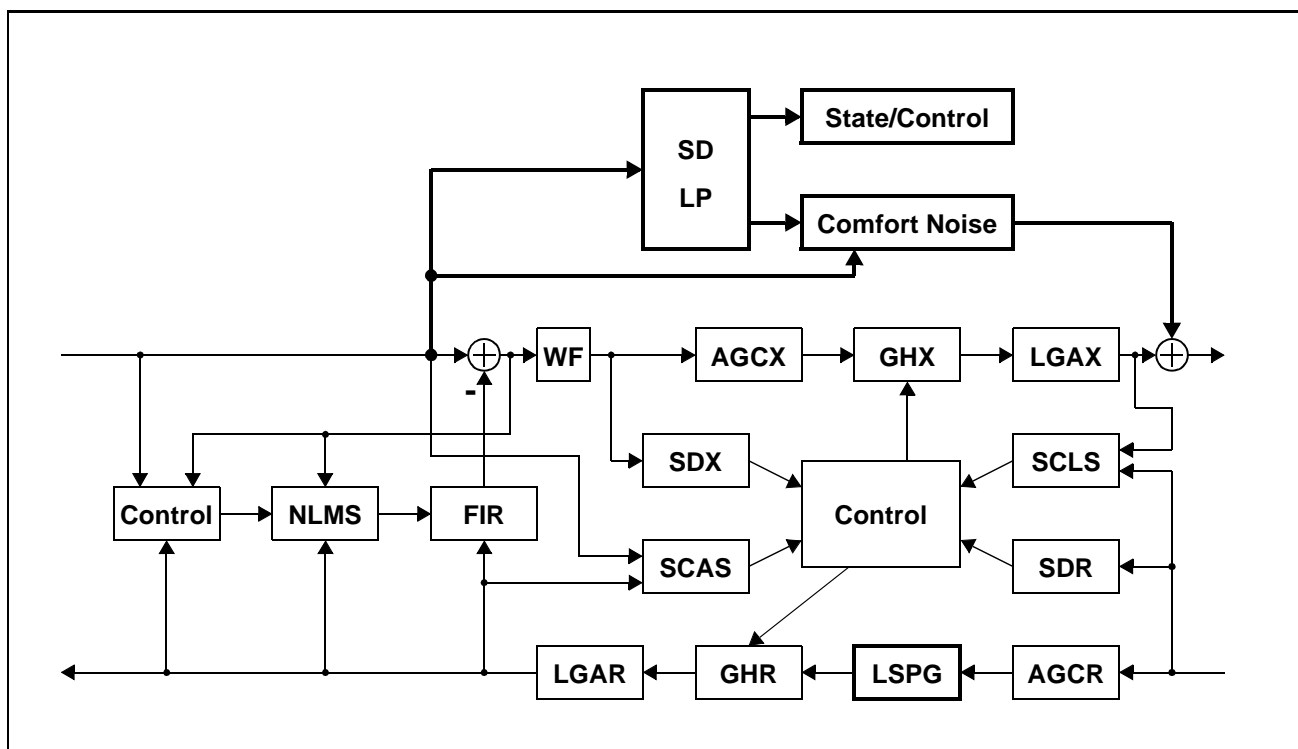


Figure 23 Comfort Noise Generator - Integration into Speakerphone

If the new blocks (SD/LP, State/Control, Comfort Noise and LSPG) are removed the remaining blocks resemble the speakerphone as shown in figures 16 and 18. Therefore the comfort noise generator can be viewed as an optional extension to the speakerphone.

The speech detector SDR should be fed by the same signal as AGCR if the adaptive loudspeaker gain (LSPG) is used (see 2.2.2.6).

## Functional Description

**2.2.1 Modes of Operation**

For enhanced operation in noisy environments the speakerphone of the PSB 2170 provides two modes of operation:

1. Noise Controlled Adaptation
2. Noise Controlled Adaptation and Comfort Noise Generation

If the echo cancellation unit is used in subband mode then it is mandatory to reduce the number of taps. The tables 14 and 15 summarize the available modes and the associated register settings.

**Table 14 Comfort Noise - Mode Control Bits**

Register	# of Bits	Name	Comment
SCTL	1	NAD	Noise Adaptation
SCTL	1	RED	Tap Reduction (subband only)
SCTL	1	CN	Comfort Noise

**Table 15 Comfort Noise - Modes of Operations**

NAD	RED <sup>1)</sup>	CN	Mode
0	0	0	Normal Speakerphone
1	0	0	Speakerphone with Noise Controlled Adaptation, CPT and CID must be disabled
1	1	0	Speakerphone with Noise Controlled Adaptation and reduced filter length (car application)
1	1	1	Speakerphone with Noise Controlled Adaptation and Comfort Noise Generation

<sup>1)</sup> don't care in fullband mode

The parameters for noise controlled adaptation and comfort noise generation must be programmed prior to activation if either the call progress tone detector or the caller ID decoder have been used.

NAD, RED and CN must be only set if the echo cancellation unit is also enabled.

After comfort noise is disabled the parameters for the DTMF detector, the caller ID decoder, the alert tone detector, the call progress tone detector and the line echo canceller must be reprogrammed.

---

**Functional Description**
**2.2.2 Noise Controlled Adaptation**

The purpose of the noise controlled adaptation is to reduce the effects of the echo suppression unit (half-duplex speakerphone) and to minimize the effect of wrong adaptations of the echo cancellation unit (full-duplex speakerphone) in noisy environments.

The three core blocks of the Noise Controlled Adaptation are the Speech Detector/ Low Pass (SD/LP) the State/Control block and the adaptive loudspeaker gain (LSPG). The speech detector is used to detect speech in the input signal (microphone). The speech detector has the same structure and parameters as the speech detectors SDX and SDR (see chapter 2.1.3.1). However, the parameters used for the speech detector are usually set to different values compared with SDX and SDR.

The low pass is used to determine the energy of the microphone signal. It has only the time constant as a programmable parameter (table 16).

**Table 16 Low Pass Register**

Register	# of Bits	Name	Comment
SCLPT	15	TC	Time constant for the low pass

Therefore the output of the SD/LP block is the information, whether noise is present (no speech detected by SD) and the current noise level (estimated by LP). The speech detector should be programmed more sensitive (in terms of detecting speech) than SDX or SDR.

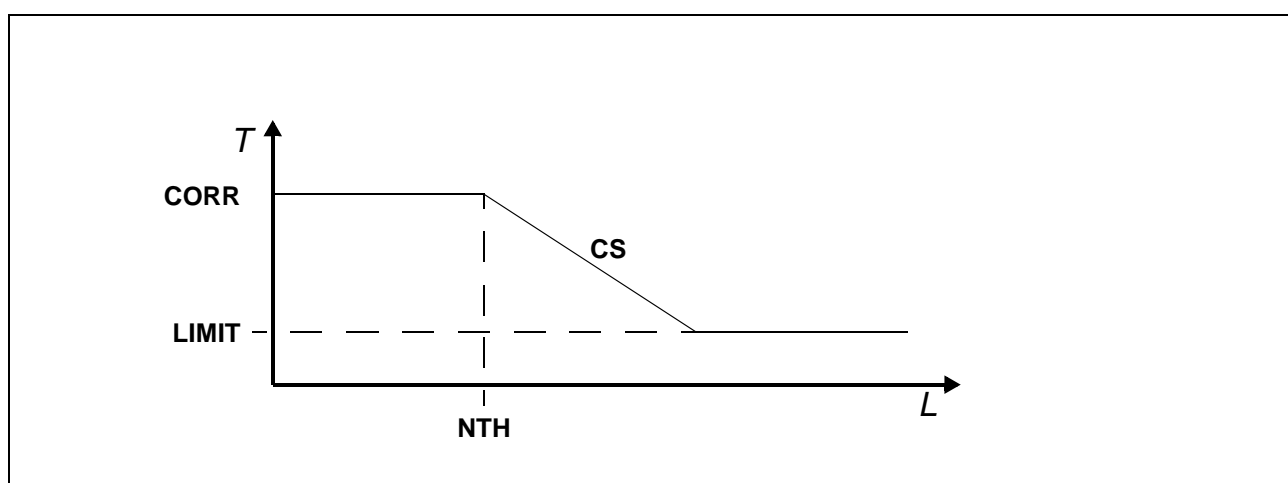
The noise level is used for several calculations performed by the State/Control block. It is referred to by the variable  $L$  where needed.



**2.2.2.1 Correlation Adaptation**

The attenuation achieved by the echo cancellation unit is measured only when the correlation of the loudspeaker and microphone signal exceeds a threshold  $T$ . In a noisy environment the correlation will decrease even if the echo cancellation unit is fully adapted. Therefore the threshold  $T$  might not be exceeded in this situation. As a result the echo cancellation unit would not report any achieved echo return loss enhancement and thus the echo suppression unit would have to switch all of the desired attenuation.

To avoid this situation the threshold  $T$  can be adjusted dynamically with the noise level  $L$ . Figure 24 shows the available parameters for the adaptation of the threshold.



**Figure 24 Correlation Adaptation**

As long as the noise level  $L$  is less than the threshold  $NTH$  the threshold  $T$  remains at its programmed value. Once the threshold exceeded, the threshold decreases with the programmable slope  $CS$ . However, the threshold will not fall below the programmable limit  $LIMIT$  even if the noise level  $L$  increases further. Table 17 shows the registers associated with the threshold adaptation.

**Table 17 Correlation Adaptation Registers**

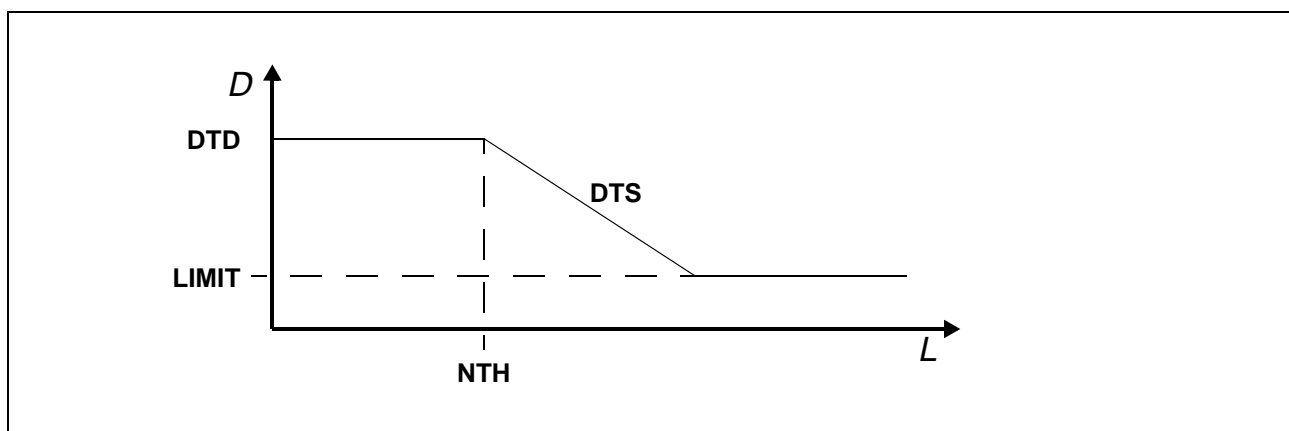
Register	# of Bits	Name	Comment
SCCR	14	CORR	Factor C
SCCRN	15	NTH	Noise Threshold
SCCRS	12	CS	Slope
SCCRL	14	LIMIT	Limit for C

**2.2.2.2 Double Talk Detection Adaptation**

During double talk the necessary echo return loss for comfortable full duplex conversation may be reduced. The PSB 2170 provides the parameter SAEATT:ATT for this purpose. In subband mode double talk is detected when the difference between the signal before and after the echo cancellation (subtraction point) suddenly decreases by an amount  $D$ .

The noisier the environment gets the smaller the amount  $D$  should be. Otherwise the echo cancellation would fail to detect the relatively smaller change which indicates a double talk detection.

Figure 25 shows the provisions made by the PSB 2170 for an adaptive double talk detection.



**Figure 25 Double Talk Detection Adaptation**

As long as the noise level  $L$  is less than the threshold  $NTH$  the necessary difference  $DTD$  remains at its programmed value. Once the threshold exceeded,  $DTD$  decreases with the programmable slope  $DTS$ . However, it will not fall below the programmable limit  $LIMIT$  even if the noise level  $L$  increases further. Table 18 shows the registers associated with the double talk detection adaptation.

**Table 18 Double Talk Detection Adaptation Registers**

Register	# of Bits	Name	Comment
SCDT	15	DTD	Difference DTD
SCDTN	15	NTH	Noise Threshold
SCDTS	12	DTS	Slope
SCDTL	15	LIMIT	Limit for DTD

In fullband mode double talk is detected if the difference of the expected and the measured error signal exceeds a threshold. In this mode  $DTD$  should be set to  $0x0400$  and  $LIMIT$  to  $0xFC00$ .

Functional Description

2.2.2.3 Attenuation Reduction Adaptation

In noisy environments it is acceptable to reduce the overall attenuation as the noise level increases. This is due to the fact that the noise already presents some kind of local talk. Hence an increased echo is not perceived as disturbing as in a silent environment.

In order to exploit this the PSB 2170 provides an attenuation decrease dependent on the noise level.

Figure 26 shows the attenuation reduction provided by the PSB 2170.

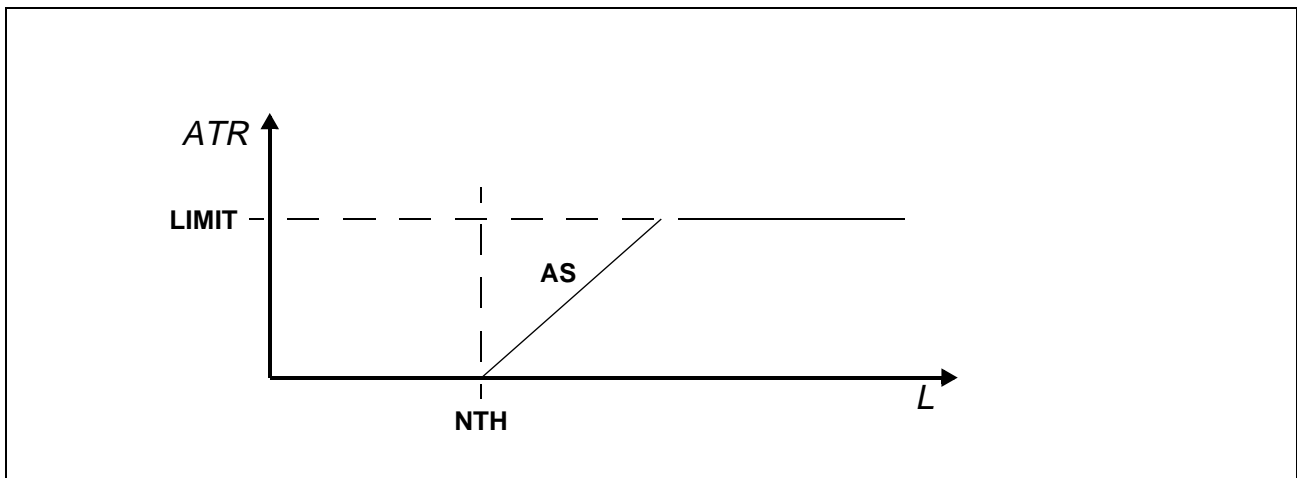


Figure 26 Attenuation Reduction Adaptation

As long as the noise level  $L$  is less than the threshold  $NTH$  the overall attenuation is not reduced at all. Once the threshold exceeded, the overall attenuation is decreased more and more by increasing  $ATR$ . The sensitivity is programmable by the parameter  $AS$ . However, it will not exceed the programmable limit  $LIMIT$  even if the noise level  $L$  increases further. Table 20 shows the registers associated with the double talk detection adaptation.

Table 19 Double Talk Detection Adaptation Registers

Register	# of Bits	Name	Comment
SCATTN	15	NTH	Noise Threshold
SCATTS	15	AS	Attenuation Sensitivity
SCATTL	15	LIMIT	Limit for DTD

## Functional Description

### 2.2.2.4 Minimal Attenuation

In case of a significant change of the characteristics of the acoustics the attenuation reported by the echo cancellation unit may be too high until it has adapted itself again. If, in addition, double talk or attenuation reduction ATR is in effect then the remaining attenuation for the echo suppression might be too low to avoid echoes. Therefore a maximal echo return loss enhancement reported by the echo cancellation unit can be programmed by the parameter GLIMIT.

**Table 20 Minimal Attenuation**

Register	# of Bits	Name	Comment
SCAECL	15	GLIMIT	Global limit for attenuation

2.2.2.5 Adaptation Timing Control

While there is no signal ( $SDR=0$  and  $SDX=0$ ) at all the echo cancellation unit cannot adapt to changes of the acoustic characteristics of the room. Therefore it is quite likely that after an extended period of silence the echo cancellation unit is not very well adapted any more. Therefore there may be some echo remaining during the adaptation time once there is a signal ( $SDR=1$ ) again.

In order to minimize this short periods of audible echo the PSB 2170 can increase the additional attenuation provided by the echo suppression unit according to figure 27.

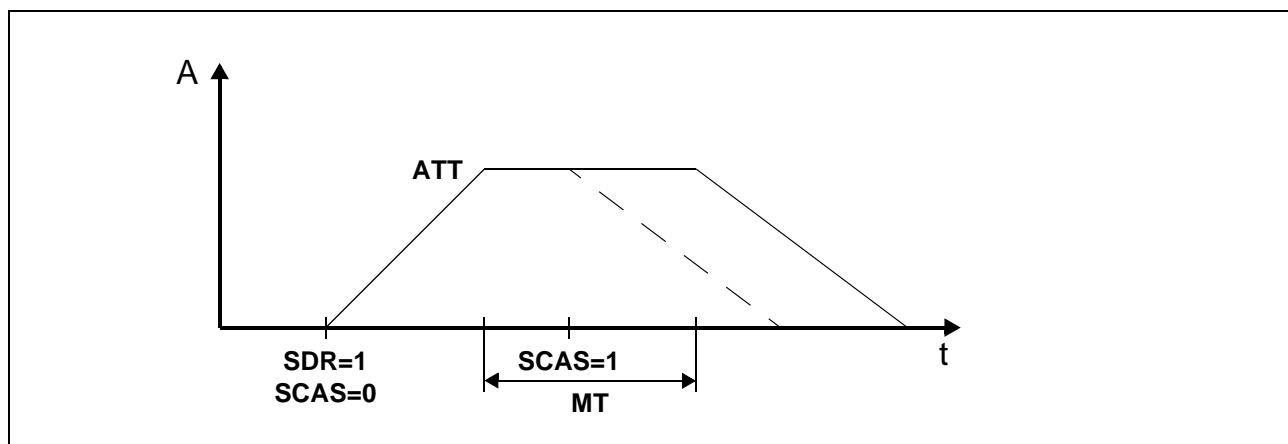


Figure 27 Attenuation Timing

First of all a signal gap (both sides) of at least time  $GT$  is needed. Otherwise no additional attenuation  $A$  will be added dynamically. Once the time  $GT$  has been exceeded and a signal at the far end ( $SDR=1$ ,  $SCAS=0$ ) only has been detected, an additional attenuation  $A$  will be provided by the echo suppression unit. Both the attack speed  $ASP$  and the maximum value  $ATT$  are programmable. The maximum value will be inserted for a duration of at most  $MT$ . Then the additional attenuation is reduced again with the programmable decay speed  $DSP$  until is zero again.

If during this process double talk is detected ( $SCAS=1$ ) then the decay phase is entered immediately as shown by the dotted line in figure 27. The maximum value  $ATT$  itself can be reduced automatically in accordance with the noise level as shown in figure 28.

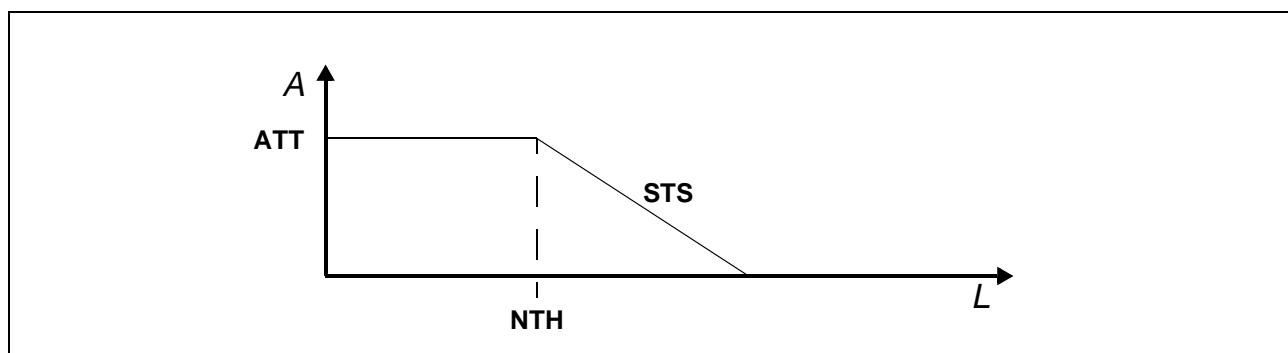


Figure 28 Adaptation of Additional Attenuation

## Functional Description

Table 21 shows the registers associated with the adaptation timing control.

**Table 21 Adaptation of Additional Attenuation Registers**

Register	# of Bits	Name	Comment
SCSTGP	16	GT	Minimal Gap Time
SCSTATT	15	ATT	Maximal Attenuation
SCSTNL	15	NTH	Noise Threshold
SCSTS	12	STS	Noise Sensitivity
SCSTTIM	16	MT	Maximum Attenuation Time for ATT
SCSTIS	15	ASP	Attack Speed
SCSTDS	16	DSP	Decay Speed

**Example:**

As an example the following values for the parameters are used:

Register	Name	Value
SCSTGP	GT	1 s
SCSTATT	ATT	20 dB
SCSTNL	NTH	-60 dB
SCSTS	STS	1 dB <sup>-1</sup>
SCSTTIM	MT	2 s
SCSTIS	ASP	1 dB/ms
SCSTDS	DSP	6 dB/ms

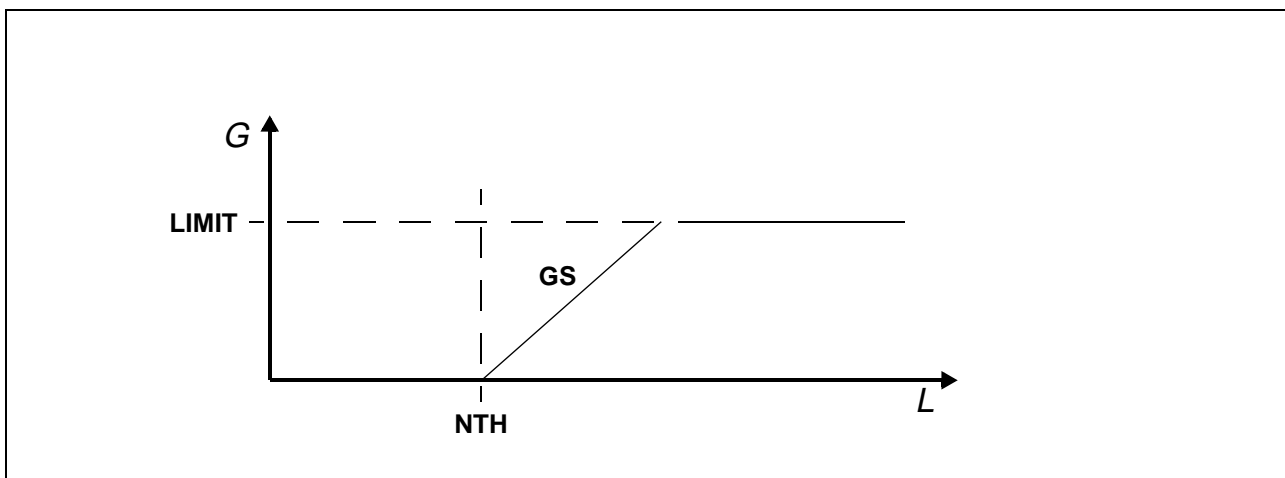
The noise level is -55 dB, at t=0 conversation ceases, at t=3 s the far end speaker starts to talk and at t=4 s the local speaker also starts to speak.

First of all the Minimal Gap Time (1 s) is exceeded by the signal gap of 3 s and therefore the adaptation timing control is activated. As soon as the far end speaker starts to speak (SDR=1) while the local speaker is silent (SCAS=0) the additional attenuation starts to rise with the programmed attack speed (1 dB/ms). The maximum value for the additional attenuation is 20 dB-5 dB=15 dB. The first term is the parameter ATT. The second term (5 dB) is the adapted attenuation. The noise threshold NTH is exceeded by 5 dB by the actual noise. As the sensitivity STS is 1 dB<sup>-1</sup>, 5 dB are subtracted from ATT.

At 1 dB/ms, this value is reached after 15 ms. Then the attenuation remains constant until the local speaker also starts to speak. Then the additional attenuation decreases by 6 dB/ms. Therefore after 3 ms the additional attenuation is 0 dB again.

**2.2.2.6 Loudspeaker Gain Adaptation**

In noisy environments it is useful to automatically increase the signal level of the loudspeaker output whenever the noise level increases. The PSB 2170 features such an automatic gain adaptation by the gain stage LSPG. Figure 29 shows the adaptive gain provided by the PSB 2170.



**Figure 29 Loudspeaker Gain Adaptation**

As long as the noise level  $L$  is less than the threshold  $NTH$  there is no additional gain. Once the threshold is exceeded, the gain  $G$  is increased with the programmable sensitivity  $GS$ . However, it will not exceed the programmable limit  $LIMIT$  even if the noise level  $L$  increases further.

The level of the signal fed into the speech detector  $SDR$  should not vary with the adaptive gain provided by LSPG. Therefore it is recommended to set  $SCTL:SDR=1$ .

Table 22 shows the registers associated with the double talk detection adaptation.

**Table 22 Loudspeaker Gain Adaptation Registers**

Register	# of Bits	Name	Comment
SCLSPN	15	NTH	Noise Threshold
SCLSPS	15	GS	Gain Sensitivity
SCLSPL	15	LIMIT	Limit for G

*Note: The total attenuation programmed for the speakerphone in register  $SATT1:ATT$  is not automatically increased when the gain of LSPG increases. Therefore the attenuation reduction (chapter 2.2.2.3) should be reduced accordingly.*

---

**Functional Description**
**2.2.2.7 Comfort Noise Generator**

The comfort noise generator adapts itself to the currently present noise at the input signal with respect to the energy level and the spectrum. Furthermore it is possible to program a constant noise level which is always present (even if there is no noise at the input signal present).

There are only three parameters for this block:

1. The adaptation speed LP
2. The constant noise level CONST
3. The factor FAC by which the present noise is scaled for the output of the noise generator.

Table 23 shows the associated registers.

**Table 23 Comfort Noise Generator Registers**

<b>Register</b>	<b># of Bits</b>	<b>Name</b>	<b>Comment</b>
SCCN1	15	CONST	Level of Constant Noise
SCCN2	15	FAC	Factor for Multiplication
SCCN3	15	LP	Adaptation Time Constant



Functional Description

2.3 Line Echo Cancellation Unit

The PSB 2170 contains an adaptive line echo cancellation unit for the cancellation of near end echoes. A block diagram is shown in figure 30.

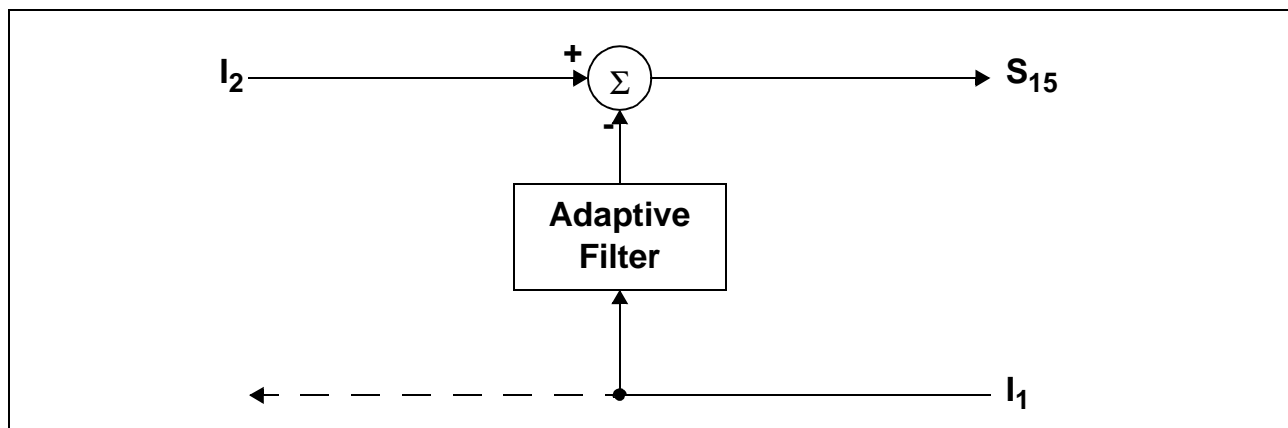


Figure 30 Line Echo Cancellation Unit - Block Diagram

The line echo canceller provides only one outgoing signal ( $S_{15}$ ) as the other outgoing signal would be identical with the input signal  $I_1$ . Input  $I_2$  is usually connected to the line input while input  $I_1$  is connected to the outgoing signal.

The adaptation process can be controlled by three parameters: MIN, ATT and MGN. Adaptation takes only place if both of the following conditions hold:

1.  $I_1 > MIN$
2.  $I_1 - I_2 - ATT + MGN > 0$

With the first condition adaptation to small signals can be avoided. The second condition avoids adaptation during double talk. The parameter ATT represents the echo loss provided by external circuitry. The adaptation stops if the power of the received signal ( $I_2$ ) exceeds the power of the expected signal ( $I_1 - ATT$ ) by more than the margin MGN.

Table 24 shows the registers associated with the line echo canceller.

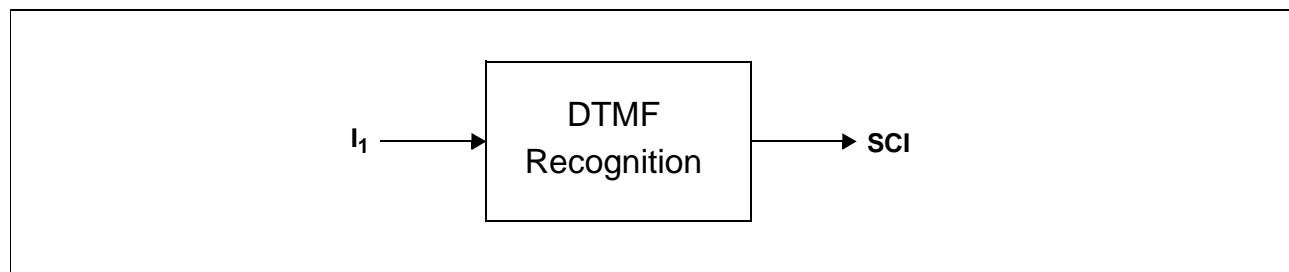
Table 24 Line Echo Cancellation Unit Registers

Register	# of Bits	Name	Comment
LECCTL	1	EN	Line echo canceller enable
LECCTL	5	I1	Input signal selection for $I_1$
LECCTL	5	I2	Input signal selection for $I_2$
LECLEV	15	MIN	Minimal power for signal $I_1$
LECATT	15	ATT	Externally provided attenuation ( $I_1$ to $I_2$ )
LECMGN	15	MGN	Margin for double talk detection

## Functional Description

### 2.4 DTMF Detector

Figure 31 shows a block diagram of the DTMF detector. The results of the detector are available in the status register and a dedicated result register that can be read via the serial control interface (SCI) by the external controller.



**Figure 31 DTMF Detector - Block Diagram**

Table 25 shows the supported modes and the input signal selection.

**Table 25 DTMF Detector Control Registers**

Register	# of Bits	Name	Comment
DDCTL	1	EN	DTMF detector enable
DDCTL	5	I1	Input signal selection

As soon as a valid DTMF tone is recognized, the status word and the DTMF tone code are updated (table 26).

**Table 26 DTMF Detector Results**

Register	# of Bits	Name	Comment
STATUS	1	DTV	DTMF code valid
DDCTL	5	DTC	DTMF tone code (valid until replaced by new code)

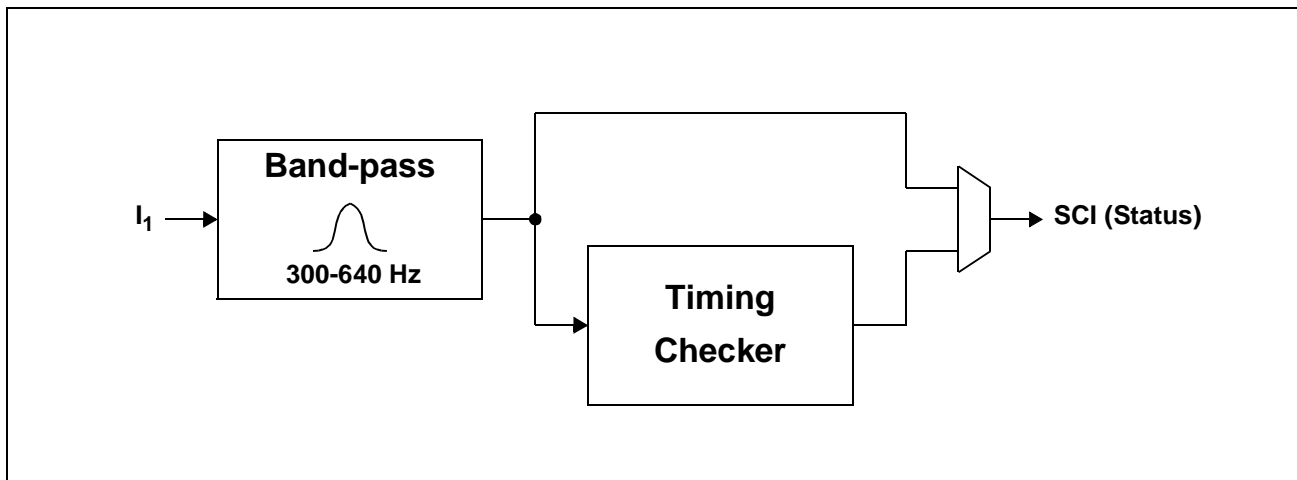
DTV is set when a standard DTMF tone is recognized and reset when no DTMF tone is recognized or the detector is disabled. The code for the DTMF tone is placed into the register DDCTL. The registers DDTW and DDLEV hold parameters for detection (table 27).

**Table 27 DTMF Detector Parameters**

Register	# of Bits	Name	Comment
DDTW	15	TWIST	Twist for DTMF recognition
DDLEV	6	MIN	Minimum signal level to detect DTMF tones

### 2.5 Call Progress Tone Detector

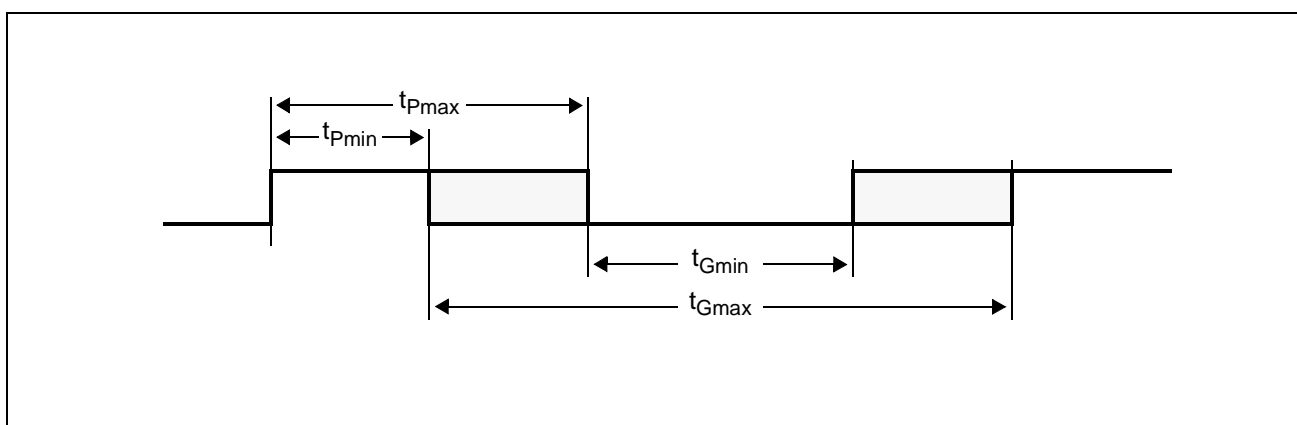
The selected signal is monitored continuously for a call progress tone. The CPT detector consists of a band-pass and an optional timing checker (figure 32).



**Figure 32 Call Progress Tone Detector - Block Diagram**

The CPT detector can be used in two modes: raw and cooked. In raw mode, the occurrence of a signal within the frequency, time and energy limits is directly reported. The timing checker is bypassed and therefore the PSB 2170 does not interpret the length or interval of the signal.

In cooked mode, the number and duration of signal bursts are interpreted by the timing checker. A signal burst followed by a gap is called a cycle. The CPT flag is set with the first burst after the programmed number of cycles has been detected. The CPT flag remains set until the unit is disabled or speech is detected, even if the conditions are not met anymore. In this mode the CPT is modelled as a sequence of identical bursts separated by gaps with identical length. The PSB 2170 can be programmed to accept a range for both the burst and the gap. It is also possible to specify a maximum aberration of two consecutive bursts (gaps). Figure 33 shows the parameters for a single cycle (burst and gap).



**Figure 33 Call Progress Tone Detector- Cooked Mode**

## Functional Description

The status bit is defined as follows:

**Table 28 Call Progress Tone Detector Results**

Register	# of Bits	Name	Comment
STATUS	1	CPT	CP tone currently detected [340 Hz; 640 Hz]

CPT is not affected by reading the status word. It is automatically reset when the unit is disabled. Table 29 shows the control register for the CPT detector.

**Table 29 Call Progress Tone Detector Registers**

Register	# of Bits	Name	Comment
CPTCTL	1	EN	Unit enable
CPTCTL	1	MD	Mode (cooked, raw)
CPTCTL	5	I1	Input signal selection
CPTMN	8	MINB	Minimum time of a signal burst ( $t_{Pmin}$ )
CPTMN	8	MING	Minimum time of a signal gap ( $t_{Gmin}$ )
CPTMX	8	MAXB	Maximum time of a signal burst ( $t_{Pmax}$ )
CPTMX	8	MAXG	Maximum time of a signal gap ( $t_{Gmax}$ )
CPTDT	8	DIFB	Maximum difference between consecutive bursts
CPTDT	8	DIFG	Maximum difference between consecutive gaps
CPTTR	3	NUM	Number of cycles (cooked mode), 0 (raw mode)
CPTTR	8	MIN	Minimum signal level to detect tones
CPTTR	4	SN	Minimal signal-to-noise ratio

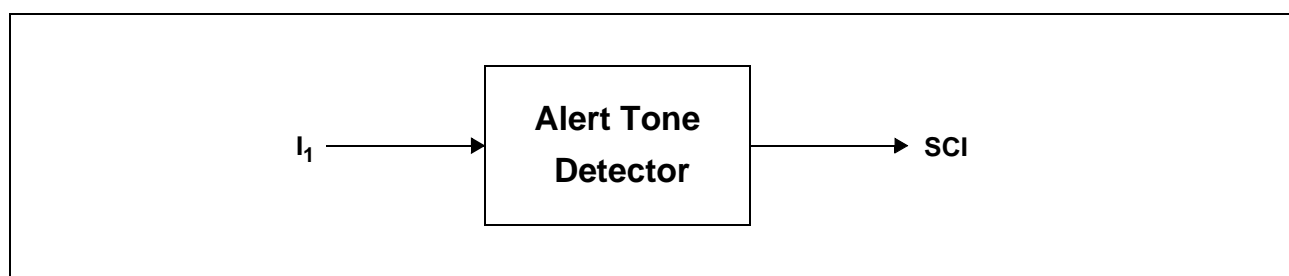
If any condition is violated during a sequence of cycles the timing checker is reset and restarts with the next valid burst.

*Note: In cooked mode CPT is set with the first burst after the programmed number of cycles has been detected. If CPTTR:NUM = 2, then CPT is set with the third signal burst.*

*Note: The number of cycles must be set to zero in raw mode.*

**2.6 Alert Tone Detector**

The alert tone detector can detect the standard alert tones (2130 Hz and 2750 Hz) for caller id protocols. The results of the detector are available in the status register and the dedicated register ATDCTL0 that can be read via the serial control interface (SCI) by the external controller.



**Figure 34 Alert Tone Detector - Block Diagram**

**Table 30 Alert Tone Detector Registers**

Register	# of Bits	Name	Comment
ATDCTL0	1	EN	Alert Tone Detector Enable
ATDCTL0	5	I1	Input signal selection
ATDCTL1	1	MD	Detection of dual tones or single tones
ATDCTL1	1	GT	Gap time
ATDCTL1	1	DEV	Maximum deviation (0.5% or 1.1%)
ATDCTL1	8	MIN	Minimum signal level to detect alert tones

As soon as a valid alert tone is recognized, the status word of the PSB 2170 and the code for the detected combination of alert tones are updated (table 31).

**Table 31 Alert Tone Detector Results**

Register	# of Bits	Name	Comment
STATUS	1	ATV	Alert tone detected
ATDCTL0	2	ATC	Alert tone code

For fast reaction time the necessary gap time (until STATUS:ATV is reset after the end of an alert tone) can be reduced by setting ATDCTL:GT. However, this also reduces robustness against speech. Therefore ATDCTL1:GT should be only set for alert tone detection if there is no speech signal present e.g.. on-hook condition).

Functional Description

2.7 Caller ID Decoder

The caller ID decoder is basically a 1200 baud modem (FSK, demodulation only). The bit stream is formatted by a subsequent UART and the data is available in a data register along with status information (figure 35).

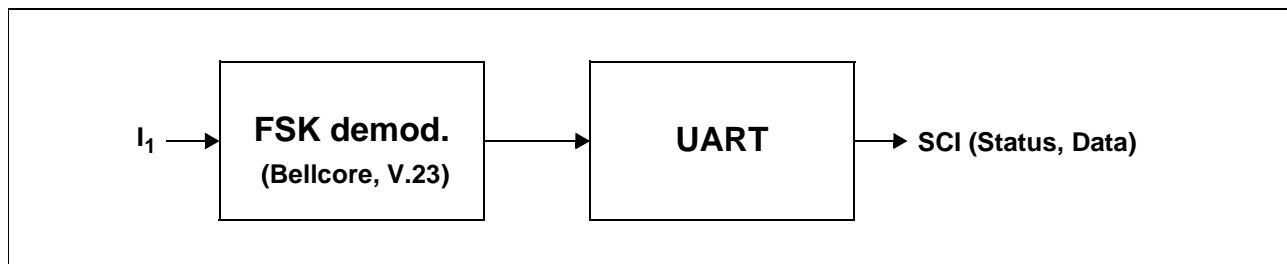


Figure 35 Caller ID Decoder - Block Diagram

The FSK demodulator supports two modes according to table 32. The appropriate mode is detected automatically.

Table 32 Caller ID Decoder Modes

Mode	Mark (Hz)	Space (Hz)	Comment
1	1200	2200	Bellcore
2	1300	2100	V.23

The CID decoder does not interpret the data received. Each byte received is placed into the CIDCTL register (table 34). The status byte of the PSB 2170 is updated (table 33).

Table 33 Caller ID Decoder Status

Register	# of Bits	Name	Comment
STATUS	1	CIA	CID byte received
STATUS	1	CD	Carrier Detected

CIA and CD are cleared when the unit is disabled. In addition, CIA is cleared when CIDCTL0 is read.

Table 34 Caller ID Decoder Registers

Register	# of Bits	Name	Comment
CIDCTL0	1	EN	Unit enable
CIDCTL0	5	I1	Input signal selection
CIDCTL0	8	DATA	Last CID data byte received

## Functional Description

Table 34 Caller ID Decoder Registers

Register	# of Bits	Name	Comment
CIDCTL1	5	NMSS	Number of mark/space sequences necessary for successful detection of carrier detect
CIDCTL1	6	NMB	Number of mark bits necessary before space of first byte after carrier detect
CIDCTL1	5	MIN	Minimum signal level for CID detection

When the CID unit is enabled, it first waits for a channel seizure signal consisting of a series of alternating space and mark signals. The number of spaces and marks that have to be received without errors before the PSB 2170 reports a carrier detect can be programmed.

Channel seizure must be followed by at least 16 continuous mark signals. The first space signal detected is then regarded as the start bit of the first message byte.

The interpretation of the data, including message type, length and checksum is completely left to the controller. The CID unit should be disabled as soon as the complete information has been received as it cannot detect the end of the transmission by itself.

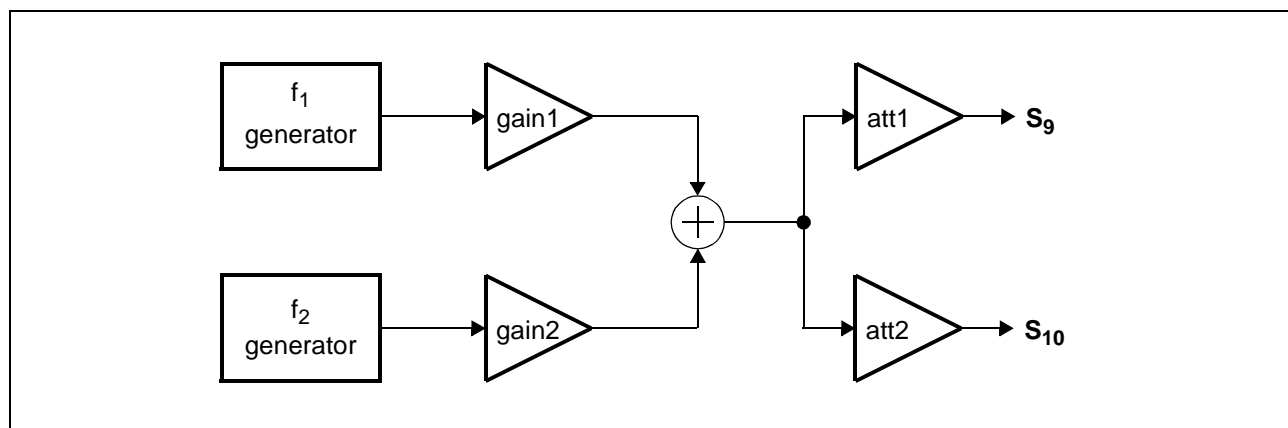
*Note: Some caller ID mechanism may require additional external components for DC coupling. These tasks must be handled by the controller.*

*Note: The controller is responsible for selecting and storing parts of the CID as needed.*

## Functional Description

## 2.8 DTMF Generator

The DTMF generator can generate single or dual tones with programmable frequency and gain. This unit is primarily used to generate the common DTMF tones but can also be used for signalling or other user defined tones. A block diagram is shown in figure 36.



**Figure 36 DTMF Generator - Block Diagram**

Both generators and amplifiers are identical. There are two modes for programming the generators, cooked mode and raw mode. In cooked mode, DTMF tones are generated by programming a single 4 bit code. In raw mode, the frequency of each generator/amplifier can be programmed individually by a separate register. The unit has two outputs which provide the same signal but with individually programmable attenuation. Table 35 shows the parameters of this unit.

**Table 35 DTMF Generator Registers**

Register	# of Bits	Name	Comment
DGCTL	1	EN	Enable for generators
DGCTL	1	MD	Mode (cooked/raw)
DGCTL	4	DTC	DTMF code (cooked mode)
DGF1	15	FRQ1	Frequency of generator 1
DGF2	15	FRQ2	Frequency of generator 2
DGL	7	LEV1	Level of signal for generator 1
DGL	7	LEV2	Level of signal for generator 2
DGATT	8	ATT1	Attenuation of S <sub>9</sub>
DGATT	8	ATT2	Attenuation of S <sub>10</sub>

*Note: DGF1 and DGF2 are undefined when cooked mode is used and must not be written.*



Functional Description

2.9 Analog Interface

There are two identical interfaces at the analog side (to PSB 4851) as shown in figure 37.

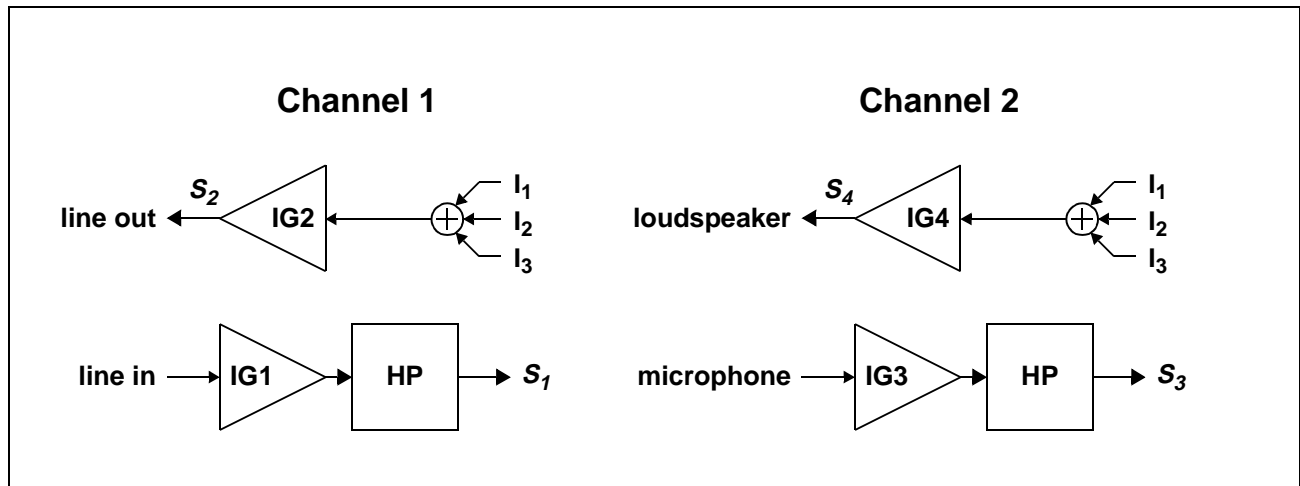


Figure 37 Analog Frontend Interface - Block Diagram

For each signal an amplifier is provided for level adjustment. The ingoing signals can be passed through an optional high-pass (HP). Furthermore, up to three signals can be mixed in order to generate the outgoing signals ( $S_2, S_4$ ). Table 36 shows the associated registers.

Table 36 Analog Frontend Interface Registers

Register	# of Bits	Name	Comment
IFG1	16	IG1	Gain for IG1
IFG2	16	IG2	Gain for IG2
IFS1	1	HP	High-pass for $S_1$
IFS1	5	I1	Input signal 1 for IG2
IFS1	5	I2	Input signal 2 for IG2
IFS1	5	I3	Input signal 3 for IG2
IFG3	16	IG3	Gain for IG3
IFG4	16	IG4	Gain for IG4
IFS2	1	HP	High-pass for $S_3$
IFS2	5	I1	Input signal 1 for IG4
IFS2	5	I2	Input signal 2 for IG4
IFS2	5	I3	Input signal 3 for IG4

Functional Description

2.10 Digital Interface

There are two almost identical interfaces at the digital side as shown in figure 38. The only difference between these two interfaces is that only channel 1 supports the SSDI mode.

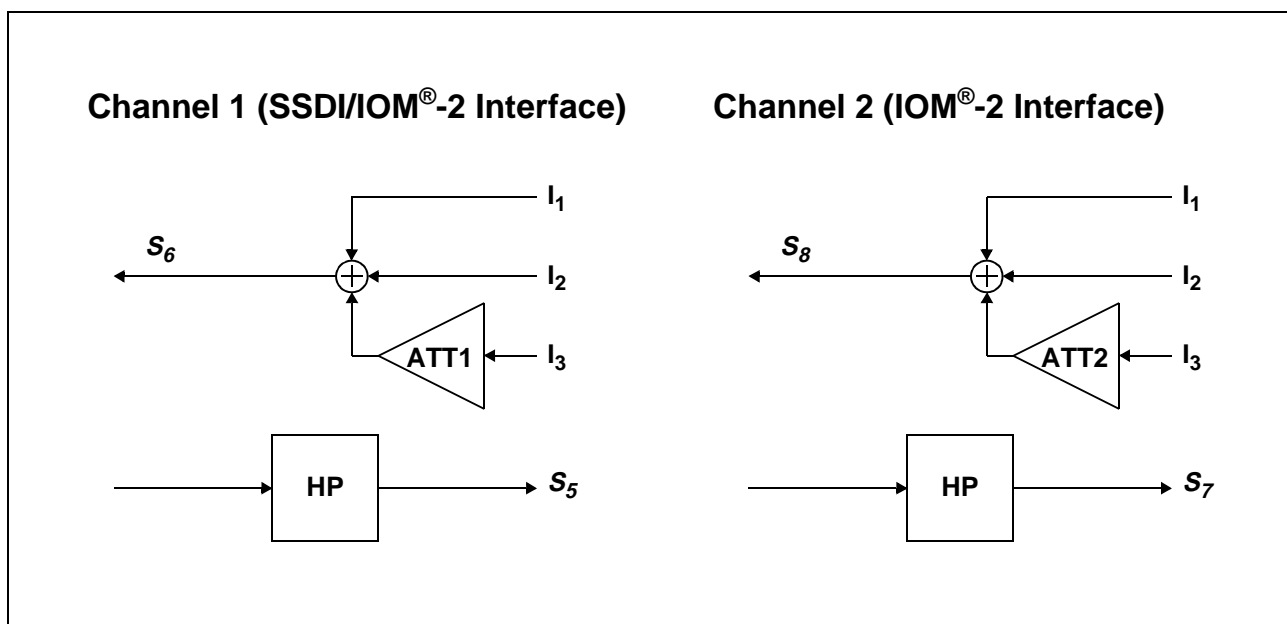


Figure 38 Digital Interface - Block Diagram

Each outgoing signal can be the sum of two signals with no attenuation and one signal with programmable attenuation (ATT). The attenuator can be used for artificial echo loss. Each input can be passed through an optional high-pass (HP). The associated registers are shown in table 37.

Table 37 Digital Interface Registers

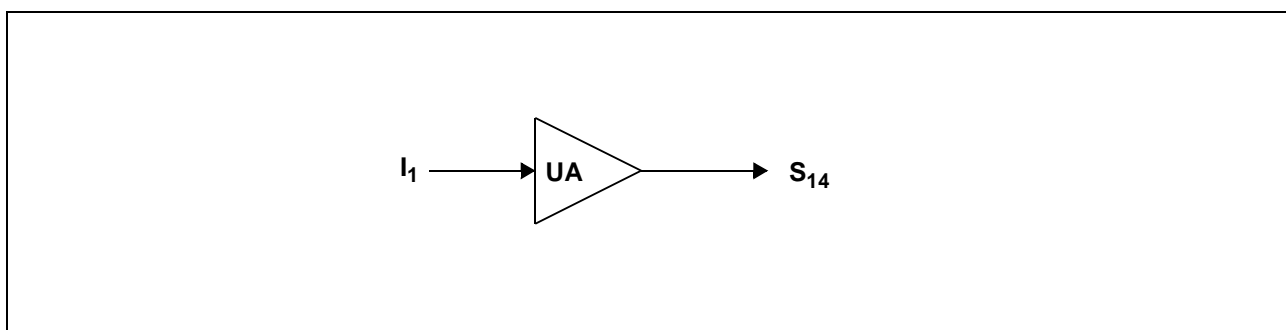
Register	# of Bits	Name	Comment
IFS3	5	I1	Input signal 1 for S <sub>6</sub>
IFS3	5	I2	Input signal 2 for S <sub>6</sub>
IFS3	5	I3	Input signal 3 for S <sub>6</sub>
IFS3	1	HP	High-pass for S <sub>5</sub>
IFS4	5	I1	Input signal 1 for S <sub>8</sub>
IFS4	5	I2	Input signal 2 for S <sub>8</sub>
IFS4	5	I3	Input signal 3 for S <sub>8</sub>
IFS4	1	HP	High-pass for S <sub>7</sub>

**Table 37 Digital Interface Registers**

Register	# of Bits	Name	Comment
IFG5	8	ATT1	Attenuation for input signal I3 (Channel 1)
IFG5	8	ATT2	Attenuation for input signal I3 (Channel 2)

**2.11 Universal Attenuator**

The PSB 2170 contains an universal attenuator that can be connected to any signal (e.g. for sidetone gain).



**Figure 39 Universal Attenuator - Block Diagram**

Table 38 shows the associated register.

**Table 38 Universal Attenuator Registers**

Register	# of Bits	Name	Comment
UA	8	ATT	Attenuation for UA
UA	5	I1	Input signal for UA

2.12 Equalizer

The PSB 2170 contains two identical equalizers which can be programmed individually. Each equalizer can be inserted into any signal path. The main application for the equalizer is the adaptation to the frequency characteristics of the microphone, transducer or loudspeaker.

Each equalizer consists of an IIR filter followed by an FIR filter as shown in figure 40.

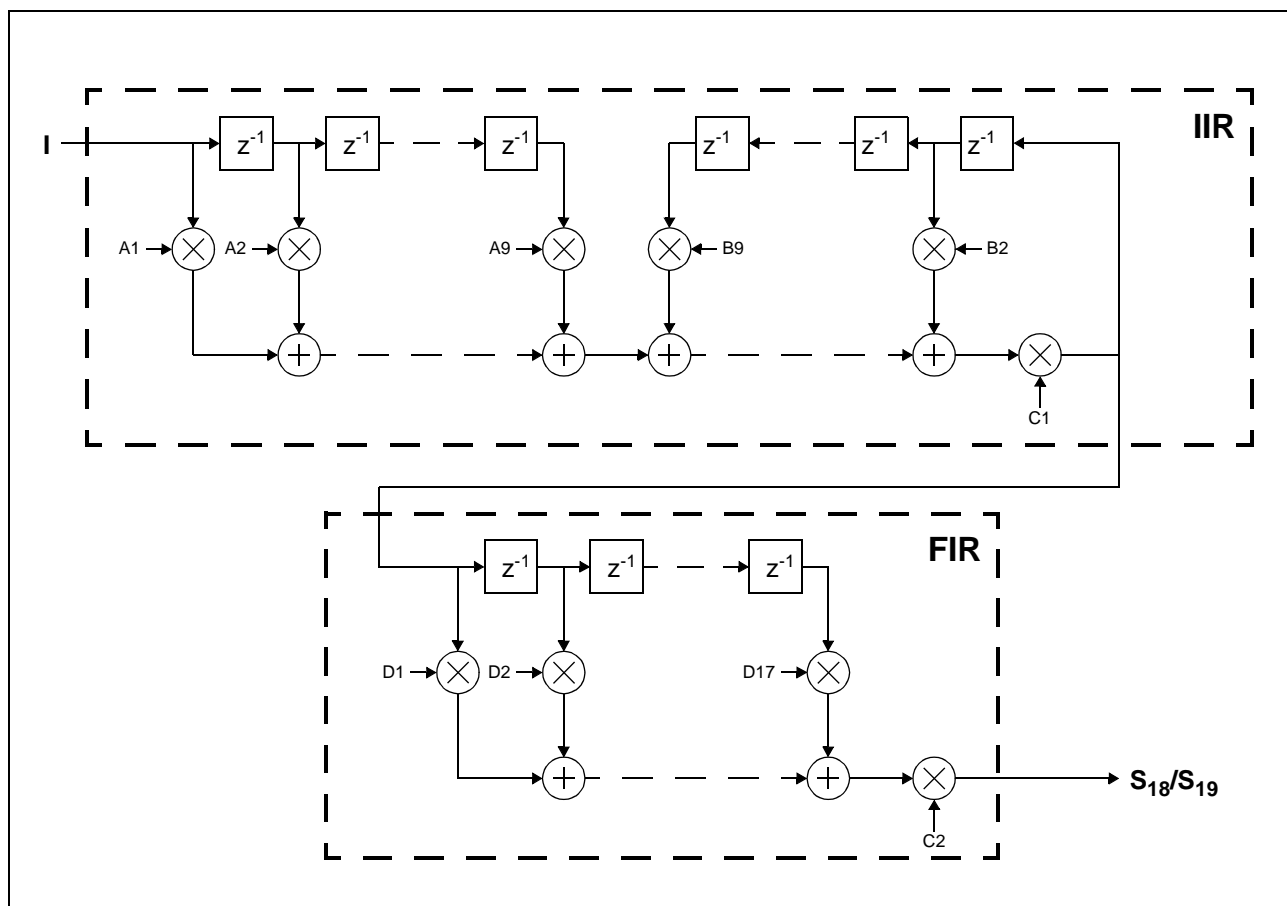


Figure 40 Equalizer - Block Diagram

The coefficients  $A_1$ - $A_9$ ,  $B_2$ - $B_9$  and  $C_1$  belong to the IIR filter, the coefficients  $D_1$ - $D_{17}$  and  $C_2$  belong to the FIR filter. Table 39 shows the registers associated with the first equalizer ( $S_{18}$ ). The second equalizer ( $S_{19}$ ) is programmed by the registers FCFCTL2 and FCFCOF2, respectively

Table 39 Equalizer Registers

Register	# of Bits	Name	Comment
FCFCTL1	1	EN	Enable
FCFCTL1	5	I	Input signal for equalizer

Functional Description

**Table 39 Equalizer Registers**

Register	# of Bits	Name	Comment
FCFCTL1	6	ADR	Filter coefficient address
FCFCOF1	16		Filter coefficient data

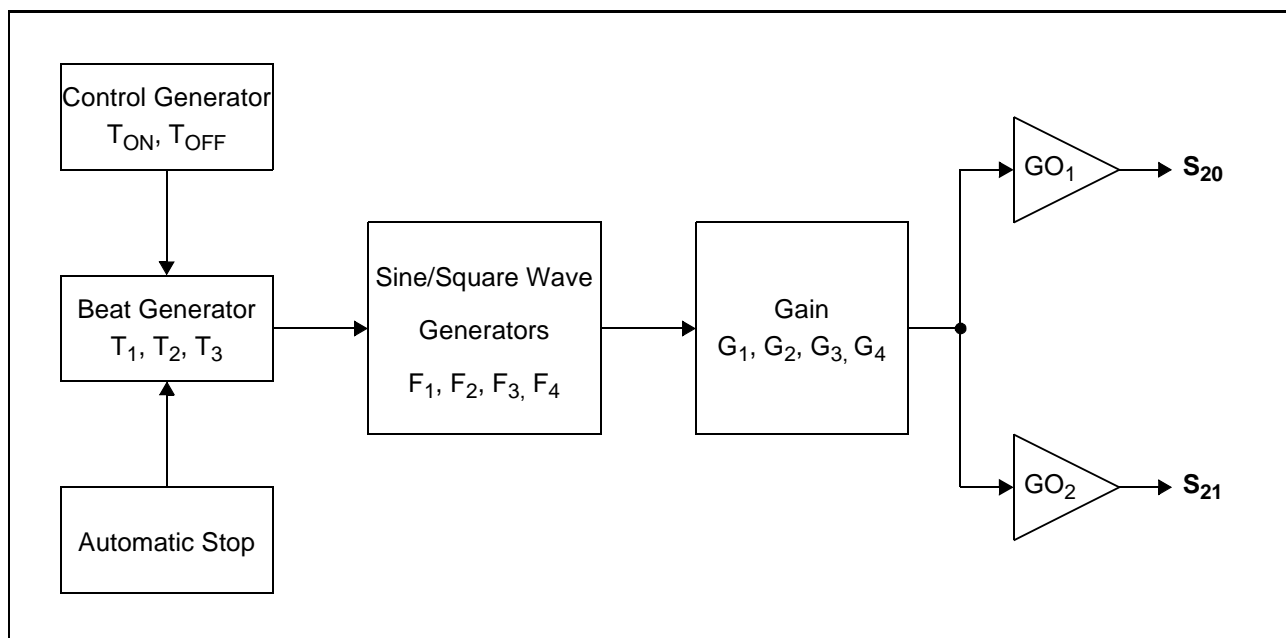
Due to the multitude of coefficients the uses an indirect addressing scheme for reading or writing an individual coefficient. The address of the coefficient is given by ADR and the actual value is read or written to register FCFCOF1.

In order to ease programming the PSB 2170 automatically increments the address ADR after each access to FCFCOF1.

*Note: Any access to an out-of-range address automatically resets FCFCTL1:ADR.*

**2.13 Tone Generator**

The PSB 2170 contains a universal tone generator which can be used for tone alerting, call progress tones or other audible feedback tones. Figure 41 shows a block diagram of this unit.



**Figure 41 Tone Generator - Block Diagram**

The heart of this unit are the four independent sine/square wave generators that can generate individually programmable frequencies ( $F_1, F_2, F_3, F_4$ ). Each generator has an associated amplifier ( $G_1, G_2, G_3, G_4$ ). The dynamic behavior of the tone generator is controlled by the beat generator.

Functional Description

If the beat generator is enabled, then the output is either a three tone cadence or a two tone cadence as shown in figure 42.

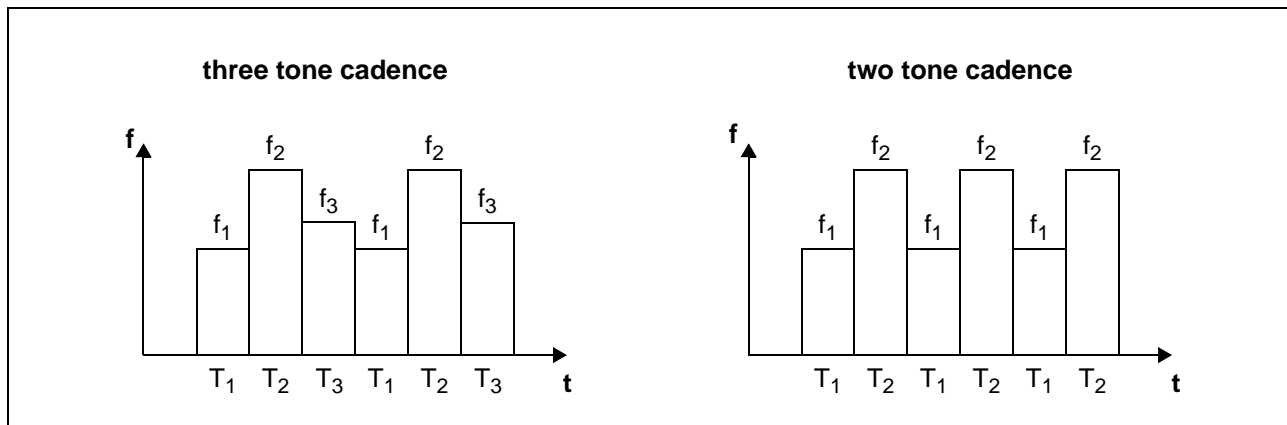


Figure 42 Tone Generator - Tone Sequences

The duration of each frequency is defined by  $T_1$ ,  $T_2$  and  $T_3$ . For each timeslot either the associated frequency can be generated or a frequency pair (table 40).

Table 40 Tone Generator Modes

Timeslot	Option 1	Option 2
$T_1$	$F_1$	$F_1+F_4$
$T_2$	$F_2$	$F_2+F_4$
$T_3$	$F_3$	$F_3+F_4$

If the beat generator is disabled, then the output is a continuous signal of either  $F_1$ ,  $F_2$ ,  $F_1+F_4$ ,  $F_2+F_4$  or silence.

The control generator is used to enable the beat generator (during  $T_{ON}$ ) and disable it during  $T_{OFF}$ . With the automatic stop feature the cadence generation the beat generator stops not immediately but after the end of a cadence (either  $T_2$  or  $T_3$ ). This avoids unpleasant sounds when stopping the tone generator unit.

Table 41 shows the registers associated with the tone and ringing generator.

Table 41 Tone Generator Registers

Register	# of Bits	Name	Comment
STATUS	1	ACT	Status bit (Tone Generator on/off)
TGCTL	2	CGM	Control generator mode
TGCTL	1	DT	Dual tone enable ( $F_4$ on/off)
TGCTL	2	BGM	Beat generator mode ( $F_1$ , $F_2$ , $F_1/F_2$ or $F_1/F_2/F_3$ )
TGCTL	1	SM	Stop mode (immediate or automatic)

Functional Description

**Table 41 Tone Generator Registers**

Register	# of Bits	Name	Comment
TGCTL	1	WF	Waveform (sine or square)
TGTON	16		T <sub>ON</sub>
TGTOFF	16		T <sub>OFF</sub>
TGT1	16		T <sub>1</sub>
TGT2	16		T <sub>2</sub>
TGT3	16		T <sub>3</sub>
TGF1	15		F <sub>1</sub>
TGF2	15		F <sub>2</sub>
TGF3	15		F <sub>3</sub>
TGF4	15		F <sub>4</sub>
TGG1	15		G <sub>1</sub>
TGG2	15		G <sub>2</sub>
TGG3	15		G <sub>3</sub>
TGG4	15		G <sub>4</sub>
TGGO1	15		GO <sub>1</sub>
TGGO2	15		GO <sub>2</sub>

This unit has two outputs (S<sub>20</sub> and S<sub>21</sub>). The signal level of these outputs can be programmed individually by the preceding gain stages (GO<sub>1</sub> and GO<sub>2</sub>).

3 Miscellaneous

3.1 Reset and Power Down Mode

The PSB 2170 can be in either reset mode, power down mode or active mode. During reset the PSB 2170 clears the hardware configuration registers and stops both internal and external activity. With the first access to a read/write register the PSB 2170 enters active mode. In this mode the main oscillator is running and normal operation takes place. The PSB 2170 can be brought to power down mode by programming over the SCI interface.

In power down mode the main oscillator is stopped. The PSB 2170 enters active mode again upon an access to a read/write register. Figure 43 shows a state chart of the modes of the PSB 2170.

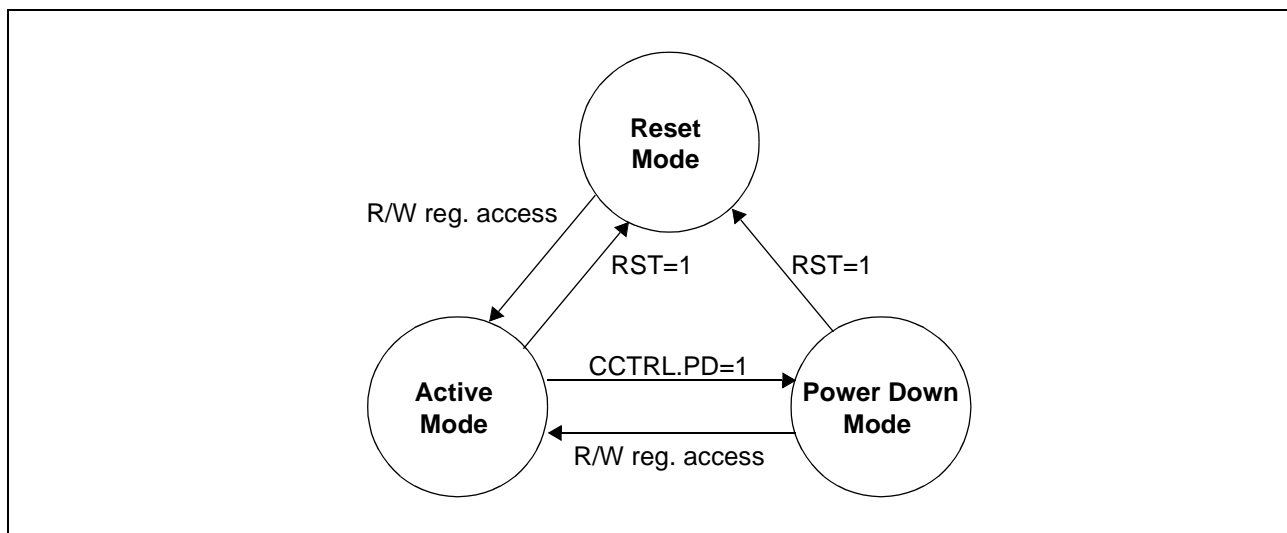


Figure 43 Operation Modes - State Chart

3.2 SPS Control Register

The two SPS outputs (SPS<sub>0</sub>, SPS<sub>1</sub>) can be used as either general purpose outputs or as indicators for the speakerphone state according to table 42.

Table 42 SPS Registers

Register	# of Bits	Name	Comment
SPSCTL	1	SP0	Output Value of SPS <sub>0</sub>
SPSCTL	1	SP1	Output Value of SPS <sub>1</sub>
SPSCTL	3	MODE	Mode of Operation (Direct, Speakerphone)



### 3.3 Interrupt

The PSB 2170 can generate an interrupt to inform the host of an update of the STATUS register according to table 43. An interrupt mask register (INTM) can be used to disable or enable the interrupting capability of each bit of the STATUS register individually.

**Table 43 Interrupt Source Summary**

STATUS (old)	STATUS (new)	Set by	Reset by
RDY=0	RDY=1	Command completed	Command issued
CIA=0	CIA=1	New Caller ID byte available	CIDCTL0 read or EN=0 <sup>1)</sup>
CD=0	CD=1	Carrier detected	Carrier lost or EN=0
CD=1	CD=0	Carrier lost or EN=0	Carrier detected
ACT=1	ACT=0	Tone generator active	Tone sequence finished or EN=0
DTV=0	DTV=1	DTMF tone detected	DTMF tone lost or EN=0
DTV=1	DTV=0	DTMF tone lost or EN=0	DTMF tone detected
ATV=0	ATV=1	Alert tone detected	Alert tone lost or EN=0
ATV=1	ATV=0	Alert tone lost or EN=0	Alert tone detected
CPT=0	CPT=1	Call progress tone detected	CPT lost
CPT=1	CPT=0	Call progress tone lost or speech detected	CPT detected

<sup>1)</sup> EN=0 denotes unit disable

An interrupt is internally generated if any combination of these events occurs. The interrupt is cleared when the host reads the STATUS register. If a new event occurs while the host reads the status register, the status register is updated *after* the current access is terminated and a new interrupt is generated immediately after the access has ended.

*Note: An interrupt is **not** generated if the microcontroller has started a command and reads the STATUS register with the already updated content. Therefore the controller should always evaluate the relevant bits of the STATUS register after reading it.*

### 3.4 Abort

If the PSB 2170 detects a corrupted configuration (e.g. due to a transient loss of power) it stops operation and initializes all read/write registers to their reset state. The PSB 2170 discards all commands with the exception of a write command to the revision register

while ABT is set. Only after the write command to the revision register (with any value) the ABT bit is reset and a reinitialization can take place.

### 3.5 Hardware Configuration

The PSB 2170 can be adapted to various external hardware configurations by two special registers: HWCONFIG0 and HWCONFIG1. These registers are written once during initialization and must not be changed while the PSB 2170 is in active mode.

### 3.6 Dependencies of Modules

There are some restrictions concerning the modules that can be enabled at the same time (table 44). A checked cell indicates that the two modules (defined by the row and the column of the cell) must not be enabled at the same time.

**Table 44 Dependencies of Modules**

	Subband (normal)	Subband (ISDN)	Subband (enhanced)	Subband (reduced)	Fullband	Comfort Noise	Noise Adaptation	DTMF Detector	Caller ID	Alert Tone Detector	CPT Detector	Line Echo Canceller	Equalizer, DTMF, Tone
Subband (normal)		X	X	X	X	X		X					
Subband (ISDN)	X		X	X	X	X	X	X	X	X	X	X	
Subband (enhanced)	X	X		X	X	X	X	X	X	X	X	X	X
Subband (reduced)	X	X	X		X			<sup>1)</sup>					
Fullband	X	X	X	X									
Comfort Noise	X	X	X					X	X	X	X	X	
Noise Adaptation		X	X						X		X		
DTMF Detector	X	X	X	<sup>1)</sup>		X							
Caller ID		X	X			X	X			X			
Alert Tone Detector		X	X			X			X				
CPT Detector		X	X			X	X						
Line Echo Canceller		X	X			X							
Equalizer 1/2, DTMF/Tone Generator			X										

<sup>1)</sup> Modules can be enabled at the same time. However, deactivation requires proper sequence: First the echo cancellation unit must be disabled, then the DTMF detector.

4 Interfaces

This section describes the interfaces of the PSB 2170. The PSB 2170 supports both an IOM<sup>®</sup>-2 interface with single and double clock mode and a strobed serial data interface (SSDI). However, these two interfaces cannot be used simultaneously as they share some pins. Both interfaces are for data transfer only and cannot be used for programming the PSB 2170. Table 45 lists the features of the two alternative interfaces.

Table 45 SSDI vs. IOM<sup>®</sup>-2 Interface

	IOM <sup>®</sup> -2	SSDI
Signals	4	6
Channels (bidirectional)	2	1
Code	linear PCM, A-law, $\mu$ -law	linear PCM (16 bit)
Synchronization within frame	by timeslot (programmable)	by signal (DXST, DRST)

4.1 IOM<sup>®</sup>-2 Interface

The data stream is partitioned into packets called frames. Each frame is divided into a fixed number of timeslots. Each timeslot is used to transfer 8 bits. Figure 44 shows a commonly used terminal mode (three channels  $ch_0$ ,  $ch_1$  and  $ch_2$  with four timeslots each).

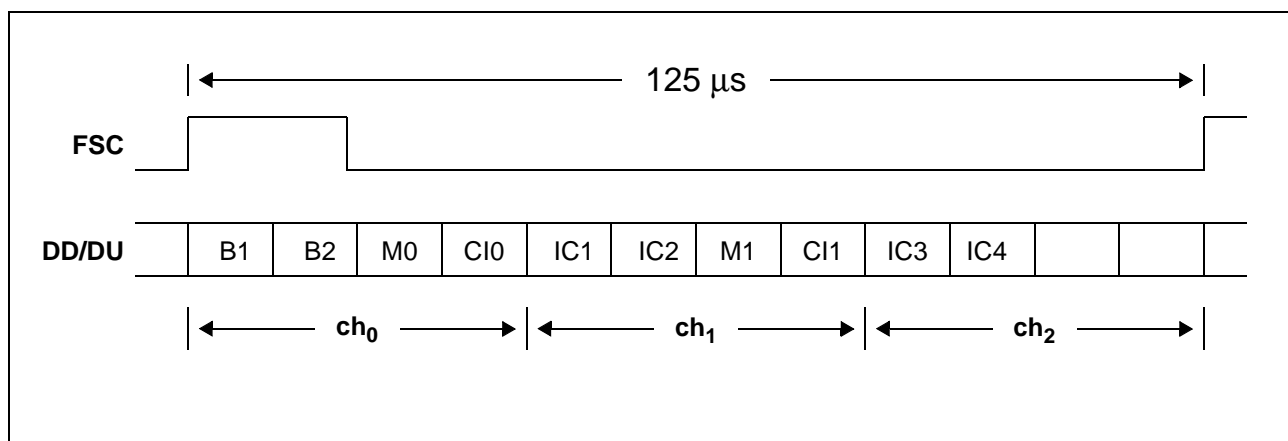
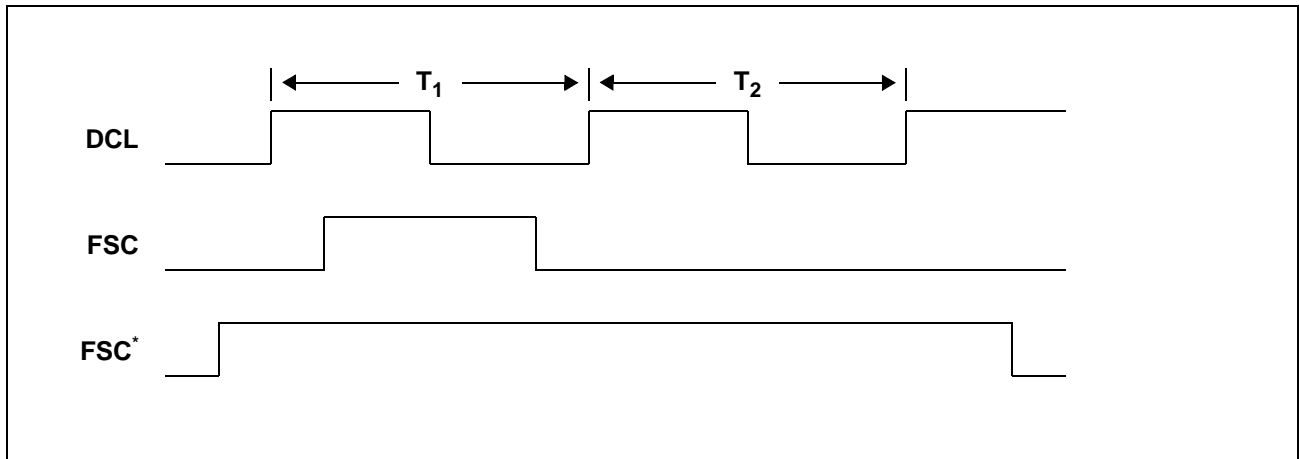


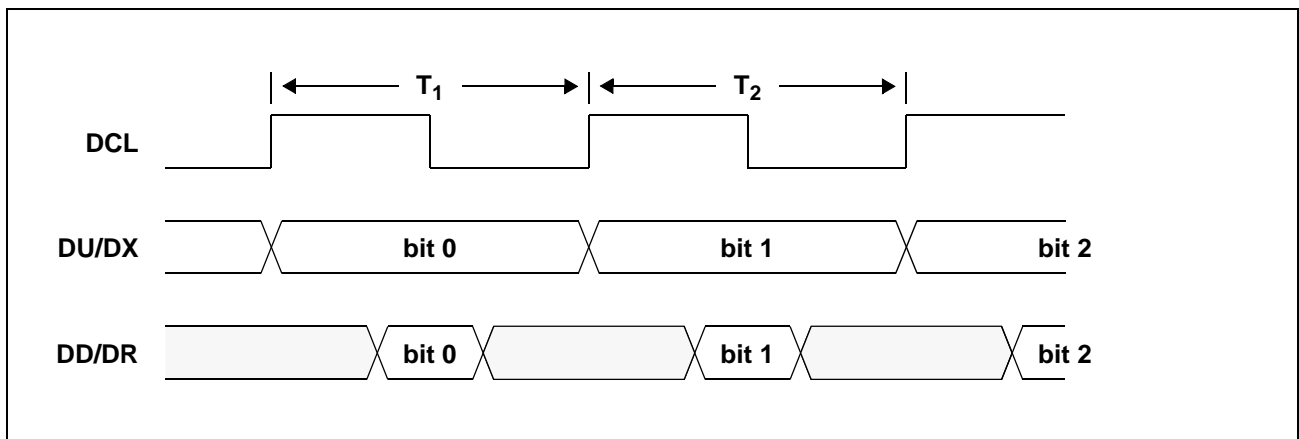
Figure 44 IOM<sup>®</sup>-2 Interface - Frame Structure

The signal FSC is used to indicate the start of a frame. Figure 45 shows as an example two valid FSC-signals (FSC, FSC<sup>\*</sup>) which both indicate the same clock cycle as the first clock cycle of a new frame ( $T_1$ ).

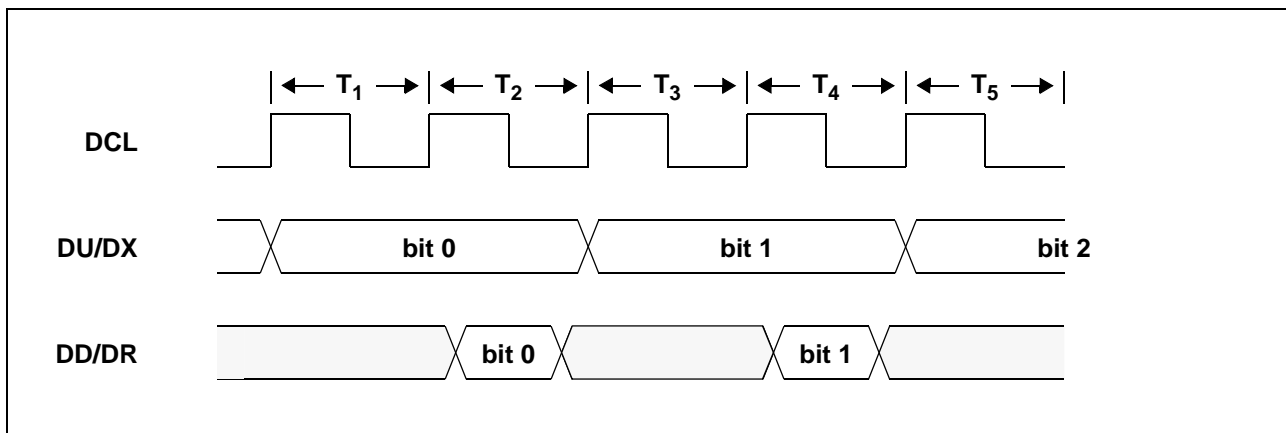


**Figure 45 SSDI/IOM<sup>®</sup>-2 Interface - Frame Start**

The PSB 2170 supports both single clock mode and double clock mode. In single clock mode, the bit rate is equal to the clock rate. Bits are shifted out with the rising edge of DCL and sampled at the falling edge. In double clock mode, the clock runs at twice the bit rate. Therefore for each bit there are two clock cycles. Bits are shifted out with the rising edge of the first clock cycle and sampled with the falling edge of the second clock cycle. Figure 46 shows the timing for single clock mode and figure 47 shows the timing for double clock mode.



**Figure 46 IOM<sup>®</sup>-2 Interface - Single Clock Mode**



**Figure 47 IOM<sup>®</sup>-2 Interface - Double Clock Mode**

The PSB 2170 supports up to two channels simultaneously for data transfer. Both the coding (PCM or linear) and the data direction (DD/DU assignment for transmit/receive) can be programmed individually for each channel. Table 46 shows the registers used for configuration of the IOM<sup>®</sup>-2 interface.

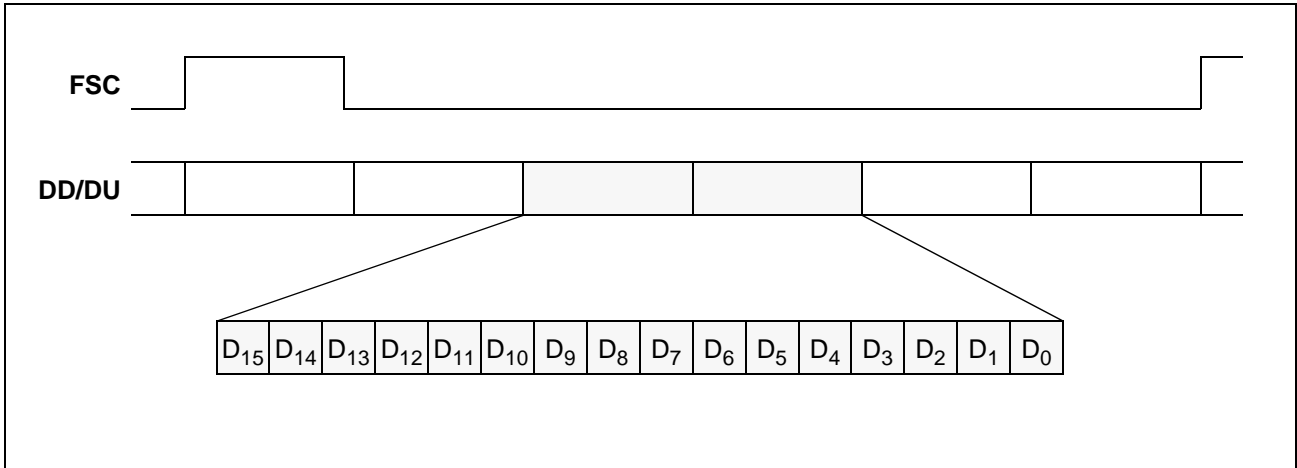
**Table 46 IOM<sup>®</sup>-2 Interface Registers**

Register	# of Bits	Name	Comment
SDCONF	1	EN	Interface enable
SDCONF	1	DCL	Selection of clock mode
SDCONF	6	NTS	Number of timeslots within frame
SDCHN1	1	EN	Channel 1 enable
SDCHN1	6	TS	First timeslot (channel 1)
SDCHN1	1	DD	Data Direction (channel 1)
SDCHN1	1	PCM	8 bit code or 16 bit linear PCM (channel 1)
SDCHN1	1	PCD	8 bit code (A-law or $\mu$ -law, channel 1)
SDCHN2	1	EN	Channel 2 enable
SDCHN2	6	TS	First timeslot (channel 2)
SDCHN2	1	DD	Data Direction (channel 2)
SDCHN2	1	PCM	8 bit code or 16 bit linear PCM (channel 2)
SDCHN2	1	PCD	8 bit code (A-law or $\mu$ -law, channel 2)

In A-law or  $\mu$ -law mode, only 8 bits are transferred and therefore only one timeslot is needed for a channel. In linear mode, 16 bits are needed for a single channel. In this mode, two consecutive timeslots are used for data transfer. Bits 8 to 15 are transferred within the first timeslot and bits 0 to 7 are transferred within the next timeslot. The first

Interfaces

timeslot must have an even number. Figure 48 shows as an example a single channel in linear mode occupying timeslots 2 and 3. Each frame consists of six timeslots and single clock mode is used.



**Figure 48 IOM<sup>®</sup>-2 Interface - Channel Structure**

At this rate the data is shifted out with the rising edge of the clock and sampled at the falling edge. The data clock runs at 384 kHz (six timeslots with 8 bit each within 125 μs).

### 4.2 SSDI Interface

The SSDI interface is intended for seamless connection to low-cost burst mode controllers (e.g. PMB 27251) and supports a single channel in each direction. The data stream is partitioned into frames. Within each frame one 16 bit value can be sent and received by the PSB 2170. The start of a frame is indicated by the rising edge of FSC. Data is always latched at the falling edge of DCL and output at the rising edge of DCL.

The SSDI transmitter and receiver are operating independently of each other except that both use the same FSC and DCL signal.

#### 4.2.1 SSDI Interface - Transmitter

The PSB 2170 indicates outgoing data (on signal DX) by activating DXST for 16 clocks. The signal DXST is activated with the same rising edge of DCL that is used to send the first bit (Bit 15) of the data. DXST is deactivated with the first rising edge of DCL after the last bit has been transferred. The PSB 2170 drives the signal DX only when DXST is activated. Figure 49 shows the timing for the transmitter.

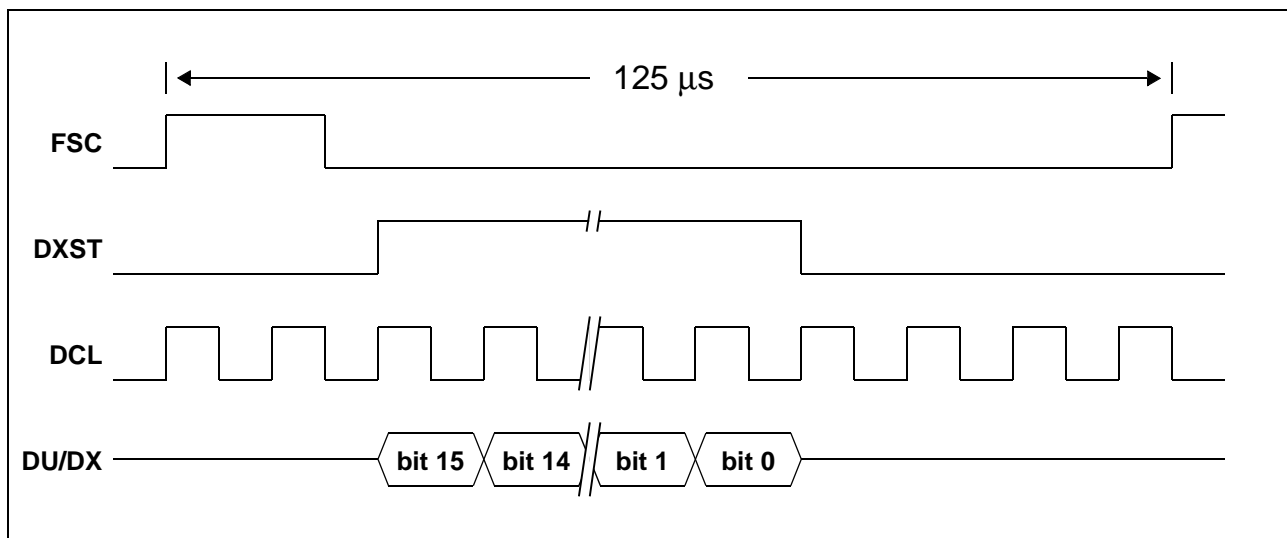


Figure 49 SSDI Interface - Transmitter Timing

#### 4.2.2 SSDI Interface - Receiver

Valid data is indicated by an active DRST pulse. Each DRST pulse must last for exactly 16 DCL clocks. As there may be more than one DRST pulses within a single frame the PSB 2170 can be programmed to listen to the n-th pulse with n ranging from 1 to 16. In order to detect the first pulse properly, DRST must not be active at the rising edge of FSC. In figure 51 the PSB 2170 is listening to the third DRST pulse (n=3).

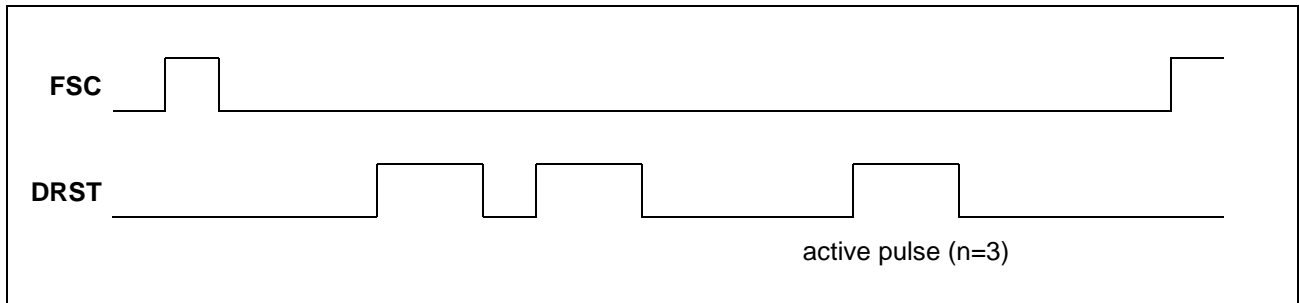


Figure 50 SSDI Interface - Active Pulse Selection

Figure 51 shows the timing for the SSDI receiver.

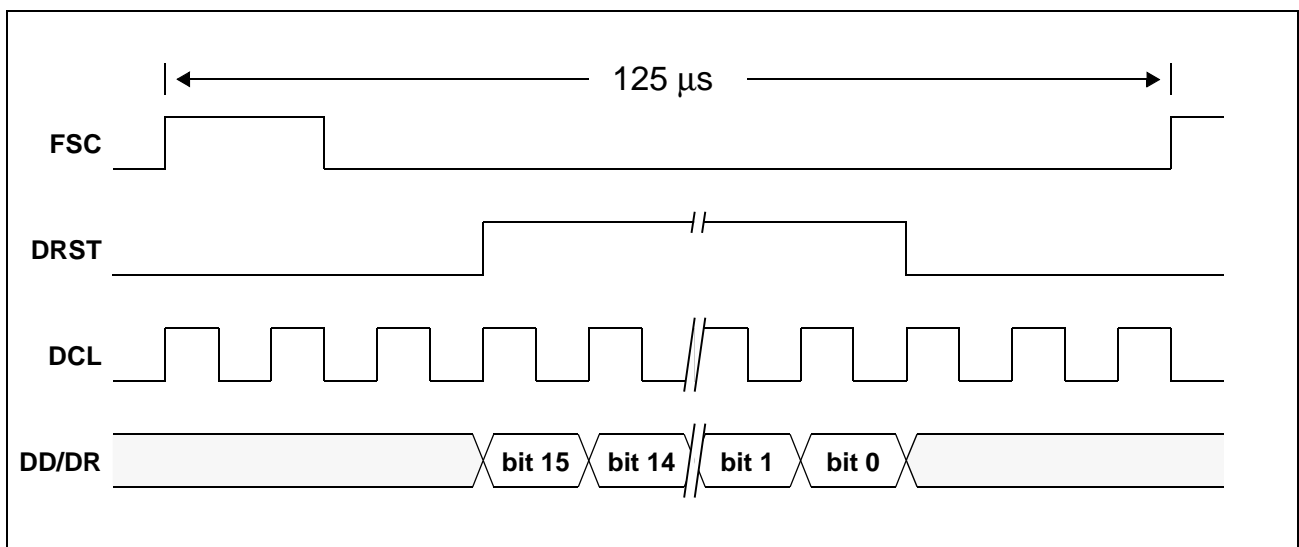


Figure 51 SSDI Interface - Receiver Timing

Table 47 shows the registers used for configuration of the SSDI interface.

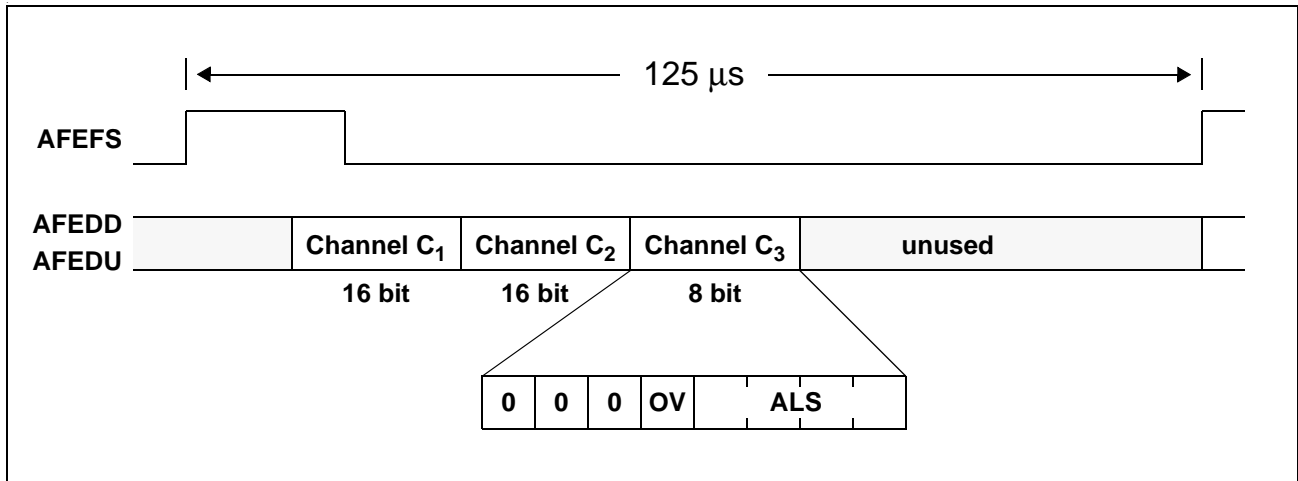
Table 47 SSDI Interface Register

Register	# of Bits	Name	Comment
SDCHN1	4	NAS	Number of active DRST strobe



**4.3 Analog Front End Interface**

The PSB 2170 uses a four wire interface similar to the IOM<sup>®</sup>-2 interface to exchange information with the analog front end (PSB 4851). The main difference is that all timeslots and the channel assignments are fixed as shown in figure 52.



**Figure 52 Analog Front End Interface - Frame Structure**

Voice data is transferred in 16 bit linear coding in two bidirectional channels C<sub>1</sub> and C<sub>2</sub>. An auxiliary channel C<sub>3</sub> is used to transfer the current setting of the loudspeaker amplifier ALS to the PSB 2170. The remaining bits are fixed to zero. In the other direction C<sub>3</sub> transfers an override value for ALS from the PSB 2170 to the PSB 4851. An additional override bit OV determines if the currently transmitted value should override the AOAR:LSC<sup>1)</sup> setting. The AOAR:LSC setting is not affected by C<sub>3</sub>:ALS override. Table 48 shows the source control of the gain for the ALS amplifier.

**Table 48 Control of ALS Amplifier**

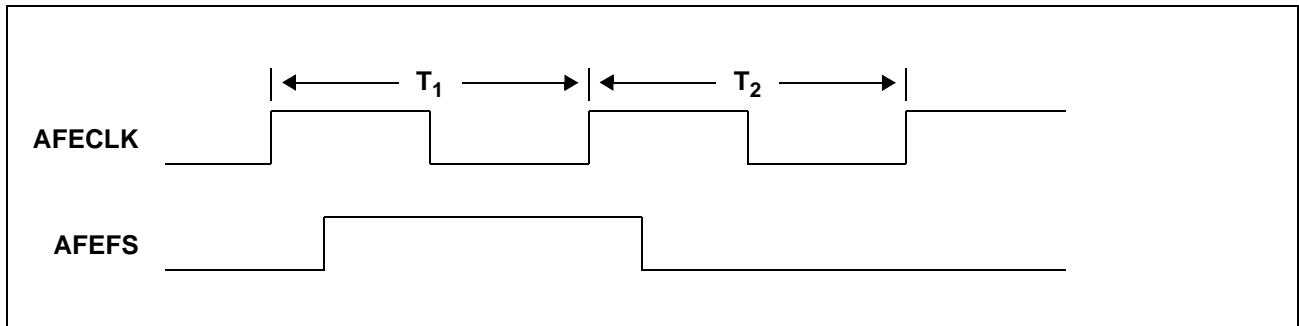
AOPR:OVRE	C <sub>3</sub> :OV	Gain of ALS amplifier
0	-	AOAR:LSC
1	0	AOAR:LSC
1	1	C <sub>3</sub> :ALS

Furthermore the AFE interface can be enabled or disabled according to table 49.

**Table 49 Analog Front End Interface Register**

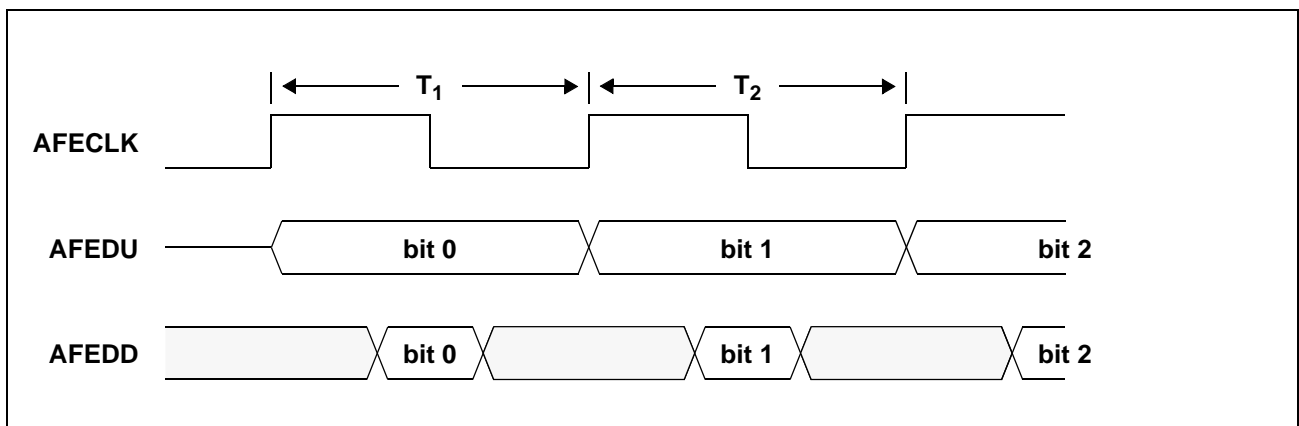
Register	# of Bits	Name	Comment
AFECTL	1	EN	Interface enable

<sup>1)</sup> See specification of PSB 4851



**Figure 53 Analog Front End Interface - Frame Start**

Figure 53 shows the synchronization of a frame by AFEFS. The first clock of a new frame ( $T_1$ ) is indicated by AFEFS switching from low to high before the falling edge of  $T_1$ . AFEFS may remain high during subsequent cycles up to  $T_{32}$ .



**Figure 54 Analog Front End Interface - Data Transfer**

The data is shifted out with the rising edge of AFECLK and sampled at the falling edge of AFECLK (figure 54). If AOPR:OVRE is not set, the channel  $C_3$  is not used by the PSB 4851. All values ( $C_1$ ,  $C_2$ ,  $C_3$ :ALS) are transferred MSB first. The data clock (AFECLK) rate is fixed at 6.912 MHz. Table 50 shows the clock cycles used for the three channels.

**Table 50 Analog Front End Interface Clock Cycles**

Clock Cycles	AFEDD (driven by PSB 2170)	AFEDU (driven by PSB 4851)
$T_1$ - $T_{16}$	$C_1$ data	$C_1$ data
$T_{17}$ - $T_{32}$	$C_2$ data	$C_2$ data
$T_{33}$ - $T_{40}$	$C_3$ data	$C_3$ data
$T_{41}$ - $T_{864}$	0	tristate

### 4.4 Serial Control Interface

The serial control interface (SCI) uses four lines. Data is transferred by the lines SDR and SDX at the rate given by SCLK. The falling edge of  $\overline{CS}$  indicates the beginning of an access. Data is sampled by the PSB 2170 at the rising edge of SCLK and shifted out at the falling edge of SCLK. Each access must be terminated by a rising edge of CS.

Data to and from the PSB 2170 is transferred in words (16 bits). A word is considered valid after every 16th rising edge of SCLK. The accesses to the PSB 2170 can be divided into three classes:

- Configuration Read/Write
- Status/Data Read
- Register Read/Write

If the PSB 2170 is in power down mode, a read access to the status register does not deliver valid data with the exception of the RDY bit. After the status has been read the access can be either terminated or extended to read data from the PSB 2170.

A register read/write access can only be performed when the PSB 2170 is ready. The RDY bit in the status register provides this information.

Any access to the PSB 2170 starts with the transfer of 16 bits to the PSB 2170 over line SDR. This first word specifies the access class, access type (read or write) and, if necessary, the register accessed. If a configuration register is written, the first word also includes the data and the access is terminated. Likewise, if a register read is issued, the access is terminated after the first word (figure 59). All other accesses continue by the transfer of the status register from the PSB 2170 over line SDX. If a register (excluding configuration) is to be written, the next 16 bits containing the data are transferred over line SDR and the access is terminated. Figures 55 to 58 show the timing diagrams for the different access classes and types to the PSB 2170.

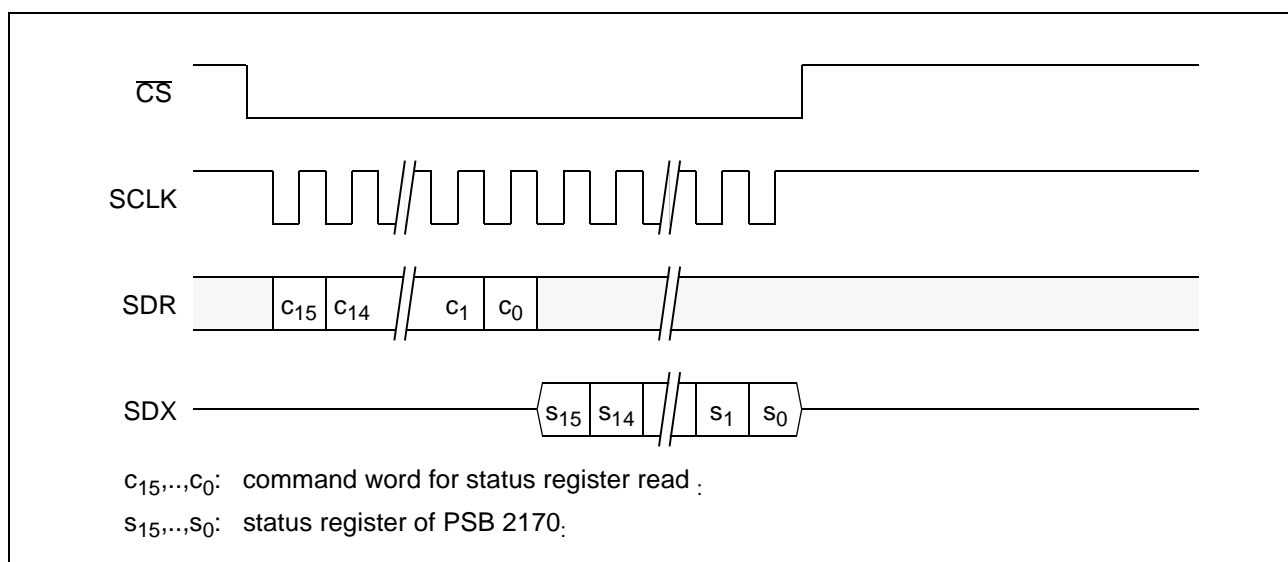


Figure 55 Status Register Read Access

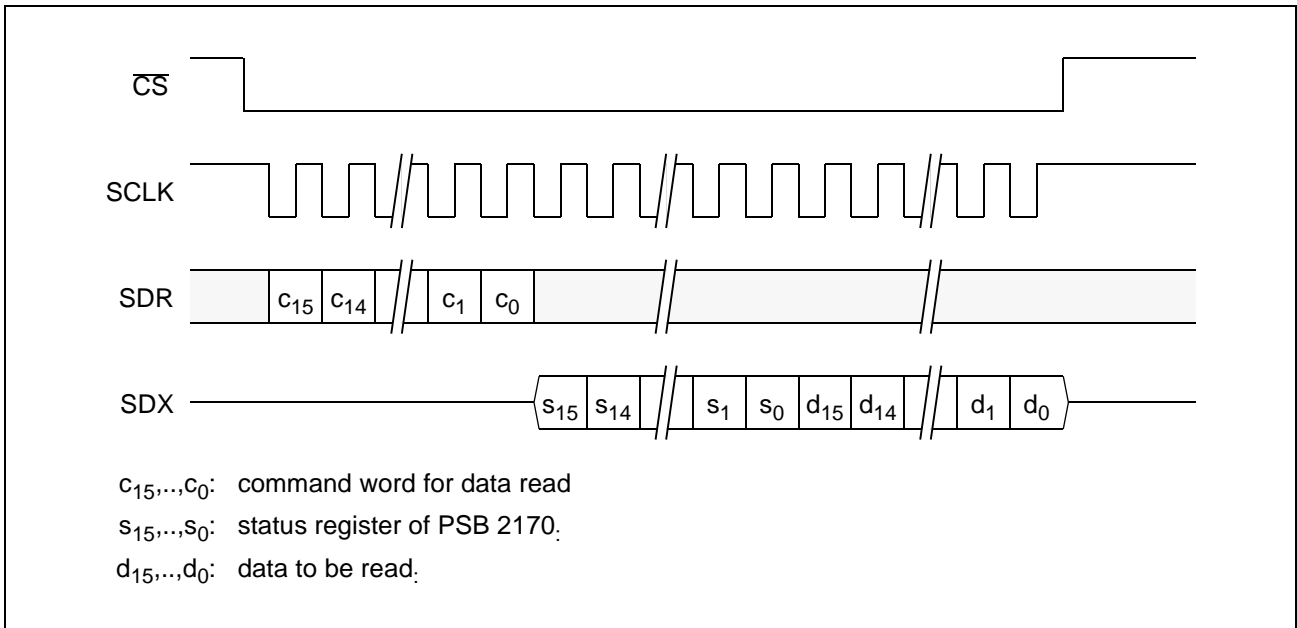


Figure 56 Data Read Access

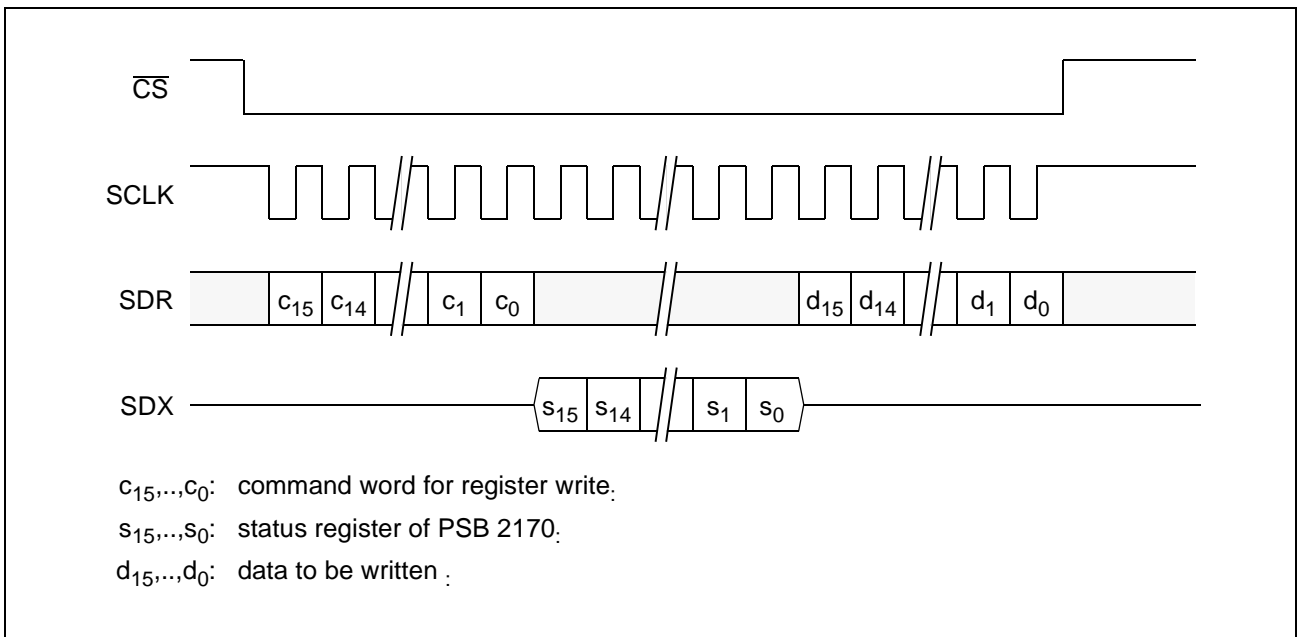
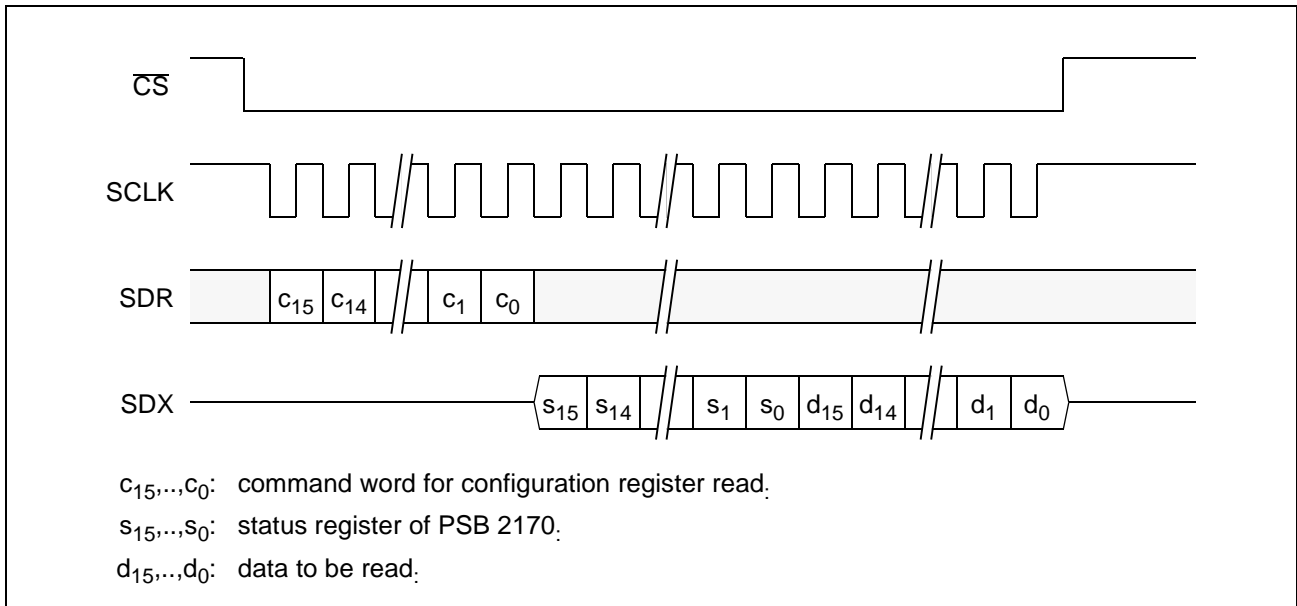
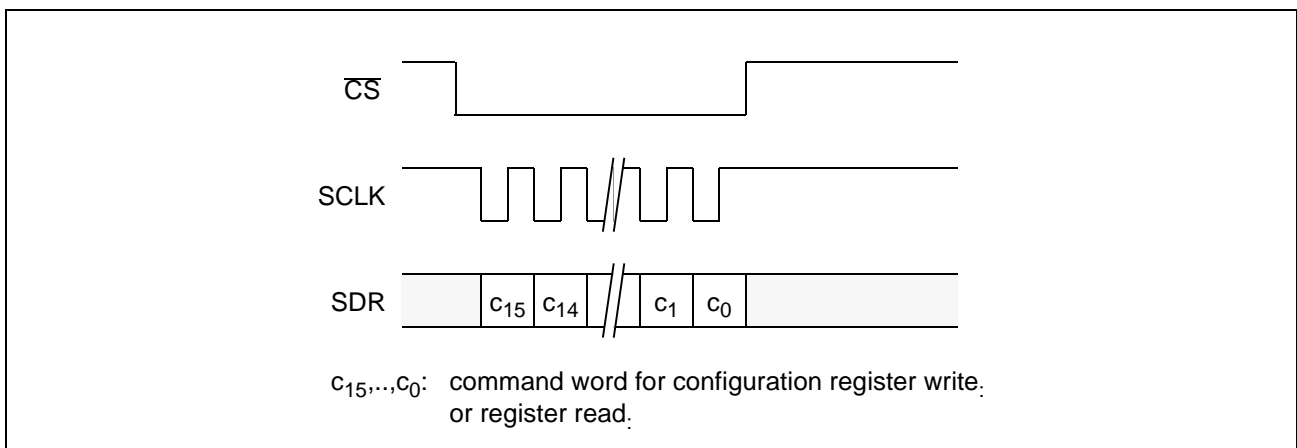


Figure 57 Register Write Access



**Figure 58 Configuration Register Read Access**

The configuration register 0 uses bit positions  $d_{15}$ - $d_8$  while the configuration register 1 uses bit positions  $d_7$ - $d_0$ .



**Figure 59 Configuration Register Write Access or Register Read Command**

The internal interrupt signal is cleared when the first bit of the status register is put on SDX. However, externally the signal  $\overline{INT}$  is deactivated as long as  $\overline{CS}$  stays low. If the internal interrupt signal is not cleared or another event causing an interrupt occurs while the microcontroller is already reading the status belonging to the first event then INT goes low again immediately after  $\overline{CS}$  is removed. Table 51 shows the formats of the different command words. All other command words are reserved.

**Table 51 Command Words for Register Access**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read Status Register or Data Read Access	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0
Read Register	0	1	0	1	REG											
Write Register	0	1	0	0	REG											
Read Configuration Reg.	0	1	1	1	0	0	R	0	0	0	0	0	0	0	0	0
Write Configuration Reg.	0	1	1	0	0	0	W	DATA								

In case of a configuration register write, W determines which configuration register is to be written (table 52):

**Table 52 Address Field W for Configuration Register Write**

9	8	Register
0	0	HWCONFIG 0
0	1	HWCONFIG 1
1	0	HWCONFIG 2
1	1	HWCONFIG 3

In case of a configuration register read, R determines which pair of configuration registers is to be read (table 53):

**Table 53 Address Field R for Configuration Register Read**

9	Register pair
0	HWCONFIG 0 / HWCONFIG 1
1	HWCONFIG 2 / HWCONFIG 3

*Note: Reading any register except the status register or a hardware configuration register requires at least two accesses. The first access is a register read command (figure 59). With this access the register address is transferred to the. After that access data read accesses (figure 56) must be executed. The first data read access with STATUS:RDY=1 delivers the value of the register.*

## 4.5 General Purpose Parallel Port

The PSB 2170 provides a general purpose parallel port (GP<sub>0</sub> to GP<sub>15</sub>). The  $\mu$ C can read/write each line individually. This port has two modes: static mode and multiplex mode.

### 4.5.1 Static Mode

In static mode all pins of the general parallel port have identical functionality. Any pin can be configured as an output or an input. Pins configured as outputs provide a static signal as programmed by the controller. Pins configured as inputs are monitoring the signal continuously without latching. The controller always reads the current value. Table 54 shows the registers used for static mode.

**Table 54 Static Mode Registers**

Register	# of bits	Comment
CCTL	2	Enable Port
DOUT3	16	Output signals (for pins configured as outputs)
DIN	16	Input signals (for pins configured as inputs)
DDIR	16	Pin direction

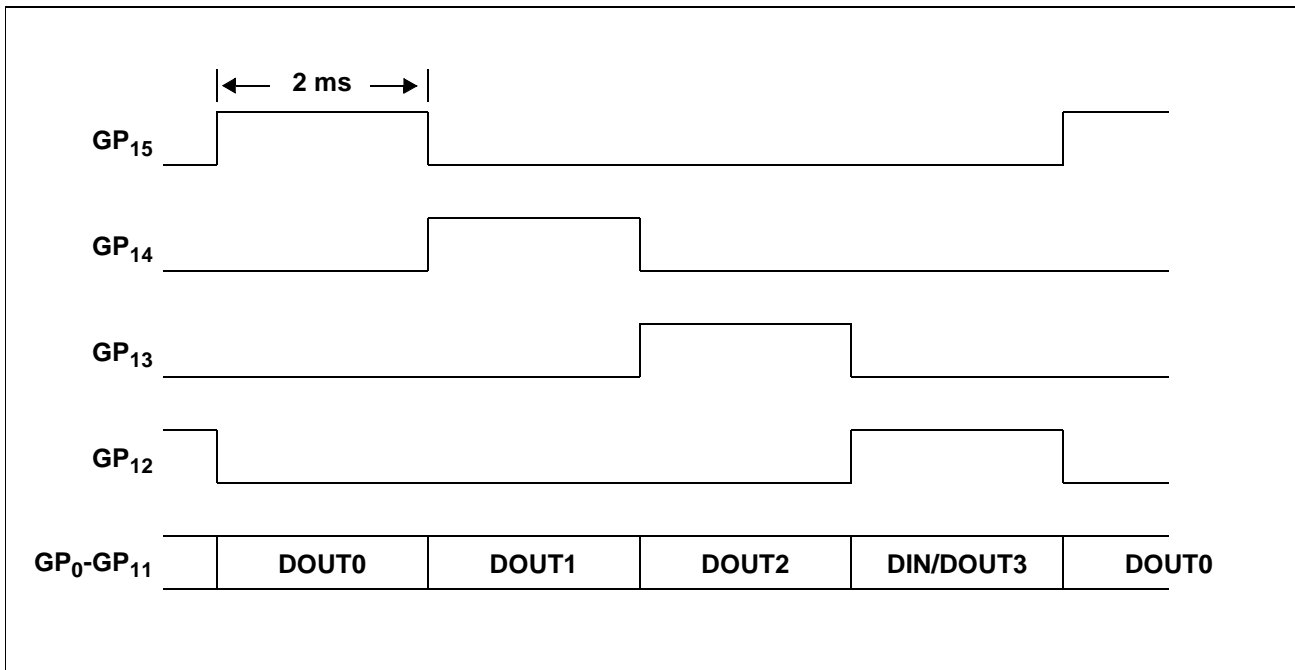
### 4.5.2 Multiplex Mode

In multiplex mode, the PSB 2170 uses GP<sub>12</sub>-GP<sub>15</sub> to distinguish four timeslots. Each timeslot has a duration of approximately 2 ms. The timeslots are separated by a gap of approximately 125  $\mu$ s in which none of the signals at GP<sub>12</sub>-GP<sub>15</sub> are active. The PSB 2170 multiplexes three more output registers to MA<sub>0</sub>-MA<sub>11</sub> in timeslots 0, 1 and 2. In timeslot 3 the direction of the pins can be programmed. For input pins, the signal is latched at the falling edge of MA<sub>15</sub>. Table 55 shows the registers used for multiplex mode.

**Table 55 Multiplex Mode Registers**

Register	# of bits	Comment
CCTL	2	Enable Port
DOUT0	12	Output signals on GP <sub>0</sub> -GP <sub>11</sub> while GP <sub>15</sub> =1
DOUT1	12	Output signals on GP <sub>0</sub> -GP <sub>11</sub> while GP <sub>14</sub> =1
DOUT2	12	Output signals on GP <sub>0</sub> -GP <sub>11</sub> while GP <sub>13</sub> =1
DOUT3	12	Output signals (for pins configured as outputs) while GP <sub>12</sub> =1
DIN	12	Input signals (for pins configured as inputs) at falling edge of GP <sub>12</sub>
DDIR	12	Pin direction during GP <sub>12</sub> =1

Figure 60 shows the timing diagram for multiplex mode.



**Figure 60 General Purpose Parallel Port - Multiplex Mode**

*Note: In either mode the voltage on any pin (GP<sub>0</sub> to GP<sub>15</sub>) must not exceed V<sub>DD</sub>.*



**Detailed Register Description**

**5 Detailed Register Description**

The PSB 2170 has a single status register (read only) and an array of data registers (read/write). The purpose of the status register is to inform the external microcontroller of important status changes of the PSB 2170 and to provide a handshake mechanism for data register reading or writing. If the PSB 2170 generates an interrupt, the status register contains the reason of the interrupt.

**5.1 Status Register**

<b>15</b>											<b>0</b>				
RDY	ABT	0	0	CIA	CD	CPT	0	0	0	0	DTV	ATV	ACT	0	0

**RDY Ready**

- 0: The last command (if any) is still in progress.
- 1: The last command has been executed.

*Note: If the PSB 2170 aborts a running command due to external conditions (e.g. power drop-out, EMV) other than reset, it generates an interrupt and resets RDY. In this case the microcontroller should check the ABT bit to avoid locking the system.*

**ABT Abort**

- 0: No exception during operation
- 1: Some exception other than reset caused the PSB 2170 to abort any operation currently in progress. The external microcontroller should reinitialize the PSB 2170 to ensure proper operation. The ABT bit is cleared by writing any value to register REV. No other command is accepted by the PSB 2170 while ABT is set.

**CIA Caller ID Available**

- 0: No new data for caller ID
- 1: New caller ID byte available

**CD Carrier Detect**

- 0: No carrier detected
- 1: Carrier detected

**CPT Call Progress Tone**

- 0: Currently no call progress tone detected or pause detected (raw mode)

---

**Detailed Register Description**

1: Currently a call progress is detected

**DTV DTMF Tone Valid**

0: No new DTMF code available

1: New DTMF code available in DDCTL

**ATV Alert Tone Valid**

0: No new alert tone code available

1: New alert tone code available in ATDCTL0

**ACT Tone Generator Status**

0: Tone Generator not running

1: Tone Generator running

## Detailed Register Description

## 5.2 Hardware Configuration Registers

## HWCONFIG 0 - Hardware Configuration Register 0

7							0
PD	ACS	0	0	PPSDI	0	PPINT	PPSDX

**PPSDX Push/Pull for SDX**

- 0: The SDX pin has open-drain characteristic
- 1: The SDX pin has push/pull characteristic

**PPINT Push/Pull for  $\overline{\text{INT}}$** 

- 0: The  $\overline{\text{INT}}$  pin has open-drain characteristic
- 1: The  $\overline{\text{INT}}$  pin has push/pull characteristic

**PPSDI Push/Pull for SDI interface**

- 0: The DU and DD pins have open-drain characteristic
- 1: The DU and DD pins have push/pull characteristic

**ACS AFE Clock Source**

- 0: AFECLK is derived from the main oscillator
- 1: AFECLK is derived from the CLK input

**PD Power Down (read only)**

- 0: The PSB 2170 is in active mode
- 1: The PSB 2170 is in power down mode

## Detailed Register Description

### HWCONFIG 1 - Hardware Configuration Register 1

7	0
GPP	SSDI

#### **GPP    General Purpose Parallel Port**

7	6	Description
0	0	reserved
0	1	APP static mode
1	0	APP multiplex mode
1	1	reserved

#### **ACT    AFE Clock Tracking**

- 0: AFECLK tracking disabled
- 1: AFECLK tracking enabled

#### **ADS    AFE Double Speed**

- 0: 8 kHz AFEFSC
- 1: 16 kHz AFEFSC

#### **MFS    Master Frame Sync Selection**

- 0: AFEFSC
- 1: FSC

#### **XTAL   XTAL frequency selection**

2	1	Description
0	0	reserved
0	1	31.104 MHz
1	0	27.648 MHz
1	1	reserved

#### **SSDI   SSDI Interface Selection**

- 0: IOM<sup>®</sup>-2 Interface
- 1: SSDI Interface

---

**Detailed Register Description****HWCONFIG 2 - Hardware Configuration Register 2**

<b>7</b>							<b>0</b>
0	ESDX	ESDR	0	0	$\bar{0}$	0	0

**ESDX Edge Select for DX**

- 0: DX is transmitted with the rising edge of DCL
- 1: DX is transmitted with the falling edge of DCL

**ESDR Edge Select for DR**

- 0: DR is latched with the falling edge of DCL
- 1: DR is latched with the rising edge of DCL

**Detailed Register Description**

**HWCONFIG 3 - Hardware Configuration Register 3**

<b>7</b>							<b>0</b>
0	0	0	0	0	0	CM1	CM0

**CM1 Clock Master 1**

0: Clock generation at AFEFS and AFECLK disabled

1: Clock generation at AFEFS and AFECLK enabled

**CM0 Clock Master 0**

0: 512 kHz (AFECLK)

1: 1.536 MHz (AFECLK)

## Detailed Register Description

## 5.3 Read/Write Registers

The following sections contains all read/write registers of the PSB 2170. The register addresses are given as hexadecimal values. Registers marked with an R are affected by reset or a wake up after power down. All other registers retain their previous value. No access must be made to addresses other than those associated with a read/write register.

## 5.3.1 Register Table

Address.	Name	Long Name	Page
00h	REV	Revision.....	100
01h R	CCTL	Chip Control .....	101
02h R	INTM	Interrupt Mask Register .....	102
03h R	AFECTL	Analog Front End Interface Control.....	103
04h R	IFS1	Interface Select 1 .....	104
05h R	IFG1	Interface Gain 1 .....	105
06h R	IFG2	Interface Gain 2.....	106
07h R	IFS2	Interface Select 2 .....	107
08h R	IFG3	Interface Gain 3.....	108
09h R	IFG4	Interface Gain 4.....	109
0Ah R	SDCONF	Serial Data Interface Configuration .....	110
0Bh R	SDCHN1	Serial Data Interface Channel 1 .....	111
0Ch R	IFS3	Interface Select 3 .....	113
0Dh R	SDCHN2	Serial Data Interface Channel 2 .....	114
0Eh R	IFS4	Interface Select 4 .....	115
0Fh R	IFG5	Interface Gain 5.....	116
10h R	UA	Universal Attenuator.....	117
11h R	DGCTL	DTMF Generator Control.....	118
12h	DGF1	DTMF Generator Frequency 1 .....	119
13h	DGF2	DTMF Generator Frequency 2 .....	120
14h	DGL	DTMF Generator Level.....	121
15h	DGATT	DTMF Generator Attenuation .....	122
1Ah R	ATDCTL0	Alert Tone Detection 0.....	123
1Bh	ATDCTL1	Alert Tone Detection 1.....	124
1Ch R	CIDCTL0	Caller ID Control 0.....	125
1Dh	CIDCTL1	Caller ID Control 1 .....	126
20h R	CPTCTL	Call Progress Tone Control .....	127
21h	CPTTR	Call Progress Tone Thresholds.....	128
22h	CPTMN	CPT Minimum Times.....	129
23h	CPTMX	CPT Maximum Times.....	130
24h	CPTDT	CPT Delta Times .....	131
25h R	LECCTL	Line Echo Cancellation Control .....	132
26h	LECLEV	Minimal Signal Level for Line Echo Cancellation .....	133

**Detailed Register Description**

27h	LECATT	Externally Provided Attenuation.....	134
28h	LECMGN	Margin for Double Talk Detection.....	135
29h R	DDCTL	DTMF Detector Control.....	136
2Ah	DDTW	DTMF Detector Signal Twist.....	137
2Bh	DDLEV	DTMF Detector Minimum Signal Level.....	138
2ChR	FCFCTL1	Equalizer 1 Control.....	139
2Dh	FCFCOF1	Equalizer 1 Coefficient Data.....	141
2Eh R	FCFCTL2	Equalizer 2 Control.....	142
2Fh	FCFCOF2	Equalizer 2 Coefficient Data.....	144
30h R	TGCTL	Tone Generator Control.....	145
31h	TGTON	Tone Generator Time TON.....	146
32h	TGTOFF	Tone Generator Time TOFF.....	147
33h	TGT1	Tone Generator Time T1.....	148
34h	TGF1	Tone Generator Frequency F1.....	149
35h	TGG1	Tone Generator Gain G1.....	150
36h	TGT2	Tone Generator Time T2.....	151
37h	TGF2	Tone Generator Frequency F2.....	152
38h	TGG2	Tone Generator Gain G2.....	153
39h	TGT3	Tone Generator Time T3.....	154
3Ah	TGF3	Tone Generator Frequency F3.....	155
3Bh	TGG3	Tone Generator Gain G3.....	156
3Ch	TGF4	Tone Generator Frequency F4.....	157
3Dh	TGG4	Tone Generator Gain G4.....	158
3Eh	TGGO1	Tone Generator Gain Output 1.....	159
3Fh	TGGO2	Tone Generator Gain Output 2.....	160
47h R	SPSCTL	SPS Control.....	161
4Ah	DOU0	Data Out (Timeslot 0).....	162
4Bh	DOU1	Data Out (Timeslot 1).....	163
4Ch	DOU2	Data Out (Timeslot 2).....	164
4Dh	DOU3	Data Out (Timeslot 3 or Static Mode).....	165
4Eh	DIN	Data In (Timeslot 3 or Static Mode).....	166
4Fh	DDIR	Data Direction (Timeslot 3 or Static Mode).....	167
60h R	SCTL	Speakerphone Control.....	168
62h R	SSRC1	Speakerphone Source 1.....	170
63h R	SSRC2	Speakerphone Source 2.....	171
64h	SSDX1	Speech Detector (Transmit) 1.....	172
65h	SSDX2	Speech Detector (Transmit) 2.....	173
66h	SSDX3	Speech Detector (Transmit) 3.....	174
67h	SSDX4	Speech Detector (Transmit) 4.....	175
68h	SSDR1	Speech Detector (Receive) 1.....	176
69h	SSDR2	Speech Detector (Receive) 2.....	177
6Ah	SSDR3	Speech Detector (Receive) 3.....	178
6Bh	SSDR4	Speech Detector (Receive) 4.....	179



## Detailed Register Description

6Ch	SSCAS1	Speech Comparator (Acoustic Side) 1 .....	180
6Dh	SSCAS2	Speech Comparator (Acoustic Side) 2 .....	181
6Eh	SSCAS3	Speech Comparator (Acoustic Side) 3 .....	182
6Fh	SSCLS1	Speech Comparator (Line Side) 1 .....	183
70h	SSCLS2	Speech Comparator (Line Side) 2 .....	184
71h	SSCLS3	Speech Comparator (Line Side) 3 .....	185
72h	SATT1	Attenuation Unit 1 .....	186
73h	SATT2	Attenuation Unit 2 .....	187
74h	SAGX1	Automatic Gain Control (Transmit) 1 .....	188
75h	SAGX2	Automatic Gain Control (Transmit) 2 .....	189
76h	SAGX3	Automatic Gain Control (Transmit) 3 .....	190
77h	SAGX4	Automatic Gain Control (Transmit) 4 .....	191
78h	SAGX5	Automatic Gain Control (Transmit) 5 .....	192
79h	SAGR1	Automatic Gain Control (Receive) 1 .....	193
7Ah	SAGR2	Automatic Gain Control (Receive) 2 .....	194
7Bh	SAGR3	Automatic Gain Control (Receive) 3 .....	195
7Ch	SAGR4	Automatic Gain Control (Receive) 4 .....	196
7Dh	SAGR5	Automatic Gain Control (Receive) 5 .....	197
7Eh	SLGA	Line Gain .....	198
80h	SAELEN	Acoustic Echo Cancellation Length .....	199
81h	SAEATT	Acoustic Echo Cancellation Double Talk Attenuation .....	200
82h	SAEGS	Acoustic Echo Cancellation Global Scale .....	201
83h	SAEPS	Acoustic Echo Cancellation Partial Scale .....	202
84h	SAEBL	Acoustic Echo Cancellation First Block .....	203
85h	SAEWFL	Wiener Filter Limit Attenuation .....	204
86h	SAEWFT	Wiener Filter Transition Time .....	205
90h	SCSD1	Speech Detector (Comfort Noise) 1 .....	206
91h	SCSD2	Speech Detector (Comfort Noise) 2 .....	207
92h	SCSD3	Speech Detector (Comfort Noise) 3 .....	208
93h	SCSD4	Speech Detector (Comfort Noise) 4 .....	209
94h	SCLPT	Low Pass Time Constant .....	210
95h	SCCR	Correlation .....	211
96h	SCCRN	Correlation Noise Threshold .....	212
97h	SCCRS	Correlation Sensitivity .....	213
98h	SCCRL	Correlation Limit .....	214
99h	SCDT	Double Talk Detection .....	215
9Ah	SCDTN	Double Talk Detection Threshold .....	216
9Bh	SCDTS	Double Talk Sensitivity .....	217
9Ch	SCDTL	Double Talk Limit .....	218
9Dh	SCATTN	Attenuation Noise .....	219
9Eh	SCATTS	Attenuation Sensitivity .....	220
9Fh	SCATTL	Attenuation Limit .....	221
A0h	SCAECL	Global Attenuation Limit (Full Duplex Speakerphone) .....	222

Detailed Register Description

A1h	SCSTGP	Single Talk Gap Time.....	223
A2h	SCSTATT	Single Talk Attenuation .....	224
A3h	SCSTNL	Single Talk Noise Level.....	225
A4h	SCSTS	Single Talk Sensitivity .....	226
A5h	SCSTTIM	Single Talk Time .....	227
A6h	SCSTIS	Single Talk Attack Speed.....	228
A7h	SCSTDS	Single Talk Decay Speed.....	229
A8h	SCLSPN	Loudspeaker Noise .....	230
A9h	SCLSPS	Loudspeaker Sensitivity .....	231
AAh	SCLSPL	Loudspeaker Limit.....	232
ABh	SCCN1	Comfort Noise Constant Level .....	233
ACh	SCCN2	Comfort Noise Multiplication Factor .....	234
ADh	SCCN3	Comfort Noise Low Pass.....	235

Note: Registers CCTL is only affected by reset. For SPSCTL see the register description.

5.3.2 Register Naming Conventions

Several registers contain one or more fields for input signal selection. All fields labelled I<sub>1</sub> (I<sub>2</sub>, I<sub>3</sub>) are five bits wide and use the same coding as shown in table 56.

Table 56 Signal Encoding

4	3	2	1	0	Signal	Description
0	0	0	0	0	S <sub>0</sub>	Silence
0	0	0	0	1	S <sub>1</sub>	Analog line input (channel 1 of PSB 4851 interface)
0	0	0	1	0	S <sub>2</sub>	Analog line output (channel 1 of PSB 4851 interface)
0	0	0	1	1	S <sub>3</sub>	Microphone input (channel 2 of PSB 4851 interface)
0	0	1	0	0	S <sub>4</sub>	Loudspeaker/Handset output (channel 2 of PSB 4851 interface)
0	0	1	0	1	S <sub>5</sub>	Serial interface input, channel 1
0	0	1	1	0	S <sub>6</sub>	Serial interface output, channel 1
0	0	1	1	1	S <sub>7</sub>	Serial interface input, channel 2
0	1	0	0	0	S <sub>8</sub>	Serial interface output, channel 2
0	1	0	0	1	S <sub>9</sub>	DTMF generator output
0	1	0	1	0	S <sub>10</sub>	DTMF generator auxiliary output
0	1	0	1	1	S <sub>11</sub>	Speakerphone output (acoustic side)
0	1	1	0	0	S <sub>12</sub>	Speakerphone output (line side)

## Detailed Register Description

**Table 56 Signal Encoding**

4	3	2	1	0	Signal	Description
0	1	1	0	1	S <sub>13</sub>	reserved
0	1	1	1	0	S <sub>14</sub>	Universal attenuator output
0	1	1	1	1	S <sub>15</sub>	Line echo canceller output
1	0	0	0	0	S <sub>16</sub>	AGC unit output (after AGC)
1	0	0	0	1	S <sub>17</sub>	AGC unit output (before AGC)
1	0	0	1	0	S <sub>18</sub>	Equalizer 1 output
1	0	0	1	1	S <sub>19</sub>	Equalizer 2 output
1	0	1	0	0	S <sub>20</sub>	Tone generator output 1
1	0	1	0	1	S <sub>21</sub>	Tone generator output 2
1	0	1	1	-		reserved
1	1	-	-	-		reserved

## Detailed Register Description

**00<sub>h</sub>**    **REV**            **Revision**

<b>15</b>																	<b>0</b>
0	0	1	1	0	0	0	0	- <sup>1)</sup>	-	-	-	-	-	-	-		

<sup>1)</sup> undefined

The revision register can only be read.

*Note: A write access to the revision register does not alter its content. It does, however, reset the ABT bit of the STATUS register.*

## Detailed Register Description

**01<sub>h</sub> CCTL Chip Control**

<b>15</b>												<b>0</b>			
0	0	0	0	0	0	0	PD	0	0	0	0	GPP	0	0	
Reset Value															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

**PD Power Down**  
 0: PSB 2170 is in active mode  
 1: enter power-down mode

**GPP Enable General Purpose Port**

3	2	Description
0	0	disabled
0	1	reserved
1	0	reserved
1	1	enabled

## Detailed Register Description

### 02<sub>h</sub> INTM Interrupt Mask Register

<b>15</b>														<b>0</b>	
RDY	1	0	0	CIA	CD	CPT	0	0	0	0	DTV	ATV	ACT	0	0
Reset Value															
0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

If a bit of this register is reset (set to 0), the corresponding bit of the status register does not generate an interrupt.

If a bit is set (set to 1), an external interrupt can be generated by the corresponding bit of the status register.

## Detailed Register Description

**03<sub>h</sub> AFECTL Analog Front End Interface Control**

<b>15</b>													<b>0</b>	
0	0	0	0	ALS			0	0	0	0	0	0	0	EN
Reset Value														
0	0	0	0	0			0	0	0	0	0	0	0	0

### ALS Loudspeaker Amplification

This value is transferred on channel C3 of the AFE interface. If the PSB 4851 is used it represents the amplification of the loudspeaker amplifier.

### EN Interface Enable

- 0: AFE interface disabled
- 1: AFE interface enabled

**Detailed Register Description**

**04<sub>h</sub> IFS1 Interface Select 1**

<b>15</b>			<b>0</b>
HP	I1	I2	I3
Reset Value			
0	0	0	0

The signal selection fields I1, I2 and I3 of IFS1 determine the outgoing signal of channel 1 of the analog interface. For the PSB 4851 this is usually the line out signal.

The HP bit enables a high-pass for the incoming signal of channel 1 of the analog interface. For the PSB 4851 this is usually the line in signal.

**HP High-Pass for S<sub>1</sub>**

0: Disabled

1: Enabled

**I1 Input signal 1 for IG2**

**I2 Input signal 2 for IG2**

**I3 Input signal 3 for IG2**

*Note: As all sources are always active, unused sources must be set to 0 (S<sub>0</sub>).*



**Detailed Register Description**

**05<sub>h</sub> IFG1 Interface Gain 1**

<b>15</b>	<b>0</b>
0	IG1
Reset Value	
0	8192 (0 dB)

IFG1 is associated with the incoming signal of channel 1 of the analog interface. For the PSB 4851 this is usually the line in signal.

**IG1**

In order to obtain a gain *G* the parameter IG1 can be calculated by the following formula:

$$IG1 = 32768 \times 10^{(G - 12.04 \text{ dB}) / 20 \text{ dB}}$$

**Detailed Register Description**

**06<sub>h</sub> IFG2 Interface Gain 2**

<b>15</b>	<b>0</b>
0	IG2
Reset Value	
0	8192 (0 dB)

IFG2 is associated with the outgoing signal of channel 1 of the analog interface. For the PSB 4851 this is usually the line out signal.

**IG2 Gain of Amplifier IG2**

In order to obtain a gain G the parameter IG2 can be calculated by the following formula:

$$IG2 = 32768 \times 10^{(G - 12.04 \text{ dB}) / 20 \text{ dB}}$$

## Detailed Register Description

**07<sub>h</sub> IFS2 Interface Select 2**

<b>15</b>			<b>0</b>
HP	I1	I2	I3
Reset Value			
0	0	0	0

The signal selection fields I1, I2 and I3 of IFS2 determine the outgoing signal of channel 2 of the analog interface. For the PSB 4851 this is usually the loudspeaker signal.

The HP bit enables a high-pass for the incoming signal of channel 2 of the analog interface. For the PSB 4851 this is usually the microphone signal.

**HP High-Pass for S<sub>3</sub>**

0: Disabled

1: Enabled

**I1 Input signal 1 for IG4**

**I2 Input signal 2 for IG4**

**I3 Input signal 3 for IG4**

*Note: As all sources are always active, unused sources must be set to 0 (S<sub>0</sub>).*

**Detailed Register Description**

**08<sub>h</sub> IFG3 Interface Gain 3**

<b>15</b>	<b>0</b>
0	IG3
Reset Value	
0	8192 (0 dB)

IFG3 is associated with the incoming signal of channel 2 of the analog interface. For the PSB 4851 this is usually the microphone signal.

**IG3 Gain of Amplifier IG3**

In order to obtain a gain G the parameter IG3 can be calculated by the following formula:

$$IG3 = 32768 \times 10^{(G - 12.04 \text{ dB}) / 20 \text{ dB}}$$

**Detailed Register Description**

**09<sub>h</sub> IFG4 Interface Gain 4**

<b>15</b>	<b>0</b>
0	IG4
Reset Value	
0	8192 (0 dB)

IFG4 is associated with the outgoing signal of channel 2 of the analog interface. For the PSB 4851 this is usually the loudspeaker signal.

**IG4 Gain of Amplifier IG4**

In order to obtain a gain G the parameter IG4 can be calculated by the following formula:

$$IG4 = 32768 \times 10^{(G - 12.04 \text{ dB}) / 20 \text{ dB}}$$

## Detailed Register Description

### 0A<sub>h</sub> SDCONF Serial Data Interface Configuration

<div style="display: flex; justify-content: space-between; width: 100%;"> <span><b>15</b></span> <span><b>0</b></span> </div>										
0	0	NTS	0	0	0	0	0	DCL	0	EN
Reset Value										
0	0	0	0	0	0	0	0	0	0	0

#### NTS Number of Timeslots

11	10	9	8	7	6	Description
0	0	0	0	0	0	1
0	0	0	0	0	1	2
...	...	...	...	...	...	...
1	1	1	1	1	1	64

#### DCL Double Clock Mode

- 0: Single Clock Mode
- 1: Double Clock Mode

#### EN Enable Interface

- 0: Interface is disabled (both channels)
- 1: Interface is enabled (depending on separate channel enable bits)

## Detailed Register Description

### 0B<sub>h</sub> SDCHN1 Serial Data Interface Channel 1

15

0

NAS	0	0	PCD	EN	PCM	DD	TS
-----	---	---	-----	----	-----	----	----

Reset Value

0	0	0	0	0	0	0	0
---	---	---	---	---	---	---	---

#### NAS Number of active DRST strobe (SSDI interface mode)

15	14	13	12	Description
0	0	0	0	1
...	...	...	...	...
1	1	1	1	16

#### PCD PCM Code

0: A-law

1:  $\mu$ -law

#### EN Enable Interface

0: Interface is disabled

1: Interface is enabled if SDCONF:EN=1

#### PCM PCM Mode

0: 16 Bit Linear Coding (two timeslots)

1: 8 Bit PCM Coding (one timeslot)

#### DD Data Direction

0: DD: Data Downstream, DU: Data Upstream

1: DD: Data Upstream, DU: Data Downstream

#### TS Timeslot for Channel 1

5	4	3	2	1	0	Description
0	0	0	0	0	0	0
...	...	...	...	...	...	...
1	1	1	1	1	1	63

---

**Detailed Register Description**

*Note: If PCM=0 then TS denotes the first timeslot of the two consecutive timeslots used.  
Only even timeslots are allowed in this case.*



**Detailed Register Description**

**0C<sub>h</sub> IFS3 Interface Select 3**

<b>15</b>			<b>0</b>
HP	I1	I2	I3
Reset Value			
0	0	0	0

The signal selection fields I1, I2 and I3 of IFS3 determine the outgoing signal of channel 1 of the IOM/SSDI-interface.

The HP bit enables a high-pass for the incoming signal of channel 1 of the analog IOM/SSDI-interface.

**HP High-Pass for S<sub>6</sub>**

0: Disabled

1: Enabled

**I1 Input signal 1 for S<sub>5</sub>**

**I2 Input signal 2 for S<sub>5</sub>**

**I3 Input signal 3 for S<sub>5</sub>**

*Note: As all sources are always active, unused sources must be set to 0 (S<sub>0</sub>).*

**Detailed Register Description**

**0D<sub>h</sub> SDCHN2 Serial Data Interface Channel 2**

**15** **0**

0	0	0	0	0	0	PCD	EN	PCM	DD	TS
---	---	---	---	---	---	-----	----	-----	----	----

Reset Value

0	0	0	0	0	0	0	0	0	0	0
---	---	---	---	---	---	---	---	---	---	---

**PCD PCM Code**

- 0: A-law
- 1:  $\mu$ -law

**EN Enable Interface**

- 0: Interface is disabled
- 1: Interface is enabled if SDCONF:EN=1

**PCM PCM Mode**

- 0: 16 Bit Linear Coding (two timeslots)
- 1: 8 Bit PCM Coding (one timeslot)

**DD Data Direction**

- 0: DD: Data Downstream, DU: Data Upstream
- 1: DD: Data Upstream, DD: Data Downstream

**TS Timeslot for Channel 2**

5	4	3	2	1	0	Description
0	0	0	0	0	0	0
0	0	0	0	0	1	1
...	...	...	...	...	...	...
1	1	1	1	1	1	63

*Note: If PCM=0 then TS denotes the first timeslot of the two consecutive timeslots used. Only even timeslots are allowed in this case.*

## Detailed Register Description

**0E<sub>h</sub> IFS4 Interface Select 4**

<b>15</b>			<b>0</b>
HP	I1	I2	I3
Reset Value			
0	0	0	0

The signal selection fields I1, I2 and I3 of IFS4 determine the outgoing signal of channel 2 of the IOM/SSDI-interface. The HP bit enables a high-pass for the incoming signal of channel 2.

**HP High-Pass for S<sub>7</sub>**

0: Disabled

1: Enabled

**I1 Input signal 1 for S<sub>8</sub>**

**I2 Input signal 2 for S<sub>8</sub>**

**I3 Input signal 3 for S<sub>8</sub>**

*As all sources are always active, unused sources must be set to 0 (S<sub>0</sub>).*

Detailed Register Description

0F<sub>h</sub> IFG5 Interface Gain 5

15	0
ATT1	ATT2
Reset Value	
255 (0 dB)	255 (0 dB)

**ATT1 Attenuation for I3 (Channel 1)**

In order to obtain an attenuation *A* the parameter ATT1 can be calculated by the following formula:

$$ATT1 = 256 \times 10^{A/20 \text{ dB}}$$

**ATT2 Attenuation for I3 (Channel 2)**

In order to obtain an attenuation *A* the parameter ATT2 can be calculated by the following formula:

$$ATT2 = 256 \times 10^{A/20 \text{ dB}}$$

## Detailed Register Description

**10<sub>h</sub> UA Universal Attenuator**

**15** **0**

ATT	0	0	0	I1
-----	---	---	---	----

Reset Value

0 (-100 dB)	0	0	0	0
-------------	---	---	---	---

### ATT Attenuation for UA

For a given attenuation  $A$  [dB] the parameter ATT can be calculated by the following formula:

$$ATT = 256 \times 10^{A/20 \text{ dB}}$$

### I1 Input Selection for UA

## Detailed Register Description

### 11<sub>h</sub> DGCTL DTMF Generator Control

15 0

EN	MD	0	0	0	0	0	0	0	0	0	0	DTC
----	----	---	---	---	---	---	---	---	---	---	---	-----

Reset Value

0	0	0	0	0	0	0	0	0	0	0	0	0
---	---	---	---	---	---	---	---	---	---	---	---	---

#### EN Generator Enable

- 0: Disabled
- 1: Enabled

#### MD Mode

- 0: raw
- 1: cooked

#### DTC Dial Tone Code (cooked mode)

3	2	1	0	Digit	Frequency
0	0	0	0	1	697/1209
0	0	0	1	2	697/1336
0	0	1	0	3	697/1477
0	0	1	1	A	697/1633
0	1	0	0	4	770/1209
0	1	0	1	5	770/1336
0	1	1	0	6	770/1477
0	1	1	1	B	770/1633
1	0	0	0	7	852/1209
1	0	0	1	8	852/1336
1	0	1	0	9	852/1477
1	0	1	1	C	852/1633
1	1	0	0	*	941/1209
1	1	0	1	0	941/1336
1	1	1	0	#	941/1477
1	1	1	1	D	941/1633

**Detailed Register Description**

**12<sub>h</sub> DGF1 DTMF Generator Frequency 1**

<b>15</b>	<b>0</b>
0	FRQ

**FRQ Frequency of Generator 1**

The parameter FRQ for a given frequency  $f$  [Hz] can be calculated by the following formula:

$$FRQ = 32768 \times \frac{f}{4000\text{Hz}}$$

---

**Detailed Register Description****13<sub>h</sub> DGF2 DTMF Generator Frequency 2**

<b>15</b>	<b>0</b>
0	FRQ

**FRQ Frequency of Generator 2**

The parameter FRQ for a given frequency  $f$  [Hz] can be calculated by the following formula:

$$\text{FRQ} = 32768 \times \frac{f}{4000\text{Hz}}$$



**Detailed Register Description**

**14<sub>h</sub> DGL DTMF Generator Level**

<b>15</b>	<b>0</b>
0	0
LEV2	LEV1

**LEV2 Signal Level of Generator 2**

In order to obtain a signal level  $L$  (relative to the PCM maximum value) for generator 2 the value of LEV2 can be calculated according to the following formula:

$$LEV2 = 128 \times 10^{L/20 \text{ dB}}$$

**LEV1 Signal Level of Generator 1**

In order to obtain a signal level  $L$  (relative to the PCM maximum value) for generator 1 the value of LEV1 can be calculated according to the following formula:

$$LEV1 = 128 \times 10^{L/20 \text{ dB}}$$

**Detailed Register Description**

**15<sub>h</sub> DGATT DTMF Generator Attenuation**

<b>15</b>	<b>0</b>
0	ATT2
0	ATT1

**ATT2 Attenuation of Signal S<sub>10</sub>**

In order to obtain attenuation *A* the parameter ATT2 can be calculated by the formula:

$$ATT2 = \begin{cases} 128 + 1024 \times 10^{A/20 \text{ dB}} & ;A > 18, 1 \text{ dB} \\ 128 \times 10^{A/20 \text{ dB}} & ;A < 18, 1 \text{ dB} \end{cases}$$

**ATT1 Attenuation of Signal S<sub>9</sub>**

In order to obtain attenuation *A* the parameter ATT1 can be calculated by the formula:

$$ATT1 = \begin{cases} 128 + 1024 \times 10^{A/20 \text{ dB}} & ;A > 18, 1 \text{ dB} \\ 128 \times 10^{A/20 \text{ dB}} & ;A < 18, 1 \text{ dB} \end{cases}$$

## Detailed Register Description

### 1A<sub>h</sub> ATDCTL0 Alert Tone Detection 0

15

0

EN	0	0	I1	0	0	0	0	0	0	0	ATC
----	---	---	----	---	---	---	---	---	---	---	-----

Reset Value

0	0	0	0	0	0	0	0	0	0	0	-1)
---	---	---	---	---	---	---	---	---	---	---	-----

1) undefined

#### EN Enable alert tone detection

0: The alert tone detection is disabled

1: The alert tone detection is enabled

#### I1 Input signal selection

#### ATC Alert Tone Code

1	0	Description
0	0	no tone
0	1	2130
1	0	2750
1	1	2130/2750

## Detailed Register Description

**1B<sub>h</sub> ATDCTL1 Alert Tone Detection 1**

**15**

**0**

MD	0	0	DEV	0	0	0	GT	MIN
----	---	---	-----	---	---	---	----	-----

**MD Alert tone detection mode**

0: Only a dual tone is detected

1: Either a dual or a single tone is detected

**DEV Maximum frequency deviation for alert tone**

0: 0.5%

1: 1.1%

**GT Gap time**

0: long

1: short

**MIN Minimum level of alert tone signal**

For a minimum signal level *min* the parameter MIN is given by the following formula:

$$MIN = 2560 \times 10^{\min/20 \text{ dB}}$$

## Detailed Register Description

**1C<sub>h</sub> CIDCTL0 Caller ID Control 0**

**15**

**0**

EN	0	0	I1	DATA
----	---	---	----	------

Reset Value

0	0	0	0	0
---	---	---	---	---

**EN CID Enable**

0: Disabled

1: Enabled

**I1 Input signal selection**

**DATA Last received data byte**

## Detailed Register Description

1D<sub>h</sub> CIDCTL1 Caller ID Control 1

15

0

NMB	NMSS	MIN
-----	------	-----

### NMB Minimum Number of Mark Bits

15	14	13	12	11	10	Description
0	0	0	0	0	0	0
0	0	0			1	10
...	...	...	...	...	...	...
1	1	1	1	1	1	630

### NMSS Minimum Number of Mark/Space Sequences

9	8	7	6	5	Description
0	0	0	0	0	1
0	0	0	0	1	11
...	...	...	...	...	
1	1	1	1	1	311

### MIN Minimum Signal Level for CID Decoder

For a minimum signal level *min* the parameter MIN is given by the following formula:

$$MIN = 640 \times 10^{\min/20 \text{ dB}}$$

## Detailed Register Description

### 20<sub>h</sub> CPTCTL Call Progress Tone Control

15

0

EN	MD	0	0	0	0	0	0	0	0	0	I1
----	----	---	---	---	---	---	---	---	---	---	----

Reset Value

0	0	0	0	0	0	0	0	0	0	0	0
---	---	---	---	---	---	---	---	---	---	---	---

#### EN CPT Detector Enable

0: Disabled

1: Enabled

#### MD CPT Mode

0: raw

1: cooked

#### I1 Input signal selection

## Detailed Register Description

### 21<sub>h</sub> CPTTR Call Progress Tone Thresholds

15

0

NUM	0	SN	MIN
-----	---	----	-----

#### NUM Number of Cycles

15	14	13	cooked mode	raw mode
0	0	0	reserved	0
0	0	1	2	reserved
...	...	...	...	reserved
1	1	1	8	reserved

#### SN Minimal Signal-to-Noise Ratio

11	10	9	8	Description
1	1	1	1	9 dB
1	0	0	0	12 dB
0	1	0	0	15 dB
0	0	1	0	18 dB
0	0	0	0	22 dB

#### MIN Minimum Signal Level for CPT Detector

Value	Description
89 <sub>h</sub>	-40 dB
85 <sub>h</sub>	-42 dB
80 <sub>h</sub>	-44 dB
9A <sub>h</sub>	-46 dB
95 <sub>h</sub>	-48 dB
90 <sub>h</sub>	-50 dB



## Detailed Register Description

22<sub>h</sub> CPTMN CPT Minimum Times

15

0

MINB	MING
------	------

**MINB Minimum Time for CPT Burst**

The parameter MINB for a minimal burst time  $TB_{min}$  can be calculated by the following formula:

$$MINB = \frac{TB_{min} - 32 \text{ ms}}{4}$$

**MING Minimum Time for CPT Gap**

The parameter MING for a minimal burst time  $TG_{min}$  can be calculated by the following formula:

$$MING = \frac{TG_{min} - 32 \text{ ms}}{4}$$

## Detailed Register Description

23<sub>h</sub> CPTMX CPT Maximum Times

15	0
MAXB	MAXG

### MAXB Maximum Time for CPT Burst

The parameter MAXB for a maximal burst time of  $TB_{max}$  can be calculated by the following formula:

$$MINB = \frac{TB_{max} - TB_{min}}{8}$$

### MAXG Maximum Time for CPT Gap

The parameter MAXG for a maximal burst time of  $TG_{max}$  can be calculated by the following formula:

$$MING = \frac{TG_{max} - TG_{min}}{8}$$

## Detailed Register Description

24<sub>h</sub> CPTDT CPT Delta Times

15

0

DIFB	DIFG
------	------

**DIFB Maximum Time Difference between consecutive Bursts**

The parameter DIFB for a maximal difference of  $t$  ms of two burst durations can be calculated by the following formula:

$$\text{DIFB} = \frac{t}{2 \text{ ms}}$$

**DIFG Maximum Time Difference between consecutive Gaps**

The parameter DIFG for a maximal difference of  $t$  ms of two gap durations can be calculated by the following formula:

$$\text{DIFG} = \frac{t}{2 \text{ ms}}$$

**Detailed Register Description**

**25<sub>h</sub> LECCTL Line Echo Cancellation Control**

<b>15</b>												<b>0</b>	
EN	0	0	0	0	0	I1				I2			
Reset Value													
0	0	0	0	0	0	0				0			

**EN Enable**

0: Disabled

1: Enabled

**I1 Input signal selection for I<sub>1</sub>**

**I2 Input signal selection for I<sub>2</sub>**

**Detailed Register Description**

**26<sub>h</sub> LECLEV Minimal Signal Level for Line Echo Cancellation**

<b>15</b>	<b>0</b>
0	MIN

**MIN**

The parameter MIN for a minimal signal level  $L$  (dB) can be calculated by the following formula:

$$MIN = \frac{512 \times (96.3 + L)}{5 \times \log 2}$$

**Detailed Register Description**

**27<sub>h</sub>    LECATT    Externally Provided Attenuation**

<b>15</b>	<b>0</b>
0	ATT

**ATT**

The parameter ATT for an externally provided attenuation A (dB) can be calculated by the following formula:

$$ATT = \frac{512 \times A}{5 \times \log 2}$$

---

**Detailed Register Description****28<sub>h</sub>    LECMGN    Margin for Double Talk Detection****15****0**

0	MGN
---	-----

**MGN**

The parameter MGN for a margin of  $L$  (dB) can be calculated by the following formula:

$$\text{MGN} = \frac{512 \times L}{5 \times \log 2}$$

Detailed Register Description

29<sub>h</sub> DDCTL DTMF Detector Control

15

0

EN	0	0	11		0	0	0	DTC <sup>1)</sup>
----	---	---	----	--	---	---	---	-------------------

Reset Value

0	0	0	0		0	0	0	_2)
---	---	---	---	--	---	---	---	-----

<sup>1)</sup> The DTC code remains valid until a new DTMF tone has been detected.

<sup>2)</sup> undefined

**EN Enable DTMF tone detection**

0: The DTMF detection is disabled

1: The DTMF detection is enabled

**11 Input signal selection**

**DTC DTMF Tone Code**

4	3	2	1	0	Frequency	Digit
1	0	0	0	0	941 / 1633	D
1	0	0	0	1	697 / 1209	1
1	0	0	1	0	697 / 1336	2
1	0	0	1	1	697 / 1477	3
1	0	1	0	0	770 / 1209	4
1	0	1	0	1	770 / 1336	5
1	0	1	1	0	770 / 1477	6
1	0	1	1	1	852 / 1209	7
1	1	0	0	0	852 / 1336	8
1	1	0	0	1	852 / 1477	9
1	1	0	1	0	941 / 1336	0
1	1	0	1	1	941 / 1209	*
1	1	1	0	0	941 / 1477	#
1	1	1	0	1	697 / 1633	A
1	1	1	1	0	770 / 1633	B
1	1	1	1	1	852 / 1633	C



## Detailed Register Description

2A<sub>h</sub> DDTW DTMF Detector Signal Twist

15

0

0	TWIST
---	-------

**TWIST Signal twist for DTMF tone**

In order to obtain a minimal signal twist  $T$  the parameter TWIST can be calculated by the following formula:

$$\text{TWIST} = 32768 \times 10^{(0.5 \text{ dB} - T)/10 \text{ dB}}$$

*Note: TWIST must be in the range [4096,20480]*

## Detailed Register Description

2B<sub>h</sub> DDLEV DTMF Detector Minimum Signal Level

15

0

1	1	1	1	1	1	1	1	1	1	1	MIN
---	---	---	---	---	---	---	---	---	---	---	-----

**MIN** Minimum Signal Level

5	4	3	2	1	0	Description
0	0	1	1	1	0	-50 dB
0	0	1	1	1	1	-49 dB
...	...	...	...	...	...	...
1	0	0	0	0	1	-31 dB
1	0	0	0	1	0	-30 dB

*Note: Values outside the given range are reserved and must not be used.*

## Detailed Register Description

### 2C<sub>h</sub> FCFCTL1 Equalizer 1 Control

15

0

EN	0	ADR	0	0	0	1
----	---	-----	---	---	---	---

Reset Value

0	0	0	0	0	0	0
---	---	---	---	---	---	---

#### EN Enable equalizer 1

0: The equalizer is disabled

1: The equalizer is enabled

#### ADR Coefficient address

13	12	11	10	9	8	Coefficient
0	0	0	0	0	0	A1
0	0	0	0	0	1	A2
0	0	0	0	1	0	A3
0	0	0	0	1	1	A4
0	0	0	1	0	0	A5
0	0	0	1	0	1	A6
0	0	0	1	1	0	A7
0	0	0	1	1	1	A8
0	0	1	0	0	0	A9
0	0	1	0	0	1	B2
0	0	1	0	1	0	B3
0	0	1	0	1	1	B4
0	0	1	1	0	0	B5
0	0	1	1	0	1	B6
0	0	1	1	1	0	B7
0	0	1	1	1	1	B8
0	1	0	0	0	0	B9
0	1	0	0	0	1	C1
0	1	0	0	1	0	D1
0	1	0	0	1	1	D2
0	1	0	1	0	0	D3
0	1	0	1	0	1	D4
0	1	0	1	1	0	D5

**Detailed Register Description**

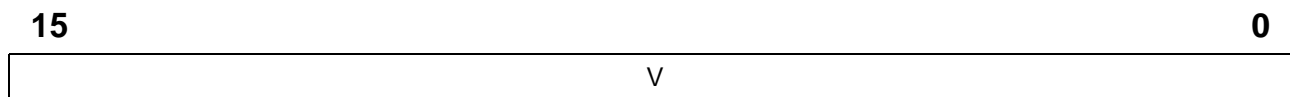
<b>13</b>	<b>12</b>	<b>11</b>	<b>10</b>	<b>9</b>	<b>8</b>	<b>Coefficient</b>
0	1	0	1	1	1	D6
0	1	1	0	0	0	D7
0	1	1	0	0	1	D8
0	1	1	0	1	0	D9
0	1	1	0	1	1	D10
0	1	1	1	0	0	D11
0	1	1	1	0	1	D12
0	1	1	1	1	0	D13
0	1	1	1	1	1	D14
1	0	0	0	0	0	D15
1	0	0	0	0	1	D16
1	0	0	0	1	0	D17
1	0	0	0	1	1	C2

**I1 Input signal selection**

---

**Detailed Register Description**

**2D<sub>h</sub> FCFCOF1 Equalizer 1 Coefficient Data**



**V Coefficient value**

For the coefficient A<sub>1</sub>-A<sub>9</sub>, B<sub>2</sub>-B<sub>9</sub> and D<sub>1</sub>-D<sub>17</sub> the following formula can be used to calculate V for a coefficient c:

$$V = 32768 \times c \quad ; -1 \leq c < 1$$

For the coefficients C<sub>1</sub> and C<sub>2</sub> the following formula can be used to calculate V for a coefficient c:

$$V = 128 \times c \quad ; 1 \leq c < 256$$

## Detailed Register Description

### 2E<sub>h</sub> FCFCTL2 Equalizer 2 Control

15

0

EN	0	ADR	0	0	0	1
----	---	-----	---	---	---	---

Reset Value

0	0	0	0	0	0	0
---	---	---	---	---	---	---

#### EN Enable equalizer 1

0: The equalizer is disabled

1: The equalizer is enabled

#### ADR Coefficient address

13	12	11	10	9	8	Coefficient
0	0	0	0	0	0	A1
0	0	0	0	0	1	A2
0	0	0	0	1	0	A3
0	0	0	0	1	1	A4
0	0	0	1	0	0	A5
0	0	0	1	0	1	A6
0	0	0	1	1	0	A7
0	0	0	1	1	1	A8
0	0	1	0	0	0	A9
0	0	1	0	0	1	B2
0	0	1	0	1	0	B3
0	0	1	0	1	1	B4
0	0	1	1	0	0	B5
0	0	1	1	0	1	B6
0	0	1	1	1	0	B7
0	0	1	1	1	1	B8
0	1	0	0	0	0	B9
0	1	0	0	0	1	C1
0	1	0	0	1	0	D1
0	1	0	0	1	1	D2
0	1	0	1	0	0	D3
0	1	0	1	0	1	D4
0	1	0	1	1	0	D5

**Detailed Register Description**

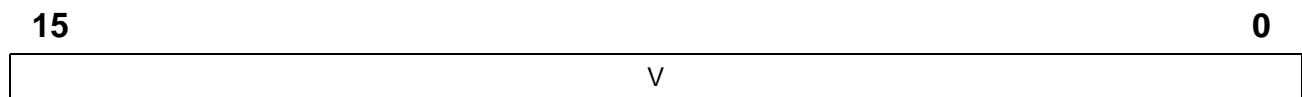
<b>13</b>	<b>12</b>	<b>11</b>	<b>10</b>	<b>9</b>	<b>8</b>	<b>Coefficient</b>
0	1	0	1	1	1	D6
0	1	1	0	0	0	D7
0	1	1	0	0	1	D8
0	1	1	0	1	0	D9
0	1	1	0	1	1	D10
0	1	1	1	0	0	D11
0	1	1	1	0	1	D12
0	1	1	1	1	0	D13
0	1	1	1	1	1	D14
1	0	0	0	0	0	D15
1	0	0	0	0	1	D16
1	0	0	0	1	0	D17
1	0	0	0	1	1	C2

**I1 Input signal selection**

---

**Detailed Register Description**

**2F<sub>h</sub> FCFCOF2 Equalizer 2 Coefficient Data**



**V Coefficient value**

For the coefficient A<sub>1</sub>-A<sub>9</sub>, B<sub>2</sub>-B<sub>9</sub> and D<sub>1</sub>-D<sub>17</sub> the following formula can be used to calculate V for a coefficient c:

$$V = 32768 \times c \quad ; -1 \leq c < 1$$

For the coefficients C<sub>1</sub> and C<sub>2</sub> the following formula can be used to calculate V for a coefficient c:

$$V = 128 \times c \quad ; 1 \leq c < 256$$



## Detailed Register Description

### 30<sub>h</sub> TGCTL Tone Generator Control

15

0

0	0	0	0	0	0	0	0	0	CGM	DT	BGM	SM	WF
---	---	---	---	---	---	---	---	---	-----	----	-----	----	----

Reset Value

0	0	0	0	0	0	0	0	0	0	0	0	0	0
---	---	---	---	---	---	---	---	---	---	---	---	---	---

### CGM Control Generator Mode

6	5	Description
0	0	Tone Generator off
0	1	Tone Generator on
1	-	Tone Generator enabled/disabled by Control Generator

### DT Dual Tone

0: F4 not added (option 1)

1: F4 added (option 2)

### BGM Beat Generator Mode

3	2	Description
0	0	Continuous Tone F1
0	1	Continuous Tone F2
1	0	two tone cadence
1	1	three tone sequence

### SM Stop Mode

0: Immediate

1: Controlled

### WF Waveform

0: Sine Wave

1: Square Wave

## Detailed Register Description

31<sub>h</sub> **TGTON** **Tone Generator Time TON**

15	TM	TE	0
----	----	----	---

**TM** **Mantissa of TON**

The mantissa TM for a time  $t$  ([ms]) can be calculated by the following formula:

$$TM = \frac{t}{2^{TE}}$$

**TE** **Exponent of TON**

The exponent TE for a time  $t$  ([ms]) can be calculated by the following formula:

$$TE = \log_2 t$$

*Note:  $TE > 0$*

## Detailed Register Description

32<sub>h</sub> TGTOFF Tone Generator Time TOFF

15	0
TM	TE

**TM Mantissa of TOFF**

The mantissa TM for a time  $t$  ([ms]) can be calculated by the following formula:

$$TM = \frac{t}{2^{TE}}$$

**TE Exponent of TOFF**

The exponent TE for a time  $t$  ([ms]) can be calculated by the following formula:

$$TE = \log_2 t$$

*Note: TE > 0*

**Detailed Register Description**

**33<sub>h</sub> TGT1 Tone Generator Time T1**

15	TIME	0
----	------	---

**TIME**

The parameter TIME for a time  $t$  ([ms]) can be calculated by the following formula:

$$\text{TIME} = \frac{t}{8}$$

## Detailed Register Description

**34<sub>h</sub> TGF1 Tone Generator Frequency F1**

<b>15</b>	<b>0</b>
0	F

### **F Frequency**

The parameter F for a frequency  $f$  ([Hz]) can be calculated by the following formula:

$$F = 8,192 \times f$$

**Detailed Register Description**

**35<sub>h</sub> TGG1 Tone Generator Gain G1**

<b>15</b>	<b>0</b>
0	G

**G Gain**

The parameter G for a gain  $g$  ([dB]) can be calculated by the following formula:

$$F = 32768 \times 10^{g/20}$$

---

**Detailed Register Description****36<sub>h</sub> TGT2 Tone Generator Time T2****15****0**

TIME

**TIME**

The parameter TIME for a time  $t$  ([ms]) can be calculated by the following formula:

$$\text{TIME} = \frac{t}{8}$$

**Detailed Register Description**

**37<sub>h</sub> TGF2 Tone Generator Frequency F2**

<b>15</b>	<b>0</b>
0	F

**F Frequency**

The parameter F for a frequency  $f$  ([Hz]) can be calculated by the following formula:

$$F = 8,192 \times f$$



## Detailed Register Description

**38<sub>h</sub> TGG2 Tone Generator Gain G2**

<b>15</b>	<b>0</b>
0	G

### **G Gain**

The parameter G for a gain  $g$  ([dB]) can be calculated by the following formula:

$$F = 32768 \times 10^{g/20}$$

## Detailed Register Description

**39<sub>h</sub> TGT3 Tone Generator Time T3**

15	TIME	0
----	------	---

### TIME

The parameter TIME for a time  $t$  ([ms]) can be calculated by the following formula:

$$\text{TIME} = \frac{t}{8}$$

---

**Detailed Register Description**

**3A<sub>h</sub> TGF3 Tone Generator Frequency F3**

<b>15</b>	<b>0</b>
0	F

**F Frequency**

The parameter F for a frequency  $f$  ([Hz]) can be calculated by the following formula:

$$F = 8,192 \times f$$

---

**Detailed Register Description**

**3B<sub>h</sub> TGG3 Tone Generator Gain G3**

<b>15</b>	<b>0</b>
0	G

**G Gain**

The parameter G for a gain  $g$  ([dB]) can be calculated by the following formula:

$$F = 32768 \times 10^{g/20}$$

---

**Detailed Register Description**

**3C<sub>h</sub> TGF4 Tone Generator Frequency F4**

<b>15</b>	<b>0</b>
0	F

**F Frequency**

The parameter F for a frequency  $f$  ([Hz]) can be calculated by the following formula:

$$F = 8,192 \times f$$

## Detailed Register Description

3D<sub>h</sub> TGG4 Tone Generator Gain G4

15	0
0	G

**G Gain**

The parameter G for a gain  $g$  ([dB]) can be calculated by the following formula:

$$F = 32768 \times 10^{g/20}$$

---

**Detailed Register Description**

**3E<sub>h</sub> TGG01 Tone Generator Gain Output 1**

<b>15</b>	<b>0</b>
0	G

**G Gain**

The parameter G for a gain *g* ([dB]) can be calculated by the following formula:

$$F = 32768 \times 10^{g/20}$$

---

**Detailed Register Description**

**3F<sub>h</sub> TGG02 Tone Generator Gain Output 2**

<b>15</b>	<b>0</b>
0	G

**G Gain**

The parameter G for a gain  $g$  ([dB]) can be calculated by the following formula:

$$F = 32768 \times 10^{g/20}$$



Detailed Register Description

47h SPSCTL SPS Control

15

0

POS	0	0	0	0	0	0	0	MODE	SP1	SP0
-----	---	---	---	---	---	---	---	------	-----	-----

Reset Value

0	0	0	0	0	0	0	0	0	_1)	_1)
---	---	---	---	---	---	---	---	---	-----	-----

1) undefined

POS Position of Status Register Window

15	14	13	12	SPS <sub>0</sub>	SPS <sub>1</sub>
0	0	0	0	Bit 0	Bit 1
0	0	0	1	Bit 1	Bit 2
...	...	...	...	...	...
1	1	1	0	Bit 14	Bit 15

MODE Mode of SPS Interface

4	3	2	Description
0	0	0	Disabled (SPS <sub>0</sub> and SPS <sub>1</sub> zero)
0	0	1	Output of SP1 and SP0
1	0	0	Output of speakerphone state
1	1	0	Output of STATUS register

SP1 Direct Control for SPS<sub>1</sub>

0: SPS<sub>1</sub> set to 0

1: SPS<sub>1</sub> set to 1

SP0 Direct Control for SPS<sub>0</sub>

0: SPS<sub>0</sub> set to 0

1: SPS<sub>0</sub> set to 1

*Note: If mode 1 has been selected prior to power-down, both mode 1 and the values of SP1 and SP0 are retained during power-down and wake-up. Other modes are reset to 0 during power down.*

---

**Detailed Register Description**

**4A<sub>h</sub> DOUT0 Data Out (Timeslot 0)**

<b>15</b>				<b>0</b>
0	0	0	0	DATA
Reset Value				
0	0	0	0	0

**DATA Output Data**

Output data for pins MA<sub>0</sub>-MA<sub>11</sub> while MA<sub>12</sub>=1 (only if HWCONFIG1:APP=10).

**Detailed Register Description**

**4B<sub>h</sub> DOUT1 Data Out (Timeslot 1)**

<b>15</b>				<b>0</b>
0	0	0	0	DATA
Reset Value				
0	0	0	0	0

**DATA Output Data**

Output data for pins MA<sub>0</sub>-MA<sub>11</sub> while MA<sub>13</sub>=1 (only if HWCONFIG1:APP=10).

## Detailed Register Description

**4C<sub>h</sub> DOUT2 Data Out (Timeslot 2)**

<b>15</b>				<b>0</b>
0	0	0	0	DATA

Reset Value				
0	0	0	0	0

### **DATA Output Data**

Output data for pins MA<sub>0</sub>-MA<sub>11</sub> while MA<sub>14</sub>=1 (only if HWCONFIG1:APP=10).

---

**Detailed Register Description**

**4D<sub>h</sub> DOUT3 Data Out (Timeslot 3 or Static Mode)**

<b>15</b>	<b>0</b>
DATA	
Reset Value	
0	

**DATA Output Data**

Output data for pins MA<sub>0</sub>-MA<sub>11</sub> while MA<sub>15</sub>=1 (only if HWCONFIG1:APP=10).

Output data for pins MA<sub>0</sub>-MA<sub>15</sub> (only if HWCONFIG1:APP=01)

## Detailed Register Description

4E<sub>h</sub>    DIN    Data In (Timeslot 3 or Static Mode)

15

0



### DATA Input Data

Input data for pins MA<sub>0</sub>-MA<sub>11</sub> at falling edge of MA<sub>12</sub> (only if HWCONFIG1:APP=10).

Input data for pins MA<sub>0</sub>-MA<sub>15</sub> (only if HWCONFIG1:APP=01)

**Detailed Register Description**

**4F<sub>h</sub> DDIR Data Direction (Timeslot 3 or Static Mode)**

<b>15</b>	<b>0</b>
DIR	
Reset Value	
0 (all inputs)	

**DIR Port Direction**

Port direction during MA<sub>12</sub>=1 or in static mode.

0: input

1: output

Detailed Register Description

60<sub>h</sub> SCTL Speakerphone Control

15

0

ENS	ENC	EM	EWF	NAD	RED	CN	MD	SDR	SDX	0	0	AGR	AGX	0
-----	-----	----	-----	-----	-----	----	----	-----	-----	---	---	-----	-----	---

Reset Value

0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
---	---	---	---	---	---	---	---	---	---	---	---	---	---	---

**ENS Enable Echo Suppression**

- 0: The echo suppression unit is disabled
- 1: The echo suppression unit is enabled

**ENC Enable Echo Cancellation**

- 0: The echo cancellation unit is disabled
- 1: The echo cancellation unit is enabled

**EM Echo Cancellation Mode**

13	12	Description
0	0	fullband mode
0	1	subband mode (submode 1)
1	0	subband mode (submode 2)
1	1	subband mode (submode 3)

**EWF Enable Wiener Filter**

- 0: The Wiener filter is disabled
- 1: The Wiener filter is enabled

**NAD Noise Adaptation**

- 0: Noise adaptation is disabled.
- 1: Noise adaptation is enabled.

**RED Tap Reduction**

- 0: The length of the subband filter is not reduced
- 1: The length of the subband filter is reduced



---

**Detailed Register Description**

- CN      Comfort Noise**  
0: The comfort noise generator is disabled.  
1: The comfort noise generator is enabled.
- MD      Mode**  
0: Speakerphone mode  
1: Loudhearing mode
- SDR     Signal Source of SDR**  
0: after AGCR  
1: before AGCR
- SDX     Signal Source of SDX**  
0: after AGCX  
1: before AGCX
- AGR     AGCR Enable**  
0: AGCR disabled  
1: AGCR enabled
- AGX     AGCX Enable**  
0: AGCX disabled  
1: AGCX enabled

## Detailed Register Description

**62<sub>h</sub> SSRC1 Speakerphone Source 1**

<b>15</b>								<b>0</b>	
0	0	0	0	0	0	I1		I2	
Reset Value									
0	0	0	0	0	0	0		0	

**I1 Input Signal Selection (Acoustic Source 1)**

**I2 Input Signal Selection (Acoustic Source 2)**

## Detailed Register Description

**63<sub>h</sub> SSRC2 Speakerphone Source 2**

<b>15</b>						<b>0</b>	
0	0	0	0	0	0	13	14
Reset Value							
0	0	0	0	0	0	0	0

**13 Input Signal Selection (Line Source 1)**

**14 Input Signal Selection (Line Source 2)**

---

Detailed Register Description

64<sub>h</sub>    SSDX1    Speech Detector (Transmit) 1

<b>15</b>		<b>0</b>
0	LP2L	LIM

**LP2L**

The parameter LP2L for a saturation level  $L$  (dB) can be calculated by the following formula:

$$LP2L = \frac{2 \times L}{5 \times \log 2}$$

**LIM**

The parameter LIM for a minimum signal level  $L$  (dB, relative to PCM max. value) can be calculated by the following formula:

$$LIM = \frac{2 \times (96.3 + L)}{5 \times \log 2}$$

---

Detailed Register Description

65<sub>h</sub>    SSDX2    Speech Detector (Transmit) 2

15

0

LP1	0	OFF
-----	---	-----

**LP1**

The parameter LP1 for a time  $t$  (ms) can be calculated by the following formula:

$$LP1 = \begin{cases} 64/t & ;0.5 < t < 64 \\ 128 + 2048/t & ;16.2 < t < 2048 \end{cases}$$

**OFF**

The parameter OFF for a level offset of  $O$  (dB) can be calculated by the following formula:

$$OFF = \frac{2 \times O}{5 \times \log 2}$$

## Detailed Register Description

66<sub>h</sub>    SSDX3    Speech Detector (Transmit) 3

<b>15</b>		<b>0</b>
	PDN	LP2N

### PDN

The parameter PDN for a time  $t$  (ms) can be calculated by the following formula:

$$PDN = \begin{cases} 64/t & ;0.5 < t < 64 \\ 128 + 2048/t & ;16.2 < t < 2048 \end{cases}$$

### LP2N

The parameter LP2N for a time  $t$  (ms) can be calculated by the following formula:

$$LP2N = \begin{cases} 64/t & ;0.5 < t < 64 \\ 128 + 2048/t & ;16.2 < t < 2048 \end{cases}$$

## Detailed Register Description

67<sub>h</sub>    SSDX4    Speech Detector (Transmit) 4

15		0
	PDS	0
		LP2S

### PDS

The parameter PDS for a time  $t$  (ms) can be calculated by the following formula:

$$PDS = \begin{cases} 64/t & ;0.5 < t < 64 \\ 128 + 2048/t & ;16.2 < t < 2048 \end{cases}$$

### LP2S

The parameter LP2S for a time  $t$  (ms) can be calculated by the following formula:

$$LP2S = \frac{262144}{t}$$

**Detailed Register Description**

**68<sub>h</sub>    SDDR1    Speech Detector (Receive) 1**

<b>15</b>			<b>0</b>
0	LP2L	0	LIM

**LP2L**

The parameter LP2L for a saturation level  $L$  (dB) can be calculated by the following formula:

$$LP2L = \frac{2 \times L}{5 \times \log 2}$$

**LIM**

The parameter LIM for a minimum signal level  $L$  (dB, relative to PCM max. value) can be calculated by the following formula:

$$LIM = \frac{2 \times (96.3 + L)}{5 \times \log 2}$$



## Detailed Register Description

69<sub>h</sub> SSSDR2 Speech Detector (Receive) 2

15

0

LP1	0	OFF
-----	---	-----

**LP1**

The parameter LP1 for a time  $t$  (ms) can be calculated by the following formula:

$$LP1 = \begin{cases} 64/t & ;0.5 < t < 64 \\ 128 + 2048/t & ;16.2 < t < 2048 \end{cases}$$

**OFF**

The parameter OFF for a level offset of  $O$  (dB) can be calculated by the following formula:

$$OFF = \frac{2 \times O}{5 \times \log 2}$$

**Detailed Register Description**

**6A<sub>h</sub> SSSDR3 Speech Detector (Receive) 3**

<b>15</b>	<b>0</b>
PDN	LP2N

**PDN**

The parameter PDN for a time  $t$  (ms) can be calculated by the following formula:

$$PDN = \begin{cases} 64/t & ;0.5 < t < 64 \\ 128 + 2048/t & ;16.2 < t < 2048 \end{cases}$$

**LP2N**

The parameter LP2N for a time  $t$  (ms) can be calculated by the following formula:

$$LP2N = \begin{cases} 64/t & ;0.5 < t < 64 \\ 128 + 2048/t & ;16.2 < t < 2048 \end{cases}$$

**Detailed Register Description**

**6B<sub>h</sub> SSSDR4 Speech Detector (Receive) 4**

<b>15</b>	<b>0</b>
PDS	LP2S

**PDS**

The parameter PDS for a time  $t$  (ms) can be calculated by the following formula:

$$PDS = \begin{cases} 64/t & ;0.5 < t < 64 \\ 128 + 2048/t & ;16.2 < t < 2048 \end{cases}$$

**LP2S**

The parameter LP2S for a time  $t$  (ms) can be calculated by the following formula:

$$LP2S = \frac{262144}{t}$$

## Detailed Register Description

6C<sub>h</sub> SSCAS1 Speech Comparator (Acoustic Side) 1

15	0
G	ET

**G**

The parameter G for a gain A (dB) can be calculated by the following formula:

$$G = \frac{2 \times A}{5 \times \log 2}$$

*Note: The parameter G is interpreted in two's complement.*

**ET**

The parameter ET for a time t (ms) can be calculated by the following formula:

$$ET = \frac{t}{4}$$

## Detailed Register Description

6D<sub>h</sub> SSCAS2 Speech Comparator (Acoustic Side) 2

15	0
0	GDN
	PDN

**GDN**

The parameter GDN for a gain  $G$  (dB) can be calculated by the following formula:

$$\text{GDN} = \frac{4 \times G}{5 \times \log 2}$$

**PDN**

The parameter PDN for a decay rate  $R$  (ms/dB) can be calculated by the following formula:

$$\text{PDN} = \frac{64 \times R}{5 \times \log 2}$$

**Detailed Register Description**

**6E<sub>h</sub> SSCAS3 Speech Comparator (Acoustic Side) 3**

<b>15</b>	<b>0</b>
0	PDS

**GDS**

The parameter GDS for a gain  $G$  (dB) can be calculated by the following formula:

$$GDS = \frac{4 \times G}{5 \times \log 2}$$

**PDS**

The parameter PDS for a decay rate  $R$  (ms/dB) can be calculated by the following formula:

$$PDS = \frac{64 \times R}{5 \times \log 2}$$

**Detailed Register Description**

**6F<sub>h</sub> SSCLS1 Speech Comparator (Line Side) 1**

<b>15</b>	<b>0</b>
G	ET

**G**

The parameter G for a gain A (dB) can be calculated by the following formula:

$$G = \frac{2 \times A}{5 \times \log 2}$$

*Note: The parameter G is interpreted in two's complement.*

**ET**

The parameter ET for a time t (ms) can be calculated by the following formula:

$$ET = \frac{t}{4}$$

## Detailed Register Description

70<sub>h</sub> SSCLS2 Speech Comparator (Line Side) 2

15	0
0	0
GDN	PDN

**GDN**

The parameter GDN for a gain  $G$  (dB) can be calculated by the following formula:

$$\text{GDN} = \frac{4 \times G}{5 \times \log 2}$$

**PDN**

The parameter PDN for a decay rate  $R$  (ms/dB) can be calculated by the following formula:

$$\text{PDN} = \frac{64 \times R}{5 \times \log 2}$$



**Detailed Register Description**

**71<sub>h</sub> SSCLS3 Speech Comparator (Line Side) 3**

<b>15</b>	<b>0</b>
0	PDS

**GDS**

The parameter GDS for a gain  $G$  (dB) can be calculated by the following formula:

$$GDS = \frac{4 \times G}{5 \times \log 2}$$

**PDS**

The parameter PDS for a decay rate  $R$  (ms/dB) can be calculated by the following formula:

$$PDS = \frac{64 \times R}{5 \times \log 2}$$

## Detailed Register Description

72<sub>h</sub> SATT1 Attenuation Unit 1

15	0
0	0
ATT	SW

**ATT**

The parameter ATT for an attenuation  $A$  (dB) can be calculated by the following formula:

$$ATT = \frac{2 \times A}{5 \times \log 2}$$

**SW**

The parameter SW for a switching rate  $R$  (ms/dB) can be calculated by the following formula:

$$SW = \begin{cases} 128 + \frac{1}{5 \times \log 2 \times SW} & ; 0.0053 < SW < 0.66 \\ \frac{16}{5 \times \log 2 \times SW} & ; 0.66 < SW < 0.63 \end{cases}$$

---

**Detailed Register Description****73<sub>h</sub> SATT2 Attenuation Unit 2**

<b>15</b>	<b>0</b>
TW	DS

**TW**

The parameter TW for a time  $t$  (ms) can be calculated by the following formula:

$$TW = \frac{t}{16}$$

**DS**

The parameter DS for a decay rate  $R$  (ms/dB) can be calculated by the following formula:

$$DS = \frac{5 \times \log_2 \times R - 1}{4}$$

**Detailed Register Description**

**74<sub>h</sub> SAGX1 Automatic Gain Control (Transmit) 1**

<b>15</b>		<b>0</b>	
	AG_INIT	0	COM

**AG\_INIT**

The parameter AG\_INIT for a gain  $G$  (dB) can be calculated by the following formula:

$$AG\_INIT = \frac{-2 \times G}{5 \times \log 2}$$

This parameter is interpreted in two's complement.

**COM**

The threshold COM for a level  $L$  (dB) can be calculated by the following formula:

$$COM = \frac{2 \times (96.3 + L)}{5 \times \log 2}$$

**Detailed Register Description**

**75<sub>h</sub> SAGX2 Automatic Gain Control (Transmit) 2**

<b>15</b>	<b>0</b>
0	SPEEDH
AG_ATT	SPEEDH

**AG\_ATT**

The parameter AG\_ATT for a gain *G* (dB) can be calculated by the following formula:

$$AG\_ATT = \frac{-2 \times G}{5 \times \log 2}$$

**SPEEDH**

The parameter SPEEDH for the regulation speed *R* (ms/dB) can be calculated by the following formula:

$$SPEEDH = \frac{512}{D \times R}$$

The variable *D* denotes the aberration (dB).

## Detailed Register Description

76<sub>h</sub> SAGX3 Automatic Gain Control (Transmit) 3

15	0
AG_GAIN	SPEEDL

**AG\_GAIN**

The parameter AG\_GAIN for a gain  $G$  (dB) can be calculated by the following formula:

$$\text{AG\_GAIN} = \frac{-2 \times G}{5 \times \log 2}$$

**SPEEDL**

The parameter COM for a gain  $G$  (dB) can be calculated by the following formula:

$$\text{COM} = \frac{2 \times (96.3 + G)}{5 \times \log 2}$$

The variable  $D$  denotes the aberration (dB).

**Detailed Register Description**

**77<sub>h</sub> SAGX4 Automatic Gain Control (Transmit) 4**

<b>15</b>			<b>0</b>
0	NOIS	0	LPA

**NOIS**

The parameter NOIS for a threshold level  $L$  (dB) can be calculated by the following formula:

$$COM = \frac{2 \times (96.3 + L)}{5 \times \log 2}$$

**LPA**

The parameter LPA for a low pass time constant  $T$  (mS) can be calculated by the following formula:

$$LPA = \frac{16}{T}$$

## Detailed Register Description

**78<sub>h</sub> SAGX5 Automatic Gain Control (Transmit) 5**

<b>15</b>	<b>0</b>
AG_CUR	0 0 0 0 0 0 0 0

### AG\_CUR

The current gain  $G$  of the AGC can be derived from the parameter Parameter AG\_CUR by the following formula:

$$G = \frac{-5 \times \log_2 \times \text{AG\_CUR}}{2}$$

AG\_CUR is interpreted in two's complement.



## Detailed Register Description

79<sub>h</sub> SAGR1 Automatic Gain Control (Receive) 1

15	0	0
AG_INIT	0	COM

**AG\_INIT**

The parameter AG\_INIT for a gain  $G$  (dB) can be calculated by the following formula:

$$AG\_INIT = \frac{-2 \times G}{5 \times \log 2}$$

This parameter is interpreted in two's complement.

**COM**

The parameter COM for a threshold  $L$  (dB) can be calculated by the following formula:

$$COM = \frac{2 \times (96.3 + L)}{5 \times \log 2}$$

## Detailed Register Description

7A<sub>h</sub> SAGR2 Automatic Gain Control (Receive) 2

15	0
0	SPEEDH

**AG\_ATT**

The parameter AG\_ATT for a gain  $G$  (dB) can be calculated by the following formula:

$$AG\_ATT = \frac{-2 \times G}{5 \times \log 2}$$

**SPEEDH**

The parameter SPEEDH for the regulation speed  $R$  (ms/dB) can be calculated by the following formula:

$$SPEEDH = \frac{512}{D \times R}$$

The variable  $D$  denotes the aberration (dB).

## Detailed Register Description

7B<sub>h</sub> SAGR3 Automatic Gain Control (Receive) 3

15

0

AG_GAIN	SPEEDL
---------	--------

**AG\_GAIN**

The parameter AG\_GAIN for a gain  $G$  (dB) can be calculated by the following formula:

$$\text{AG\_GAIN} = \frac{-2 \times G}{5 \times \log 2}$$

**SPEEDL**

The parameter SPEEDL for the regulation speed  $R$  (ms/dB) can be calculated by the following formula:

$$\text{SPEEDL} = \frac{4096}{D \times R}$$

The variable  $D$  denotes the aberration (dB).

## Detailed Register Description

7C<sub>h</sub> SAGR4 Automatic Gain Control (Receive) 4

15			0
0	NOIS	0	LPA

### NOIS

The parameter NOIS for a threshold level  $L$  (dB) can be calculated by the following formula:

$$\text{COM} = \frac{2 \times (96.3 + L)}{5 \times \log 2}$$

### LPA

The parameter LPA for a low pass time constant  $T$  (mS) can be calculated by the following formula:

$$\text{LPA} = \frac{16}{T}$$

## Detailed Register Description

7D<sub>h</sub>    SAGR5    Automatic Gain Control (Receive) 5

15	0
AG_CUR	0 0 0 0 0 0 0 0

### AG\_CUR

The current gain  $G$  of the AGC can be derived from the parameter Parameter AG\_CUR by the following formula:

$$G = \frac{-5 \times \log_2 \times \text{AG\_CUR}}{2}$$

AG\_CUR is interpreted in two's complement.

**Detailed Register Description**

**7E<sub>h</sub> SLGA Line Gain**

<b>15</b>			<b>0</b>
0	LGAR	0	LGAX

**LGAR**

The parameter LGAR for a gain  $G$  (dB) is given by the following formula:

$$LGAR = 128 \times 10^{(G - 12)/20}$$

**LGAX**

The parameter LGAX for a gain  $G$  (dB) is given by the following formula:

$$LGAX = 128 \times 10^{(G - 12)/20}$$

---

**Detailed Register Description****80<sub>h</sub>   SAELEN   Acoustic Echo Cancellation Length****15****0**

0	0	0	0	0	0	LEN
---	---	---	---	---	---	-----

**LEN**

LEN denotes the number of FIR-taps used.

**Detailed Register Description**

**81<sub>h</sub> SAEATT Acoustic Echo Cancellation Double Talk Attenuation**

<b>15</b>	<b>0</b>
0	ATT

**ATT**

The parameter ATT for an attenuation  $A$  (dB) is given by the following formula:

$$ATT = \frac{512 \times A}{5 \times \log 2}$$



## Detailed Register Description

**82<sub>h</sub>    SAEGS    Acoustic Echo Cancellation Global Scale**

<b>15</b>													<b>0</b>	
0	0	0	0	0	0	0	0	0	0	0	0	0	0	GS

### GS

All coefficients of the FIR filter are scaled by a factor C. This factor is given by the following equation:

$$C = 2^{GS}$$

## Detailed Register Description

**83<sub>h</sub>    SAEPS    Acoustic Echo Cancellation Partial Scale**

<b>15</b>													<b>0</b>	
0	0	0	0	0	0	0	0	0	0	0	0	0	0	PS

### PS

The additional scaling coefficient AC is given by the following formula:

$$AC = 2^{PS}$$

## Detailed Register Description

**84<sub>h</sub>    SAEBL    Acoustic Echo Cancellation First Block**

<b>15</b>													<b>0</b>	
0	0	0	0	0	0	0	0	0	0	0	0	0	0	FB

### FB

The parameter FB denotes the first block that is affected by the partial scaling coefficient. If the partial coefficient is one, FB is disregarded.

## Detailed Register Description

85<sub>h</sub>    SAEWFL    Wiener Filter Limit Attenuation

15	0
0	LIMIT

### LIMIT

The parameter LIMIT for a maximal attenuation  $A$  (dB) is given by the following formula:

$$\text{LIMIT} = \frac{512 \times A}{5 \times \log 2}$$

---

## Detailed Register Description

86<sub>h</sub>    SAEWFT    Wiener Filter Transition Time

15

0

0	TRTIME
---	--------

### TRTIME

T.B.D. (default: 16384)

## Detailed Register Description

**90<sub>h</sub> SCSD1 Speech Detector (Comfort Noise) 1**

<b>15</b>			<b>0</b>
0	LP2L	0	LIM

### LP2L

The parameter LP2L for a saturation level  $L$  (dB) can be calculated by the following formula:

$$LP2L = \frac{2 \times L}{5 \times \log 2}$$

### LIM

The parameter LIM for a minimum signal level  $L$  (dB, relative to PCM max. value) can be calculated by the following formula:

$$LIM = \frac{2 \times (96.3 + L)}{5 \times \log 2}$$

## Detailed Register Description

91<sub>h</sub> SCSD2 Speech Detector (Comfort Noise) 2

15

0

LP1	0	OFF
-----	---	-----

**LP1**

The parameter LP1 for a time  $t$  (ms) can be calculated by the following formula:

$$LP1 = \begin{cases} 64/t & ;0.5 < t < 64 \\ 128 + 2048/t & ;16.2 < t < 2048 \end{cases}$$

**OFF**

The parameter OFF for a level offset of  $O$  (dB) can be calculated by the following formula:

$$OFF = \frac{2 \times O}{5 \times \log 2}$$

**Detailed Register Description**

**92<sub>h</sub> SCSD3 Speech Detector (Comfort Noise) 3**

<b>15</b>	<b>0</b>
PDN	LP2N

**PDN**

The parameter PDN for a time  $t$  (ms) can be calculated by the following formula:

$$PDN = \begin{cases} 64/t & ;0.5 < t < 64 \\ 128 + 2048/t & ;16.2 < t < 2048 \end{cases}$$

**LP2N**

The parameter LP2N for a time  $t$  (ms) can be calculated by the following formula:

$$LP2N = \begin{cases} 64/t & ;0.5 < t < 64 \\ 128 + 2048/t & ;16.2 < t < 2048 \end{cases}$$



**Detailed Register Description**

**93<sub>h</sub> SCSD4 Speech Detector (Comfort Noise) 4**

<b>15</b>	<b>0</b>
PDS	0
	LP2S

**PDS**

The parameter PDS for a time  $t$  (ms) can be calculated by the following formula:

$$PDS = \begin{cases} 64/t & ;0.5 < t < 64 \\ 128 + 2048/t & ;16.2 < t < 2048 \end{cases}$$

**LP2S**

The parameter LP2S for a time  $t$  (ms) can be calculated by the following formula:

$$LP2S = \frac{262144}{t}$$

## Detailed Register Description

**94<sub>h</sub> SCLPT Low Pass Time Constant**

<b>15</b>	<b>0</b>
0	TC

### BN

The parameter TC for a time constant  $t$  (ms) can be calculated by the following formula:

$$TC = \frac{65534}{t}$$

*Note: BN must be greater than zero.*

## Detailed Register Description

95<sub>h</sub>    SCCR    Correlation

15

0

0	1	CORR
---	---	------

### CORR

The parameter CORR for a linear correlation C is given by:

$$\text{CORR} = 32768 \times C$$

*Note: CORR must be greater than 0x4FFF.*

The default value for a noise free environment is C=0.93, i.e. CORR=0x7700.

## Detailed Register Description

**96<sub>h</sub>    SCCRN    Correlation Noise Threshold**

<b>15</b>	<b>0</b>
0	NTH

### NTH

The parameter NTH for a threshold  $L$  (dB, relative to PCM max. value) can be calculated by the following formula:

$$NTH = \frac{512 \times (96.3 + L)}{5 \times \log 2}$$

## Detailed Register Description

97<sub>h</sub>    SCCRS    Correlation Sensitivity

<b>15</b>		<b>0</b>
1	1	1
1	1	CS

### CS

The parameter CS for a sensitivity  $SE$  (1/dB) can be calculated by the following formula:

$$CS = 655350 \times \log(2) \times SE$$

## Detailed Register Description

**98<sub>h</sub>    SCCRL    Correlation Limit**

<b>15</b>		<b>0</b>
0	1	LIMIT

### LIMIT

The parameter LIMIT for a correlation limit  $L$  is given by:

$$\text{LIMIT} = 32768 \times L$$

*Note:  $L$  must be greater than 0x4FFF.*

## Detailed Register Description

**99<sub>h</sub> SCDT Double Talk Detection**

<b>15</b>	<b>0</b>
0	DTD

### DTD

The parameter DTD for a level L (dB, relative to PCM max. value) can be calculated by the following formula:

$$DTD = \frac{512 \times L}{5 \times \log 2}$$

*Note: DTD must be greater than 0x7FF.*

**Detailed Register Description**

**9A<sub>h</sub> SCDTN Double Talk Detection Threshold**

<b>15</b>	<b>0</b>
0	NTH

**NTH**

The parameter NTH for a noise threshold  $L$  (dB, relative to PCM max. value) can be calculated by the following formula:

$$NTH = \frac{512 \times (96.3 + L)}{5 \times \log 2}$$



## Detailed Register Description

**9B<sub>h</sub> SCDTS Double Talk Sensitivity**

<b>15</b>				<b>0</b>
1	1	1	1	DTS

### DTS

The parameter DTS for a sensitivity  $SE$  (1/dB) can be calculated by the following formula:

$$S = 2048 \times SE$$

**Detailed Register Description**

**9C<sub>h</sub> SCDTL Double Talk Limit**

<b>15</b>	<b>0</b>
0	LIMIT

**LIMIT**

The parameter LIMIT for a level L (dB, relative to PCM max. value) can be calculated by the following formula:

$$\text{LIMIT} = \frac{512 \times L}{5 \times \log 2}$$

*Note: LIMIT must be greater than 0x7FF.*

## Detailed Register Description

**9D<sub>h</sub> SCATTN Attenuation Noise**

<b>15</b>	<b>0</b>
0	NTH

### NTH

The parameter NTH for a threshold  $L$  (dB, relative to PCM max. value) can be calculated by the following formula:

$$NTH = \frac{512 \times (96.3 + L)}{5 \times \log 2}$$

## Detailed Register Description

**9E<sub>h</sub> SCATTS Attenuation Sensitivity**

<b>15</b>	<b>0</b>
0	AS

### AS

The parameter AS for a sensitivity  $SE$  (1/dB) can be calculated by the following formula:

$$AS = 2028 \times SE$$

## Detailed Register Description

**9F<sub>h</sub> SCATTL Attenuation Limit**

<b>15</b>	<b>0</b>
0	LIMIT

### LIMIT

The parameter LIMIT for a level  $L$  (dB, relative to PCM max. value) can be calculated by the following formula:

$$\text{LIMIT} = \frac{512 \times L}{5 \times \log 2}$$

*Note: LIMIT must be greater than 0x7FF.*

## Detailed Register Description

A0<sub>h</sub> SCAECL Global Attenuation Limit (Full Duplex Speakerphone)

15	0
0	GLIMIT

**GLIMIT**

The parameter GLIMIT for a maximum attenuation  $A$  (dB) can be calculated by the following formula:

$$GLIMIT = \frac{512 \times A}{5 \times \log 2}$$

*Note: GLIMIT must be greater than 0x7FF.*

**Detailed Register Description**

**A1<sub>h</sub> SCSTGP Single Talk Gap Time**

**15**

**0**



**GT**

The minimal gap time GT for a time  $t$  (ms) can be calculated by the following formula:

$$GT = 8 \times t$$

*Note: GT must be greater than 0.*

**Detailed Register Description**

**A2<sub>h</sub> SCSTATT Single Talk Attenuation**

<b>15</b>	<b>0</b>
0	ATT

**ATT**

The parameter ATT for an attenuation *A* (dB) can be calculated by the following formula:

$$ATT = \frac{512 \times A}{5 \times \log 2}$$



## Detailed Register Description

**A3<sub>h</sub> SCSTNL Single Talk Noise Level**

<b>15</b>	<b>0</b>
0	NTH

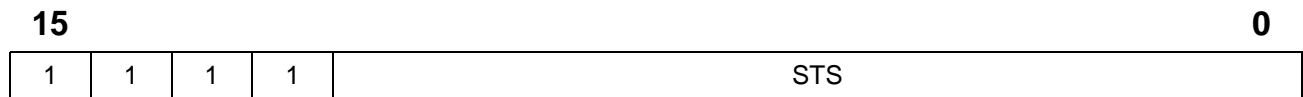
**NTH**

The parameter NTH for a noise threshold  $L$  (dB) can be calculated by the following formula:

$$NTH = \frac{512 \times L}{5 \times \log 2}$$

## Detailed Register Description

**A4<sub>h</sub> SCSTS Single Talk Sensitivity**



### STS

The parameter STS for a sensitivity  $SE$  (1/dB) can be calculated by the following formula:

$$STS = 2048 \times SE$$

## Detailed Register Description

A5<sub>h</sub> SCSTTIM Single Talk Time

15

0

MT
----

### MT

The parameter MT for a time  $t$  (ms) can be calculated by the following formula:

$$MT = 8 \times t$$

*Note: MT must be greater than 0.*

## Detailed Register Description

**A6<sub>h</sub> SCSTIS Single Talk Attack Speed**

<b>15</b>	<b>0</b>
0	ASP

### ASP

The parameter ASP for a speed  $S$  (dB/ms) can be calculated by the following formula:

$$ASP = \frac{64 \times S}{5 \times \log 2}$$

## Detailed Register Description

**A7<sub>h</sub> SCSTDS Single Talk Decay Speed**

<b>15</b>	<b>0</b>
1	DSP

### DSP

The parameter DSP for a speed  $S$  (dB/ms) can be calculated by the following formula:

$$DSP = \frac{64 \times S}{5 \times \log 2}$$

*Note: DSP is a negative value (0x7FFF = -1)*

## Detailed Register Description

**A8<sub>n</sub> SCLSPN Loudspeaker Noise**

<b>15</b>	<b>0</b>
0	NTH

### NTH

The parameter NTH for a threshold  $L$  (dB, relative to PCM max. value) can be calculated by the following formula:

$$NTH = \frac{512 \times (96.3 + L)}{5 \times \log 2}$$

## Detailed Register Description

**A9<sub>h</sub> SCLSPS Loudspeaker Sensitivity**

<b>15</b>	<b>0</b>
0	GS

### GS

The parameter GS for a sensitivity *SE* (1/dB) can be calculated by the following formula:

$$GS = 2028 \times SE$$

## Detailed Register Description

AA<sub>h</sub> SCLSPL Loudspeaker Limit

15	0
0	LIMIT

### LIMIT

The parameter LIMIT for a level  $L$  (dB, relative to PCM max. value) can be calculated by the following formula:

$$\text{LIMIT} = \frac{512 \times L}{5 \times \log 2}$$

*Note: LIMIT must be greater than 0x7FF.*



## Detailed Register Description

**AB<sub>n</sub> SCCN1 Comfort Noise Constant Level**

<b>15</b>	<b>0</b>
0	CONST

### CONST

The parameter CONST controls the level of the comfort noise. The range is from 0 (off) to 32767 (max.). The parameter has linear behavior.

**Detailed Register Description**

**AC<sub>h</sub> SCCN2 Comfort Noise Multiplication Factor**

<b>15</b>	<b>0</b>
0	FAC

**FAC**

The parameter FAC for a factor *f* can be calculated by the following formula:

$$FAC = 2048 \times f$$

## Detailed Register Description

AD<sub>h</sub>    SCCN3    Comfort Noise Low Pass

15	0
0	LP

### LP

The parameter LP for a time constant  $TS$  (1/ms) can be calculated by the following formula:

$$LP = 983.025 \times TS$$

## Electrical Characteristics

### 6 Electrical Characteristics

#### 6.1 Absolute Maximum Ratings

Parameter	Symbol	Limit Values	Unit
Ambient temperature under bias	$T_A$	-20 to 85	°C
Storage temperature	$T_{STG}$	- 65 to 125	°C
Supply Voltage	$V_{DD}$	-0.5 to 4.2	V
Supply Voltage	$V_{DDA}$	-0.5 to 4.2	V
Supply Voltage	$V_{DDP}$	-0.5 to 6	V
Voltage of pin with respect to ground: XTAL <sub>1</sub> , XTAL <sub>2</sub>	$V_S$	0 to $V_{DDA}$	V
Voltage on any pin with respect to ground	$V_S$	If $V_{DDP}^{1)} < 3\text{ V}$ : - 0.4 to $V_{DD} + 0.5$ If $V_{DDP} > 3\text{ V}$ : - 0.4 to $V_{DDP} + 0.5$	V

<sup>1)</sup>  $V_{DDP}$  must never be fixed to a potential below  $V_{DD}$ .

ESD integrity (according MIL-Std. 883D, method 3015.7): 2 kV

Exception: The pins  $\overline{INT}$ , SDX, DU/DX, DD/DR, SPS<sub>0</sub> and SPS<sub>1</sub> are not protected against voltage stress >1 kV.

*Note: Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.*

#### 6.2 DC Characteristics

$V_{DD}/V_{DDA} = 3.3\text{ V} \pm 0.3\text{ V}$ ;  $V_{DDP} = 5\text{ V} \pm 10\%$ ;  $V_{SS}/V_{SSA} = 0\text{ V}$ ;  $T_A = 0\text{ to }70\text{ °C}$

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Input leakage current	$I_{IL}$	- 1.0		1.0	μA	$0\text{ V} \leq V_{IN} \leq V_{DD}$
H-input level (except GP <sub>0</sub> -GP <sub>15</sub> , XTAL <sub>1</sub> )	$V_{IH1}$	2.0		$V_{DDP} + 0.3$	V	
H-input level (XTAL <sub>1</sub> )	$V_{IH2}$	2.4		$V_{DD}$	V	
H-input level (GP <sub>0</sub> -GP <sub>15</sub> )	$V_{IH4}$	2.0		$V_{DD}$	V	
L-input level (except XTAL <sub>1</sub> )	$V_{IL1}$	- 0.3		0.8	V	
L-input level (XTAL <sub>1</sub> )	$V_{IL2}$	0		0.4	V	

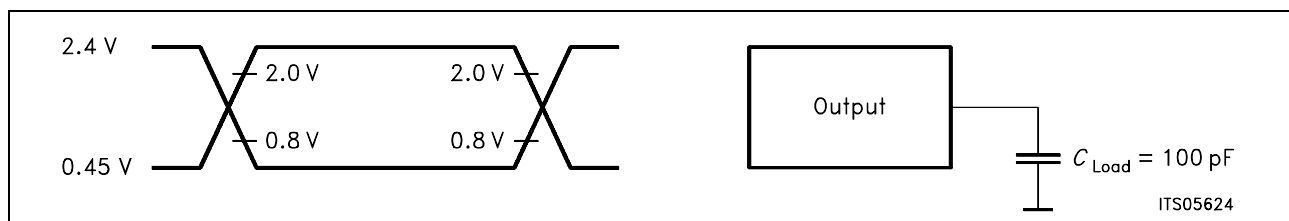
## Electrical Characteristics

$V_{DD}/V_{DDA} = 3.3 \text{ V} \pm 0.3 \text{ V}$ ;  $V_{DDP} = 5 \text{ V} \pm 10\%$ ;  $V_{SS}/V_{SSA} = 0 \text{ V}$ ;  $T_A = 0 \text{ to } 70 \text{ }^\circ\text{C}$

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
H-output level (except DU/DX, DD/DR, GP <sub>0</sub> -GP <sub>15</sub> , SPS <sub>0</sub> , SPS <sub>1</sub> )	V <sub>OH1</sub>	$V_{DD} - 0.45$			V	$I_O = 2 \text{ mA}$
H-output level (SPS <sub>0</sub> , SPS <sub>1</sub> , SDX)	V <sub>OH2</sub>	$V_{DD} - 0.6$			V	$I_O = 2 \text{ mA}$
H-output level (GP <sub>0</sub> -GP <sub>15</sub> )	V <sub>OH3</sub>	$V_{DD} - 0.45$			V	$I_O = 5 \text{ mA}$
H-output level (DU/DX, DD/DR)	V <sub>OH4</sub>	$V_{DD} - 0.6$			V	$I_O = 7 \text{ mA}$
L-output level (except DU/DX, DD/DR, GP <sub>0</sub> -GP <sub>15</sub> )	V <sub>OL1</sub>			0.45	V	$I_O = -2 \text{ mA}$
L-output level (GP <sub>0</sub> -GP <sub>15</sub> )	V <sub>OL2</sub>			0.45	V	$I_O = -5 \text{ mA}$
L-output current (GP <sub>0</sub> -GP <sub>15</sub> ) (after reset)	I <sub>LO</sub>		125		μA	RST=1
L-output level (DU/DX, DD/DR)	V <sub>OL3</sub>			0.45	V	$I_O = -7 \text{ mA}$
Input capacitance	C <sub>I</sub>			10	pF	
Output capacitance	C <sub>O</sub>			15	pF	
V <sub>DD</sub> supply current (powerdown)	I <sub>DDS1</sub>		10	50	μA	
V <sub>DD</sub> supply current (operating)	I <sub>DDO</sub>		55	70	mA	$V_{DD} = 3.3 \text{ V}$
V <sub>DDP</sub> supply current	I <sub>DDP</sub>		1	10	μA	

### 6.3 AC Characteristics

Digital inputs are driven to 2.4 V for a logical “1” and to 0.45 V for a logical “0”. Timing measurements are made at 2.0 V for a logical “1” and 0.8 V for a logical “0”. The AC-testing input/output waveforms are shown below.



**Figure 61 Input/Output Waveforms for AC-Tests**

## Electrical Characteristics

### DTMF Detector

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Frequency deviation accept		-1.5		1.5	%	
Frequency deviation reject		3.5		-3.5	%	
Acceptance level		-45		0	dB	rel. to max. PCM
Rejection level				-50	dB	rel. to max. PCM
Twist deviation accept		+/-2		+/-8	dB	programmable
Noise Tolerance				12	dB	
Signal duration accept		40			ms	
Signal duration reject				19	ms	
Gap duration accept		18			ms	

### Caller ID Decoder

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Frequency deviation accept		-2		2	%	
Acceptance level		-45		0	dB	rel. to max. PCM
Transmission rate		1188	1200	1212	baud	
Noise Tolerance				12	dB	

### Echo Cancellation Unit (subband mode)

subband (Hz)		filter length (ms)		
lower limit	upper limit	submode 1	submode 2	submode 3
0	250	105	130	130
250	750	178	208	208
750	1250	94	113	126
1250	1750	65	84	94
1750	2250	65	84	94
2250	2750	63	71	87
2750	3250	32	40	52
3250	3750	32	40	52

## Electrical Characteristics

## Alert Tone Detector

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Frequency deviation accept		-0.5		0.5	%	ATDCTL1:DEV=0
Frequency deviation accept		-1.1		1.1	%	ATDCTL1:DEV=1
Frequency deviation reject		3.5		-3.5	%	
Acceptance level		-40		0	dB	rel. to max. PCM
Rejection level				-5	dB	rel. to acceptance level
Twist deviation accept				+/-7	dB	
Noise Tolerance				20	dB	
Signal duration accept		75			ms	
Gap duration accept		40			ms	ATDCTL1:GT=0
Gap duration accept		12			ms	ATDCTL1:GT=1

## Electrical Characteristics

### Status Register Update Time

The individual bits of the STATUS register may change due to an event (like a recognized DTMF tone) or a command. The timing can be divided into four classes

**Table 57 Status Register Update Timing**

Class	Timing		Comment
	Min.	Max.	
I	0	0	Immediately after command has been issued
A	0	125 $\mu$ s <sup>1)</sup>	Command has been accepted
D	125 $\mu$ S	250 $\mu$ s	Deactivation time after command has been issued
E	-	-	Associated event has happened

<sup>1)</sup> one FSC period

With these definitions the timing of the individual bits in the STATUS register can be given as shown in the following table:

Bit	RDY	ABT	CIA	CD	CPT	CNG	DTV	ATV	ATC
<b>0-&gt;1</b>	A	E	E	E	E	E	E	E	A
<b>1-&gt;0</b>	I	A	A,D	E,D	E,D	D	E,D	E,D	E,D



Electrical Characteristics

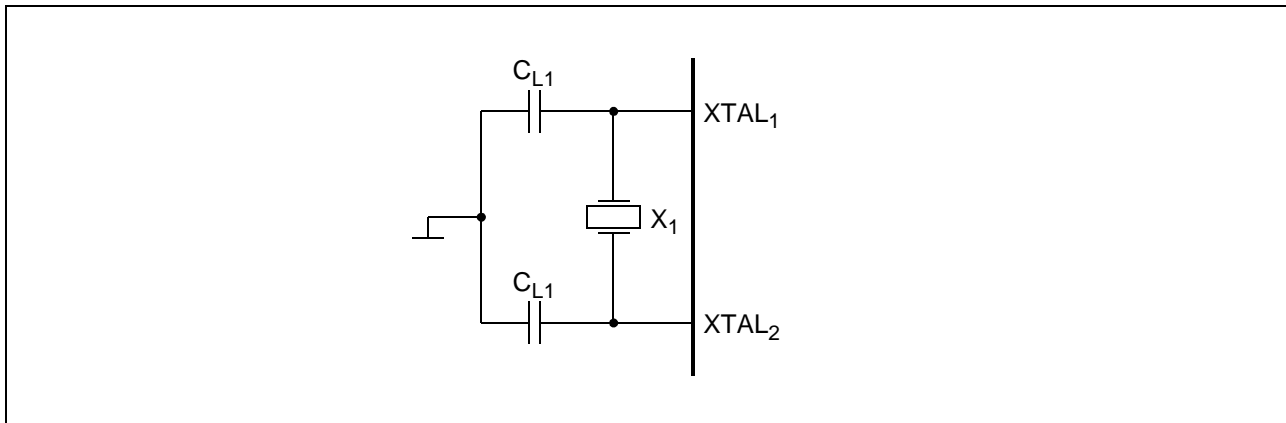


Figure 62 Oscillator Circuit

Recommended Values Oscillator Circuit	Value			Unit
	Min	Typ	Max	
Load $CL_1$			40	pF
Static capacitance $X_1$			5	pF
Motional capacitance $X_1$			17	fF
Resonance resistor $X_1$			60	$\Omega$

Electrical Characteristics

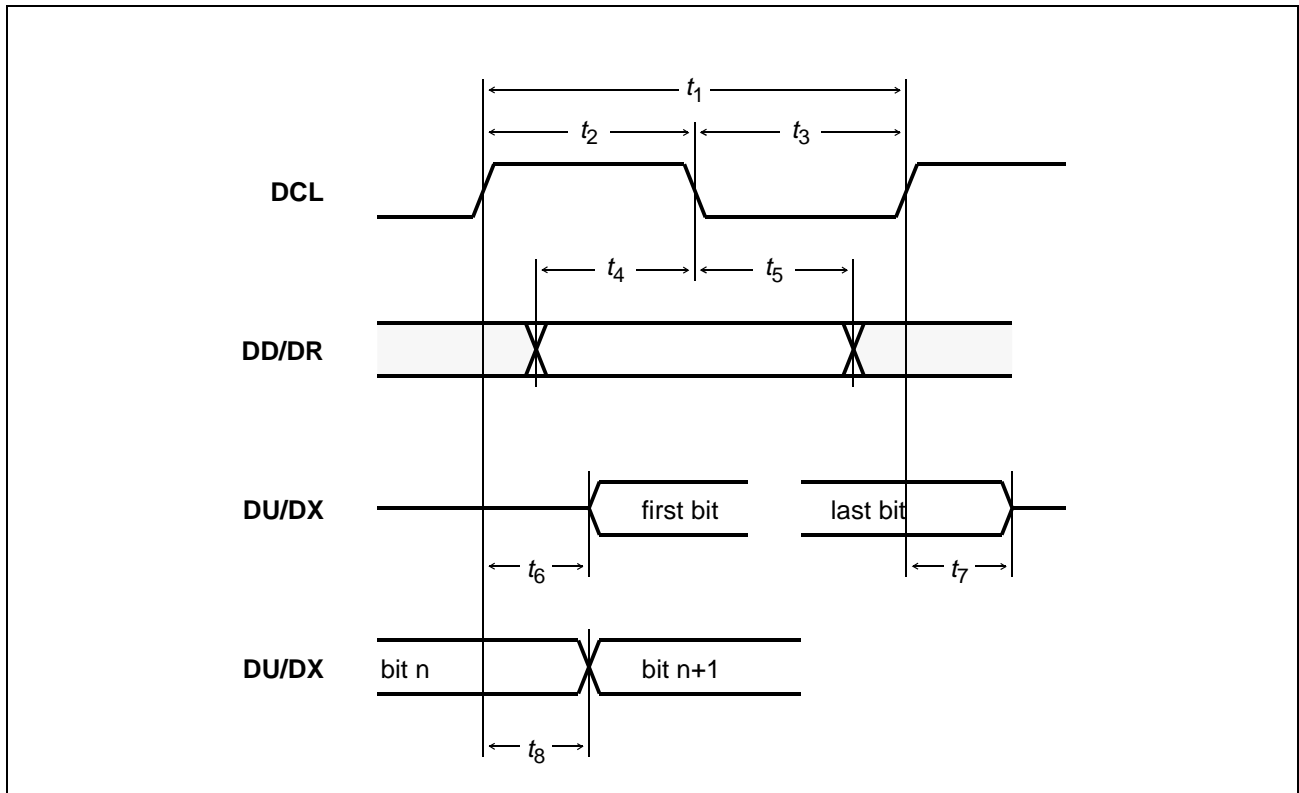


Figure 63 SSDI/IOM<sup>®</sup>-2 Interface - Bit Synchronization Timing

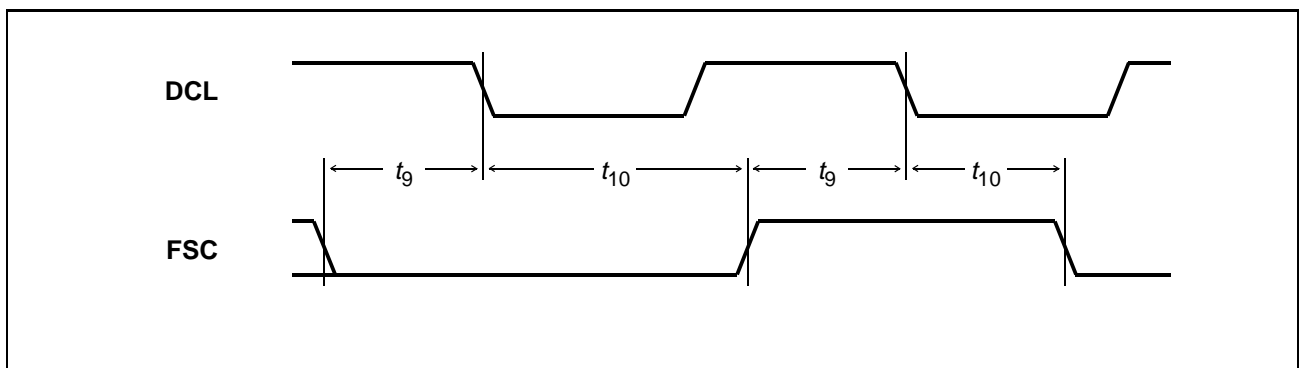


Figure 64 SSDI/IOM<sup>®</sup>-2 Interface - Frame Synchronization Timing

Parameter SSDI/IOM <sup>®</sup> -2 Interface	Symbol	Limit values		Unit
		Min	Max	
DCL period	$t_1$	90		ns
DCL high	$t_2$	35		ns
DCL low	$t_3$	35		ns
Input data setup	$t_4$	20		ns

## Electrical Characteristics

Parameter SSDI/IOM <sup>®</sup> -2 Interface	Symbol	Limit values		Unit
		Min	Max	
Input data hold	$t_5$	10		ns
Output data from high impedance to active (FSC high or other than first timeslot)	$t_6$		30	ns
Output data from active to high impedance	$t_7$		30	ns
Output data delay from clock	$t_8$		30	ns
FSC setup	$t_9$	40		ns
FSC hold	$t_{10}$	40		ns
FSC jitter (deviation per frame)		-200	200	ns

Electrical Characteristics

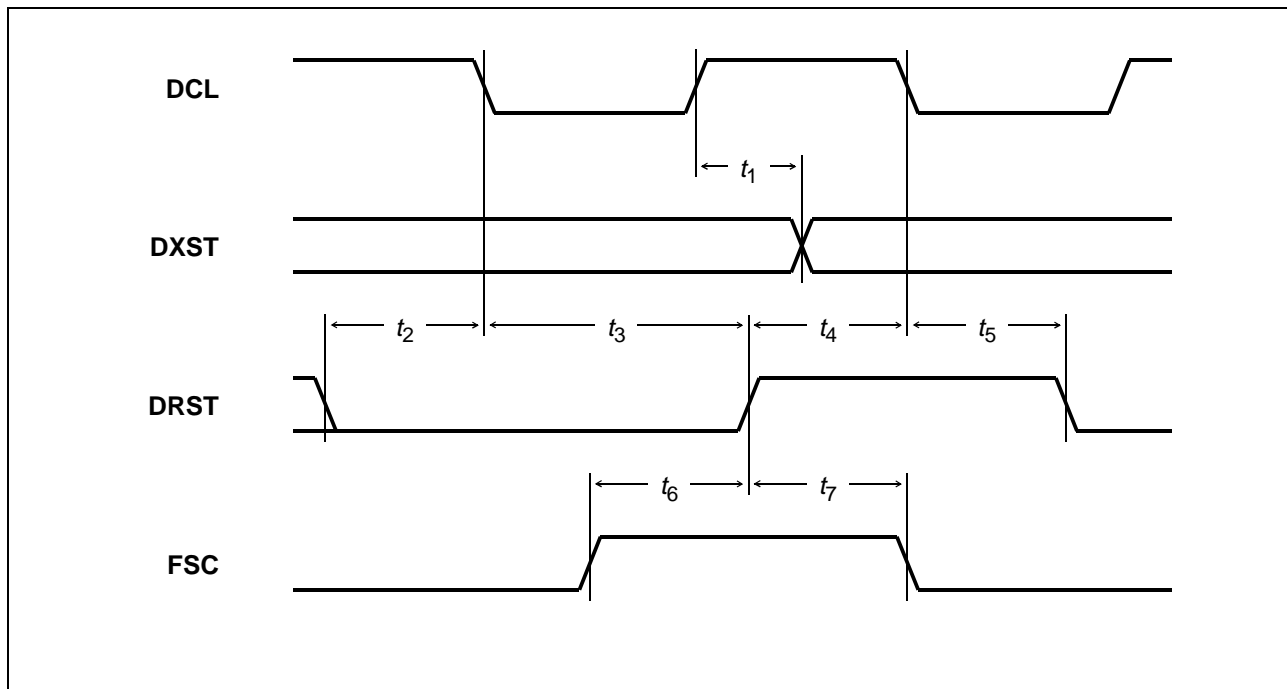


Figure 65 SSDI Interface - Strobe Timing

Parameter SSDI Interface	Symbol	Limit values		Unit
		Min	Max	
DXST delay	$t_1$		20	ns
DRST inactive setup	$t_2$	20		ns
DRST inactive hold	$t_3$	20		ns
DRST active setup	$t_4$	20		ns
DRST active hold	$t_5$	20		ns
FSC setup	$t_6$	8		DCL cycles
FSC hold	$t_7$	40		ns

Electrical Characteristics

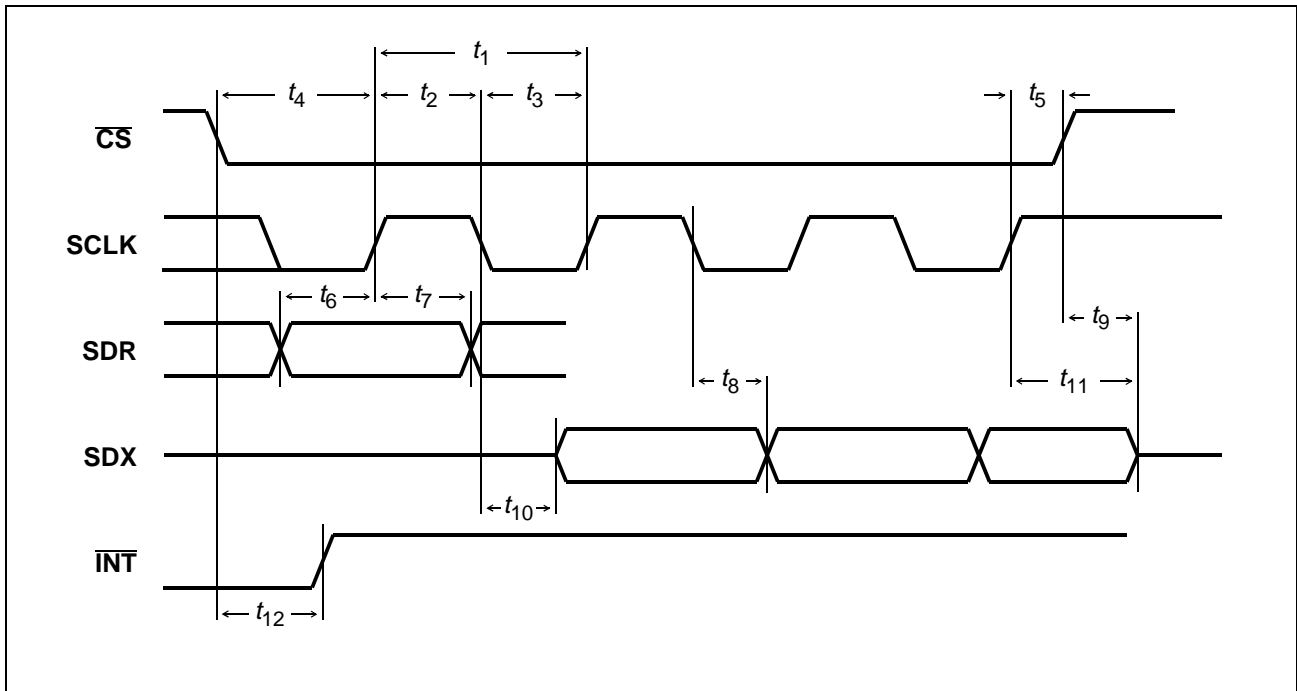


Figure 66 SCI Interface

Parameter SCI Interface	Symbol	Limit values		Unit
		Min	Max	
SCLK cycle time	$t_1$	500		ns
SCLK high time	$t_2$	100		ns
SCLK low time	$t_3$	100		ns
$\overline{CS}$ setup time	$t_4$	40		ns
$\overline{CS}$ hold time	$t_5$	10		ns
SDR setup time	$t_6$	40		ns
SDR hold time	$t_7$	40		ns
SDX data out delay	$t_8$		80	ns
$\overline{CS}$ high to SDX tristate	$t_9$		40	ns
SCLK to SDX active	$t_{10}$		80	ns
SCLK to SDX tristate	$t_{11}$		40	ns
$\overline{CS}$ to $\overline{INT}$ delay	$t_{12}$		80	ns

Electrical Characteristics

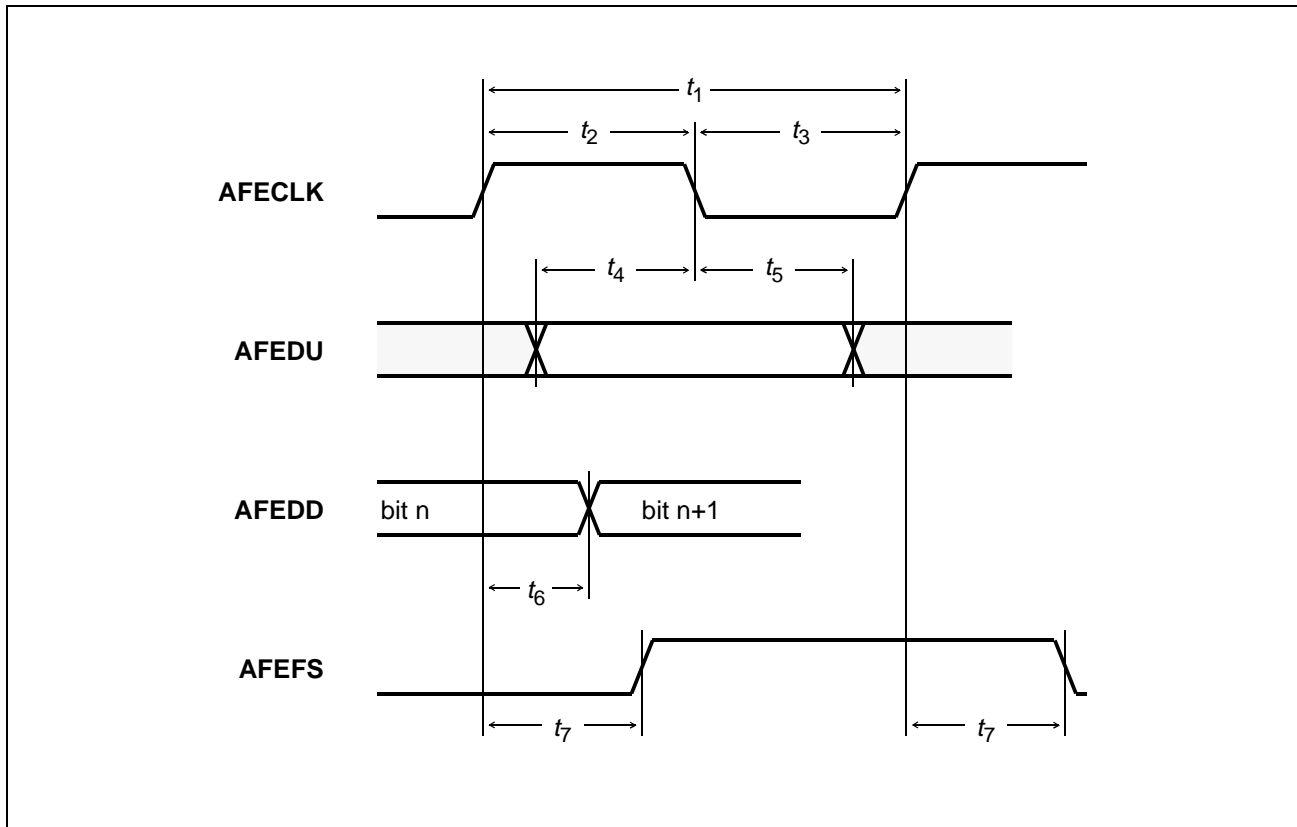


Figure 67 Analog Front End Interface

Parameter AFE Interface	Symbol	Limit values		Unit
		Min	Max	
AFECLK period	$t_1$	125	165	ns
AFECLK high	$t_2$	2		$1/f_{XTAL}$
AFECLK low	$t_3$	2		$1/f_{XTAL}$
AFEDU setup	$t_4$	20		ns
AFEDU hold	$t_5$	20		ns
AFEDD output delay	$t_6$		30	ns
AFEFS output delay	$t_7$		30	ns

Electrical Characteristics

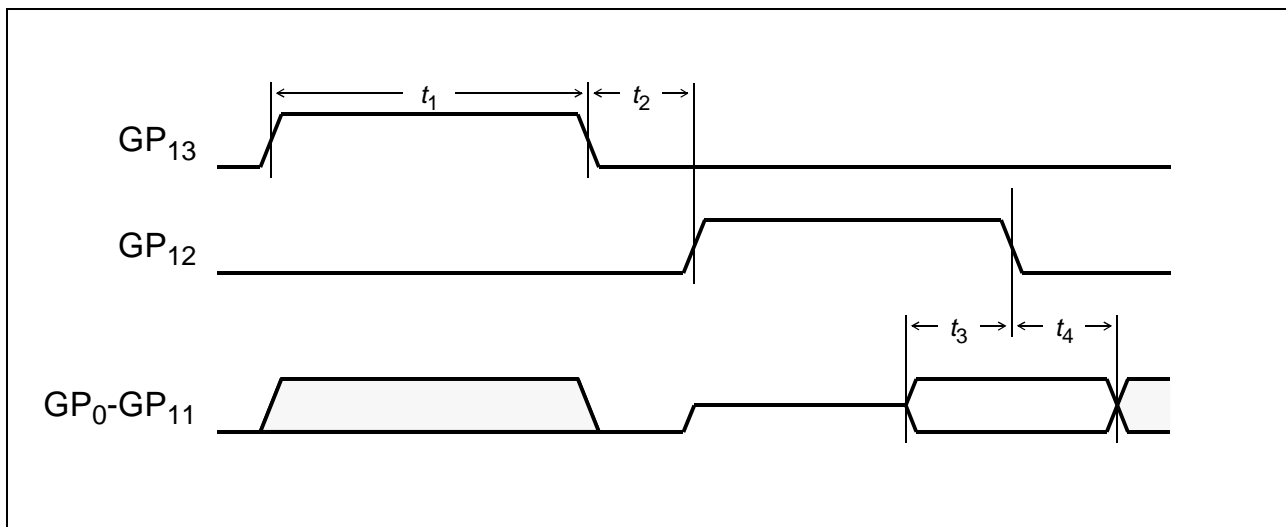


Figure 68 General Purpose Parallel Port - Multiplex Mode

Parameter	Symbol	Limit values			Unit
		Min	Typ	Max	
General Purpose Parallel Port - Multiplex Mode					
Active time (GP <sub>0</sub> -GP <sub>15</sub> )	<i>t</i> <sub>1</sub>		2		ms
Gap time (GP <sub>0</sub> -GP <sub>15</sub> )	<i>t</i> <sub>2</sub>		125		μs
Data setup time	<i>t</i> <sub>3</sub>	50			ns
Data hold time	<i>t</i> <sub>4</sub>	0			ns

Electrical Characteristics

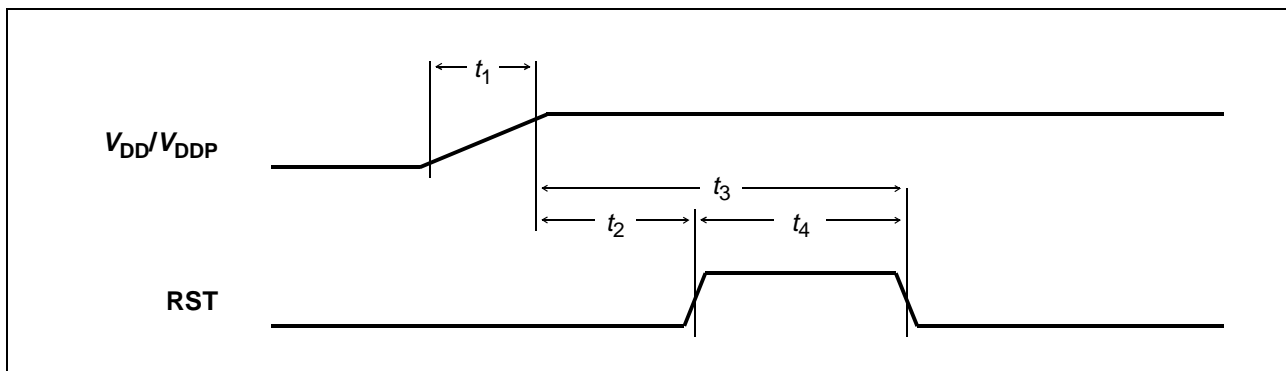


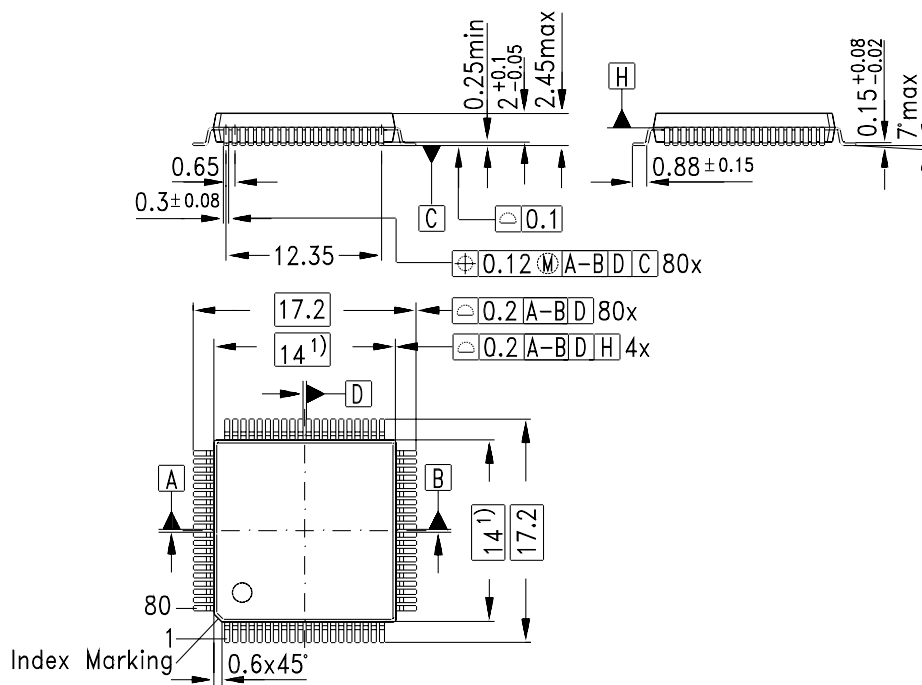
Figure 69 Reset Timing

Parameter Reset Timing	Symbol	Limit values		Unit
		Min	Max	
$V_{DD}/V_{DDP}/V_{DDA}$ rise time 5%-95%	$t_1$		20	ms
Supply voltages stable to RST high	$t_2$	0		ns
Supply voltages stable to RST low	$t_3$	0.1		ms
RST high time	$t_4$	1000		ns



7 Package Outlines

**Plastic Package, P-MQFP-80 (SMD)**  
(Plastic Metric Quad Flat Package)



1) Does not include plastic or metal protrusions of 0.25 max per side

**Sorts of Packing**

Package outlines for tubes, trays etc. are contained in our Data Book "Package Information".

SMD = Surface Mounted Device

Dimensions in mm

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