

512 Kbit / 1 Mbit / 2 Mbit / 4 Mbit (x8) Many-Time Programmable Flash

SST37VF512 / SST37VF010 / SST37VF020 / SST37VF040



Data Sheet

FEATURES:

- **Organized as 64K x8 / 128K x8 / 256K x8 / 512K x8**
- **2.7-3.6V Read Operation**
- **Superior Reliability**
 - Endurance: At least 1000 Cycles
 - Greater than 100 years Data Retention
- **Low Power Consumption:**
 - Active Current: 10 mA (typical)
 - Standby Current: 2 μ A (typical)
- **Fast Read Access Time:**
 - 70 ns
 - 90 ns
- **Latched Address and Data**
- **Fast Byte-Program Operation:**
 - Byte-Program Time: 10 μ s (typical)
 - Chip Program Time:
 - 0.6 seconds (typical) for SST37VF512
 - 1.2 seconds (typical) for SST37VF010
 - 2.4 seconds (typical) for SST37VF020
 - 4.8 seconds (typical) for SST37VF040
- **Electrical Erase Using Programmer**
 - Does not require UV source
 - Chip-Erase Time: 100 ms (typical)
- **CMOS I/O Compatibility**
- **JEDEC Standard Byte-wide Flash EEPROM Pinouts**
- **Packages Available**
 - 32-pin PLCC
 - 32-pin TSOP (8mm x 14mm)
 - 32-pin PDIP

PRODUCT DESCRIPTION

The SST37VF512/010/020/040 devices are 64K x8 / 128K x8 / 256K x8 / 512K x8 CMOS, Many-Time Programmable (MTP), low cost flash, manufactured with SST's proprietary, high performance CMOS SuperFlash technology. The split-gate cell design and thick oxide tunneling injector attain better reliability and manufacturability compared with alternate approaches. The SST37VF512/010/020/040 can be electrically erased and programmed at least 1000 times using an external programmer, e.g., to change the contents of devices in inventory. The SST37VF512/010/020/040 have to be erased prior to programming. These devices conform to JEDEC standard pinouts for byte-wide flash memories.

Featuring high performance Byte-Program, the SST37VF512/010/020/040 provide a typical Byte-Program time of 10 μ s. Designed, manufactured, and tested for a wide spectrum of applications, these devices are offered with an endurance of at least 1000 cycles. Data retention is rated at greater than 100 years.

The SST37VF512/010/020/040 are suited for applications that require infrequent writes and low power nonvolatile storage. These devices will improve flexibility, efficiency, and performance while matching the low cost in nonvolatile applications that currently use UV-EPROMs, OTPs, and mask ROMs.

To meet surface mount and conventional through hole requirements, the SST37VF512/010/020/040 are offered in 32-pin PLCC, TSOP, and PDIP packages. See Figures 1, 2, and 3 for pinouts.

Device Operation

The SST37VF512/010/020/040 devices are nonvolatile memory solutions that can be used instead of standard flash devices if in-system programmability is not required. It is functionally (Read) and pin compatible with industry standard flash products. The device supports electrical Erase operation via an external programmer.

Read

The Read operation of the SST37VF512/010/020/040 is controlled by CE# and OE#. Both CE# and OE# have to be low for the system to obtain data from the outputs. Once the address is stable, the address access time is equal to the delay from CE# to output (T_{CE}). Data is available at the output after a delay of TOE from the falling edge of OE#, assuming the CE# pin has been low and the addresses have been stable for at least $T_{CE} - T_{OE}$. When the CE# pin is high, the chip is deselected and a standby current of only 10 μ A (typical) is consumed. OE# is the output control and is used to gate data from the output pins. The data bus is in high impedance state when either CE# or OE# is V_{IH} . Refer to Figure 4 for the timing diagram.

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Byte-Program Operation

The SST37VF512/010/020/040 are programmed by using an external programmer. The programming mode is activated by asserting 12V ($\pm 5\%$) on OE# pin and V_{IL} on CE# pin. The device is programmed using a single pulse (WE# pin low) of 10 μ s per byte. Using the MTP programming algorithm, the Byte-Program process continues byte-by-byte until the entire chip has been programmed. Refer to Figure 10 for the flowchart and Figure 6 for the timing diagram.

Chip-Erase Operation

The only way to change a data from a "0" to "1" is by electrical erase that changes every bit in the device to "1". The SST37VF512/010/020/040 use an electrical Chip-Erase operation. The entire chip can be erased in 100 ms (WE# pin low). In order to activate erase mode, the 12V ($\pm 5\%$) is applied to OE# and A_9 pins while CE# is low. All other address and data pins are "don't care". The falling edge of WE# will start the Chip-Erase operation. Once the chip has been erased, all bytes must be verified for FFH. Refer to Figure 9 for the flowchart and Figure 5 for the timing diagram.

Product Identification Mode

The Product Identification mode identifies the devices as SST37VF512, SST37VF010, SST37VF020, and SST37VF040 and manufacturer as SST. This mode may be accessed by the hardware method. To activate this mode, the programming equipment must force V_H ($12V \pm 5\%$) on address A_9 . Two identifier bytes may then be sequenced from the device outputs by toggling address line A_0 . For details, see Table 3 for hardware operation.

TABLE 1: PRODUCT IDENTIFICATION

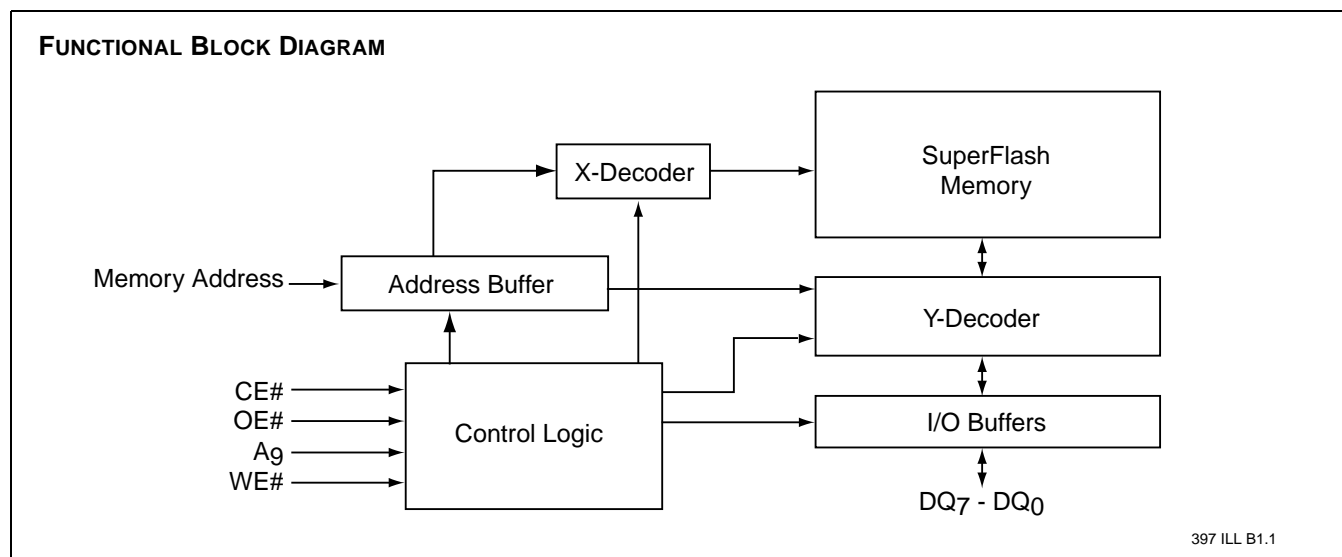
| | Address | Data |
|-------------------|---------|------|
| Manufacturer's ID | 0000H | BFH |
| Device ID | | |
| SST37VF512 | 0001H | C4H |
| SST37VF010 | 0001H | C5H |
| SST37VF020 | 0001H | C6H |
| SST37VF040 | 0001H | C2H |

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Design Considerations

The SST37VF512/010/020/040 should have a 0.1 μ F ceramic high frequency, low inductance capacitor connected between V_{DD} and GND. This capacitor should be placed as close to the package terminals as possible.

OE# and A_9 must remain stable at V_H for the entire duration of an Erase operation. OE# must remain stable at V_H for the entire duration of the Program operation.



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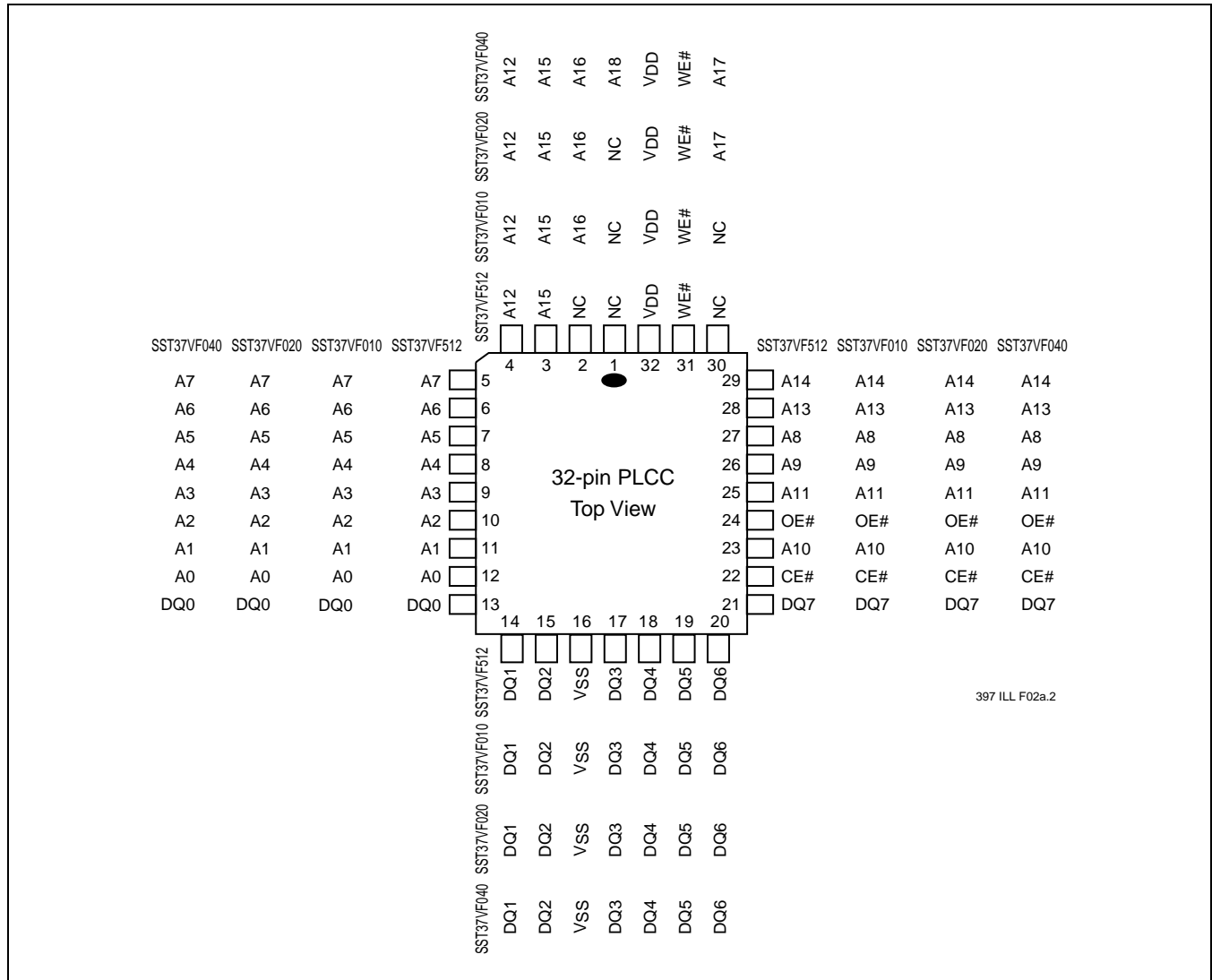


FIGURE 1: PIN ASSIGNMENTS FOR 32-PIN PLCC

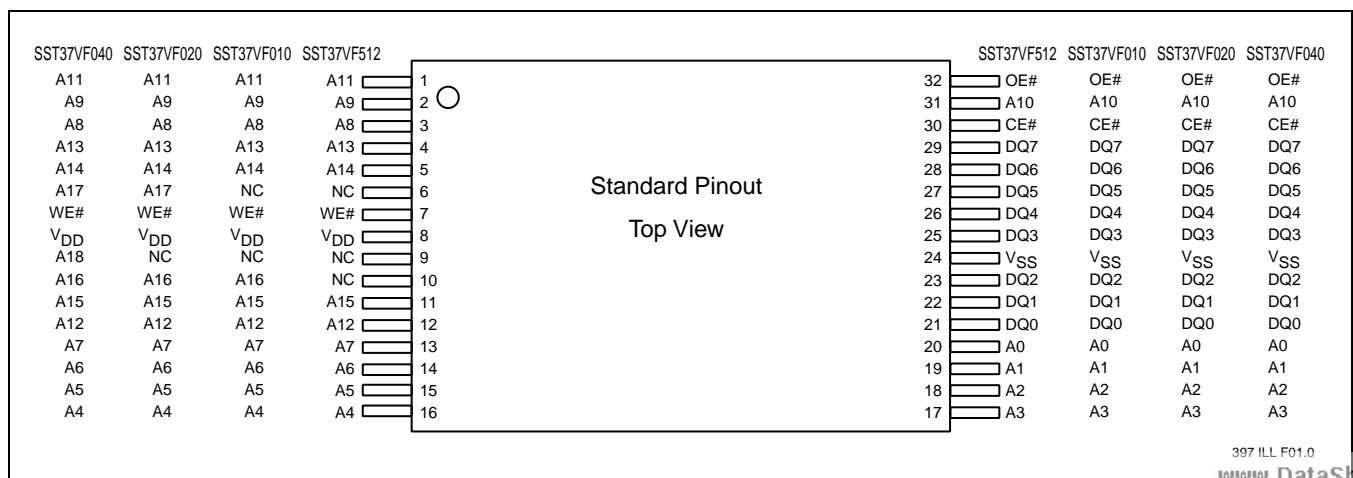


FIGURE 2: PIN ASSIGNMENTS FOR 32-PIN TSOP (8MM X 14MM)



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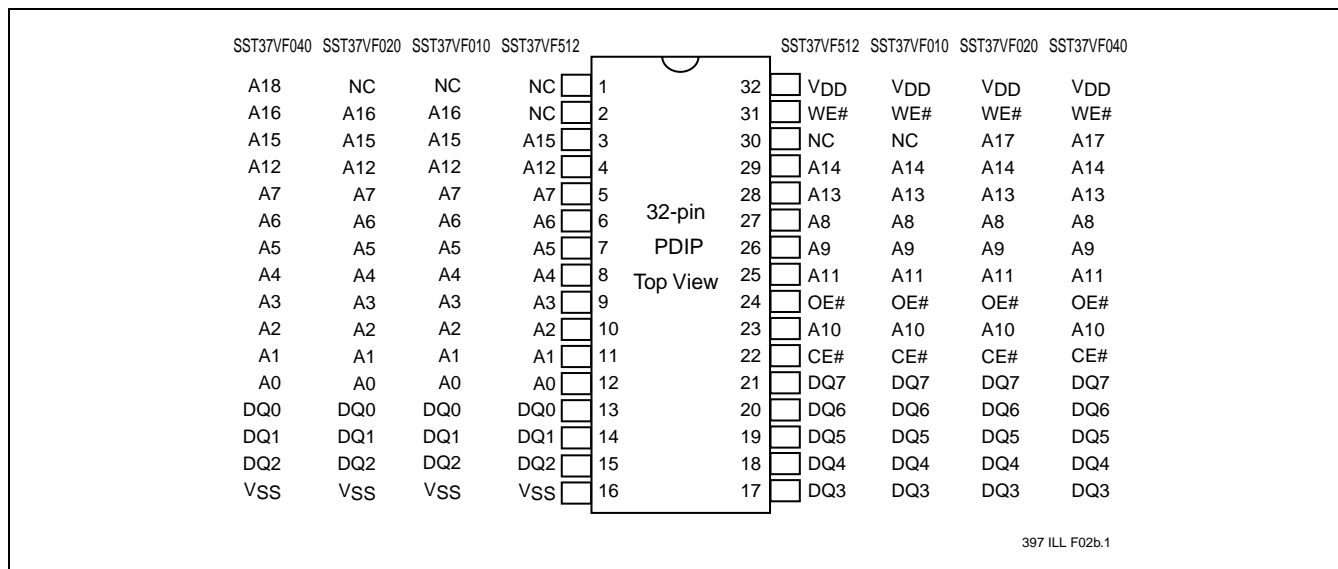


FIGURE 3: PIN ASSIGNMENTS FOR 32-PIN PDIP

TABLE 2: PIN DESCRIPTION

| Symbol | Pin Name | Functions |
|----------------------------------|-------------------|---|
| A_{MS}^1 -A ₀ | Address Inputs | To provide memory addresses. |
| DQ ₇ -DQ ₀ | Data Input/output | To output data during Read cycles and receive input data during Program cycles. The outputs are in tri-state when OE# or CE# is high. |
| CE# | Chip Enable | To activate the device when CE# is low. |
| WE# | Write Enable | To program or erase (WE# = V _{IL} pulse during Program or Erase) |
| OE# | Output Enable | To gate the data output buffers during Read operation when low |
| V _{DD} | Power Supply | To provide 3.0V supply (2.7-3.6V) |
| V _{SS} | Ground | |
| NC | No Connection | Unconnected pins. |

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1. A_{MS} = Most significant address

A_{MS} = A₁₅ for SST37VF512, A₁₆ for SST37VF010, A₁₇ for SST37VF020, and A₁₈ for SST37VF040



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TABLE 3: OPERATION MODES SELECTION

| Mode | CE# | WE# | A ₉ | OE# | DQ | Address |
|------------------------|-----------------|-----------------|-----------------|------------------------------------|---|--|
| Read | V _{IL} | V _{IH} | A _{IN} | V _{IL} | D _{OUT} | A _{IN} |
| Output Disable | V _{IL} | X | X | V _{IH} | High Z | A _{IN} |
| Standby | V _{IH} | X | X | X | High Z | X |
| Chip-Erase | V _{IL} | V _{IL} | V _H | V _H | High Z | X |
| Byte-Program | V _{IL} | V _{IL} | A _{IN} | V _H | D _{IN} | A _{IN} |
| Program/Erase Inhibit | X | V _{IH} | X | X | High Z | X |
| | X | X | X | V _{IL} or V _{IH} | High Z/ D _{OUT} | X |
| Product Identification | V _{IL} | V _{IH} | V _H | V _{IL} | Manufacturer's ID (BFH) Device ID ¹ | A _{MS} ² - A ₁ = V _{IL} , A ₀ = V _{IL} A _{MS} ² - A ₁ = V _{IL} , A ₀ = V _{IH} |

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1. Device ID = C4H for SST37VF512, C5H for SST37VF020, C6H for SST37VF020, and C2H for SST37VF040

2. A_{MS} = Most significant address

A_{MS} = A₁₅ for SST37VF512, A₁₆ for SST37VF010, A₁₇ for SST37VF020, and A₁₈ for SST37VF040

Note: X = V_{IL} or V_{IH} (or V_H in case of OE# and A₉)

V_H = 12V±5%

Absolute Maximum Stress Ratings (Applied conditions greater than those listed under "Absolute Maximum Stress Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

| | |
|--|---------------------------------|
| Temperature Under Bias | -55°C to +125°C |
| Storage Temperature | -65°C to +150°C |
| D. C. Voltage on Any Pin to Ground Potential | -0.5V to V _{DD} + 0.5V |
| Transient Voltage (<20 ns) on Any Pin to Ground Potential | -1.0V to V _{DD} + 1.0V |
| Voltage on A ₉ Pin to Ground Potential | -0.5V to 13.2V |
| Package Power Dissipation Capability (T _a = 25°C) | 1.0W |
| Through Hold Lead Soldering Temperature (10 Seconds) | 300°C |
| Surface Mount Lead Soldering Temperature (3 Seconds) | 240°C |
| Output Short Circuit Current ¹ | 50 mA |

1. Outputs shorted for no more than one second. No more than one output shorted at a time.

OPERATING RANGE

| Range | Ambient Temp | V _{DD} |
|------------|--------------|-----------------|
| Commercial | 0°C to +70°C | 2.7-3.6V |

AC CONDITIONS OF TEST

| | |
|----------------------|-------------------------|
| Input Rise/Fall Time | 5 ns |
| Output Load | C _L = 100 pF |
| See Figures 7 and 8 | |



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TABLE 4: READ MODE DC OPERATING CHARACTERISTICS $V_{DD}=2.7-3.6V$ ($T_a = 0^{\circ}C$ to $+70^{\circ}C$ (Commercial))

| Symbol | Parameter | Limits | | | Test Conditions |
|-----------|--|--------------|-----|---------|---|
| | | Min | Max | Units | |
| I_{DD} | V_{DD} Read Current | | 12 | mA | Address input= V_{IL}/V_{IH} , at $f=1/T_{RC}$ Min $V_{DD}=V_{DD}$ Max $CE\#=OE\#=V_{IL}$, all I/Os open |
| I_{SB} | Standby V_{DD} Current | | 15 | μA | $CE\#=V_{IHC}$, $V_{DD}=V_{DD}$ Max |
| I_{LI} | Input Leakage Current | | 1 | μA | $V_{IN}=GND$ to V_{DD} , $V_{DD}=V_{DD}$ Max |
| I_{LO} | Output Leakage Current | | 10 | μA | $V_{OUT}=GND$ to V_{DD} , $V_{DD}=V_{DD}$ Max |
| V_{IL} | Input Low Voltage | | 0.8 | V | $V_{DD}=V_{DD}$ Min |
| V_{IH} | Input High Voltage | $0.7 V_{DD}$ | | V | $V_{DD}=V_{DD}$ Max |
| V_{IHC} | Input High Voltage (CMOS) | $V_{DD}-0.3$ | | V | $V_{DD}=V_{DD}$ Max |
| V_{OL} | Output Low Voltage | | 0.2 | V | $I_{OL}=100 \mu A$, $V_{DD}=V_{DD}$ Min |
| V_{OH} | Output High Voltage | $V_{DD}-0.3$ | | V | $I_{OH}=-100 \mu A$, $V_{DD}=V_{DD}$ Min |
| I_H | Supervoltage Current for A_9 for Read-ID | | 200 | μA | $CE\#=OE\#=V_{IL}$, $A_9=V_H$ Max |

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TABLE 5: PROGRAM/ERASE DC OPERATING CHARACTERISTICS $V_{DD}=2.7-3.6V$ ($T_a = 25^{\circ}C \pm 5^{\circ}C$)

| Symbol | Parameter | Limits | | | Test Conditions |
|----------|---|--------|------|---------|---|
| | | Min | Max | Units | |
| I_{DD} | V_{DD} Erase or Program Current | | 20 | mA | $CE\#=V_{IL}$, $OE\#=V_H$, $V_{DD}=V_{DD}$ Max, $WE\#=V_{IL}$ |
| I_{LI} | Input Leakage Current | | 1 | μA | $V_{IN}=GND$ to V_{DD} , $V_{DD}=V_{DD}$ Max |
| I_{LO} | Output Leakage Current | | 10 | μA | $V_{OUT}=GND$ to V_{DD} , $V_{DD}=V_{DD}$ Max |
| V_H | Supervoltage for A_9 and $OE\#$ | 11.4 | 12.6 | V | |
| I_H | Supervoltage Current for A_9 and $OE\#$ | | 200 | μA | $OE\#=V_H$ Max, $A_9=V_H$ Max, $V_{DD}=V_{DD}$ Max, $CE\#=V_{IL}$ |

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TABLE 6: RECOMMENDED SYSTEM POWER-UP TIMINGS

| Symbol | Parameter | Minimum | Units |
|------------------|-----------------------------|---------|---------|
| $T_{PU-READ}^1$ | Power-up to Read Operation | 100 | μs |
| $T_{PU-WRITE}^1$ | Power-up to Write Operation | 100 | μs |

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1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 7: CAPACITANCE ($T_a = 25^{\circ}C$, $f=1$ Mhz, other pins open)

| Parameter | Description | Test Condition | Maximum |
|-------------|---------------------|----------------|---------|
| $C_{I/O}^1$ | I/O Pin Capacitance | $V_{I/O} = 0V$ | 12 pF |
| C_{IN}^1 | Input Capacitance | $V_{IN} = 0V$ | 6 pF |

T7.0 397

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 8: RELIABILITY CHARACTERISTICS

| Symbol | Parameter | Minimum Specification | Units | Test Method |
|-------------|----------------|-----------------------|--------|---------------------|
| N_{END}^1 | Endurance | 10,000 | Cycles | JEDEC Standard A117 |
| T_{DR}^1 | Data Retention | 100 | Years | JEDEC Standard A103 |
| I_{LTH}^1 | Latch Up | $100 + I_{DD}$ | mA | JEDEC Standard 78 |

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.



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AC CHARACTERISTICS

TABLE 9: READ CYCLE TIMING PARAMETERS $V_{DD} = 2.7-3.6V$ ($T_a = 0^\circ C$ to $+70^\circ C$ (Commercial))

| Symbol | Parameter | SST37VF512-70 SST37VF010-70 SST37VF020-70 SST37VF040-70 | | SST37VF512-90 SST37VF010-90 SST37VF020-90 SST37VF040-90 | | Units |
|-------------|---------------------------------|--|-----|--|-----|-------|
| | | Min | Max | Min | Max | |
| T_{RC} | Read Cycle Time | 70 | | 90 | | ns |
| T_{CE} | Chip Enable Access Time | | 70 | | 90 | ns |
| T_{AA} | Address Access Time | | 70 | | 90 | ns |
| T_{OE} | Output Enable Access Time | | 35 | | 45 | ns |
| T_{CLZ}^1 | CE# Low to Active Output | 0 | | 0 | | ns |
| T_{OLZ}^1 | OE# Low to Active Output | 0 | | 0 | | ns |
| T_{CHZ}^1 | CE# High to High-Z Output | | 30 | | 30 | ns |
| T_{OHZ}^1 | OE# High to High-Z Output | | 30 | | 30 | ns |
| T_{OH}^1 | Output Hold from Address Change | 0 | | 0 | | ns |

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1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 10: PROGRAM/ERASE CYCLE TIMING PARAMETERS $V_{DD} = 2.7-3.6V$ ($T_a = 25^\circ C \pm 5^\circ C$)

| Symbol | Parameter | Min | Max | Units |
|-----------|--|-----|-----|---------|
| T_{BP} | Byte-Program Time | 12 | 20 | μs |
| T_{CES} | CE# Setup Time | 1 | | ns |
| T_{CEH} | CE# Hold Time | 1 | | ns |
| T_{AS} | Address Setup Time | 1 | | ns |
| T_{AH} | Address Hold Time | 1 | | ns |
| T_{DS} | Data Setup Time | 1 | | ns |
| T_{DH} | Data Hold Time | 1 | | ns |
| T_{PRT} | OE# Rise Time for Program and Erase | 1 | | ns |
| T_{VPS} | OE# Setup Time for Program and Erase | 1 | | ns |
| T_{VPH} | OE# Hold Time for Program and Erase | 1 | | ns |
| T_{PW} | WE# Program Pulse Width | 10 | 15 | ns |
| T_{EW} | WE# Erase Pulse Width | 100 | 500 | ns |
| T_{VR} | OE#/A ₉ Recovery Time for Erase | 1 | | ns |
| T_{ART} | A ₉ Rise Time to 12V during Erase | 1 | | ns |
| T_{A9S} | A ₉ Setup Time during Erase | 1 | | ms |
| T_{A9H} | A ₉ Hold Time during Erase | 1 | | ms |

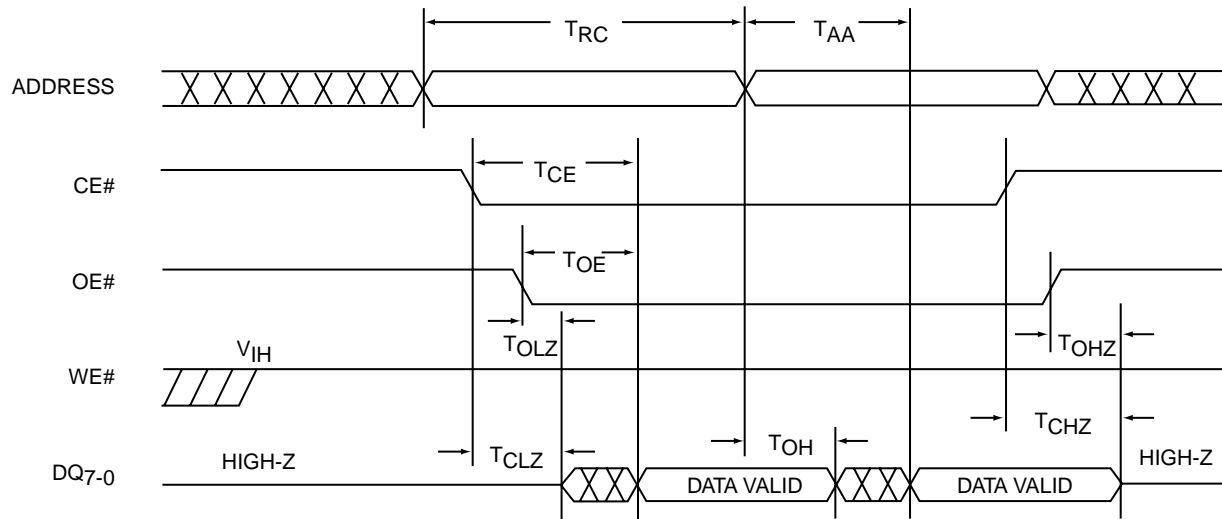
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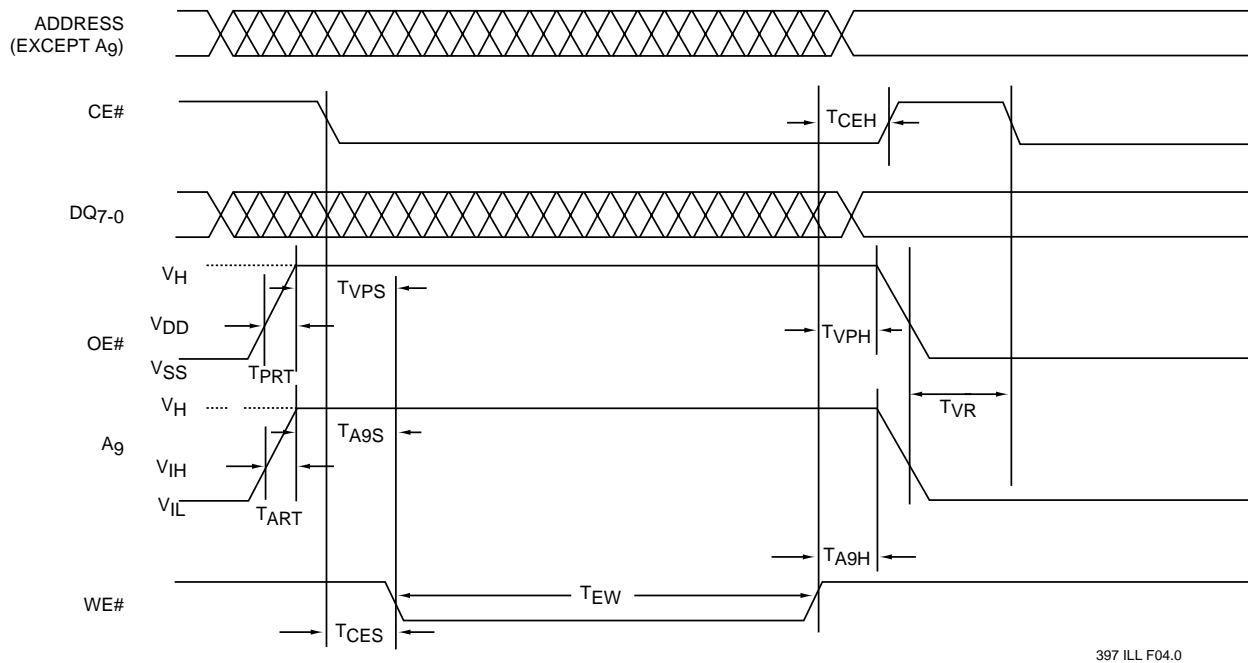
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FIGURE 4: READ CYCLE TIMING DIAGRAM



397 ILL F04.0

FIGURE 5: CHIP-ERASE TIMING DIAGRAM

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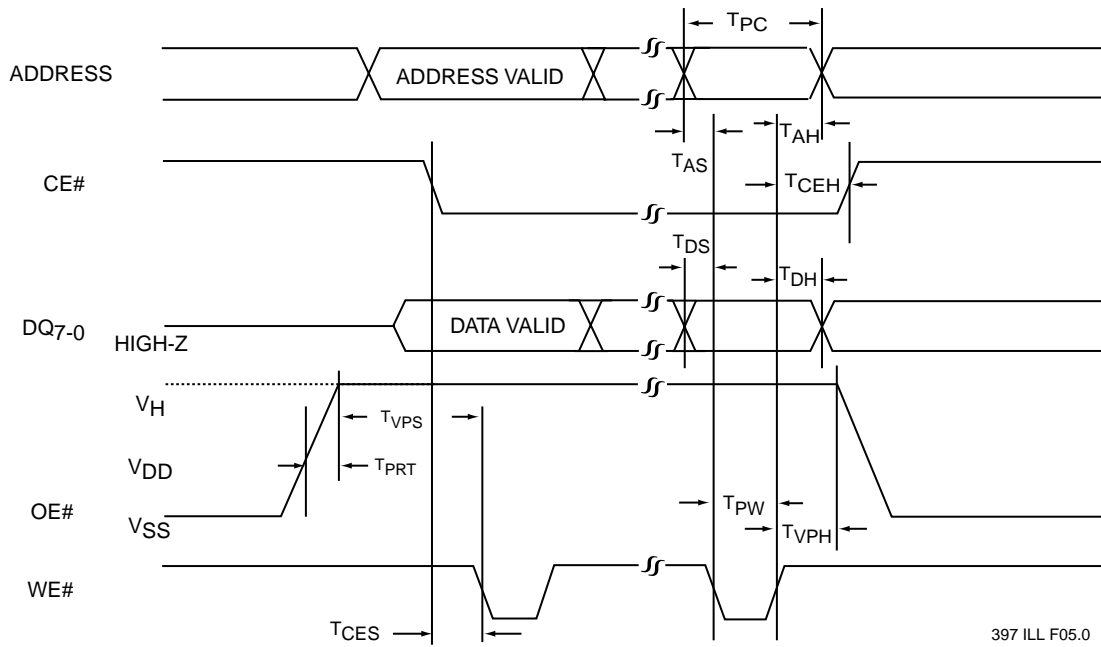
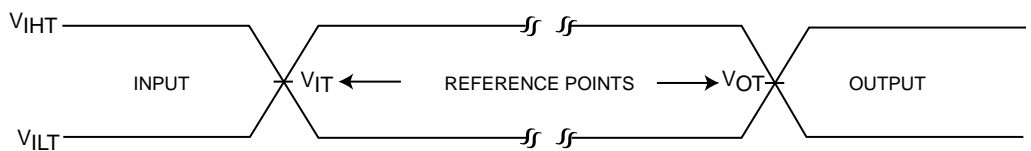


FIGURE 6: BYTE-PROGRAM TIMING DIAGRAM



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AC test inputs are driven at V_{IHT} ($0.9 V_{DD}$) for a logic "1" and V_{ILT} ($0.1 V_{DD}$) for a logic "0". Measurement reference points for inputs and outputs are V_{IT} ($0.5 V$) and V_{OT} ($0.5 V_{DD}$). Input rise and fall times ($10\% \leftrightarrow 90\%$) are <5 ns.

Note: V_{IT} - V_{INPUT} Test
 V_{OT} - V_{OUTPUT} Test
 V_{IHT} - V_{INPUT} HIGH Test
 V_{ILT} - V_{INPUT} LOW Test

FIGURE 7: AC INPUT/OUTPUT REFERENCE WAVEFORMS

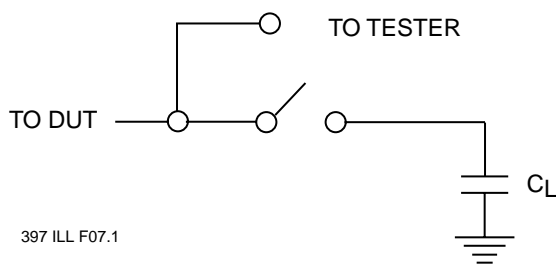


FIGURE 8: A TEST LOAD EXAMPLE



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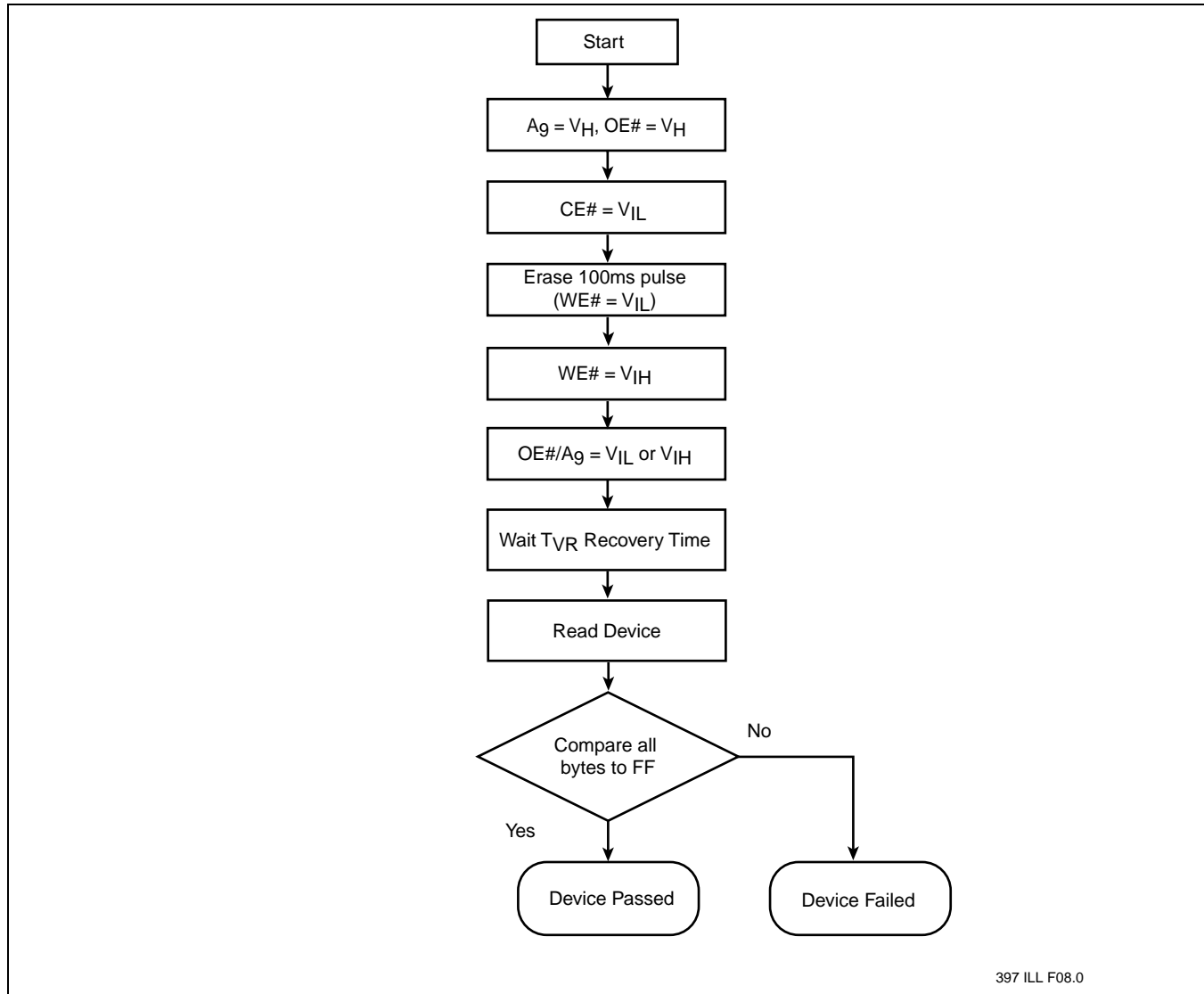


FIGURE 9: CHIP-ERASE ALGORITHM



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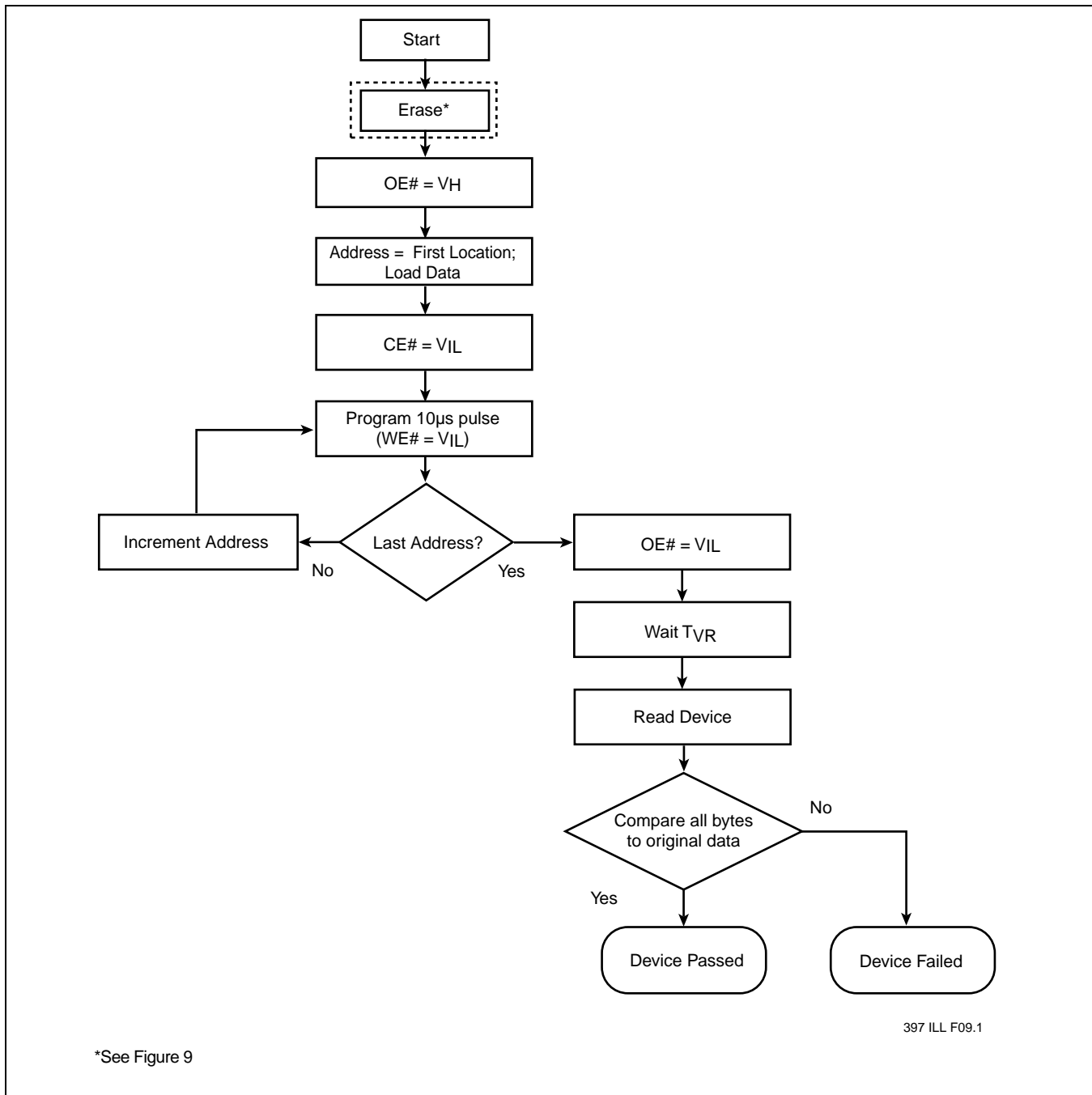


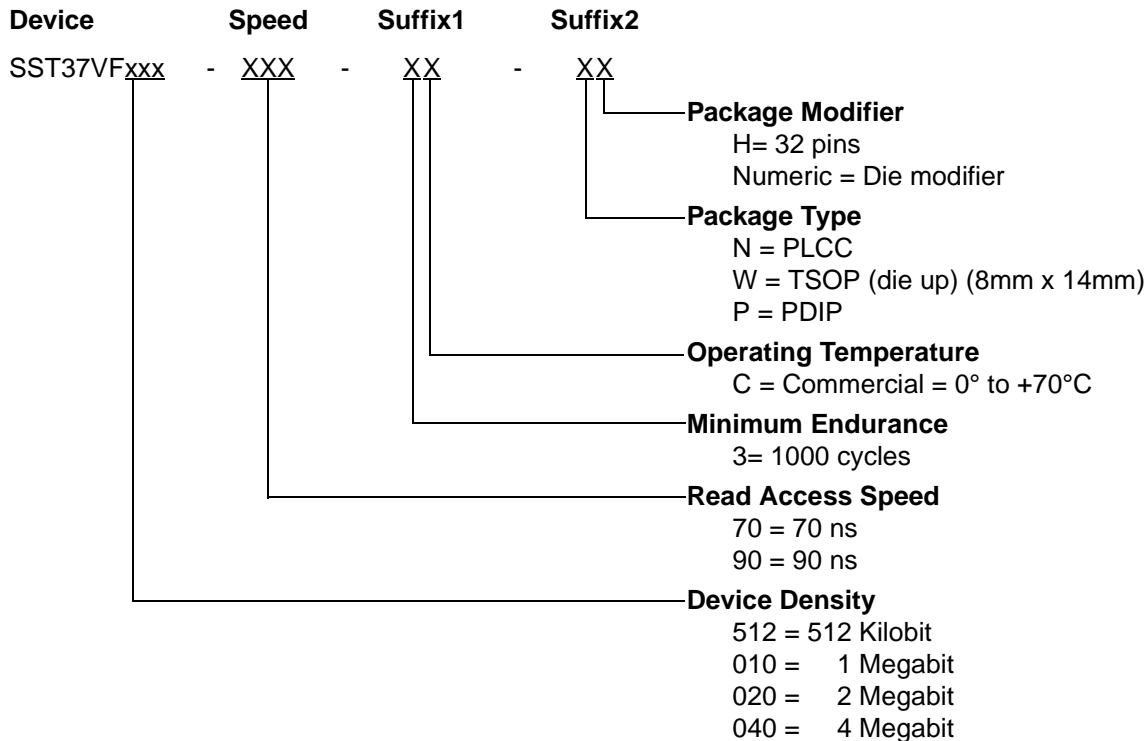
FIGURE 10: BYTE-PROGRAM ALGORITHM



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SST37VF512 Valid combinations

SST37VF512-70-3C-NH SST37VF512-70-3C-WH
 SST37VF512-90-3C-NH SST37VF512-90-3C-WH SST37VF512-90-3C-PH

SST37VF010 Valid combinations

SST37VF010-70-3C-NH SST37VF010-70-3C-WH
 SST37VF010-90-3C-NH SST37VF010-90-3C-WH SST37VF010-90-3C-PH

SST37VF020 Valid combinations

SST37VF020-70-3C-NH SST37VF020-70-3C-WH
 SST37VF020-90-3C-NH SST37VF020-90-3C-WH SST37VF020-90-3C-PH

SST37VF040 Valid combinations

SST37VF040-70-3C-NH SST37VF040-70-3C-WH
 SST37VF040-90-3C-NH SST37VF040-90-3C-WH SST37VF040-90-3C-PH

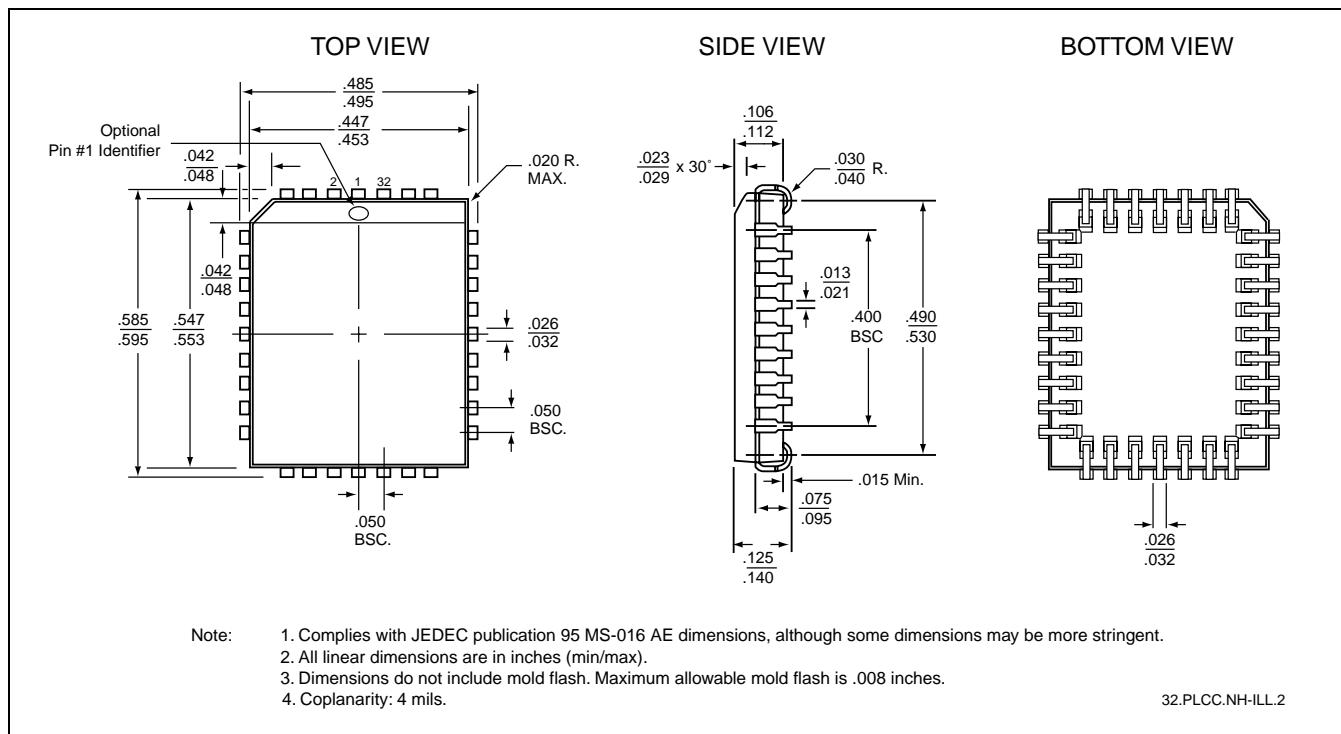
Example: Valid combinations are those products in mass production or will be in mass production. Consult your SST sales representative to confirm availability of valid combinations and to determine availability of new combinations.



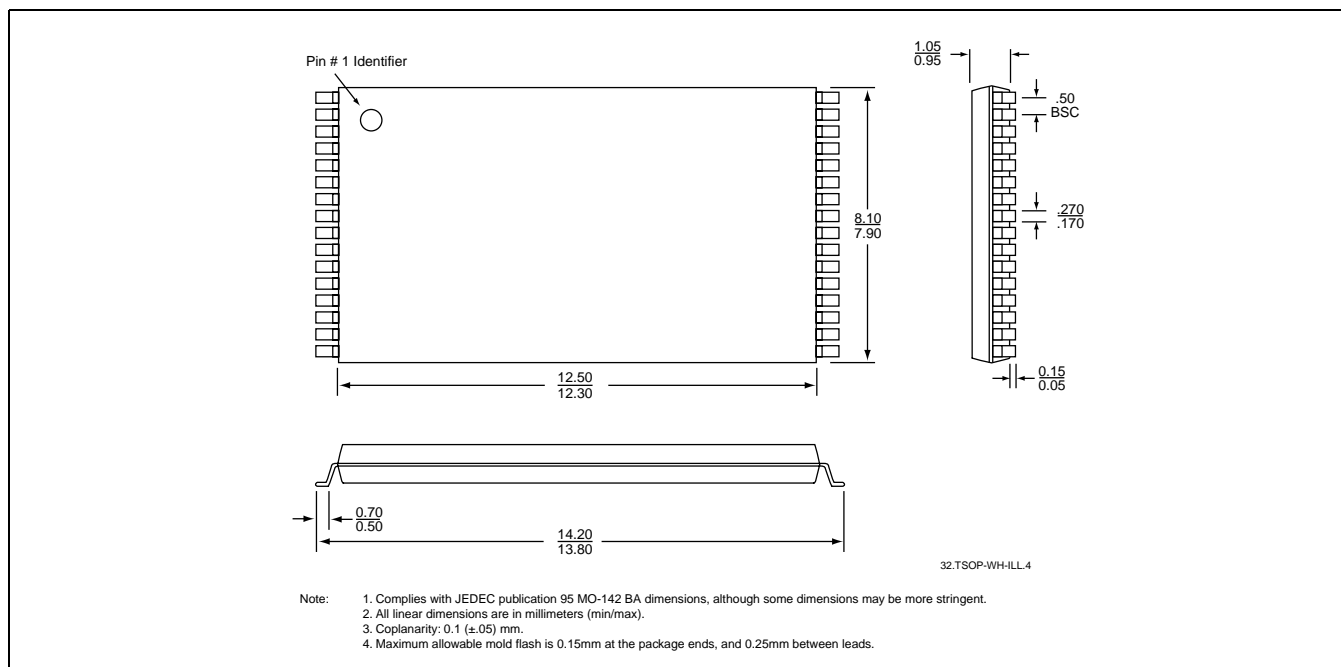
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PACKAGING DIAGRAMS



**32-PIN PLASTIC LEAD CHIP CARRIER (PLCC)
SST PACKAGE CODE: NH**



**32-PIN THIN SMALL OUTLINE PACKAGE (TSOP) 8MM X 14MM
SST PACKAGE CODE: WH**

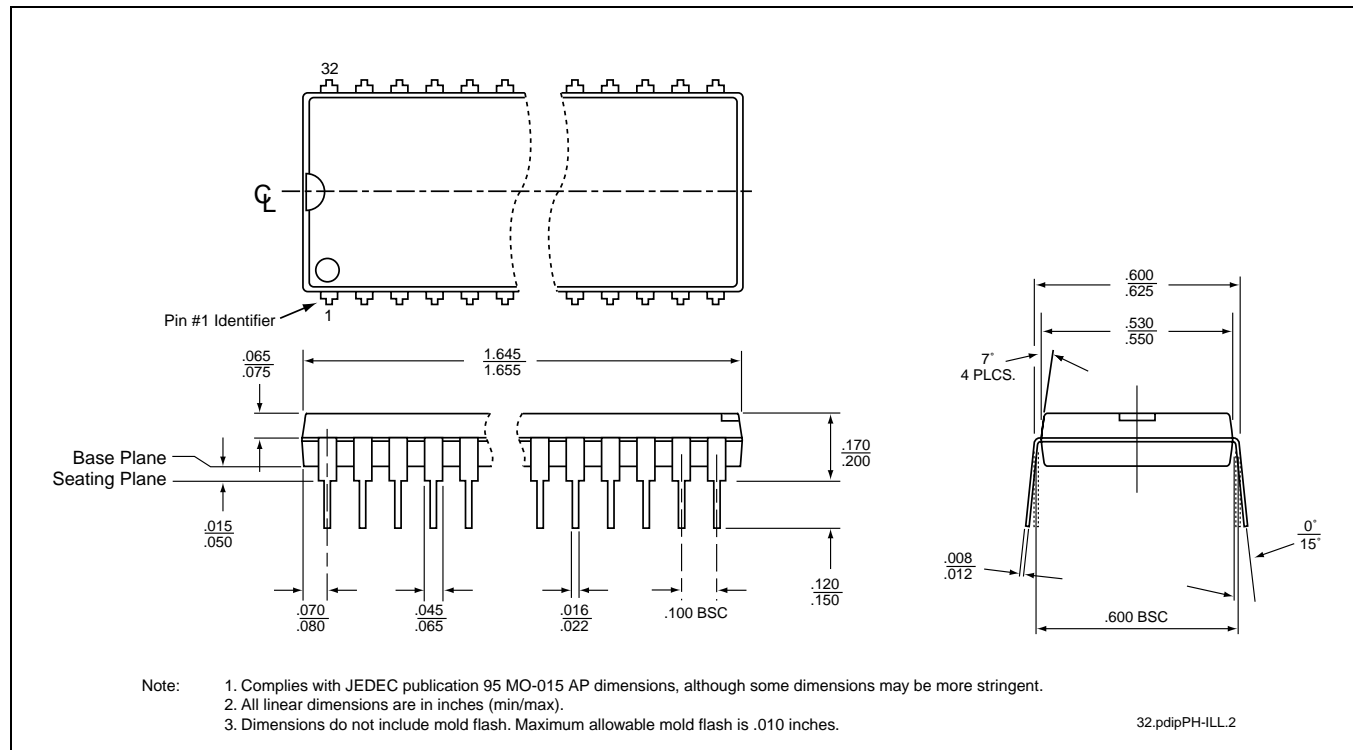
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32-PIN PLASTIC DUAL-IN-LINE PACKAGE (PDIP)

SST PACKAGE CODE: PH



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