REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add device types 04, 05, and 06. Editorial changes throughout.	96-01-17	Monica L. Poelking
B	Add device types 07, 08, and 09. Update boilerplate. Editorial changes throughout. - tvn	99-04-12	Monica L. Poelking

REV	B	B	B	B	B	B	B													
SHEET	35	36	37	38	39	40	41													
REV	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34

REV STATUS OF SHEETS																
REV	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14		

PMIC N/A

PREPARED BY
Thomas M. Hess

CHECKED BY
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APPROVED BY
Monica L. Poelking

DRAWING APPROVAL DATE
95-03-28

REVISION LEVEL
B

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43216

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

MICROCIRCUIT, DIGITAL, SERIAL MICROCODED MULTI-MODE INTELLIGENT TERMINAL, SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-94758**

SHEET 1 OF 41

DSCC FORM 2233
APR 97

5962-E114-99

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:

5962	-	94758	01	Q	X	X
Federal stock class designator		RHA designator (see 1.2.1)	Device type (see 1.2.2)	Device class designator (see 1.2.3)	Case outline (see 1.2.4)	Lead finish (see 1.2.5)

Drawing number

1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	69151XT15	Serial microcoded monolithic multi-mode intelligent terminal with +5 V/-15 V operation
02	69151XT5	Serial microcoded monolithic multi-mode intelligent terminal with +5 V operation
03	69151XT12	Serial microcoded monolithic multi-mode intelligent terminal with +5 V/-12 V operation
04	69151XTE15	Enhanced serial microcoded monolithic multi-mode intelligent terminal with +5 V/-15V operation
05	69151XTE5	Enhanced serial microcoded monolithic multi-mode intelligent terminal with +5 V operation
06	69151XTE12	Enhanced serial microcoded monolithic multi-mode intelligent terminal with +5 V/-12V operation
07	69151XTE15	Enhanced serial microcoded monolithic multi-mode intelligent terminal with +5 V/-15V operation
08	69151XTE5	Enhanced serial microcoded monolithic multi-mode intelligent terminal with +5 V operation
09	69151XTE12	Enhanced serial microcoded monolithic multi-mode intelligent terminal with +5 V/-12V operation

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	139	Pin grid array
Y	See figure 1	140	Quad flat package

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/

Storage temperature range (T_{STG}) ..... -65 C to +150 C
Operating case temperature range (T_C) ..... -55 C to +125 C
Transceiver supply voltage (V_{EE}):
  Device types 01, 03, 04, 06, 07, 09 ..... -22 V dc
Transceiver supply voltage range (V_{CC}):
  Device types 02, 05, 08 ..... -0.3 V dc to +7.0 V dc
Logic supply voltage range (V_{DD}) ..... -0.3 V dc to +7.0 V dc
Input voltage range (receiver) (V_{DR}):
  Device types 01, 03, 04, 06, 07, 09 ..... 42 $V_{P,L-L}$
  Device types 02, 05, 08 ..... 10 $V_{P,L-L}$
Maximum power dissipation (P_D) ..... 5 W
Logic voltage on any pin range ($V_{I/O}$) ..... -0.3 V dc to V_{DD} + 0.3 V dc
Logic latch-up immunity (I_{LU}) ..... 150 mA
Logic input current (I_I) ..... 10 mA
Peak output current (transmitter) (I_O):
  Device types 01, 03, 04, 06, 07, 09 ..... 190 mA
  Device types 02, 05, 08 ..... 1000 mA
Maximum junction temperature (T_J):
  Device types 01, 03, 04, 06, 07, 09 ..... +150 C
  Device types 02, 05, 08 ..... +135 C
Receiver common mode input voltage range (V_{IC}):
  Device types 01, 03, 04, 06, 07, 09 ..... -11 V dc to +11 V dc
  Device types 02, 05, 08 ..... -5 V dc to +5 V dc
Lead temperature (soldering, 5 seconds) ..... +300 C
Thermal resistance junction-to-case ($_{JC}$): 2/
  Cases X and Y ..... 7 C/W

1/ Stress outside the listed absolute maximum rating may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond limits indicated in the opertional sections of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2/ Mounting in accordance with MIL-STD-883, method 1012.

1.4 Recommended operating conditions.

Transceiver supply voltage range (V_{CC}):	
Device types 01, 03, 04, 06, 07, 09	+4.75 V dc to +5.5 V dc
Device types 02, 05, 08	+4.5 V dc to +5.5 V dc
Logic supply voltage range (V_{DD})	+4.5 V dc to +5.5 V dc
Transceiver supply voltage range (V_{EE}):	
Device types 01, 04, 07	-15 V dc 5%
Device types 03, 06, 09	-12 V dc 5%
Receiver differential voltage (V_{DR}):	
Device types 01, 03, 04, 06, 07, 09	40 V_{P-P}
Device types 02, 05, 08	8.0 V_{P-P}
Logic dc input voltage range (V_{IN})	0 V dc to V_{DD}
Receiver common mode input voltage (V_{IC}):	
Device types 01, 03, 04, 06, 07, 09	10 V dc
Device types 02, 05, 08	5.0 V dc
Driver peak output current (I_O):	
Device types 01, 03, 04, 06, 07, 09	180 mA
Device types 02, 05, 08	700 mA
Serial data rate range (S_D)	0 to 1 MHz
Clock duty cycle (D_C)	50 5%
Case operating temperature range (T_C)	-55 C to +125 C
Operating frequency (F_{IN})	24 MHz 0.01%

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	95.12 percent

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Interface Standard For Microcircuit Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
MIL-HDBK-780 - Standard Microcircuit Drawings.
MIL-HDBK-1553 - Multiplex Application Handbook.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DOD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation.

INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS (IEEE)

IEEE Standard 1149.1 - IEEE Standard Test Access Port and Boundary Scan Architecture.

(Applications for copies shouldbe addressed to the Institute of Electrical and Electronics Engineers, 445 Hoes Lane, Piscataway, NJ 08854-4150.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents may also be available in or through libraries or other informational sevices.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 and figure 1 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Block diagram. The block diagram shall be as specified on figure 3.

3.2.4 Boundary scan instruction codes. The boundary scan instruction codes shall be as specified on figure 4.

3.2.5 Timing waveforms. The timing waveforms shall be as specified on figure 5.

3.2.6 Radiation exposure connections. The radiation exposure connecttions shall be as specified when available.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number H (see MIL-PRF-38535, appendix A).

3.11 IEEE 1149.1 compliance. Theses devices shall be compliant to IEEE 1149.1.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) T_A = +125 C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

TABLE I. Electrical performance characteristics.

Test	Symbol	Test conditions 1/ -55 C T_C +125 C 4.5 V V_{DD} 5.5 V unless otherwise specified		Device type	Group A subgroups	Limits		Unit
						Min	Max	
Low level input voltage	V_{IL1}			All	1, 2, 3		0.8	V
Low level input voltage, TCK only	V_{IL2}			01, 02 03, 04 05, 06	1, 2, 3		0.8	
				07, 08 09	1, 2, 3		0.7	
High level input voltage	V_{IH}			All	1, 2, 3	2.2		V
Low level input voltage 2/	V_{ILC}			All	1, 2, 3		0.3 V_{DD}	V
High level intput voltage 2/	V_{IHC}			All	1, 2, 3	0.7 V_{DD}		V
Low level output voltage	V_{OL}	I_{OL} = 4.0 mA		All	1, 2, 3		0.4	V
		I_{OL} = 1.0 A 3/					0.05	
High level output voltage	V_{OH}	I_{OH} = 4.0 mA		All	1, 2, 3	2.4		V
		I_{OH} = 1.0 A 3/				V_{DD}-0.05		
Input leakage current	I_{IN}	TTL inputs	V_{IN} = V_{DD} or V_{SS}	All	1, 2, 3	-10	+10	A
		Inputs with pull-up resistors	V_{IN} = V_{DD}	All	1, 2, 3	-10	+10	
			V_{IN} = V_{SS}	01, 02 03, 04 05, 06		-900	-150	
				07, 08 09		-167	-27	
Three-state output leakage current, TTL loaded outputs, single-drive buffer	I_{OZ}	V_O = V_{DD} or V_{SS}		All	1, 2, 3	-10	+10	A
Short-circuit output current, TTL outputs, single-drive buffer	I_{OS} 4/ 5/	V_{DD} = 5.5 V, V_O = 0 V V_{DD} = 5.5 V, V_O = V_{DD}		All	1, 2, 3	-100	+100	mA
Input capacitance	C_{IN}	f = 1 MHz at 0 V See 4.4.1c		All	4		45	pF
Output capacitance	C_{OUT}			All	4		45	
Bidirectional capacitance 6/	C_{IO}			All	4		45	
Quiescent current 7/	I_{DDQ}	f = 0 MHz		01, 02 03	1, 2, 3		10	mA
				04, 05 06, 07 08, 09	1, 2, 3		15	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 1/ -55 C T_C +125 C 4.5 V V_{DD} 5.5 V unless otherwise specified		Device type	Group A subgroups	Limits		Unit
						Min	Max	
Standby operating current	I_{DDS}	f = 24 MHz		01, 02 03, 04 05, 06	1, 2, 3		80	mA
				07, 08 09	1, 2, 3		40	
V_{CC} supply current	I_{CC}	V_{EE} = -12 V V_{CC} = 5 V	0% duty cycle (non-transmitting)	03, 06 09	1, 2, 3		140	mA
			50% duty cycle (f = 1 MHz) 8/				140	
			100% duty cycle (f = 1 MHz) 8/				140	
		V_{EE} = -15 V V_{CC} = 5 V V_{CCA} = 5 V to 15 V	0% duty cycle (non-transmitting)	01, 04 07			140	
			50% duty cycle (f = 1 MHz) 8/				140	
			100% duty cycle (f = 1 MHz) 8/				140	
		V_{CC} = 5 V	0% duty cycle (non-transmitting)	02, 05	1, 2, 3		110	
				08			55	
			25% duty cycle 8/	02, 05			355	
				08			250	
			50% duty cycle (f = 1 MHz) 8/	02, 05			555	
				08			410	
			87.5% duty cycle (f = 1 MHz) 8/	02, 05			855	
				08			650	
			100% duty cycle (f = 1 MHz) 9/	02, 05			855	
				08			855	
I_{EE} supply current	I_{EE}	V_{EE} = -12 V V_{CC} = 5 V	0% duty cycle (non-transmitting)	03, 06 09	1, 2, 3		80	mA
			50% duty cycle (f = 1 MHz) 8/				180	
			100% duty cycle (f = 1 MHz) 8/				270	
		V_{EE} = -15 V V_{CC} = 5 V	0% duty cycle (non-transmitting)	01, 04 07			80	
			50% duty cycle (f = 1 MHz) 8/				180	
			100% duty cycle (f = 1 MHz) 8/				270	
Functional tests		See 4.4.1b		All	7, 8			

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 1/ -55 C T_C +125 C 4.5 V V_{DD} 5.5 V unless otherwise specified	Device Type	Group A subgroups	Limits		Unit
					Min	Max	
Non-multiplexed memory/register write (8-bit) 10/ 11/							
Address setup time 3/	t_{AS}	See figure 5	All	9, 10, 11	5		ns
Data setup time 3/	t_{DS}		01, 02, 03 04, 05, 06	9, 10, 11		0	
			07, 08 09	9, 10, 11		20	
Write pulse width (non-contented) 3/	t_{WP1}		All	9, 10, 11	230 12/		
Write pulse width (contented) 3/	t_{WP2}		All	9, 10, 11	1700 12/ 13/		
Address hold time 3/	t_{AH}		All	9, 10, 11	0		
Data hold time 3/	t_{DH}		01, 02, 03 04, 05, 06	9, 10, 11	5		
			07, 08 09	9, 10, 11	0		
$\overline{RDY}$ low time (non-contented) 14/	t_{RDYL1}		All	9, 10, 11		245	
$\overline{RDY}$ low time (contented) 3/	t_{RDYL2}		All	9, 10, 11		1700 13/	
$\overline{RDY}$ high time 3/	t_{RDYH}		All	9, 10, 11	0	25	
$\overline{RDY}$ low Z 3/	t_{RDYX}		All	9, 10, 11	3		
$\overline{RDY}$ high Z 3/	t_{RDYZ}		All	9, 10, 11		33	
Minimum cycle time 3/	t_{CYC}		All	9, 10, 11	20		
Non-multiplexed memory/register read (8-bit) 15/ 16/							
Address setup time 3/	t_{AS}	See figure 5	All	9, 10, 11	5		ns
Data low Z 3/	t_{QX}		All	9, 10, 11	0	30	
Address hold time 3/	t_{AH}		All	9, 10, 11	0		
Data valid 3/	t_{QV}		All	9, 10, 11	12		
Data high Z 3/	t_{QZ}		All	9, 10, 11	0	32	
$\overline{RDY}$ low time (non-contented) 3/	t_{RDYL1}		All	9, 10, 11		245	
$\overline{RDY}$ low time (contented) 3/	t_{RDYL2}		All	9, 10, 11		1700 13/	
$\overline{RDY}$ high time 3/	t_{RDYH}		All	9, 10, 11	0	25	
$\overline{RDY}$ low Z 3/	t_{RDYX}		All	9, 10, 11	3		
$\overline{RDY}$ high Z 3/	t_{RDYZ}		All	9, 10, 11		33	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 1/ -55 C T_C +125 C 4.5 V V_{DD} 5.5 V unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
Non-multiplexed memory/register write (16-bit) 10/ 11/							
Address setup time 9/	t_{AS}	See figure 5	All	9, 10, 11	5		ns
Data setup time 9/	t_{DS}		All	9, 10, 11		20	
Write pulse width (non-contented) 3/	t_{WP1}		All	9, 10, 11	230 12/		
Write pulse width (contented) 3/	t_{WP2}		All	9, 10, 11	1700 12/ 13/		
Address hold time 9/	t_{AH}		All	9, 10, 11	0		
Data hold time 9/	t_{DH}		All	9, 10, 11	0		
$\overline{RDY}$ low time (non-contented) 14/	t_{RDYL1}		All	9, 10, 11		245	
$\overline{RDY}$ low time (contented) 3/	t_{RDYL2}		All	9, 10, 11		1700 13/	
$\overline{RDY}$ high time 9/	t_{RDYH}		All	9, 10, 11	0	25	
$\overline{RDY}$ low Z 9/	t_{RDYX}		All	9, 10, 11	3		
$\overline{RDY}$ high Z	t_{RDYZ}		All	9, 10, 11		33	
Minimum cycle time 3/	t_{CYC}		All	9, 10, 11	20		
Non-multiplexed memory/register read (16-bit) 15/ 16/							
Address setup time 9/	t_{AS}	See figure 5	All	9, 10, 11	5		ns
Data low Z 9/	t_{QX}		All	9, 10, 11	0	30	
Address hold time 9/	t_{AH}		All	9, 10, 11	0		
Data valid 9/	t_{QV}		All	9, 10, 11	20		
Data high Z 9/	t_{QZ}		All	9, 10, 11	0	32	
$\overline{RDY}$ low time (non-contented) 14/	t_{RDYL1}		All	9, 10, 11		245	
$\overline{RDY}$ low time (contented) 3/	t_{RDYL2}		All	9, 10, 11		1700 13/	
$\overline{RDY}$ high time 9/	t_{RDYH}		All	9, 10, 11	0	25	
$\overline{RDY}$ low Z 9/	t_{RDYX}		All	9, 10, 11	3		
$\overline{RDY}$ high Z	t_{RDYZ}		All	9, 10, 11		33	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 1/ -55 C T_C +125 C 4.5 V V_{DD} 5.5 V unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
Multiplexed memory/register write (8-bit) 10/ 11/							
Address setup time 3/	t_{AS}	See figure 5	All	9, 10, 11	0		ns
ALE pulse width 3/	t_{AHAL}		All	9, 10, 11	20		
Data setup time 9/	t_{DS}		01, 02, 03 04, 05, 06	9, 10, 11		0	
			07, 08, 09	9, 10, 11		20	
Write pulse width (non-contented) 3/	t_{WP1}		All	9, 10, 11	230 12/		
Write pulse width (contented) 3/	t_{WP2}		All	9, 10, 11	1700 12/ 13/		
Address hold time 9/	t_{AH}		All	9, 10, 11	5		
Data hold time 9/	t_{DH}		01, 02, 03 04, 05, 06	9, 10, 11	5		
			07, 08, 09	9, 10, 11	0		
$\overline{RDY}$ low time (non-contented) 9/	t_{RDYL1}		All	9, 10, 11		245	
$\overline{RDY}$ low time (contented) 3/	t_{RDYL2}		All	9, 10, 11		1700 13/	
$\overline{RDY}$ high time 3/	t_{RDYH}		All	9, 10, 11	0	25	
$\overline{RDY}$ low Z 3/	t_{RDYX}		All	9, 10, 11	3		
$\overline{RDY}$ high Z 3/	t_{RDYZ}		All	9, 10, 11		33	
Address latch setup time 9/	t_{ALS}		01, 02, 03 04, 05, 06	9, 10, 11	22		
			07, 08, 09	9, 10, 11	5		
Minimum cycle time 3/	t_{CYC}		All	9, 10, 11	20		
Multiplexed memory/register read (8-bit) 15/ 16/							
Address setup time 3/	t_{AS}	See figure 5	All	9, 10, 11	0		ns
ALE pulse width 3/	t_{AHAL}		All	9, 10, 11	20		
Data low Z 3/	t_{QX}		All	9, 10, 11	0	30	
Address hold time 3/	t_{AH}		All	9, 10, 11	5		
Data valid 3/	t_{QV}		All	9, 10, 11	12		
Data high Z 3/	t_{QZ}		All	9, 10, 11	3	32	
$\overline{RDY}$ low time (non-contented) 3/	t_{RDYL1}		All	9, 10, 11		245	
$\overline{RDY}$ low time (contented) 3/	t_{RDYL2}		All	9, 10, 11		1700 13/	
$\overline{RDY}$ high time 3/	t_{RDYH}		All	9, 10, 11	0	25	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 1/ -55 C T_C +125 C 4.5 V V_{DD} 5.5 V unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
Multiplexed memory/register read (8-bit) - Continued 15/ 16/							
$\overline{RDY}$ low Z 3/	t_{RDYX}	See figure 5	All	9, 10, 11	3		ns
$\overline{RDY}$ high Z 3/	t_{RDYZ}		All	9, 10, 11		33	
Address latch setup time 3/	t_{ALS}		01, 02, 03 04, 05, 06	9, 10, 11	22		
			07, 08, 09	9, 10, 11	5		
Multiplexed memory/register write (16-bit) 10/ 11/							
Address setup time 3/	t_{AS}	See figure 5	All	9, 10, 11	0		ns
ALE pulse width 3/	t_{AHAL}		All	9, 10, 11	20		
Data setup time 3/	t_{DS}		All	9, 10, 11		20	
Write pulse width (non-contented) 3/	t_{WP1}		All	9, 10, 11	230 12/		
Write pulse width (contented) 3/	t_{WP2}		All	9, 10, 11	1700 12/ 13/		
Address hold time 3/	t_{AH}		All	9, 10, 11	5		
Data hold time 3/	t_{DH}		01, 02, 03 04, 05, 06	9, 10, 11	5		
			07, 08, 09	9, 10, 11	0		
$\overline{RDY}$ low time (non-contented) 3/	t_{RDYL1}		All	9, 10, 11		245	
$\overline{RDY}$ low time (contented) 3/	t_{RDYL2}		All	9, 10, 11		1700 13/	
$\overline{RDY}$ high time 3/	t_{RDYH}		All	9, 10, 11	0	25	
$\overline{RDY}$ low Z 3/	t_{RDYX}		All	9, 10, 11	3		
$\overline{RDY}$ high Z 3/	t_{RDYZ}		All	9, 10, 11		33	
Address latch setup time 3/	t_{ALS}		01, 02, 03 04, 05, 06	9, 10, 11	22		
			07, 08, 09	9, 10, 11	5		
Minimum cycle time 3/	t_{CYC}		All	9, 10, 11	20		
Multiplexed memory/register read (16-bit) 15/ 16/							
Address setup time 3/	t_{AS}	See figure 5	All	9, 10, 11	0		ns
ALE pulse width 3/	t_{AHAL}		All	9, 10, 11	20		
Data low Z 3/	t_{QX}		All	9, 10, 11	0	30	
Address hold time 3/	t_{AH}		All	9, 10, 11	5		
Data valid 3/	t_{QV}		All	9, 10, 11	20		
Data high Z 3/	t_{QZ}		All	9, 10, 11	3	32	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 1/ -55 C T_C +125 C 4.5 V V_{DD} 5.5 V unless otherwise specified		Device type	Group A subgroups	Limits		Unit
						Min	Max	
Multiplexed memory/register read (16-bit) - Continued 15/ 16/								
$\overline{RDY}$ low time (non-contented) 3/	t_{RDYL1}	See figure 5		All	9, 10, 11		245	ns
$\overline{RDY}$ low time (contented) 3/	t_{RDYL2}			All	9, 10, 11		1700 13/	
$\overline{RDY}$ high time 3/	t_{RDYH}			All	9, 10, 11	0	25	
$\overline{RDY}$ low Z 3/	t_{RDYX}			All	9, 10, 11	3		
$\overline{RDY}$ high Z 3/	t_{RDYZ}			All	9, 10, 11		33	
Address latch setup time 3/	t_{ALS}			01, 02, 03 04, 05, 06	9, 10, 11	22		
				07, 08, 09	9, 10, 11	5		
Auto-initialization read cycle								
Address setup time 9/	t_{AS}	See figure 5		All	9, 10, 11	35		ns
Address hold time 9/	t_{AH}			All	9, 10, 11	35		
Data setup time 3/	t_{DS}			All	9, 10, 11	41		
Data hold time 3/	t_{DH}			All	9, 10, 11	5		
Read pulse width 3/	t_{RP}			All	9, 10, 11	160		
Setup time 3/	t_S			All	9, 10, 11	45		
Maximum cycle time								
Maximum register/ memory time 3/	t_a	See figure 5	Bus controller	All	9, 10, 11		16	s
			Remote terminal	All	9, 10, 11		7	
			Remote terminal with monitor	All	9, 10, 11		7	
			Monitor	All	9, 10, 11		7	
JTAG timing								
TCK frequency		See figure 5		All	9, 10, 11		1	MHz
TCK period	t_a			All	9, 10, 11	1000		ns
TCK high time	t_b			All	9, 10, 11	$1/2t_a$		
TCK low time	t_c			All	9, 10, 11	$1/2t_a$		
TCK rise time	t_d			All	9, 10, 11		5	
TCK fall time	t_e			All	9, 10, 11		5	
TDI, TMS setup time	t_f			All	9, 10, 11	250		
TDI, TMS hold time	t_g			All	9, 10, 11	250		
TDO valid delay	t_h			All	9, 10, 11	250		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 1/ -55 C T_C +125 C 4.5 V V_{DD} 5.5 V unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
Receiver electrical characteristics							
Differential (receiver) input impedance 8/	R_{IZ}	Input f = 1 MHz (no transformer in circuit)	01, 03 04, 06 07, 09	1, 2, 3	15		k
Common mode input voltage 3/	V_{IC}	Direct-coupled stub, input 1.2 V_{PP} , 200 ns rise/fall time 25 ns, f = 1 MHz	01, 03 04, 06 07, 09	1, 2, 3	-10	+10	V
			02, 05 08	1, 2, 3	-5	+5	
Input threshold voltage (no response)	V_{TH1}	Transformer-coupled stub, input at f = 1 MHz, rise/fall time 200 ns (receiver output 0 1 transition) 3/	All	1, 2, 3		0.20	$V_{PP,L-L}$
		Direct-coupled stub, input at f = 1 MHz, rise/fall time 200 ns (receiver output 0 1 transition)	All	1, 2, 3		0.28	
Input threshold voltage (response)	V_{TH2}	Transformer-coupled stub, input at f = 1 MHz, rise/fall time 200 ns (receiver output 0 1 transition) 3/	All	1, 2, 3	0.86	14.0	$V_{PP,L-L}$
		Direct-coupled stub, input at f = 1 MHz, rise/fall time 200 ns (receiver output 0 1transition)	All	1, 2, 3	1.20	20.0 3/	
Common mode rejection ratio 8/	CMRR		All	1, 2, 3	Pass/ Fail 17/		N/A
Differential input voltage level	V_{IDR}		02	1, 2, 3		8.0	V_{P-P}
Transmitter electrical characteristics							
Output voltage swing	V_O	See figure 5 Transformer-coupled stub, point A, input f = 1 MHz, R_L = 70 3/	All	1, 2, 3	18	27	$V_{PP,L-L}$
		See figure 5 Direct-coupled stub, point A, input f = 1 MHz, R_L = 35	All	1, 2, 3	6.0	9.0	
		See figure 5 Point A, input f = 1 MHz, R_L = 35 3/	All	1, 2, 3	6.0	20	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 1/ -55 C T_C +125 C 4.5 V V_{DD} 5.5 V unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
Transmitter electrical characteristics - Continued							
Output noise voltage differential 8/	V_{NS}	See figure 5 Transformer-coupled stub, point A, input f = DC to 10 MHz, R_L = 70	All	1, 2, 3		14	mV-RMS$_{L-L}$
		See figure 5 Direct-coupled stub, point A, input f = DC to 10 MHz, R_L = 35	All	1, 2, 3		5	
Output symmetry 18/	V_{OS}	Transformer-coupled stub, point A, R_L = 70 , measurement taken 2.5 s after end of transmission 3/	01, 03 04, 05 06, 07 08, 09	1, 2, 3	-250	+250	mV$_{PP,L-L}$
			02	1, 2, 3	-360	+360	
		Direct-coupled stub, point A, R_L = 35 , measurement taken 2.5 s after end of transmission 14/	01, 03 04, 05 06, 07 08, 09	1, 2, 3	-90	+90	
			02	1, 2, 3	-90	+90	
Output voltage distortion (overshoot or ring)	V_{DIS}	See figure 5 Transformer-coupled stub, point A, R_L = 70 3/	01, 03 04, 05 06, 07 08, 09	1, 2, 3	-900	+900	mV$_{peak,L-L}$
			02	1, 2, 3	-2.0	+2.0	V$_{peak,L-L}$
		See figure 5 Direct-coupled stub, point A, R_L = 35 14/	01, 03 04, 05 06, 07 08, 09	1, 2, 3	-300	+300	mV$_{peak,L-L}$
			02	1, 2, 3	-1.0	+1.0	V$_{peak,L-L}$
Terminal input impedance 8/	T_{IZ}	See figure 5 Transformer-coupled stub, point A, input f = 75 kHz to 1 MHz, (power on or power off, non-transmitting, R_L removed from circuit)	All	1, 2, 3	1		k
		See figure 5 Direct-coupled stub, point A, input f = 75 kHz to 1MHz, (power on or power off, non-transmitting, R_L removed from circuit)	All	1, 2, 3	2		
Differential output impedance 8/	T_{OZ}	Input f = 1 MHz (no transformer in circuit)	02	1, 2, 3	10		k

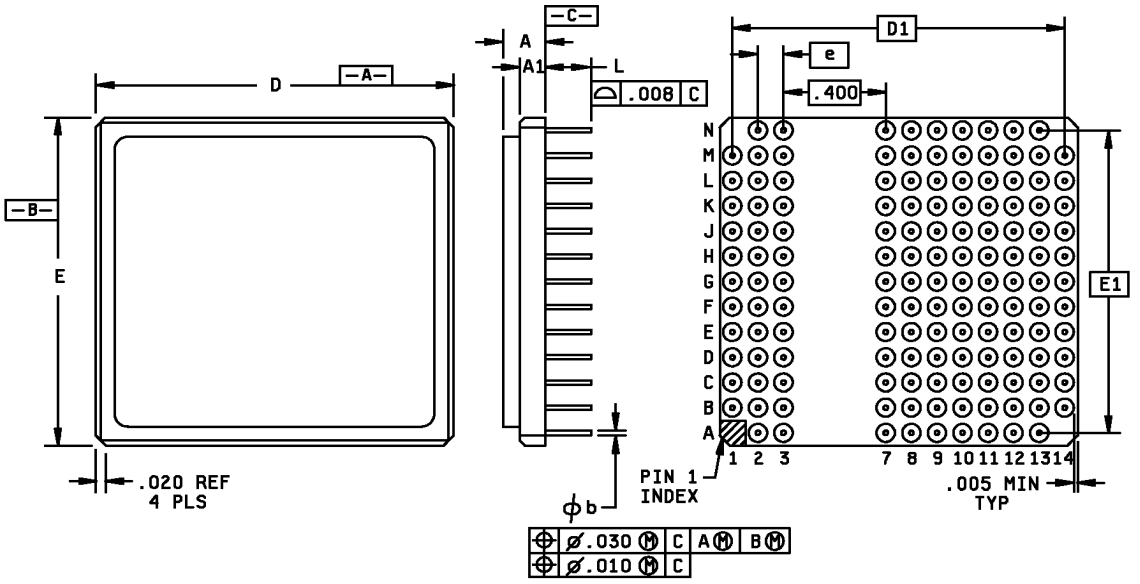
See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 1/ -55 C T_C +125 C 4.5 V V_{DD} 5.5 V unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
AC electrical characteristics							
Transmitter output rise/fall time	t_R, t_F	See figure 5 Input f = 1 MHz 50% duty cycle: direct-coupled, R_L = 35 , output at 10% through 90% points TXOUT, $\overline{\text{TXOUT}}$	All	9, 10, 11	100	300	ns
Zero crossing distortion	t_{RZCD}	See figure 5 Direct-coupled stuff, Input f = 1 MHz, 3 V_{PP} (skew input 150 ns), rise/fall time 200 ns	All	9, 10, 11	-150	+150	ns
Zero crossing stability	t_{TZCS}	See figure 5 Input TXIN and $\overline{\text{TXIN}}$ should create transmitter output zero crossings at 500 ns, 1000 ns, 1500 ns, and 2000 ns. These zero crossings should not deviate more than 25 ns	All	9, 10, 11	-25	+25	ns

1/ All testing to be performed using worst case test conditions unless otherwise specified. GND may not vary from 0 V by more than 50 mV. Unless otherwise specified, V_{CC} = 5.0 V 5% for device type 02; V_{CC} = 5.0 V 10% for device types 05 and 08; V_{CC} = 5.0 V +10%, -5% and V_{EE} = -12.0 V or -15.0 V 5% for device types 01, 03, 04, 06, 07, and 09.
2/ 24 MHz input only.
3/ Guaranteed by design but not tested.
4/ Supplied as a design limit but not guaranteed or tested.
5/ Not more than one output may be shorted at a time for maximum duration of one second.
6/ For all pins except CHA, $\overline{\text{CHA}}$, CHB, and $\overline{\text{CHB}}$.
7/ All inputs tied to V_{DD}.
8/ Guaranteed by characterization but not tested.
9/ For device types 07, 08, and 09, this parameter is guaranteed by characterization, but not tested.
10/ A cycle begins on the latter falling edge of $\overline{\text{CS}}$, $\overline{\text{DS}}$, and $\overline{\text{WR}}$ or R/$\overline{\text{WR}}$.
11/ A cycle ends on the rising edge of either $\overline{\text{CS}}$, $\overline{\text{DS}}$, and $\overline{\text{WR}}$ or R/$\overline{\text{WR}}$.
12/ For applications not using $\overline{\text{RDY}}$ signal.
13/ Non-buffered mode of operation.
14/ Tested on device types 07, 08, and 09 only. Guaranteed by design on device types 01 through 06.
15/ A cycle begins on the latter falling edge of $\overline{\text{CS}}$, $\overline{\text{DS}}$, and $\overline{\text{RD}}$.
16/ A cycle ends on the rising edge of either $\overline{\text{CS}}$, $\overline{\text{DS}}$, and $\overline{\text{RD}}$.
17/ Pass/fail criteria per the test method described in MIL-STD-1553, appendix A, RT validation test plan, section 5.1.2.2, common mode rejection.
18/ Test in accordance with the method described in MIL-STD-1553B output symmetry, section 4.5.2.1.1.4.

Case X



Case X				
Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A		4.191		.165
A1		2.540		.100
b	0.406	0.508	.016	.020
D	35.31	35.81	1.390	1.410
D1	33.02 BSC		1.300 BSC	
E	32.77	33.27	1.290	1.310
E1	30.48 BSC		1.200 BSC	
e	2.54 BSC		.100 BSC	
L	4.368	4.775	.172	.188

NOTE: The US Government preferred system of measurement is the metric SI system. However, this item was originally designed using inch-pound units of measurements. In the event of conflict between the metric and inch-pound units, the inch-pound units shall take precedence.

FIGURE 1. Case outlines.

Case Y

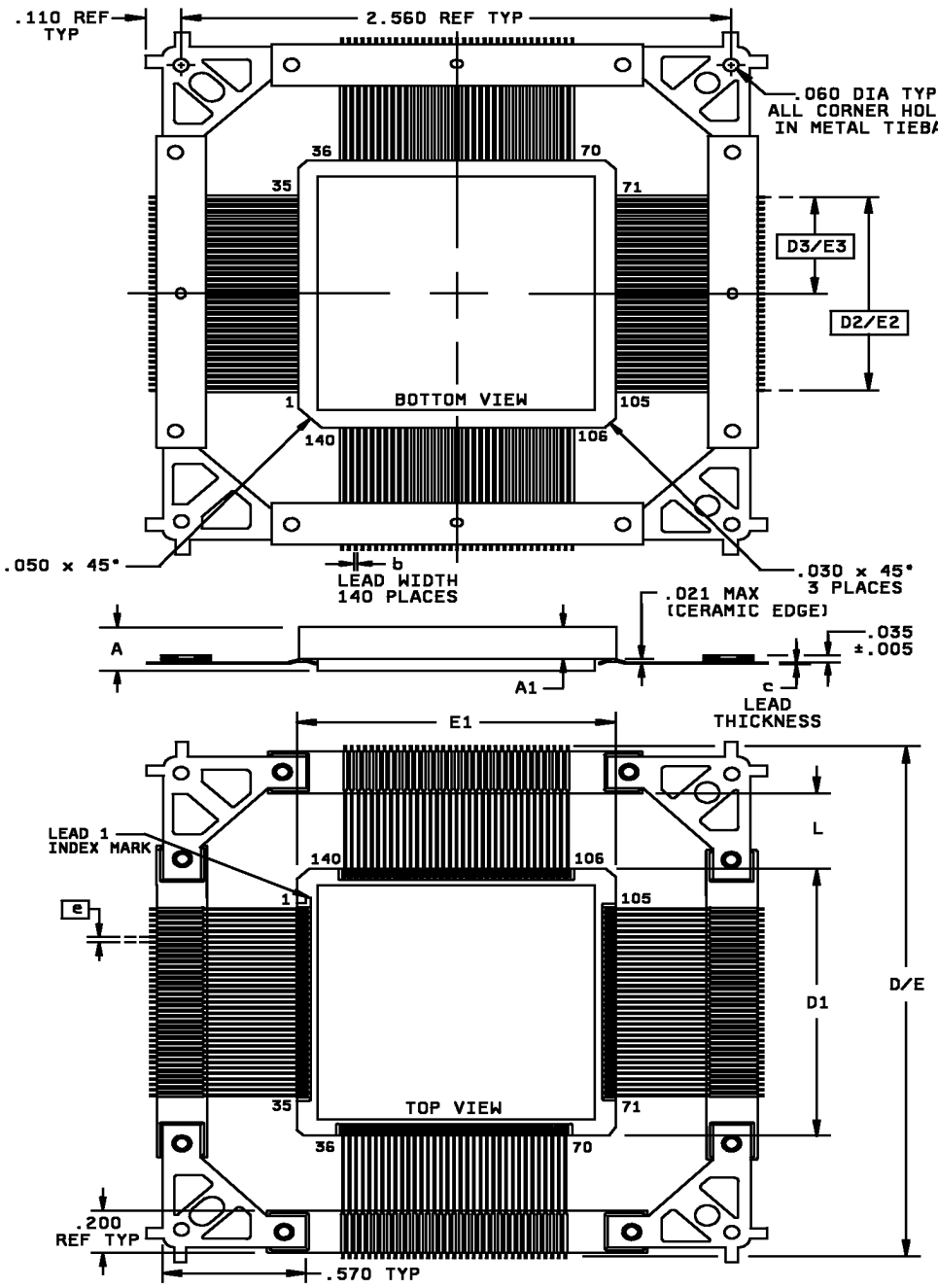


FIGURE 1. Case outlines - Continued.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-94758
		REVISION LEVEL B	SHEET 18

DSCC FORM 2234
APR 97

Case Y				
Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A		3.81		.150
A1		2.54		.100
b	0.1524	0.254	.006	.010
c	0.1270	0.203	.005	.008
D/E		72.90		2.870
D1	36.96	37.72	1.455	1.485
D2/E2	21.59 BSC		.850 BSC	
D3/E3	10.80 BSC		.425 BSC	
E1	34.19	34.90	1.346	1.374
e	0.635 BSC		.025 BSC	
L	9.652		.380	

NOTE: The US Government preferred system of measurement is the metric SI system. However, this item was originally designed using inch-pound units of measurements. In the event of conflict between the metric and inch-pound units, the inch-pound units shall take precedence.

FIGURE 1. Case outlines - Continued.

Device type	All								
Case outline	X								
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
A2	$\overline{CHB}$	C12	MSEL3	F7	$\overline{TERACT}$	H13	A12	L8	ED2
A3	CHB	C13	A2	F8	V_{CC}	H14	V_{SS}	L9 1/	TDIM
A7	$\overline{CHA}$	C14	A0	F9	EA12	J1	MSEL0	L10	DA14
A8	V_{DD}	D1	$\overline{SSYSF}$	F10	EA11	J2	TMSS	L11	DA12
A9	V_{SS}	D2	V_{EE}	F11	A7	J3	MSEL1	L12	DA9
A10	$\overline{CS}$	D3	V_{CC}	F12	A6	J7	EA2	L13	DA8
A11	MSEL2	D7	V_{EE}	F13	A5	J8	$\overline{MRST}$	L14	DA6
A12	$\overline{DS}$	D8	V_{EE}	F14	V_{DD}	J9	EA1	M1	V_{SS}
A13	V_{SS}	D9	$\overline{READY}$	G1	RTPTY	J10	EA0	M2	$\overline{AUTOEN}$
B1	GND	D10	$\overline{BIST}$	G2	RTA1	J11	DA2	M3	$\overline{YF\_INT}$
B2	V_{SS}	D11	EC1	G3	RTA3	J12	DA1	M7	ED6
B3	V_{DD}	D12	MSEL5	G7	V_{DD}	J13	DA0	M8	ED3
B7	CHA	D13	A4	G8	EA4	J14	A15	M9	ED0
B8	V_{SS}	D14	V_{SS}	G9	EA8	K1	V_{DD}	M10 1/	TMSM
B9	GND	E1	GND	G10	EA10	K2	TDIS	M11	DA13
B10	EC2	E2	RTA4	G11	A11	K3	TDOS	M12	DA10
B11	$\overline{ECS}$	E3	GND	G12	A10	K7	R/$\overline{WR}$ or $\overline{WR}$	M13	DA7
B12	EC0	E7	GND	G13	A9	K8	$\overline{RD}$	M14	V_{SS}
B13	MSEL4	E8	V_{CC}	G14	A8	K9	$\overline{MSG\_ACK}$	N2	V_{DD}
B14	V_{DD}	E9	EA5	H1	V_{SS}	K10	ED7	N3	ED5
C1	V_{CC}	E10	EA6	H2	A/$\overline{B}$ STD	K11	DA5	N7	24 MHz
C2	V_{EE}	E11	EA7	H3	$\overline{LOCK}$	K12	DA3	N8	ED4
C3	GND	E12	ALE	H7	V_{SS}	K13	DA4	N9	ED1
C7	GND	E13	A3	H8	EA3	K14	V_{DD}	N10 2/	TDOM
C8	GND	E14	A1	H9	$\overline{YF\_ACK}$	L1	$\overline{MSG\_INT}$	N11	DA15
C9	V_{CC}	F1	V_{DD}	H10	$\overline{RDY}$	L2	TCK	N12	DA11
C10	V_{CC}	F2	RTA0	H11	A14	L3	$\overline{TRST}$	N13	V_{DD}
C11	EA9	F3	RTA2	H12	A13	L7	TCLK		

1/ V_{SS} for device types 07, 08, and 09.
2/ No connection for device types 07, 08, and 09.

FIGURE 2. Terminal connections.

Device type	All								
Case outline	Y								
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	V_{SS}	29	DA4	57 1/	TMSM	85	EA12	113	$\overline{SSYSF}$
2	V_{DD}	30	DA3	58 1/	TDIM	86	V_{EE}	114	$\overline{BIST}$
3	$\overline{YF\_ACK}$	31	DA2	59 2/	TDOM	87	V_{CC}	115	RTA4
4	$\overline{YF\_INT}$	32	DA1	60	V_{DD}	88	GND	116	RTA3
5	$\overline{MSG\_ACK}$	33	DA0	61	ED0	89	GND	117	RTA2
6	$\overline{MSG\_INT}$	34	V_{DD}	62	ED1	90	GND	118	RTA1
7	24 MHz	35	V_{SS}	63	ED2	91	V_{EE}	119	RTA0
8	NC	36	V_{SS}	64	ED3	92	CHA	120	RTPTY
9	V_{DD}	37	V_{DD}	65	ED4	93	$\overline{CHA}$	121	$\overline{LOCK}$
10	$\overline{RD}$	38	A15	66	ED5	94	V_{CC}	122	A/$\overline{B}$ STD
11	R/$\overline{WR}$ or $\overline{WR}$	39	A14	67	ED6	95	GND	123	V_{SS}
12	$\overline{DS}$	40	A13	68	ED7	96	$\overline{ECS}$	124	MSEL5
13	ALE	41	A12	69	V_{DD}	97	EC2	125	MSEL4
14	$\overline{CS}$	42	A11	70	V_{SS}	98	EC1	126	MSEL3
15	$\overline{RDY}$	43	A10	71	V_{SS}	99	EC0	127	MSEL2
16	V_{DD}	44	V_{DD}	72	V_{DD}	100	V_{EE}	128	MSEL1
17	DA15	45	A9	73	EA0	101	V_{CC}	129	MSEL0
18	DA14	46	A8	74	EA1	102	CHB	130	$\overline{MRST}$
19	DA13	47	A7	75	EA2	103	$\overline{CHB}$	131	$\overline{AUTOEN}$
20	DA12	48	A6	76	EA3	104	V_{EE}	132	V_{SS}
21	DA11	49	A5	77	EA4	105	GND	133	$\overline{TRST}$
22	DA10	50	A4	78	EA5	106	GND	134	TDOS
23	DA9	51	A3	79	EA6	107	V_{CC}	135	TDIS
24	DA8	52	A2	80	EA7	108	GND	136	TMSS
25	DA7	53	V_{SS}	81	EA8	109	NC	137	TCK
26	DA6	54	A1	82	EA9	110	$\overline{READY}$	138	TCLK
27	V_{SS}	55	A0	83	EA10	111	$\overline{TERACT}$	139	V_{DD}
28	DA5	56	NC	84	EA11	112	GND	140	V_{SS}

NC = No connection
1/ V_{SS} for device types 07, 08, and 09.
2/ No connection for device types 07, 08, and 09.

FIGURE 2. Terminal connections - Continued.

Device types 01, 02, 03, 04, 05, and 06

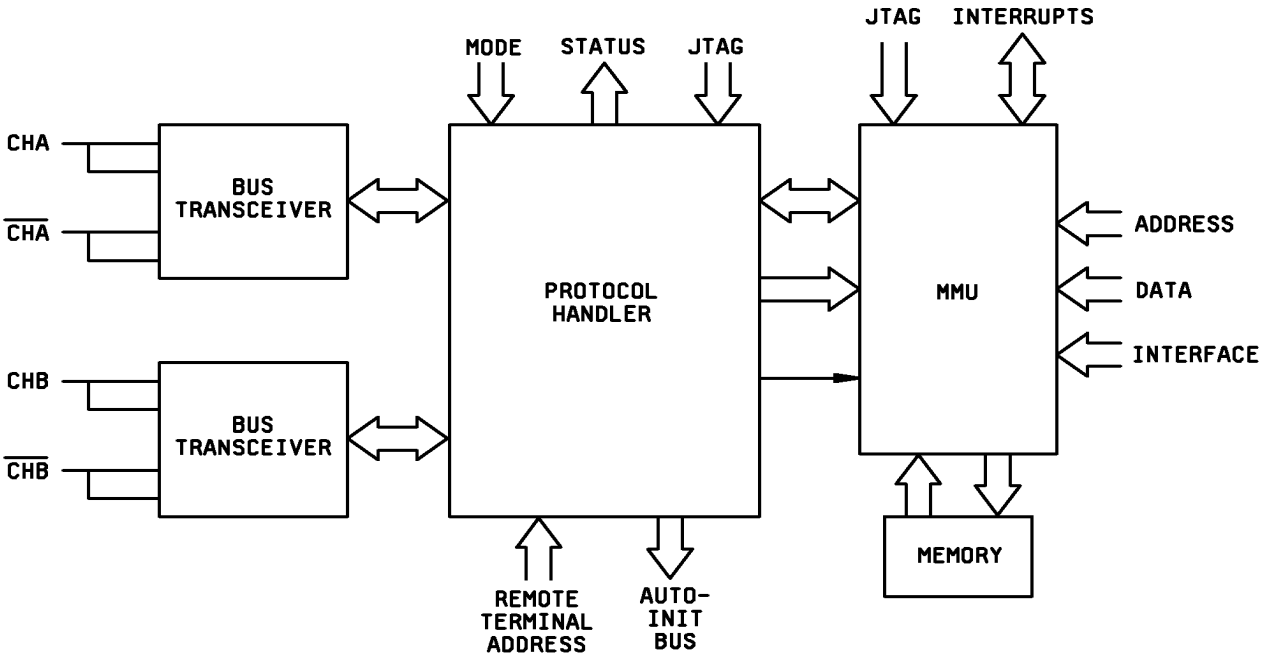


FIGURE 3. Block diagram.

Device types 07, 08, and 09

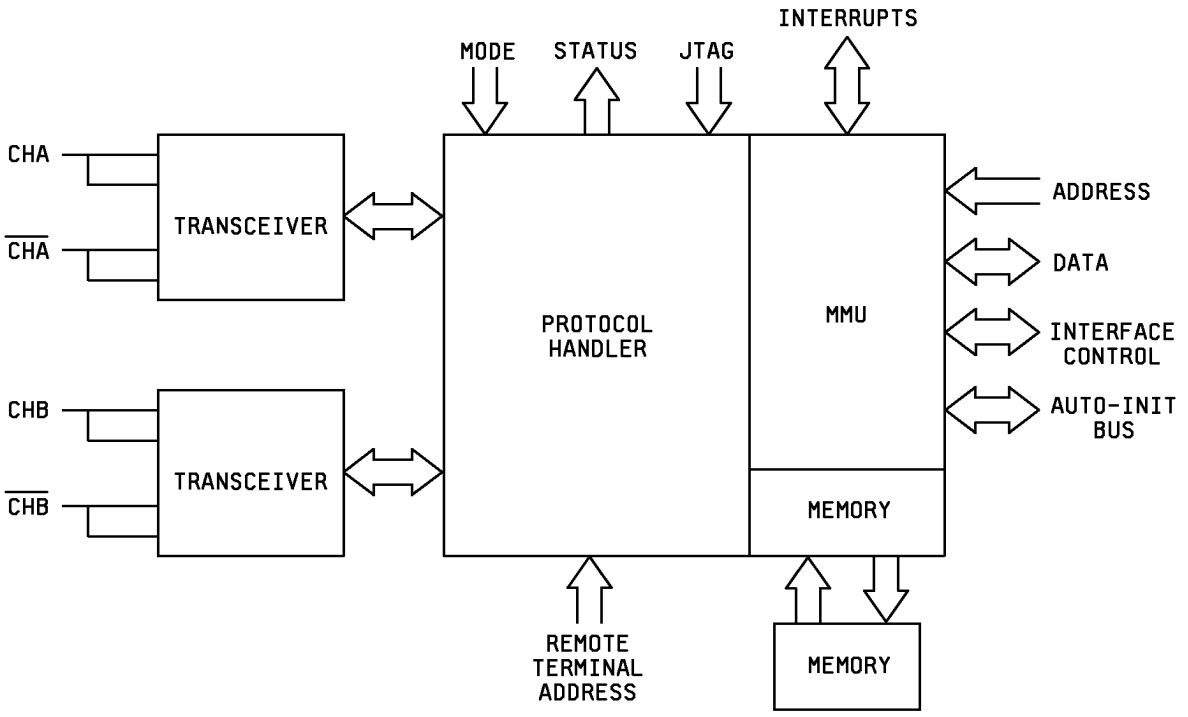
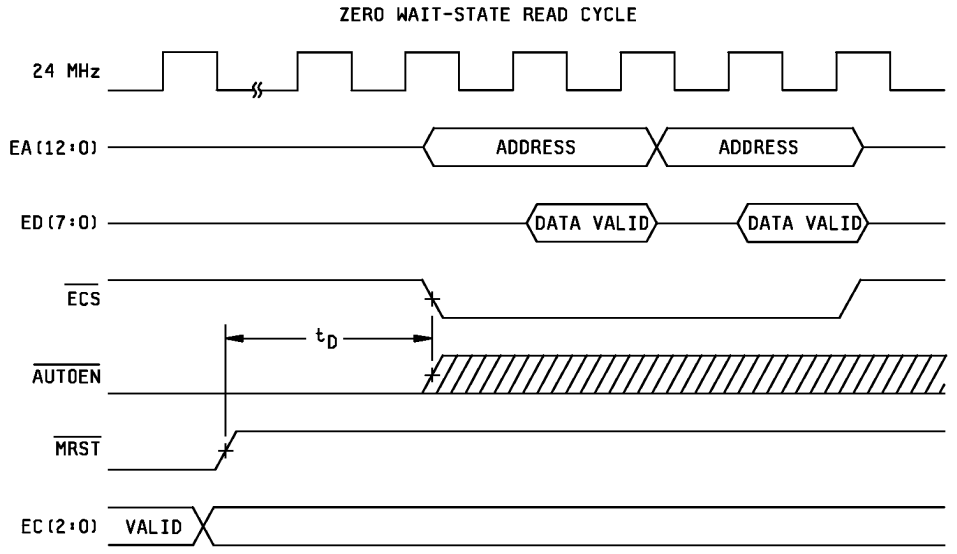


FIGURE 3. Block diagram - Continued.

Device types 01, 02, 03, 04, 05, 06	
Instruction name	Instruction code
BYPASS	1111
SAMPLE/PRELOAD	0010
EXTEST	0000
INTEST	0001
RUNBIST	0111
IDCODE	0100
GL-TRISTATE	0011
INTERNAL-SCAN	0101
PRIVATE	0110
USER-SELECTABLE	1000 1110

Device types 07, 08, 09	
Instruction name	Instruction code
BYPASS	1111
SAMPLE/PRELOAD	0010
EXTEST	0000

FIGURE 4. Boundary scan instruction codes.



NOTE: Two bytes are read on each $\overline{\text{ECS}}$ cycle using only an address transition (AT).

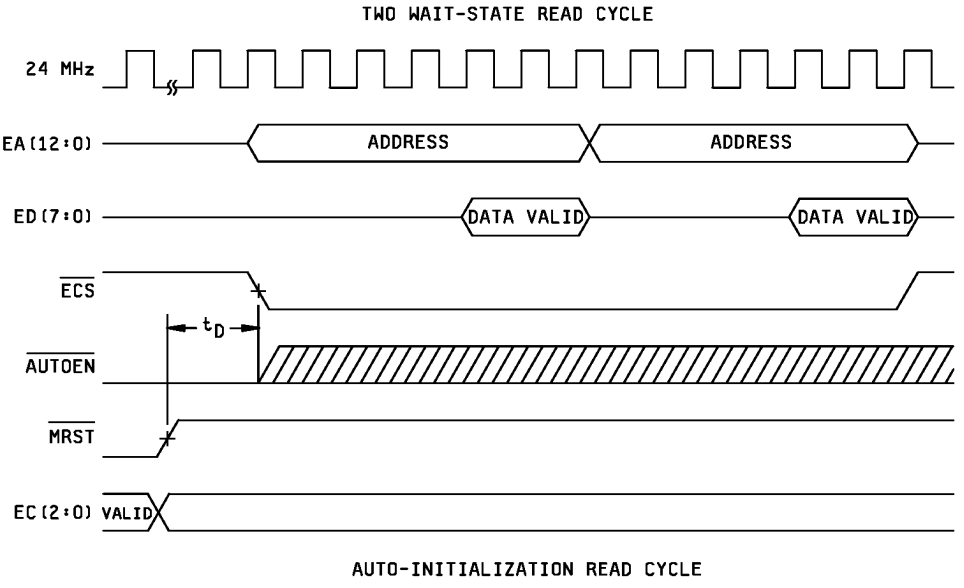
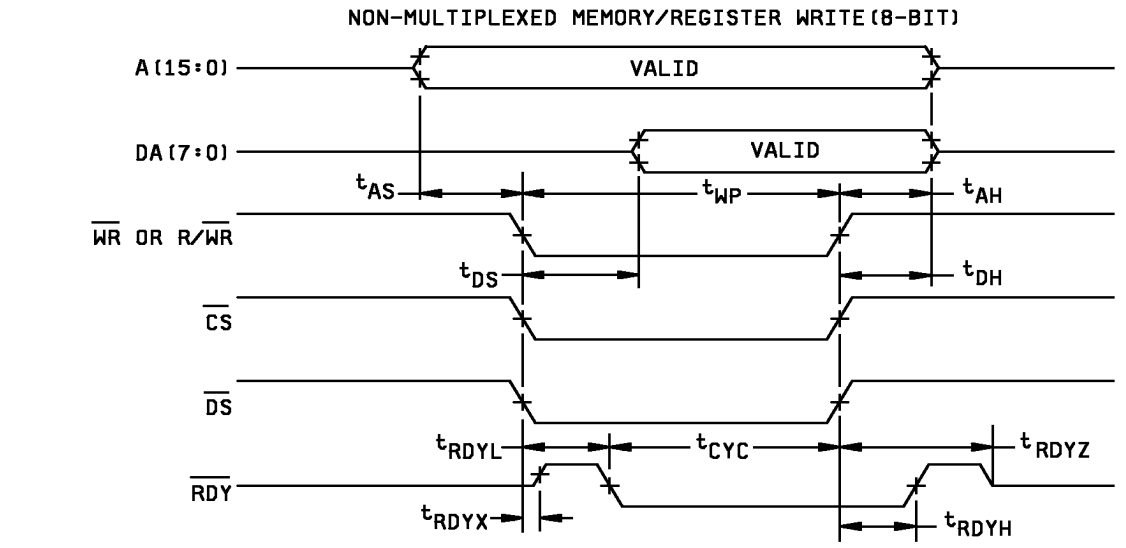


FIGURE 5. Timing waveforms.



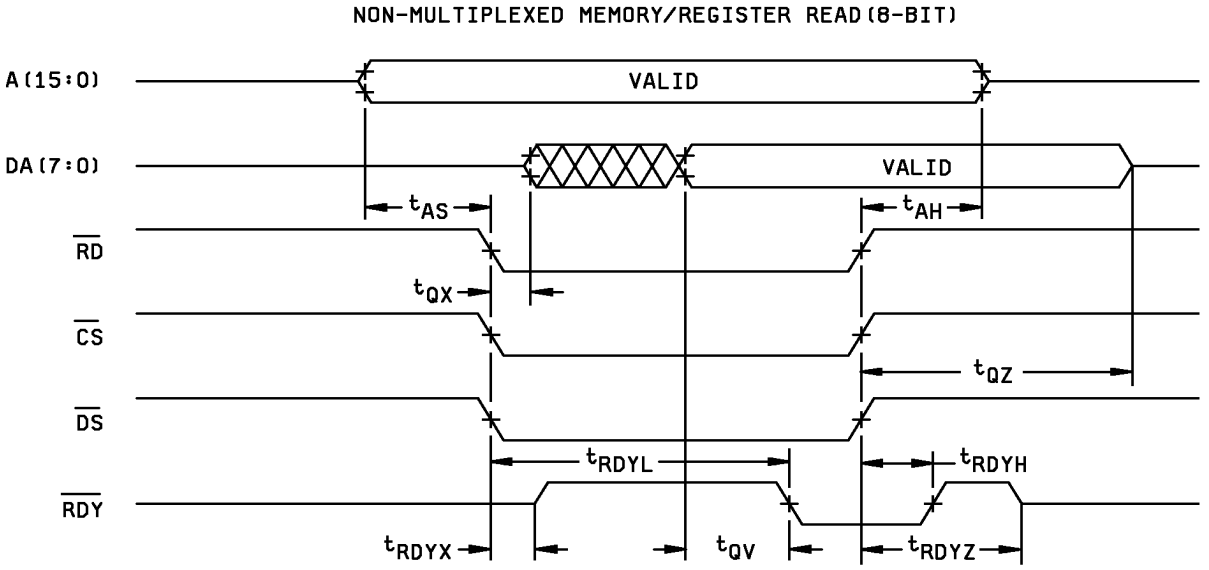
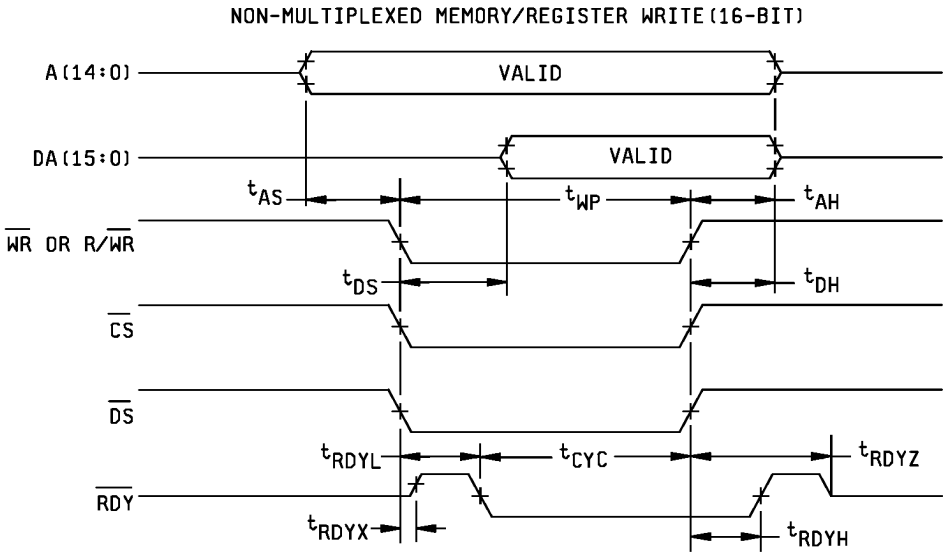
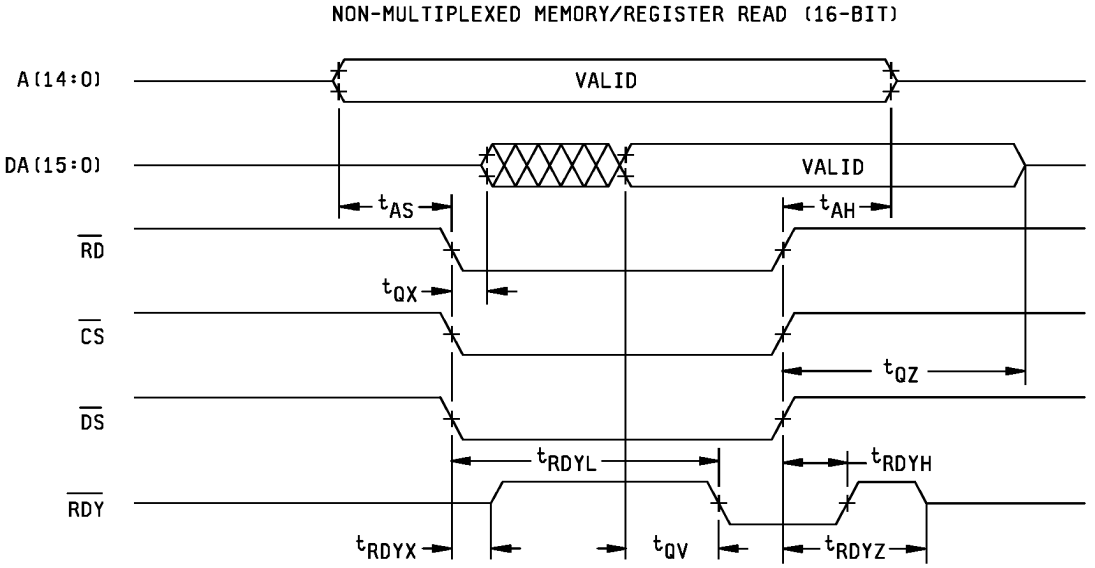


FIGURE 5. Timing waveforms - Continued.



NOTE: Most Significant Bit of A (A[14]) must be zero when address is driven.



NOTE: Most Significant Bit of A (A[14]) must be zero when address is driven.

FIGURE 5. Timing waveforms - Continued.

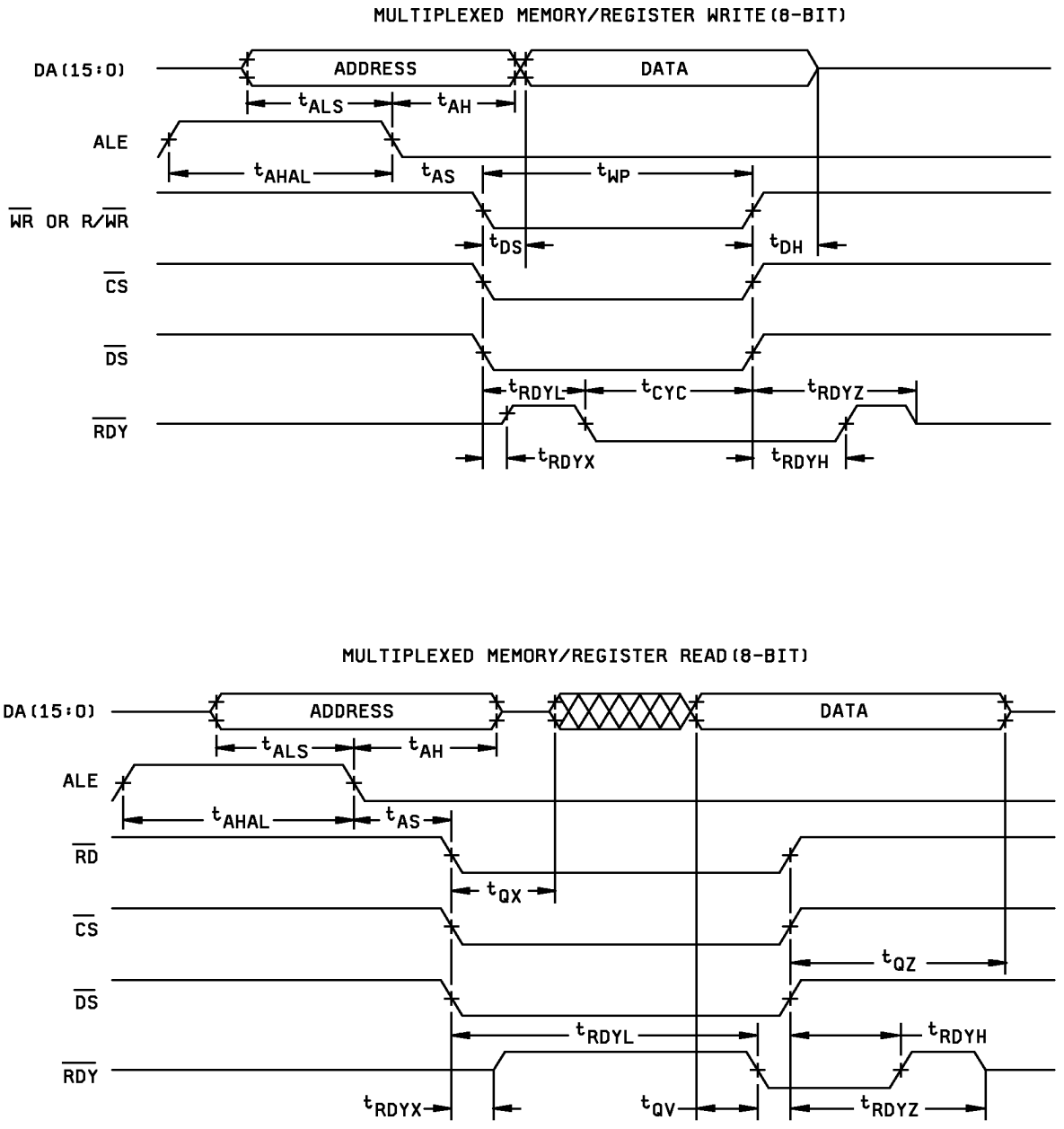
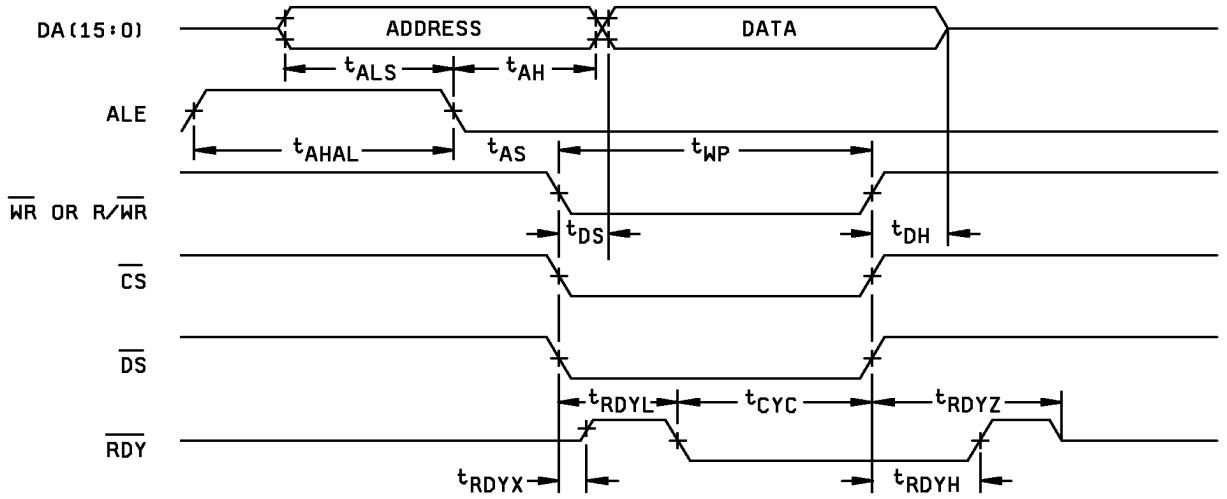


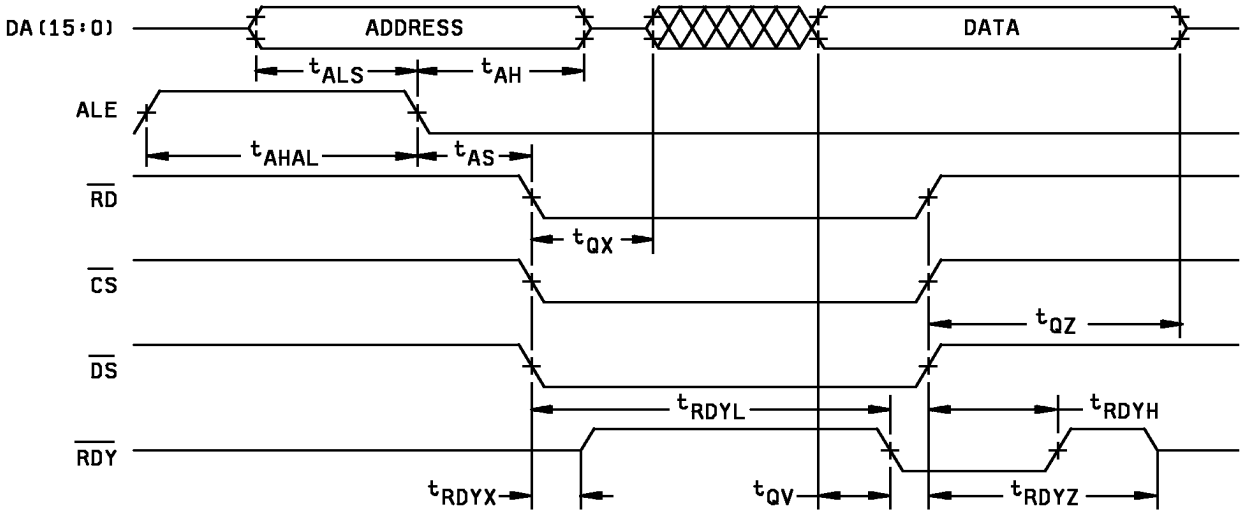
FIGURE 5. Timing waveforms - Continued.

MULTIPLEXED MEMORY/REGISTER WRITE (16-BIT)



NOTE: Most Significant Bit of DA (DA[15]) must be zero when address is driven.

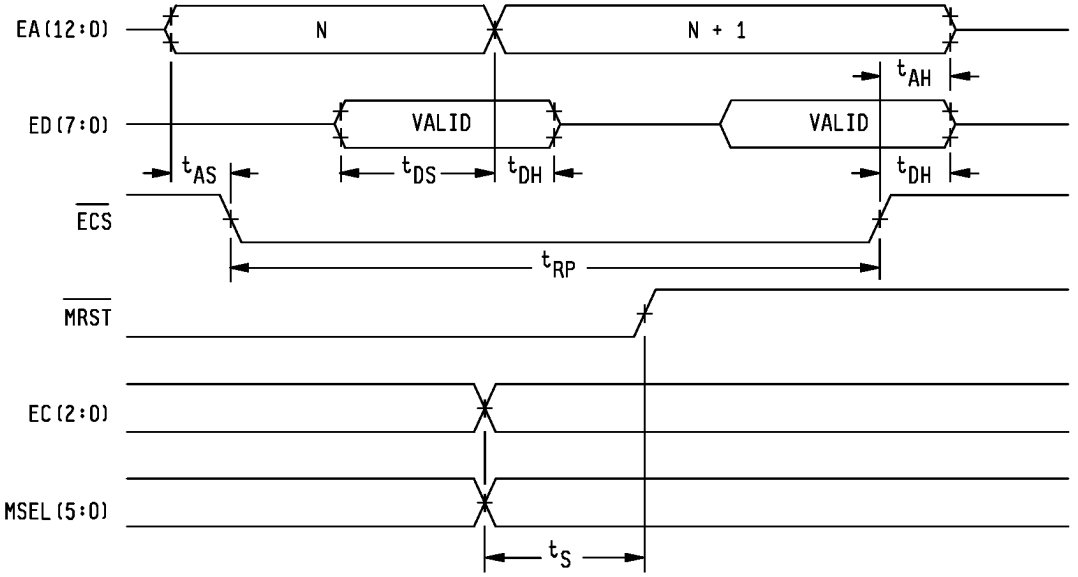
MULTIPLEXED MEMORY/REGISTER READ(16-BIT)

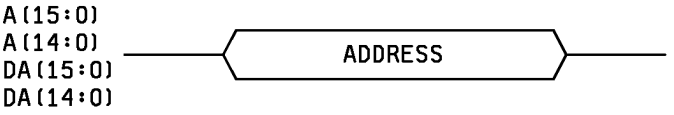


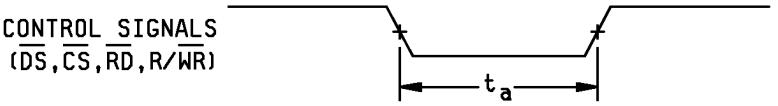
NOTE: Most Significant Bit of DA (DA[15]) must be zero when address is driven.

FIGURE 5. Timing waveforms - Continued.

AUTO-INITIALIZATION READ CYCLE



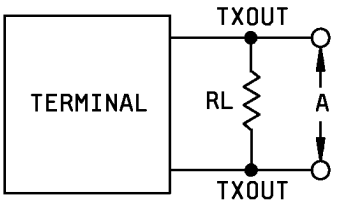




MAXIMUM CYCLE TIME

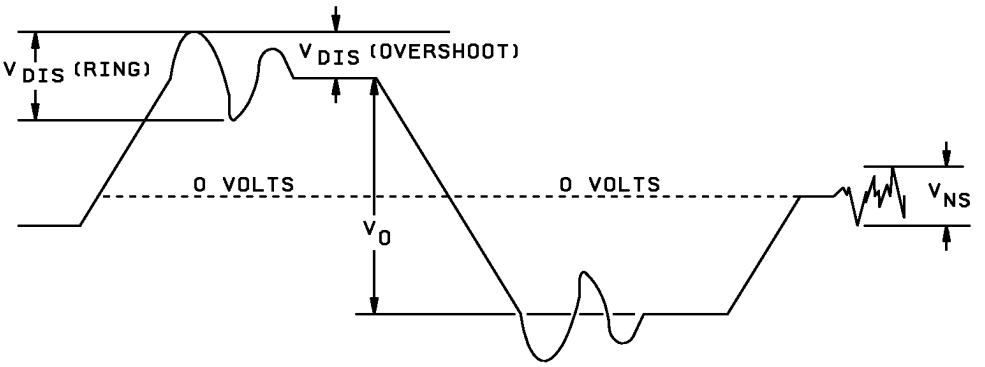
FIGURE 5. Timing waveforms - Continued.

TRANSCEIVER TEST CIRCUIT MIL-STD-1553B

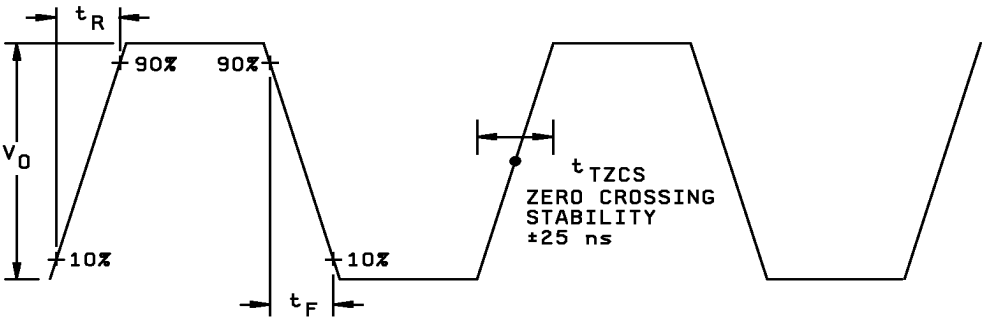


NOTES:
1. Transformer coupled stub:
   Terminal is defined as a transceiver plus isolation transformer.
2. Direct coupled stub:
   Terminal is defined as transceiver plus isolation transformer and fault resistor.

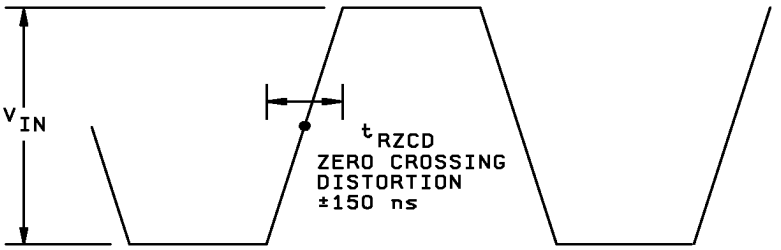
FIGURE 5. Timing waveforms - Continued.



TRANSMITTER OUTPUT CHARACTERISTICS (V_{DIS}, V_{NS}, V_O)

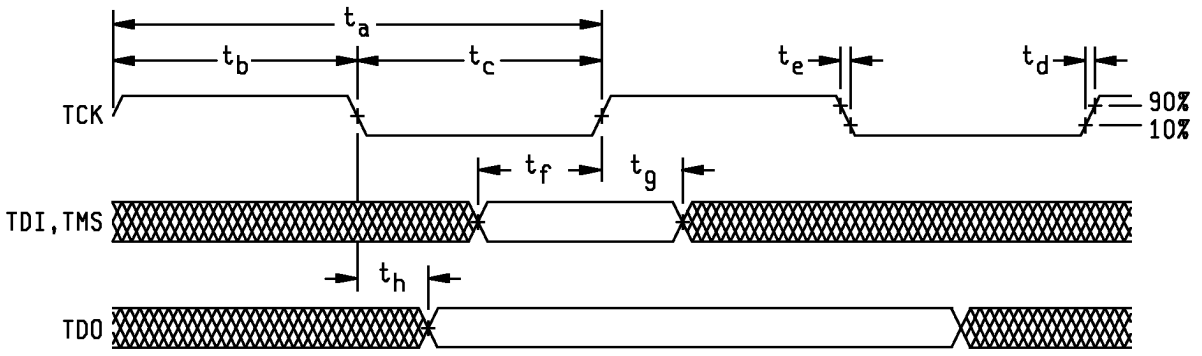


TRANSMITTER OUTPUT ZERO CROSSING STABILITY (t_{TZCS}, t_R, t_F)



RECEIVER INPUT ZERO CROSSING DISTORTION (t_{RZCD})

FIGURE 5. Timing waveforms - Continued.



JTAG TIMING

FIGURE 5. Timing waveforms - Continued.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-PRF-38535 permits alternate in-line control testing. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the functionality of the device. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

c. Subgroup 4 (C_{IN}, C_{OUT}, and C_{IO}) shall be measured only for the initial test and after process or design changes which may affect input capacitance. A minimum sample of 5 devices with zero failures shall be required.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

b. T_A = +125 C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1, 7, 9	1, 7, 9	1, 7, 9
Final electrical parameters (see 4.2)	1, 2, 3, 7, 8, 9, 10, 11 1/	1, 2, 3, 7, 8, 9, 10, 11 1/	1, 2, 3, 7, 8, 9, 10, 11 2/
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9
Group D end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9
Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25 C 5 C, after exposure, to the subgroups specified in table II herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0525.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA , Columbus, Ohio 43216-5000, or telephone (614) 692-0674.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535, MIL-HDBK-1331, and table III herein.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

TABLE III. Pin descriptions.

Name	Type 1/	Active 2/	Description
Data bus			
DA0	TTB	--	Bit 0 (LSB) of the bidirectional Data bus.
DA1	TTB	--	Bit 1 of the bidirectional Data bus.
DA2	TTB	--	Bit 2 of the bidirectional Data bus.
DA3	TTB	--	Bit 3 of the bidirectional Data bus.
DA4	TTB	--	Bit 4 of the bidirectional Data bus.
DA5	TTB	--	Bit 5 of the bidirectional Data bus.
DA6	TTB	--	Bit 6 of the bidirectional Data bus.
DA7	TTB	--	Bit 7 of the bidirectional Data bus.
DA8	TTB	--	Bit 8 of the bidirectional Data bus.
DA9	TTB	--	Bit 9 of the bidirectional Data bus.
DA10	TTB	--	Bit 10 of the bidirectional Data bus.
DA11	TTB	--	Bit 11 of the bidirectional Data bus.
DA12	TTB	--	Bit 12 of the bidirectional Data bus.
DA13	TTB	--	Bit 13 of the bidirectional Data bus.
DA14	TTB	--	Bit 14 of the bidirectional Data bus.
DA15	TTB	--	Bit 15 (MSB) of the bidirectional Data bus.
Address bus			
A0	TI	--	Bit 0 (LSB) of the Address bus.
A1	TI	--	Bit 1 of the Address bus.
A2	TI	--	Bit 2 of the Address bus.
A3	TI	--	Bit 3 of the Address bus.
A4	TI	--	Bit 4 of the Address bus.
A5	TI	--	Bit 5 of the Address bus.
A6	TI	--	Bit 6 of the Address bus.
A7	TI	--	Bit 7 of the Address bus.
A8	TI	--	Bit 8 of the Address bus.
A9	TI	--	Bit 9 of the Address bus.
A10	TI	--	Bit 10 of the Address bus.
A11	TI	--	Bit 11 of the Address bus.
A12	TI	--	Bit 12 of the Address bus.
A13	TI	--	Bit 13 of the Address bus.
A14	TI	--	Bit 14 of the Address bus.
A15	TI	--	Bit 15 (MSB) of the Address bus.

See footnotes at end of table.

TABLE III. Pin descriptions - Continued.

Name	Type 1/	Active 2/	Description
Auto-initialization address bus			
EA0	TO	--	Bit 0 (LSB) of the auto-init Address bus.
EA1	TO	--	Bit 1 of the auto-init Address bus.
EA2	TO	--	Bit 2 of the auto-init Address bus.
EA3	TO	--	Bit 3 of the auto-init Address bus.
EA4	TO	--	Bit 4 of the auto-init Address bus.
EA5	TO	--	Bit 5 of the auto-init Address bus.
EA6	TO	--	Bit 6 of the auto-init Address bus.
EA7	TO	--	Bit 7 of the auto-init Address bus.
EA8	TO	--	Bit 8 of the auto-init Address bus.
EA9	TO	--	Bit 9 of the auto-init Address bus.
EA10	TO	--	Bit 10 of the auto-init Address bus.
EA11	TO	--	Bit 11 of the auto-init Address bus.
EA12	TO	--	Bit 12 (MSB) of the auto-init Address bus.
Auto-initialization data bus			
ED0	TUI	--	Bit 0 (LSB) of the auto-init data.
ED1	TUI	--	Bit 1 of the auto-init data.
ED2	TUI	--	Bit 2 of the auto-init data.
ED3	TUI	--	Bit 3 of the auto-init data.
ED4	TUI	--	Bit 4 of the auto-init data.
ED5	TUI	--	Bit 5 of the auto-init data.
ED6	TUI	--	Bit 6 of the auto-init data.
ED7	TUI	--	Bit 7 (MSB) of the auto-init data.
Remote terminal address inputs			
RTA0	TUI	--	Remote Terminal Address bit 0. This input is the least significant bit for the RT address.
RTA1	TUI	--	Remote Terminal Address bit 1. This is bit 1 of the RT address.
RTA2	TUI	--	Remote Terminal Address bit 2. This is bit 2 of the RT address.
RTA3	TUI	--	Remote Terminal Address bit 3. This is bit 3 of the RT address.
RTA4	TUI	--	Remote Terminal Address bit 4. This is the most significant bit of the RT address.
RTPTY	TUI	--	Remote Terminal Parity. This is an odd parity input for the RT address.

See footnotes at end of table.

TABLE III. Pin descriptions - Continued.

Name	Type 1/	Active 2/	Description
JTAG testability pins			
TDOM	TTO	--	Memory Management Unit (MMU) TDO. This output performs the operation of Test Data Output as defined in the IEEE Standard 1149.1.
TDIM	TUI	--	MMU TDI. This input performs the operation of Test Data Input as defined in the IEEE Standard 1149.1.
TMSM	TUI	--	MMU TMS. This input performs the operation of Test Mode Select as defined in the IEEE Standard 1149.1.
TDOS	TTO	--	Device TDO. This output performs the operation of Test Data Output as defined in the IEEE Standard 1149.1.
TDIS	TUI	--	Device TDI. This input performs the operation of Test Data Input as defined in the IEEE Standard 1149.1.
TMSS	TUI	--	Device TMS. This input performs the operation of Test Mode Select as defined in the IEEE Standard 1149.1.
TCK	TI	--	TCK. This input performs the operation of Test Clock as defined in the IEEE Standard 1149.1.
$\overline{\text{TRST}}$	TUI	AL	$\overline{\text{TRST}}$. This input provides the RESET to the TAP controller as defined in the IEEE Standard 1149.1. This non-inverting input buffer is optimized for driving TTL input levels. When not exercising JTAG, tie $\overline{\text{TRST}}$ to a logical 0.
Biphase inputs/outputs			
CHA	DIO	--	Channel A (true). This is the Manchester-encoded true signal for channel A.
$\overline{\text{CHA}}$	DIO	--	Channel A (complement). This is the Manchester-encoded complement signal for channel A.
CHB	DIO	--	Channel B (true). This is the Manchester-encoded true signal for channel B.
$\overline{\text{CHB}}$	DIO	--	Channel B (complement). This is the Manchester-encoded complement signal for channel B.
Control signals			
$\overline{\text{CS}}$	TI	AL	Chip Select. This pin selects the device's internal memory and registers.
$\overline{\text{DS}}$	TI	AL	Data Strobe. During a write cycle, assert $\overline{\text{DS}}$ to indicate that data is valid on the data bus. During a read cycle, assert $\overline{\text{DS}}$ to signal the device to drive the data bus.
$\overline{\text{RD}}$	TI	AL	Read Strobe. During a read cycle, assert $\overline{\text{RD}}$ to signal the device to drive the data bus.
R/$\overline{\text{WR}}$ or $\overline{\text{WR}}$	TI	--	Read/Write or Write Strobe. During a write cycle, assert $\overline{\text{WR}}$ to signal the device that data is valid on the data bus. R/$\overline{\text{WR}}$ indicates the direction of data flow with respect to the device . R/$\overline{\text{WR}}$ high indicates the device will drive the data bus. R/$\overline{\text{WR}}$ low indicates an outside source will drive the data bus.
MSEL0	TI	--	Mode Select 0. This pin in conjunction with MSEL1 selects the device's mode of operation.

See footnotes at end of table.

TABLE III. Pin descriptions - Continued.

Name	Type 1/	Active 2/	Description
			Control signals – Continued
MSEL1	TI	--	Mode Select 1. This pin is in conjunction with MSEL0 selects the device's mode of operation. Latched on the rising edge of $\overline{MRST}$. MSEL1 / MSEL0 / Mode of Operation 0 / 0 / Bus Controller 0 / 1 / Remote Terminal 1 / 0 / Monitor Terminal 1 / 1 / Remote terminal and Monitor
MSEL2	TUI	--	Mode Select 2. A logical zero selects control signals $\overline{RD}$, $\overline{WR}$, $\overline{CS}$, $\overline{DS}$, and $\overline{RDY}$. A logical one selects control signals R/$\overline{WR}$, $\overline{CS}$, $\overline{DS}$, and $\overline{RDY}$. Latched on the rising edge of $\overline{MRST}$.
MSEL3	TUI	--	Mode Select 3. A logical zero enables the device's multiplexed address and data bus interface. A logical one enables the non-multiplexed interface. Latched on the rising edge of $\overline{MRST}$.
MSEL4	TUI	--	Mode Select 4. A logical zero enables a pulsed interrupt output. A logical one enables a level interrupt output. Latched on the rising edge of $\overline{MRST}$.
MSEL5	TUI	--	Mode Select 5. A logical zero enables the device's 16-bit interface. A logical one enables the 8-bit interface. Latched on the rising edge of $\overline{MRST}$.
EC0	TUI	--	Latched on the rising edge of $\overline{MRST}$ this input sizes the auto-initialization cycle.
EC1	TUI	--	Latched on the rising edge of $\overline{MRST}$ this input sizes the auto-initialization cycle.
EC2	TUI	--	Latched on the rising edge of $\overline{MRST}$ this input sizes the auto-initialization cycle.
24 MHz	CI	--	24 MHz Clock. The 24 MHz input clock requires a 50% 5% duty cycle with an accuracy of 0.01%.
$\overline{MRST}$	TUI	AL	Master Reset. This input pin resets the internal encoders, decoders, all registers, and associated logic.
ALE	TI	AH	Address Latch Enable. The falling edge of this strobe latches address information into the device when operating with a multiplexed address and data bus.
TCLK	TI	--	Timer Clock. The internal timer is a 16-bit counter with a 64 s resolution when using the 24 MHz input clock. For different applications requiring a different resolution, the user may input a clock from 0 to 60 MHz to establish the timer resolution. (Duty cycle equals 50% 10%).
A/$\overline{B}$ STD	TUI	--	A/$\overline{B}$. Military Standard A or B. This pin defines whether the device operates per MIL-STD-1553A or MIL-STD-1553B. Input is latched on the rising edge of $\overline{MRST}$.
$\overline{LOCK}$	TUI	AL	Lock. A logical zero applied to this pin prevents software changing the RT address, A/$\overline{B}$ STD, or mode of operation. Input is latched on the rising edge of $\overline{MRST}$.
$\overline{AUTOEN}$	TUI	AL	Auto Enable. When active this pin enables the device's auto-initialization function. Input is latched on the rising edge of $\overline{MRST}$.
$\overline{YF\_ACK}$	TUI	AL	You Failed Interrupt Acknowledge. Assertion of this input resets interrupt output $\overline{YF\_INT}$ when operating in the level mode.

See footnotes at end of table.

TABLE III. Pin descriptions - Continued.

Name	Type 1/	Active 2/	Description
Control signals – Continued			
$\overline{\text{MSG\_ACK}}$	TUI	AL	Message Interrupt Acknowledge. Assertion of this input resets interrupt output $\overline{\text{MSG\_INT}}$ when operating in the level mode.
$\overline{\text{SSYSF}}$	TUI	AL	Subsystem Fail. Upon assertion, this signal propagates directly to the RT's 1553 Status Word.
Status signals			
$\overline{\text{YF\_INT}}$	TTO 3/	AL	You Failed Interrupt. This pin asserts upon the occurrence of interrupt events which are not masked. Either a level output or pulse output.
$\overline{\text{MSG\_INT}}$	TTO 3/	AL	Message Interrupt. This pin asserts upon the occurrence of interrupt events which are not masked. Either a level output or pulse output.
$\overline{\text{READY}}$	TO	AL	$\overline{\text{READY}}$. Assertion of this output indicates the device has completed initialization or BIT, and regular opeation may begin.
$\overline{\text{ECS}}$	TO	AL	Chip Select. Auto-initialization device select.
$\overline{\text{RDY}}$	TTO	AL	Access Ready. Assertion of this output indicates that the host can complete the device access.
$\overline{\text{TERACT}}$	TO	AL	$\overline{\text{TERACT}}$. This output indicates that the terminal is actively processing a 1553 command.
$\overline{\text{BIST}}$	TO	AL	Built-In Test. Assertion of this output indicates the device is performing an internal memory test.
Power/Ground			
V_{DD}	--	--	+5 Volt Logic Power (10%)
V_{CC}	--	--	Device types 01, 03, 04, 06, 07, and 09: +5 Volt Transceiver Power (+10%, -5%). Recommended de-coupling capacitors: 4.7 F and 0.1 F. Device types 02, 05, and 08: +5 Volt Transceiver Power (10%). Recommended de-coupling capacitors: 4.7 F and 0.1 F.
V_{EE}	--	--	Device types 01, 03, 04, 06, 07, and 09 only: -12 or -15 Volt Transceiver Power (5%).
V_{SS}	--	--	Digital Ground.
GND	--	--	Transceiver Ground.

1/ TO = TTL output
TTB = Three-state TTL bidirectional
CI = CMOS input
TUI = TTL input (internally pulled high)
TI = TTL input
TTO = Three-state TTL output
DIO = Differential input/output
All pins designed for TTL are actually CMOS transistors, but designed for TTL compatibility.

2/ AH = Active high
AL = Active low

3/ High impedance and active low.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 99-04-12

Approved sources of supply for SMD 5962-94758 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and/or QML-38535 during the next revision. MIL-HDBK-103 and/or QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and/or QML-38535.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9475801QXA	3/	
5962-9475801QXC	3/	
5962-9475801QYA	3/	
5962-9475801QYC	3/	
5962-9475802QXA	3/	
5962-9475802QXC	3/	
5962-9475802QYA	3/	
5962-9475802QYC	3/	
5962-9475803QXA	3/	
5962-9475803QXC	3/	
5962-9475803QYA	3/	
5962-9475803QYC	3/	
5962-9475804QXA	3/	
5962-9475804QXC	3/	
5962-9475804QYA	3/	
5962-9475804QYC	3/	
5962-9475805QXA	3/	
5962-9475805QXC	3/	
5962-9475805QYA	3/	
5962-9475805QYC	3/	
5962-9475806QXA	3/	
5962-9475806QXC	3/	
5962-9475806QYA	3/	
5962-9475806QYC	3/	
5962-9475807QXA	65342	UT69151XTE15/GCA
5962-9475807QXC	65342	UT69151XTE15/GCC
5962-9475807QYA	65342	UT69151XTE15/WCA
5962-9475807QYC	65342	UT69151XTE15/WCC

See footnotes at end of table.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9475808QXA	65342	UT69151XTE5/GCA
5962-9475808QXC	65342	UT69151XTE5/GCC
5962-9475808QYA	65342	UT69151XTE5/WCA
5962-9475808QYC	65342	UT69151XTE5/WCC
5962-9475809QXA	65342	UT69151XTE12/GCA
5962-9475809QXC	65342	UT69151XTE12/GCC
5962-9475809QYA	65342	UT69151XTE12/WCA
5962-9475809QYC	65342	UT69151XTE12/WCC

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed, contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ No longer available from an approved source of supply.

Vendor CAGE number	Vendor name and address
65342	UTMC Microelectronics System Inc. 4350 Centennial Boulevard Colorado Springs, Colorado 80907-3486

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