

4-Mbit (256K x 16) Static RAM

Features

- Very high speed: 45 ns
- Wide voltage range: 2.2 V to 3.6 V and 4.5 V to 5.5 V
- Ultra low standby power
 - Typical Standby current: 1 μ A
 - Maximum Standby current: 7 μ A
- Ultra low active power
 - Typical active current: 2 mA at f = 1 MHz
- Easy memory expansion with \overline{CE} and \overline{OE} features
- Automatic power down when deselected
- Complementary metal oxide semiconductor (CMOS) for optimum speed and power
- Available in Pb-free 44-pin thin small outline package (TSOP) II package

Functional Description

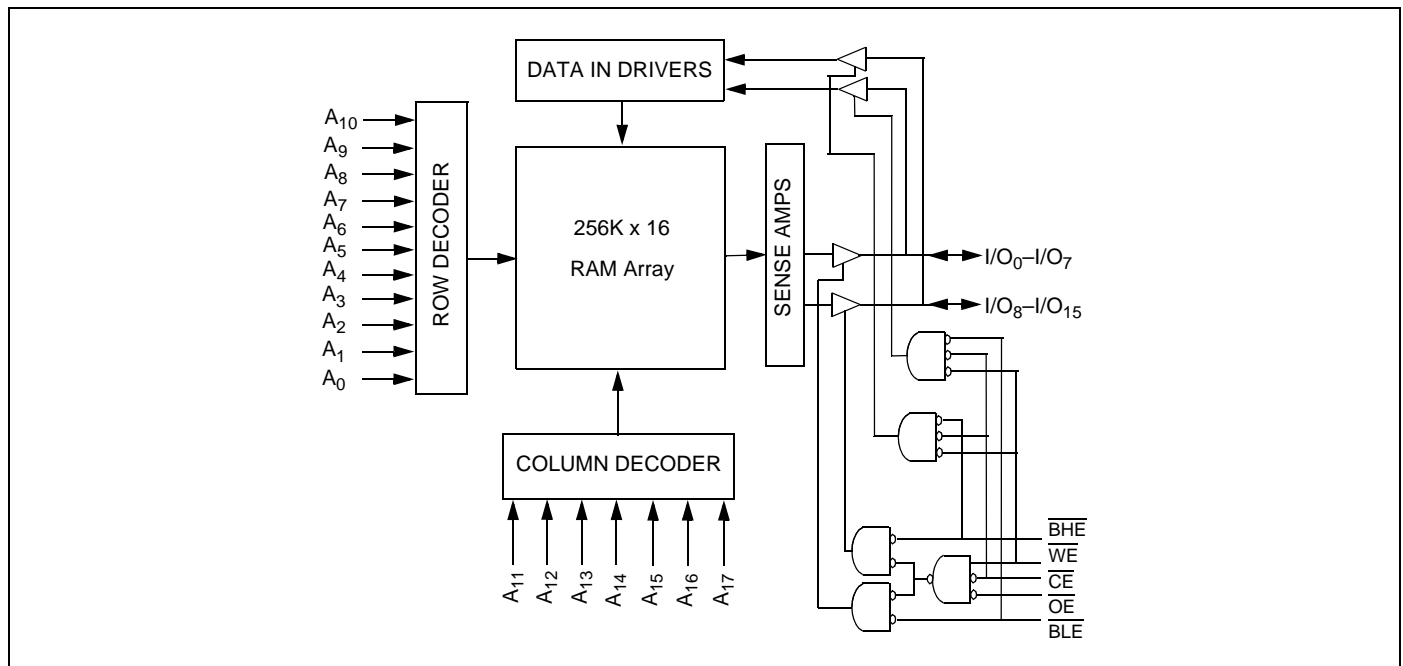
The CY62146ESL is a high performance CMOS static RAM organized as 256K words by 16 bits. This device features advanced circuit design to provide ultra low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable

applications such as cellular telephones. The device also has an automatic power down feature that reduces power consumption when addresses are not toggling. Placing the device into standby mode reduces power consumption by more than 99% when deselected (\overline{CE} HIGH). The input and output pins (I/O_0 through I/O_{15}) are placed in a high impedance state when the device is deselected (\overline{CE} HIGH), the outputs are disabled (\overline{OE} HIGH), both Byte High Enable and Byte Low Enable are disabled (\overline{BHE} , \overline{BLE} HIGH) or during a write operation (\overline{CE} LOW and \overline{WE} LOW).

To write to the device, take Chip Enable (\overline{CE}) and Write Enable (\overline{WE}) inputs LOW. If Byte Low Enable (\overline{BLE}) is LOW, then data from I/O pins (I/O_0 through I/O_7) is written into the location specified on the address pins (A_0 through A_{17}). If Byte High Enable (\overline{BHE}) is LOW, then data from I/O pins (I/O_8 through I/O_{15}) is written into the location specified on the address pins (A_0 through A_{17}).

To read from the device, take Chip Enable (\overline{CE}) and Output Enable (\overline{OE}) LOW while forcing the Write Enable (\overline{WE}) HIGH. If Byte Low Enable (\overline{BLE}) is LOW, then data from the memory location specified by the address pins appears on I/O_0 to I/O_7 . If Byte High Enable (\overline{BHE}) is LOW, then data from memory appears on I/O_8 to I/O_{15} . See the "Truth Table" on page 11 for a complete description of read and write modes.

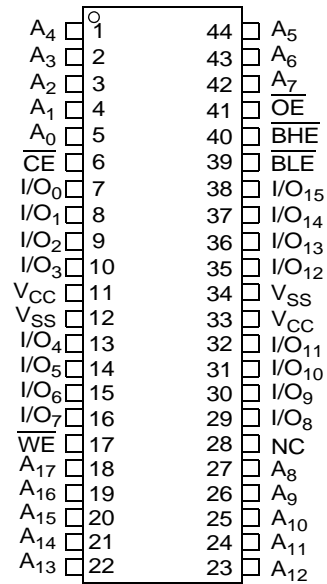
Logic Block Diagram



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Pin Configuration

Figure 1. 44-Pin TSOP II (Top View)^[1]


Product Portfolio

Product	Range	V _{CC} Range (V) ^[2]	Speed (ns)	Power Dissipation					
				Operating I _{CC} , (mA)				Standby, I _{SB2} (μA)	
				f = 1MHz		f = f _{max}			
				Typ ^[3]	Max	Typ ^[3]	Max	Typ ^[3]	Max
CY62146ESL	Industrial	2.2 V–3.6 V and 4.5 V–5.5 V	45	2	2.5	15	20	1	7

Notes

1. NC pins are not connected on the die.
2. Datasheet specifications are not guaranteed for V_{CC} in the range of 3.6 V to 4.5 V
3. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = 3 V, and V_{CC} = 5 V, T_A = 25 °C.

Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature -65 °C to +150 °C
 Ambient temperature with power applied -55 °C to +125 °C
 Supply voltage to ground potential -0.5 V to 6.0 V
 DC voltage applied to outputs in High-Z State^[4, 5] -0.5 V to 6.0 V
 DC input voltage^[4, 5] -0.5 V to 6.0 V
 Output current into outputs (LOW) 20 mA

Static discharge voltage >2001 V (MIL-STD-883, Method 3015)

Latch up current >200 mA

Operating Range

Device	Range	Ambient Temperature	V _{CC} ^[6]
CY62146ESL	Industrial	-40 °C to +85 °C	2.2 V–3.6 V, and 4.5 V–5.5 V

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	45 ns			Unit	
			Min	Typ ^[7]	Max		
V _{OH}	Output high voltage	2.2 ≤ V _{CC} ≤ 2.7	I _{OH} = -0.1 mA	2.0		V	
		2.7 ≤ V _{CC} ≤ 3.6	I _{OH} = -1.0 mA	2.4			
		4.5 ≤ V _{CC} ≤ 5.5	I _{OH} = -1.0 mA	2.4			
V _{OL}	Output low voltage	2.2 ≤ V _{CC} ≤ 2.7	I _{OL} = 0.1 mA		0.4	V	
		2.7 ≤ V _{CC} ≤ 3.6	I _{OL} = 2.1 mA		0.4		
		4.5 ≤ V _{CC} ≤ 5.5	I _{OL} = 2.1 mA		0.4		
V _{IH}	Input high voltage	2.2 ≤ V _{CC} ≤ 2.7		1.8	V _{CC} + 0.3	V	
		2.7 ≤ V _{CC} ≤ 3.6		2.2	V _{CC} + 0.3		
		4.5 ≤ V _{CC} ≤ 5.5		2.2	V _{CC} + 0.5		
V _{IL}	Input low voltage	2.2 ≤ V _{CC} ≤ 2.7		-0.3	0.6	V	
		2.7 ≤ V _{CC} ≤ 3.6		-0.3	0.8		
		4.5 ≤ V _{CC} ≤ 5.5		-0.5	0.8		
I _{IX}	Input Leakage Current	GND ≤ V _I ≤ V _{CC}		-1	+1	μA	
I _{OZ}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} , Output Disabled		-1	+1	μA	
I _{CC}	V _{CC} Operating Supply Current	f = f _{max} = 1/t _{RC}	V _{CC} = V _{CCmax}		15	20	mA
		f = 1 MHz	I _{OUT} = 0 mA, CMOS levels		2	2.5	
I _{SB1} ^[8]	Automatic CE Power down Current — CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.2 \text{ V}, V_{IN} \geq V_{CC} - 0.2 \text{ V}$ or $V_{IN} \leq 0.2 \text{ V}$, $f = f_{max}$ (Address and Data Only), I/O $f = 0$ (OE, BHE, BLE and WE), V _{CC} = V _{CC(max)}			1	7	μA
I _{SB2} ^[8]	Automatic CE Power down Current — CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.2 \text{ V}, V_{IN} \geq V_{CC} - 0.2 \text{ V}$ or $V_{IN} \leq 0.2 \text{ V}$, $f = 0, V_{CC} = V_{CC(max)}$			1	7	μA

Notes

4. V_{IL}(min) = -2.0V for pulse durations less than 20 ns.
5. V_{IH}(max) = V_{CC} + 0.75 V for pulse durations less than 20 ns.
6. Full Device AC operation assumes a 100 μs ramp time from 0 to V_{CC} (min) and 200 μs wait time after V_{CC} stabilization.
7. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = 3 V, and V_{CC} = 5 V, T_A = 25 °C.
8. Chip enable (CE) must be HIGH at CMOS level to meet the I_{SB1} / I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.

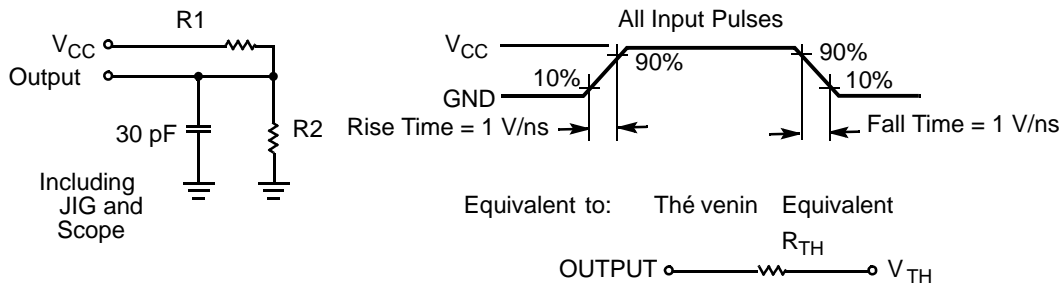
Capacitance

Parameter ^[9]	Description	Test Conditions	Max	Unit
C _{IN}	Input capacitance	T _A = 25 °C, f = 1 MHz, V _{CC} = V _{CC(typ)}	10	pF
C _{OUT}	Output capacitance		10	pF

Thermal Resistance

Parameter ^[9]	Description	Test Conditions	TSOP II	Unit
Θ _{JA}	Thermal resistance (Junction to ambient)	Still Air, soldered on a 3 x 4.5 inch, two-layer printed circuit board	77	°C/W
Θ _{JC}	Thermal resistance (Junction to case)		13	°C/W

Figure 2. AC Test Loads and Waveforms



Parameters	2.5 V	3.0 V	5.0 V	Unit
R1	16667	1103	1800	Ω
R2	15385	1554	990	Ω
R _{TH}	8000	645	639	Ω
V _{TH}	1.20	1.75	1.77	V

Note

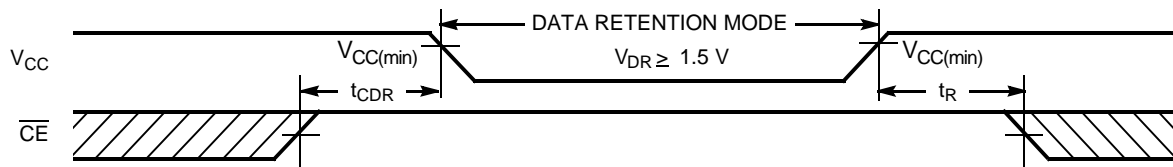
9. Tested initially and after any design or process changes that may affect these parameters.

Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions	Min	Typ ^[10]	Max	Unit
V_{DR}	V_{CC} for data retention		1.5			V
I_{CCDR} ^[11]	Data retention current	$\overline{CE} \geq V_{CC} - 0.2\text{ V}$, $V_{IN} \geq V_{CC} - 0.2\text{ V}$ or $V_{IN} \leq 0.2\text{ V}$		1	7	μA
t_{CDR} ^[12]	Chip deselect to data retention time		0			ns
t_R ^[13]	Operation recovery time		45			ns

Figure 3. Data Retention Waveform



Notes

- 10. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = 3\text{ V}$, and $V_{CC} = 5\text{ V}$, $T_A = 25\text{ }^\circ\text{C}$.
- 11. Chip enable (\overline{CE}) must be HIGH at CMOS level to meet the I_{SB1} / I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.
- 12. Tested initially and after any design or process changes that may affect these parameters.
- 13. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \geq 100\text{ }\mu\text{s}$ or stable at $V_{CC(min)} \geq 100\text{ }\mu\text{s}$.

Switching Characteristics

Over the Operating Range

Parameter ^[14]	Description	45 ns		Unit
		Min	Max	
Read Cycle				
t _{RC}	Read cycle time	45		ns
t _{AA}	Address to data valid		45	ns
t _{OHA}	Data hold from address change	10		ns
t _{ACE}	\overline{CE} LOW to data valid		45	ns
t _{DOE}	\overline{OE} LOW to data valid		22	ns
t _{LZOE}	\overline{OE} LOW to Low-Z ^[15]	5		ns
t _{HZOE}	\overline{OE} HIGH to High-Z ^[15, 16]		18	ns
t _{LZCE}	\overline{CE} LOW to Low-Z ^[15]	10		ns
t _{HZCE}	\overline{CE} HIGH to High-Z ^[15, 16]		18	ns
t _{PU}	\overline{CE} LOW to power up	0		ns
t _{PD}	\overline{CE} HIGH to power down		45	ns
t _{DBE}	$\overline{BLE}/\overline{BHE}$ LOW to data valid		22	ns
t _{LZBE}	$\overline{BLE}/\overline{BHE}$ LOW to Low-Z ^[15]	5		ns
t _{HZBE}	$\overline{BLE}/\overline{BHE}$ HIGH to HIGH-Z ^[15, 16]		18	ns
Write Cycle^[17]				
t _{WC}	Write cycle time	45		ns
t _{SCE}	\overline{CE} LOW to write end	35		ns
t _{AW}	Address setup to write end	35		ns
t _{HA}	Address hold from write end	0		ns
t _{SA}	Address setup to Write Start	0		ns
t _{PWE}	\overline{WE} pulse width	35		ns
t _{BW}	$\overline{BLE}/\overline{BHE}$ LOW to write end	35		ns
t _{SD}	Data Setup to write end	25		ns
t _{HD}	Data Hold from write end	0		ns
t _{HZWE}	\overline{WE} LOW to High-Z ^[15, 16]		18	ns
t _{LZWE}	\overline{WE} HIGH to Low-Z ^[15]	10		ns

Notes

14. Test conditions for all parameters other than tri-state parameters assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3 V, and output loading of the specified I_{OL}/I_{OH} as shown in the [AC Test Loads and Waveforms on page 5](#).

15. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZBE} is less than t_{LZBE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any device.

16. t_{HZOE}, t_{HZCE}, t_{HZBE}, and t_{HZWE} transitions are measured when the outputs enter a high-impedance state.

17. The internal write time of the memory is defined by the overlap of \overline{WE} , $\overline{CE} = V_{IL}$, \overline{BHE} , \overline{BLE} or both = V_{IL} . All signals must be active to initiate a write and any of these signals can terminate a write by going inactive. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.

Switching Waveforms

Figure 4. Read Cycle No.1: Address Transition Controlled. [18, 19]

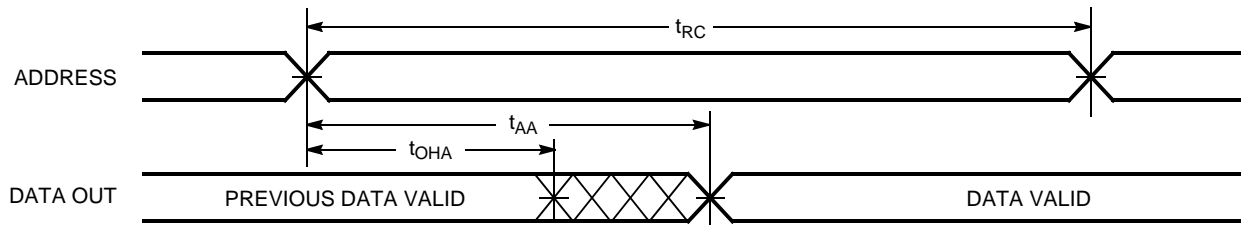
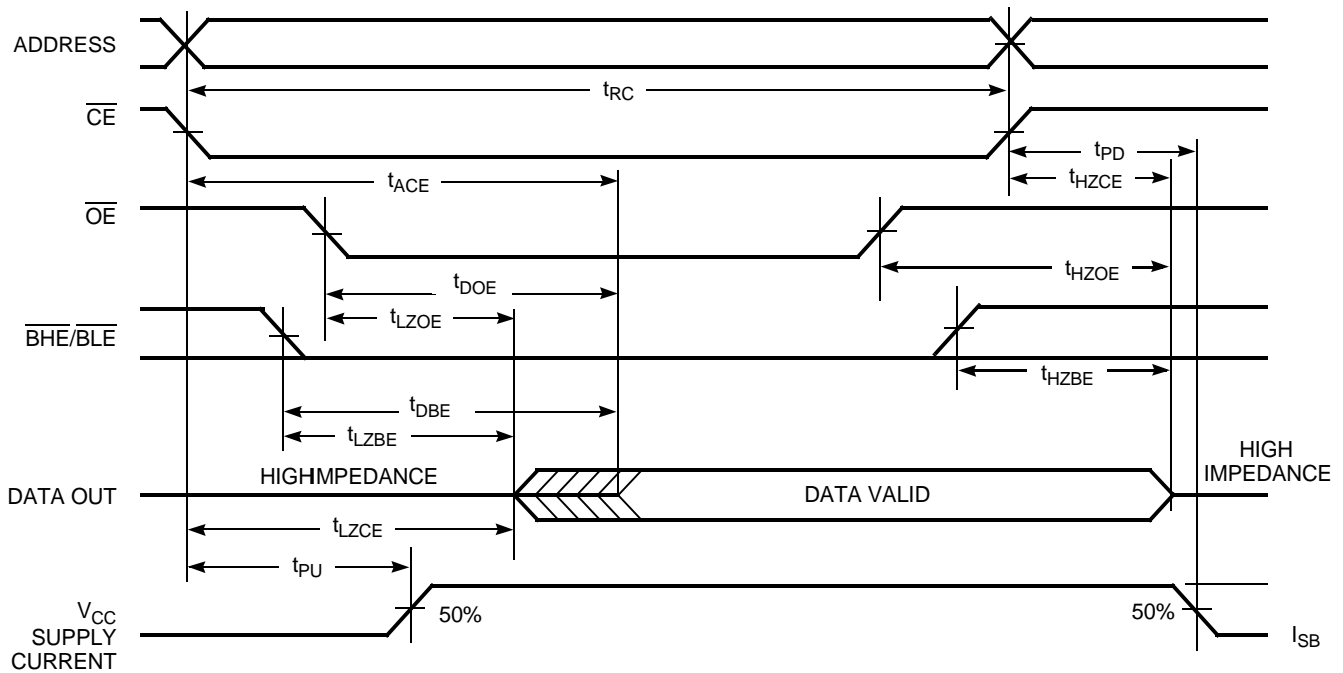


Figure 5. Read Cycle No. 2: \overline{OE} Controlled [19, 20]



Notes

- 18. The device is continuously selected. \overline{OE} , $\overline{CE} = V_{IL}$, \overline{BHE} , \overline{BLE} , or both = V_{IL} .
- 19. \overline{WE} is HIGH for read cycle.
- 20. Address valid before or similar to \overline{CE} , \overline{BHE} , \overline{BLE} transition LOW.

Switching Waveforms (continued)

Figure 6. Write Cycle No 1: \overline{WE} Controlled [21, 22, 23]

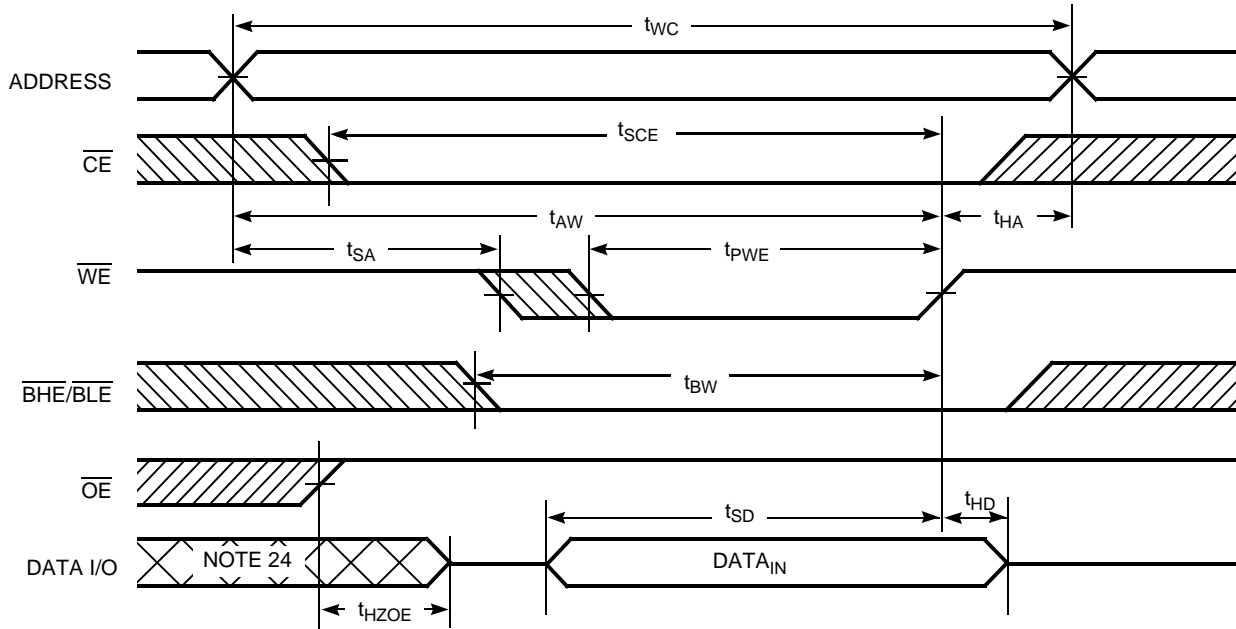
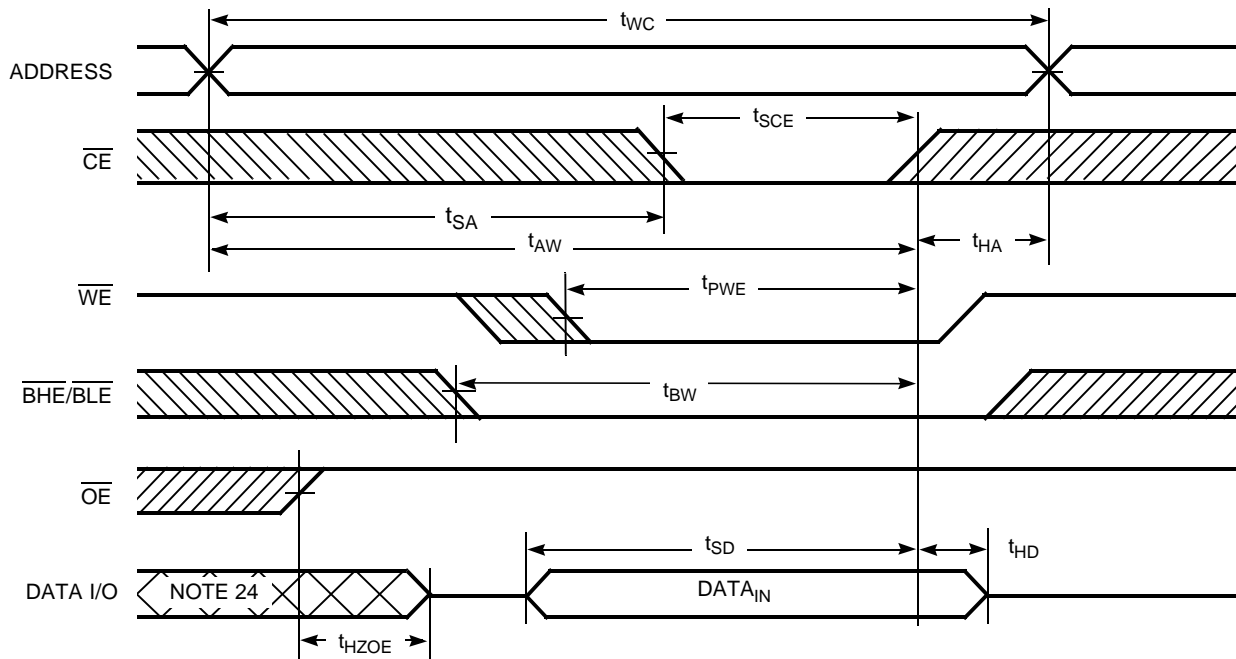


Figure 7. Write Cycle 2: \overline{CE} Controlled [21, 22, 23]



Notes

- 21. The internal write time of the memory is defined by the overlap of \overline{WE} , $\overline{CE} = V_{IL}$, \overline{BHE} , \overline{BLE} or both = V_{IL} . All signals must be active to initiate a write and any of these signals can terminate a write by going inactive. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.
- 22. Data I/O is high impedance if $OE = V_{IH}$.
- 23. If \overline{CE} goes HIGH simultaneously with $WE = V_{IH}$, the output remains in a high impedance state.
- 24. During this period, the I/Os are in output state. Do not apply input signals.

Switching Waveforms (continued)

Figure 8. Write Cycle 3: \overline{WE} controlled, \overline{OE} LOW [25]

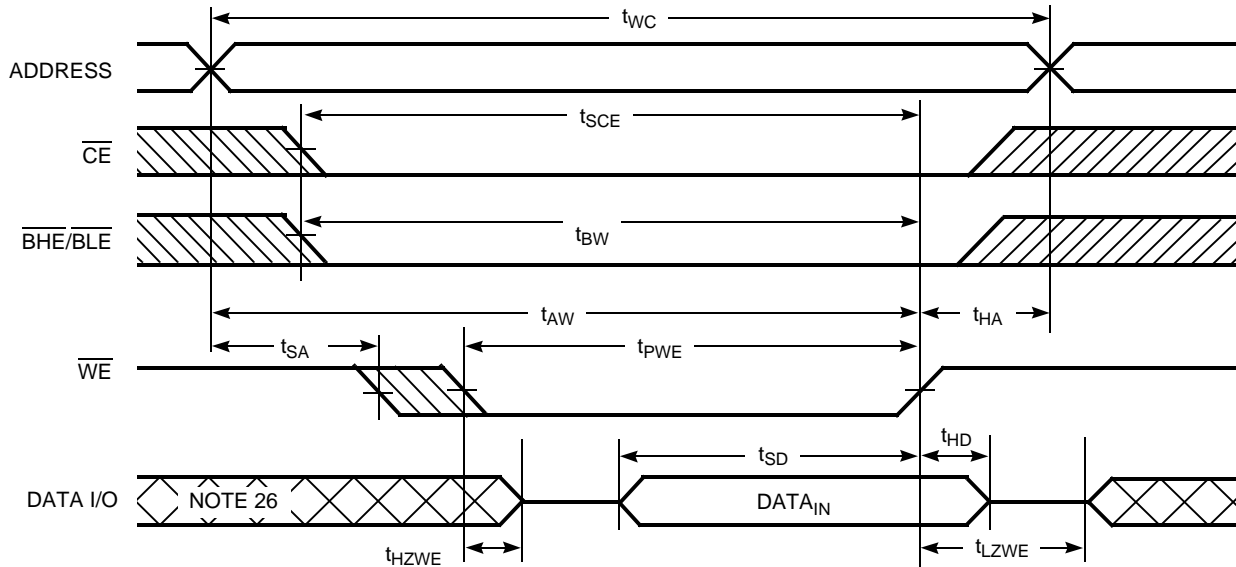
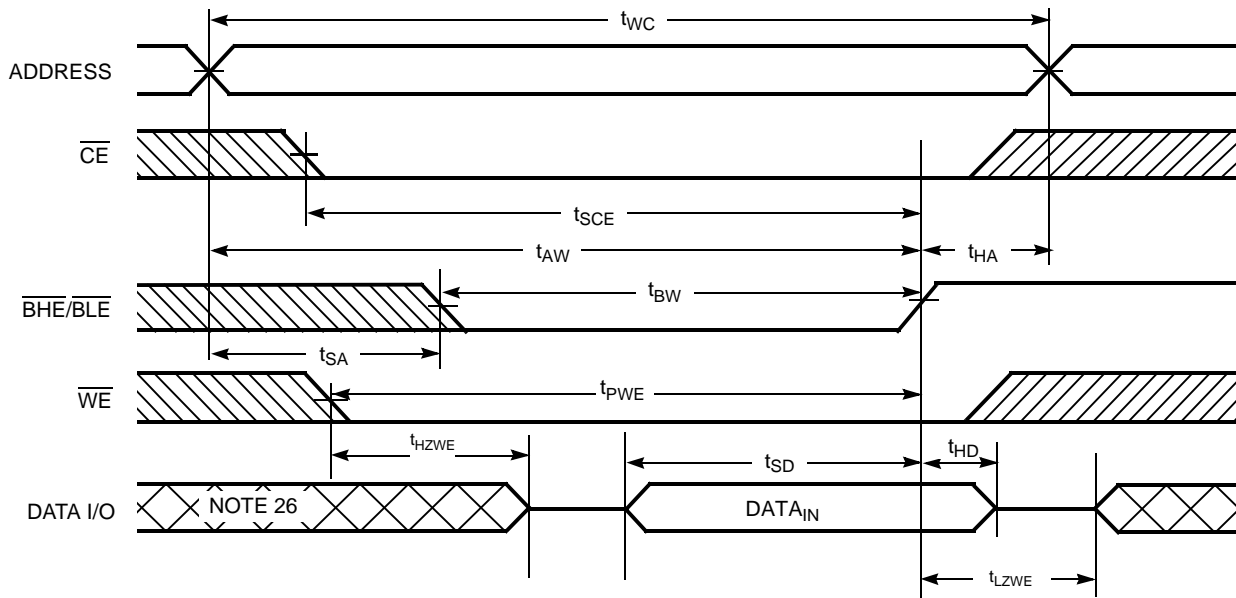


Figure 9. Write Cycle 4: $\overline{BHE}/\overline{BLE}$ Controlled, \overline{OE} LOW [25]



Notes

- 25. If \overline{CE} goes HIGH simultaneously with $\overline{WE} = V_{IH}$, the output remains in a high impedance state.
- 26. During this period, the I/Os are in output state. Do not apply input signals.

Truth Table

$\overline{CE}^{[27]}$	\overline{WE}	\overline{OE}	\overline{BHE}	\overline{BLE}	Inputs/Outputs	Mode	Power
H	X	X	X	X	High-Z	Deselect/Power down	Standby (I_{SB})
L	X	X	H	H	High-Z	Output disabled	Active (I_{CC})
L	H	L	L	L	Data Out (I/O ₀ –I/O ₁₅)	Read	Active (I_{CC})
L	H	L	H	L	Data Out (I/O ₀ –I/O ₇); I/O ₈ –I/O ₁₅ in High-Z	Read	Active (I_{CC})
L	H	L	L	H	Data Out (I/O ₈ –I/O ₁₅); I/O ₀ –I/O ₇ in High-Z	Read	Active (I_{CC})
L	H	H	L	L	High-Z	Output disabled	Active (I_{CC})
L	H	H	H	L	High-Z	Output disabled	Active (I_{CC})
L	H	H	L	H	High-Z	Output disabled	Active (I_{CC})
L	L	X	L	L	Data In (I/O ₀ –I/O ₁₅)	Write	Active (I_{CC})
L	L	X	H	L	Data In (I/O ₀ –I/O ₇); I/O ₈ –I/O ₁₅ in High-Z	Write	Active (I_{CC})
L	L	X	L	H	Data In (I/O ₈ –I/O ₁₅); I/O ₀ –I/O ₇ in High-Z	Write	Active (I_{CC})

Note

27. Chip enable must be at CMOS levels (not floating). Intermediate voltage levels on this pin is not permitted.

Acronyms

Acronym	Description
BHE	byte high enable
BLE	byte low enable
CE	chip enable
CMOS	complementary metal oxide semiconductor
I/O	input/output
OE	output enable
SRAM	static random access memory
TSOP	thin small outline package
VFBGA	very fine ball gird array
WE	write enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
μA	microamperes
mA	milliamperes
MHz	megahertz
ns	nanoseconds
pF	picofarads
V	volts
Ω	ohms
W	watts

Document History Page

Document Title: CY62146ESL MoBL [®] 4-Mbit (256K x 16) Static RAM Document Number: 001-43142				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	1875228	See ECN	VKN/AESA	New Data Sheet
*A	2944332	06/04/2010	VKN	Added Contents Added footnote for I _{SB2} parameter in Electrical Characteristics Added footnote related to chip enable in Truth Table Updated Package Diagram Added Sales, Solutions, and Legal Information
*B	3109186	12/13/2010	PRAS	Changed Table Footnotes to Footnotes. Added Ordering Code Definitions.
*C	3296704	06/29/2011	RAME	Removed reference to AN1064 SRAM system guidelines. Added footnote 9 to parameter sections of Capacitance and Thermal Resistance . Added I _{SB1} to footnote 8. Added footnote 11. Changed t _{RC} value as 45 in Data Retention Characteristics table. Footnote 14 moved to parameter section in Switching Characteristics Added Units of Measure .

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