

Am9122/Am91L22

256x4 Static RAM

DISTINCTIVE CHARACTERISTICS

- High-performance replacement for 93422/93L422
- Fast access times — as low as 25 ns
- Low-power dissipation
 - Low power: 440 mW (Commercial)
 - 495 mW (Military)
- Single 5-volt power supply — $\pm 10\%$ tolerance both Commercial and Military

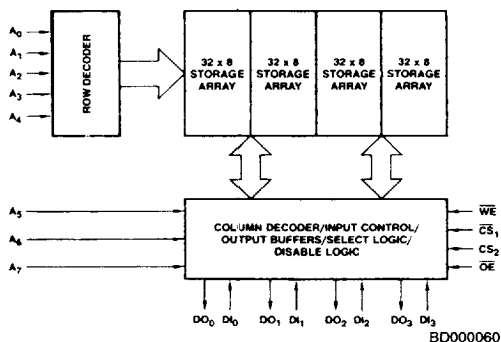
GENERAL DESCRIPTION

The Am9122/Am91L22 Series is a MOS pin-for-pin and functional replacement for the 93422/93L422 bipolar memories. These devices are high-performance, low-power, 1024-bit, static, read/write random access memories. They offer a wide range of access times including versions as fast as 25 ns. Each memory is implemented as 256 words by 4 bits per word. This organization permits efficient

design of small memory systems and allows finer resolution of incremental memory depth.

The Am9122/91L22 employs an output enable and two chip enable inputs to give the user better data control. High noise immunity, high output drive (4 TTL loads) and TTL logic voltage levels allow easy conversion from bipolar to MOS. 10% power supply tolerances give better margins in the memory system.

BLOCK DIAGRAM



MODE SELECT TABLE

Inputs					Outputs	Mode
OE	CS ₁	CS ₂	WE	D ₀ -D ₃		
X	H	X	X	X	Hi-Z	Not Selected
X	X	L	X	X	Hi-Z	Not Selected
L	L	H	H	X	O ₀ -O ₃	Read Stored Data
X	L	H	L	L	Hi-Z	Write "0"
X	L	H	L	H	Hi-Z	Write "1"
H	L	H	H	X	Hi-Z	Output Disabled
H	L	H	L	L	Hi-Z	Write "0" (Output Disabled)
H	L	H	L	H	Hi-Z	Write "1" (Output Disabled)

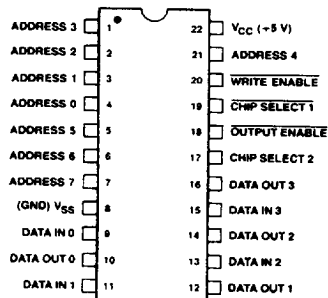
H = HIGH Voltage
L = LOW Voltage
X = Don't Care (HIGH or LOW)
Hi-Z = High Impedance

PRODUCT SELECTOR GUIDE

Part Number		Am9122-25	Am9122-35	Am91L22-35	Am91L22-45
Maximum Access Time (ns)		25	35	35	45
Maximum Operating Current (mA)	0° to +70°C	120	120	80	80
	-55° to +125°C	N/A	135	N/A	90

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CONNECTION DIAGRAM **Top View** **DIPs**

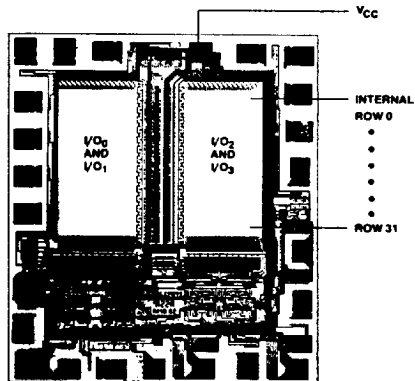


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Note: Pin 1 is marked for orientation.

METALLIZATION AND PAD LAYOUT

Address Designators	
External	Internal
A ₀	A ₀
A ₁	A ₁
A ₂	A ₂
A ₃	A ₃
A ₄	A ₄
A ₅	A ₅
A ₆	A ₆
A ₇	A ₇



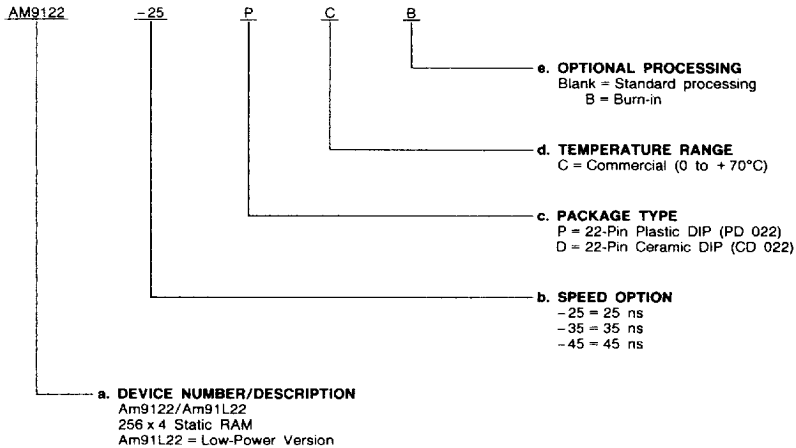
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ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

- a. **Device Number**
- b. **Speed Option** (if applicable)
- c. **Package Type**
- d. **Temperature Range**
- e. **Optional Processing**



Valid Combinations	
AM9122-25	DC, DCB, PC, PCB
AM91L22-35	
AM9122-35	
AM91L22-45	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult MSIS sales department to confirm availability of specific valid combinations, and to obtain additional data on MSIS's standard military grade products.

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Am9122/Am91L22

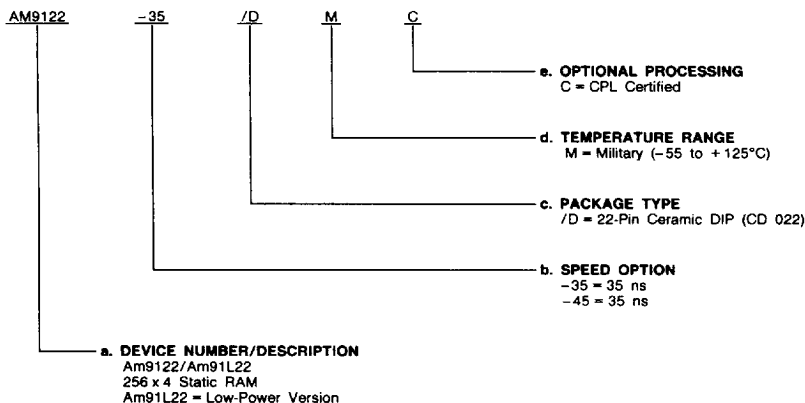
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MILITARY ORDERING INFORMATION

CPL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. CPL (Controlled Products List) products are processed in accordance with MIL-STD-883C, but are inherently non-compliant because of packages, solderability, or surface treatment exceptions to those specifications. The order number (Valid Combination) is formed by a combination of:

- a. Device Number
- b. Speed Option (if applicable)
- c. Package Type
- d. Temperature Range
- e. Optional Processing



Valid Combinations	
AM9122-35	/DMC
AM91L22-45	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult MSIS sales department to confirm availability of specific valid combinations, and to obtain additional data on MSIS's standard military grade products.

Group A Tests

Group A tests consist of Subgroups
1, 2, 3, 7, 8, 9, 10, 11.

PIN DESCRIPTION

A₀ - A₇ Address (Input)

The 8 address inputs select one of the 256 4-bit words in the RAM.

CS₁ Chip Select 1 (Input)

CS₂ Chip Select 2 (Input)

CS₁ is active LOW and CS₂ is active HIGH. The device can be accessed only when both Chip Selects are active. If either Chip Select is not active, the device is deselected and the outputs will be in a high-impedance state.

WE Write Enable Input

WE controls read and write operations. When WE is HIGH and OE is LOW, data will be present at the data outputs. When WE is LOW, data present on the data inputs will be

written into the selected memory location. The data outputs will be in a high-impedance state.

OE Output Enable (Input)

OE controls the state of the data outputs in conjunction with Chip Select and WE.

DI₀ - DI₃ Data IN (Input)

Data inputs to the RAM.

DO₀ - DO₃ Data Out (Output)

Data output from the RAM. The data output will be in a high-impedance state when either Chip Select is not active or OE is HIGH or WE is LOW.

V_{CC} Power Supply +5 Volts

V_{SS} Ground

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ABSOLUTE MAXIMUM RATINGS (Note 1)

Storage Temperature	-65 to +150°C
Ambient Temperature with Power Applied	-55 to +125°C
Supply Voltage	-0.5 V to +7.0 V
DC Voltage Applied to Outputs	-0.5 V to +7.0 V
DC Input Voltage	-0.5 V to +7.0 V
Power Dissipation	1.0 W
DC Output Current	20 mA

Stresses above those listed under **ABSOLUTE MAXIMUM RATINGS** may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES (Note 2)

Commercial (C) Devices	
Ambient Temperature (T _A)	0 to +70°C
Supply Voltage (V _{CC})	+4.5 V to +5.5 V
Military (M) Devices	
Ambient Temperature (T _A)	-55 to +125°C
Supply Voltage (V _{CC})	+4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating ranges unless otherwise specified (for CPL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions		Am91L22-35 Am91L22-45			Am9122-25 Am9122-35			Unit
				Min.	Typ.	Max.	Min.	Typ.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min.	I _{OH} = -5.2 mA	2.4			2.4			V
V _{OL}	Output LOW Voltage	V _{CC} = Min.	I _{OL} = 8.0 mA			0.4			0.4	V
V _{IH}	Input HIGH Voltage			2.1		V _{CC}	2.1		V _{CC}	V
V _{IL}	Input LOW Voltage			-2.5		0.8	-2.5		0.8	V
I _{IL}	Input LOW Current	V _{CC} = Max., V _{IN} = GND		-10			-10			μA
I _{IH}	Input HIGH Current	V _{CC} = Max., V _{IN} = V _{CC}				10			10	μA
V _{CD}	Input Diode Clamp Voltage					Note 3			Note 3	V
I _{OFF}	Output Current (Hi-Z)	V _{OL} ≤ V _{OUT} ≤ V _{OH} Output Disabled	T _A = Max.	-10		10	-10		10	μA
I _{OS}	Output Short Circuit Current (Note 4)	V _{CC} = Max., V _{OUT} = GND	COM'L			-85			-85	mA
			MIL			-100			-100	
I _{CC}	Power Supply Current	V _{CC} = Max., I _{OUT} = 0 mA	T _A = 0°C			80			120	mA
			T _A = -55°C			90			135	
C _{IN}	Input Capacitance V _{IN} = 0 V	T _A = 25°C, f = 1 MHz V _{CC} = 4.5 V (Note 5)			3	5		3	5	pF
C _{OUT}	Output Capacitance V _{OUT} = 0 V				5	8		5	8	

Notes: 1. Absolute Maximum Rating are intended for user guidelines and are not tested.

2. For test and correlation purposes, ambient temperature is defined as the "instant-ON" case temperature.

3. The NMOS process does not provide a clamp diode. However, the Am9122/91L22 is insensitive to -3 V DC input levels and -5 V undershoot pulses of less than 10 ns (measured at 50% point).

4. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.

5. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

6. Test conditions assume signal transition times of 10 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance as in A under Switching Test Circuits.

7. Transition is measured at 1.5 V on the input to V_{OH} - 500 mV and V_{OL} + 500 mV on the outputs using the load shown in B.

C_L = 5 pF.

8. t_w measured at t_{wsa} = Min.; t_{wsa} measured at t_w = Min.

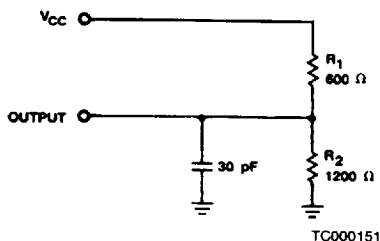
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SWITCHING CHARACTERISTICS over operating ranges unless otherwise specified (for CPL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted) (Notes 6, 7, 8)

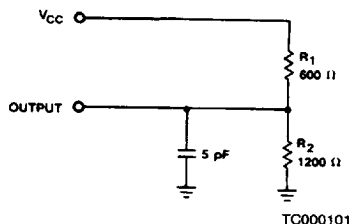
No.	Parameter Symbol	Parameter Description	Am9122-25		Am91L22-35 Am9122-35		Am91L22-45		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
1	t _{ACS}	Chip Select Time		15		25		30	ns
2	t _{ZRCS}	Chip Select to Hi-Z (Note 5 & 7)		20		30		30	ns
3	t _{AOS}	Output Enable Time		15		25		30	ns
4	t _{ZROS}	Output Enable to Hi-Z (Note 5 & 7)		20		30		30	ns
5	t _{AA}	Address Access Time		25		35		45	ns
6	t _{ZWS}	Write Disable to Hi-Z (Note 5 & 7)		20		30		35	ns
7	t _{WR}	Write Recovery Time		20		25		40	ns
8	t _W	Write Pulse Width (Note 8)	15		25		30		ns
9	t _{WSD}	Data Setup Time Prior to Write	5		5		5		ns
10	t _{WHD}	Data Hold Time After Write	5		5		5		ns
11	t _{WSA}	Address Setup Time (Note 8)	5		5		10		ns
12	t _{WHA}	Address Hold Time	5		5		5		ns
13	t _{WSCS}	Chip Select Setup Time	5		5		5		ns
14	t _{WHCS}	Chip Select Hold Time	5		5		5		ns

Notes: See notes following DC Characteristics table.

SWITCHING TEST CIRCUITS

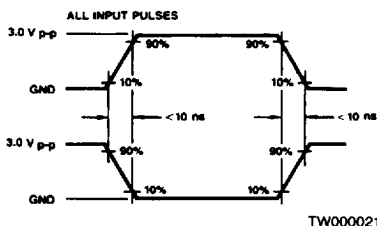


A



B

SWITCHING TEST WAVEFORM



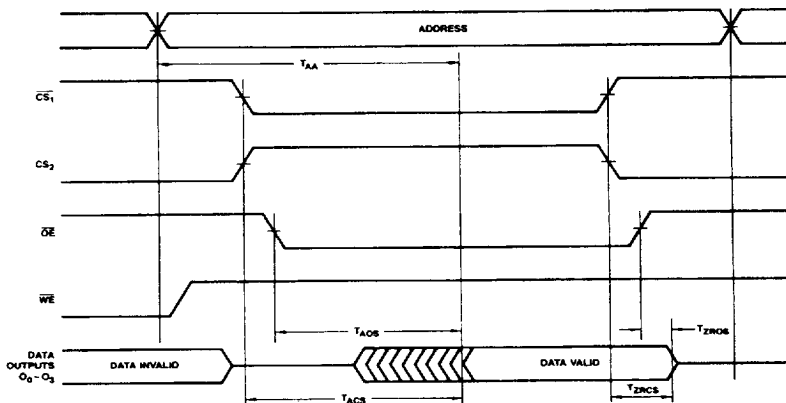
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SWITCHING WAVEFORMS

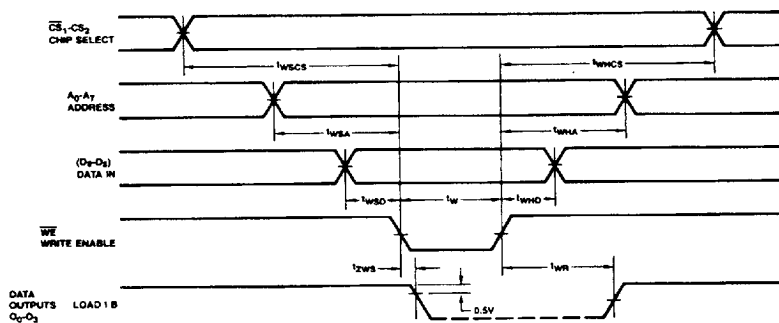
KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE ANY CHANGE PERMITTED	CHANGING STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE OFF STATE

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Read Mode



Write Mode

(All above measurements implemented to 1.5 V unless otherwise stated.)

Note: Timing diagram represents one solution which results in an optimum cycle time. Timing may be changed in various applications as long as the worst-case limits are not violated.

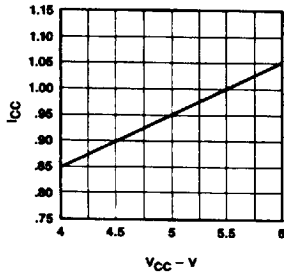
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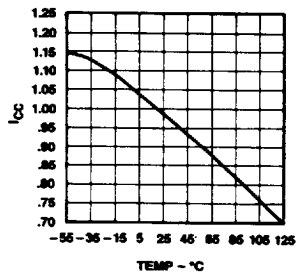
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TYPICAL PERFORMANCE CURVES

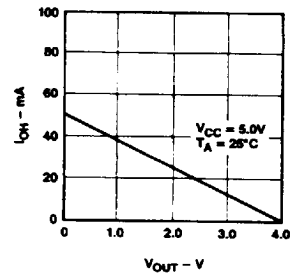
Normalized I_{CC}
versus Supply Voltage



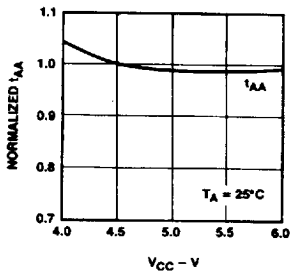
Normalized I_{CC}
versus Ambient Temperature



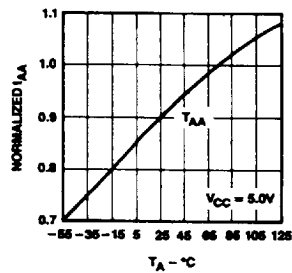
Output Source Current
versus Output Voltage



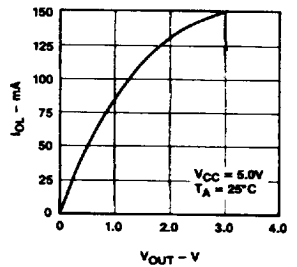
Normalized Access Time
versus Supply Voltage



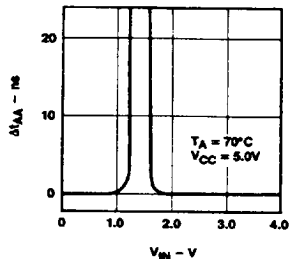
Normalized Access Time
versus Ambient Temperature



Output Sink Current
versus Output Voltage



Access Time Change
versus Input Voltage



Access Time Change
versus Output Loading

