STANDARD MICROSYSTEMS CORPORATION

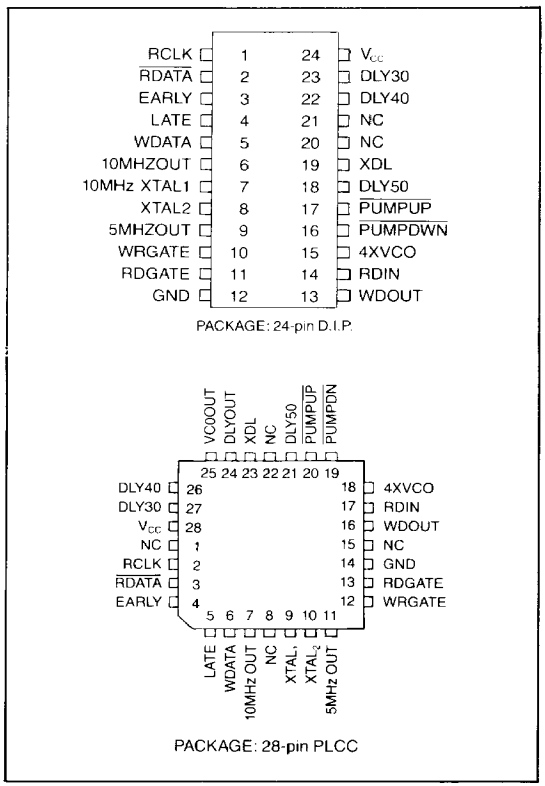
HDC 9226

HIGH PERFORMANCE HARD DISK DATA SEPARATOR "HDDS"

FEATURES

- Significantly reduces component count in hard disk systems
- Completely compatible with the HDC 9224 Universal Disk Controller
- Simplifies design and improves performance of ST506 Hard Disk Controller sub-system
- Built-in write precompensation logic
- Eliminates costly critical "tune up" adjustments
- Space saving 24 pin package saves board space and reduces critical layout problems.
- Printed Circuit Board Artwork available to facilitate prototyping and evaluation

PIN CONFIGURATION

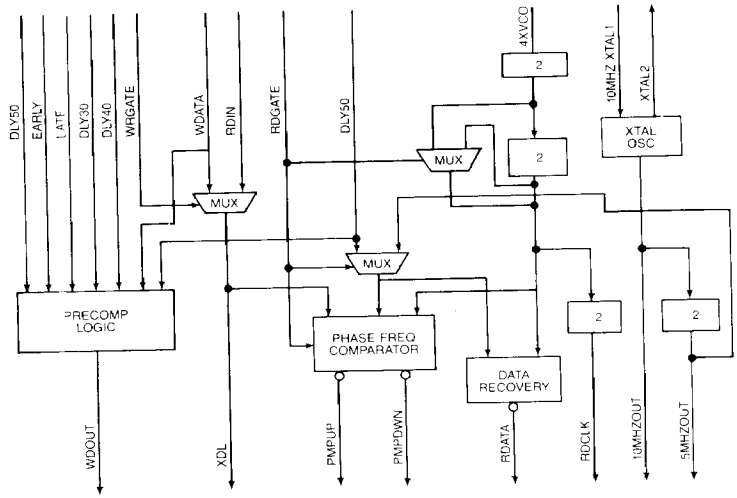


GENERAL DESCRIPTION

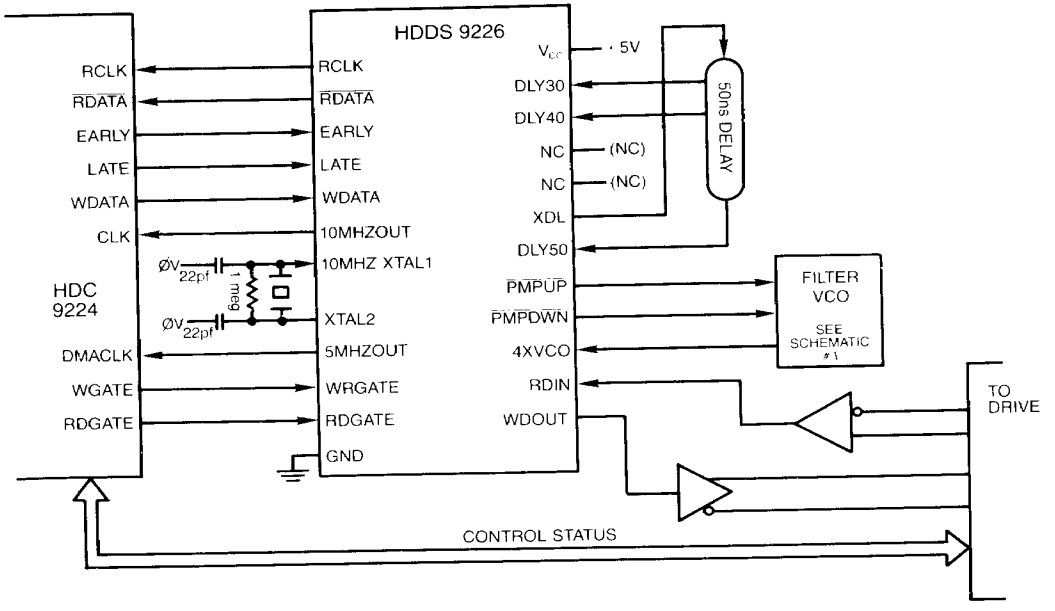
The HDC 9226 Hard Disk Data Separator (HDDS) is a 24 pin CMOS/LSI device, which when used with the HDC 9224 Universal Disk Controller significantly simplifies the design of a high performance hard disk data separator.

The HDC 9226, combined with a few discrete components, form a phase locked loop which performs phase and frequency locking onto either the FM or MFM data stream output by ST506/ST412 type drives.

By reducing the number of critical discrete components to a minimum and eliminating all critical adjustments, the HDC 9226 simplifies the task of the designer.



HDC 9226
BLOCK DIAGRAM



TYPICAL CIRCUIT CONFIGURATION

DESCRIPTION OF PIN FUNCTIONS

PIN. NO.	NAME	SYMBOL	DESCRIPTION
1	Read Clock	RCLK	Read clock output with nominal frequency of 5 MHz which defines the half bit boundaries of the RDATA output.
2	Read Data	RDATA	This output is the regenerated raw read data from the drive. This signal conforms to all timing requirements of the UDC.
3	Early	EARLY	This input is connected to the HDC 9224, and causes the HDDS to send out the write data early.
4	Late	LATE	This input is connected to the HDC 9224, and causes the HDDS to send out the write data late.
5	Write Data	WDATA	This input is connected to the HDC 9224, and is the MFM encoded write data signal. This signal is passed through the HDDS and is delayed according to the write precompensation inputs EARLY and LATE.
6	10 Mhz Out	10MHZOUT	This output is normally connected to the CLK input on the HDC 9224.
7, 8	Crystal 1, 2	XTAL 1,2	A 10 Mhz crystal may be connected between these two inputs. If a TTL signal is used in place of a crystal, the TTL signal (with pullup) should be connected to the XTAL 1 and the XTAL 2 input should be left open.
9	5 Mhz Out	5MHZOUT	This output is normally tied to the HDC 9224 DMACLK pin in systems that do not use the HDC 9225 Disk Buffer Management Unit.
10	Write Gate	WRGATE	This input is connected to the WRGATE output of the HDC 9224. When low the RDIN input is selected and is output to the delay line via the XDL pin. When in write mode (WRGATE active), the WDATA input is selected and output to the delay line via the XDL pin for precompensation.
11	Read Gate	RDGATE	This input signal, when active, allows the external VCO to begin locking on the incoming data from the drive. When this signal is inactive, the VCO will lock on to the 5 MHz output signal.
12	Ground	GND	This is the ground pin for the device
13	Write Data Out	WDOUT	This output is the precompensated version of the WDATA input. This output is normally connected to the write data signal of the hard disk drive.
14	Read Data In	RDIN	This input is normally connected to the Disk Data output of the drive. The leading edge of this input arms the internal phase comparator, and then also asserts the PMPUP output 50 ns later.
15	4 Times VCO	4XVCO	This input is connected to the external VCO and runs at a frequency of 4 times the data rate with RDGATE asserted. This signal is internally divided by 2 and feeds the phase comparator to generate the PMPDN signal. 4XVCO is also divided by four and output as the RCLK signal.
16	Pump Down	PMPDN	When active (low) this output will decrease the frequency of the VCO.
17	Pump Up	PMPUP	When active (low) this output will increase the frequency of the VCO.
18	Delay 50 ns	DLY50	This is the 50 ns delay of the XDL signal. The 50 ns tap is used to arm the phase detector and create a reclocked version of the raw read data from the drive.
19	Excite Delay Line	XDL	During write operations, when WRGATE is active, this output is identical to WDATA, and is output to the delay line, creating precise delays which are used to perform write precompensation. When WRGATE is inactive, this output is the image of the raw read data the RDIN input. XDL is output to the delay line and is used to provide proper arming for the phase comparator and clocking for the data recovery circuitry.
20, 21	No Connect	NC	No connection should be made to these pins.
22 23	Delay 40 Delay 30	DLY40 DLY30	These inputs are delays of 30 and 40 ns of the XDL signal, and come from the external delay line. These signals are used for the nominal, late and early positioning of the databits in the WDOUT data stream.
24	V_{CC}	V_{CC}	+5V supply connected to this pin.

DESCRIPTION OF OPERATION

DATA SEPARATION

The HDC 9226, in conjunction with an external VCO, tapped delay line and filter, allows the system designer to implement a high performance phase locked loop circuit to perform phase and frequency locking onto either an MFM or FM encoded data stream (from an ST-506 style disk drive.)

In most applications, the data on the hard disk is recorded in double density (MFM). In MFM mode, an input pulse on RDIN indicates not a 1 or 0 but rather a flux transition on the media and (by definition) these flux transitions may be spaced at T, 1.5T or 2T time intervals, where T equals the inverse of the bit data rate. For the standard ST-506 drive, these time intervals are 200 ns, 300 ns, and 400 ns.

Due to the nature of magnetic storage phenomena, the bit spacing found on the hard disk is not constant, but instead will modulate due to magnetic effects and drive rotational speed variations. The HDC 9226 compensates for these shifts in the RDIN signal coming from the drive and regenerates $\overline{\text{RDATA}}$ and RCLK.

The RCLK signal is derived from the VCO which changes its period as a function of the variations in the raw disk data and permits the data from the drive to be correctly clocked into the HDC 9224 Universal Disk Controller, independent of the bit spacing variations found in the raw data coming from the drive.

The VCO nominally runs at 20 Mhz. Since the half bit time (for data from the disk) is 100 ns, the HDC 9226 divides the 4XVCO signal in half and compares the phase and frequency of the VCO with the incoming data. The read data signal is regenerated by the HDC 9266 and is placed correctly within the RCLK window so as to satisfy the input timing requirements of the HDC 9224 Universal Disk Controller.

WRITE PRECOMPENSATION GENERATOR

The HDC 9226 also performs write precompensation which is needed because of tendency of written data to "re-align" itself on the magnetic media.

Certain bit patterns, when written, and later read back, will cause a phenomena known as "peak" or "bit" shift. Since this shifting is predictable, it is common when writing to magnetic media to intentionally pre-shift when these bits are to be written. This intentional "pre-shifting" minimizes the amount of shifting which occurs when the data is read back, and facilitates proper data recovery.

The HDC 9224 recognizes those patterns which require "pre-shifting" or precompensation, and outputs EARLY and LATE signals to alert the HDC 9226 to the need for precompensation.

Typical ST-506 applications may require "pre-shifting" the data bits by approximately 10 ns (either early or late). Three taps of the delay line (DLY30, DLY40, DLY50) are normally used to implement precompensation. The HDC 9226 then outputs the precompensated data via the WDOUT pin.

PERFORMANCE SPECIFICATIONS

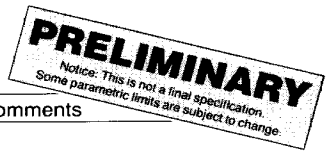
Complete performance specifications and specification definitions are contained in Technical Note 6-4, which is available from SMC Sales Offices and sales representatives. Technical Note 6-4 also contains full size PC board drawings and a complete bill of materials, useful in the prototyping of designs using the HDC 9226.

MAXIMUM GUARANTEED RATINGS

Operating Temperature Range ..... 0 to 70 C
Storage Temperature Range ..... −55 C to +150 C
Lead Temperature (soldering, 10 sec) ..... +325 C
Positive Voltage on any Pin, with respect to Ground ..... V_{CC} + 0.5V
Negative Voltage on any Pin, with respect to Ground ..... −0.5 V

Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied.

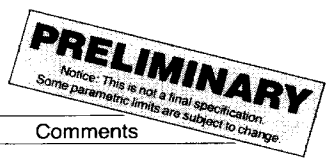
NOTE: When powering this device from laboratory or system power supplies, it is important that the "Maximum Guaranteed Ratings" not be exceeded, or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when AC power is switched off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists it is suggested that a clamp circuit be used.



DC ELECTRICAL SPECIFICATIONS (TA = 0 C to 70 C, V_{CC} = 5.0V, ± 5%)

Parameter	Min.	Max.	Units	Comments
SUPPLY CURRENT				
I_{CC}		30	mA	
OUTPUT VOLTAGE				
V_{OH} (1)	2.4		V	I_{OH} = 400 uA
V_{OH} (2)	4.3		V	I_{OH} = 400 uA
V_{OL}		0.4	V	I_{OL} = 2.0 mA
INPUT VOLTAGE				
V_{IH} (3)	2.0		V	
V_{IL} (3)		0.8	V	
V_{IH} (4)	3.5		V	
V_{IL} (4)		1.5	V	
INPUT CURRENT				
I_{IH}		10	uA	V_{IH} = 2.0V
I_{IL}		2.0	mA	V_{IL} = 0.4V

Notes:
(1) For all outputs except 10MHzOUT and 5MHzOUT
(2) For 10MHzOUT and 5MHzOUT
(3) For all inputs except XTAL 1 and 4XVCO
(4) For XTAL1 and 4XVCO



AC ELECTRICAL CHARACTERISTICS (TA = 0 C to + 70 C, V_{CC} = 5.0V, ± 5%)

Symbol	Min.	Typ.	Max.	Unit	Comments
T_1			70	ns	figure 1
T_2			80	ns	figure 1
T_3			65	ns	figure 2
T_4			70	ns	figure 2
T_5			100	ns	figure 3
T_6			100	ns	figure 3
T_7			35	ns	figure 4
T_8			35	ns	figure 4
T_9			60	ns	figure 4
T_{10}			70	ns	figure 4
T_{11}			65	ns	figure 5
T_{12}			65	ns	figure 5
T_{13}			65	ns	figure 5
T_{14}			65	ns	figure 5
T_{15}			45	ns	figure 6
T_{16}			45	ns	figure 7
T_{17}			45	ns	figure 8
T_{18}	45	50	55	ns	figure 9
T_{19}		50		ns	figure 10
T_{20}		50		ns	figure 11
T_{21}	6			ns	figure 12
T_{22}	50			ns	figure 12

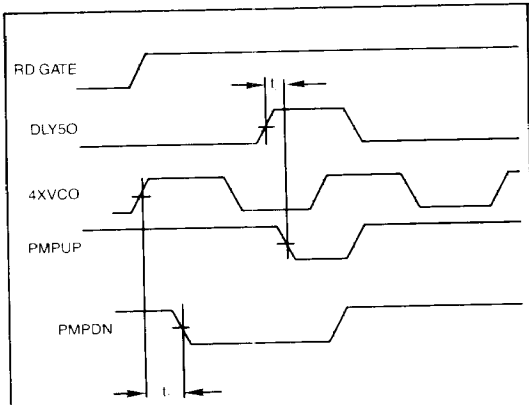


FIGURE 1

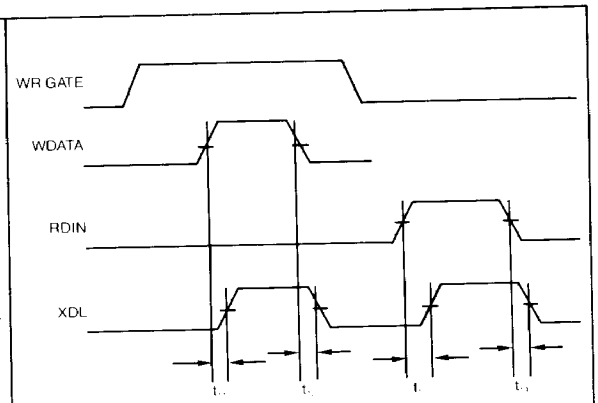


FIGURE 5

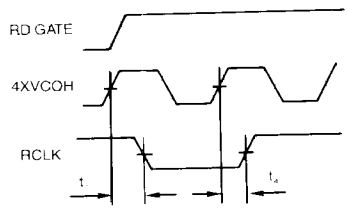


FIGURE 2

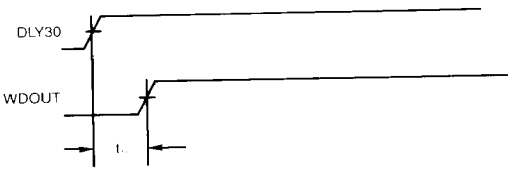


FIGURE 6

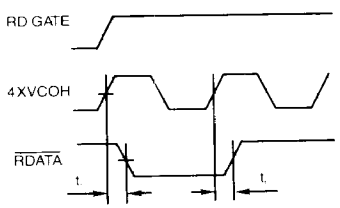


FIGURE 3

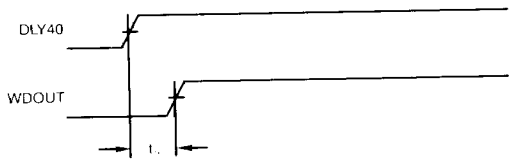


FIGURE 7

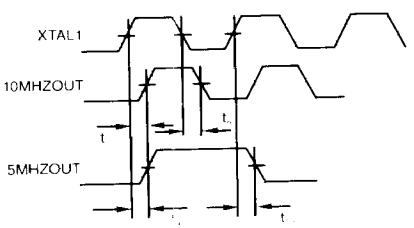


FIGURE 4

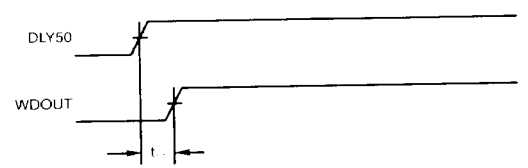


FIGURE 8

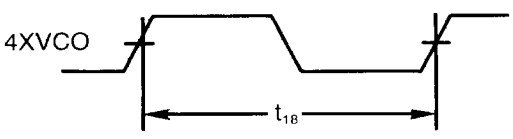


FIGURE 9

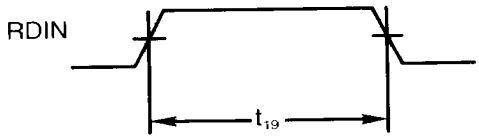
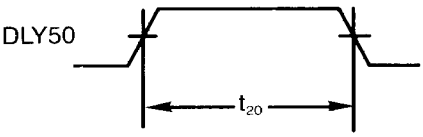


FIGURE 10



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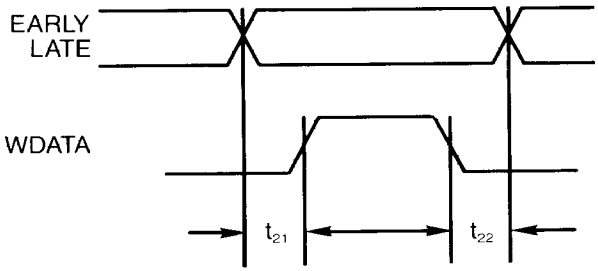
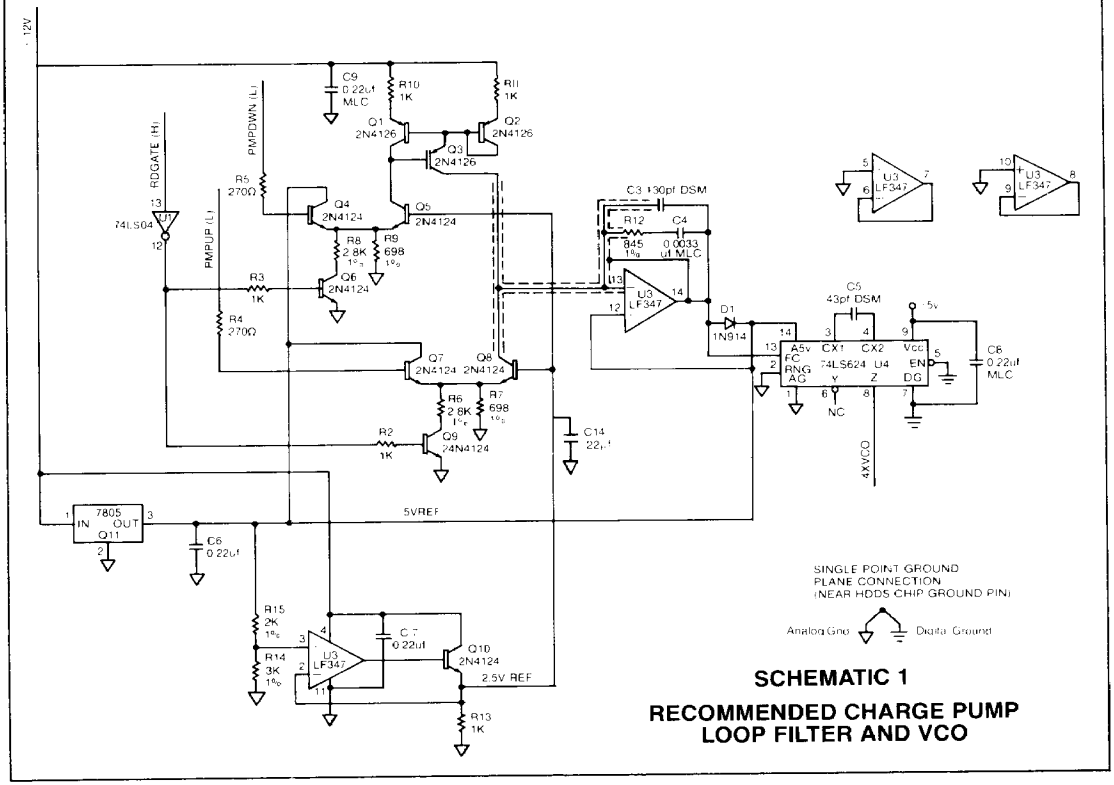


FIGURE 12

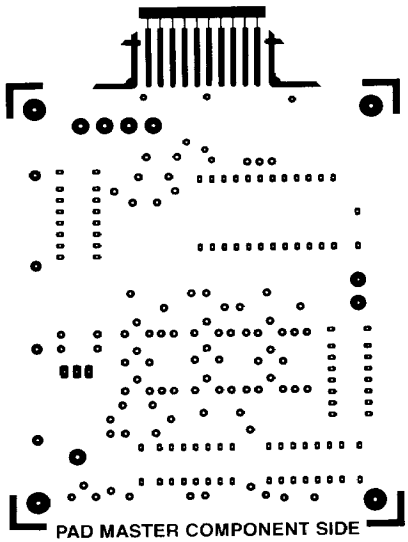


SCHEMATIC 1

RECOMMENDED CHARGE PUMP LOOP FILTER AND VCO

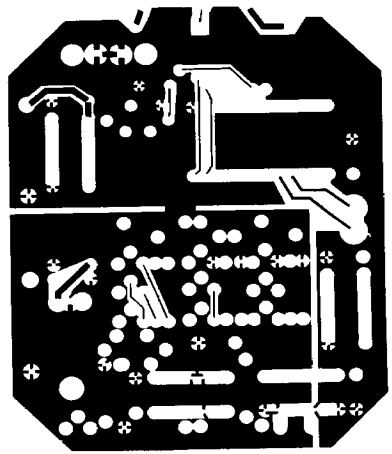
SECTION VI

PC 1



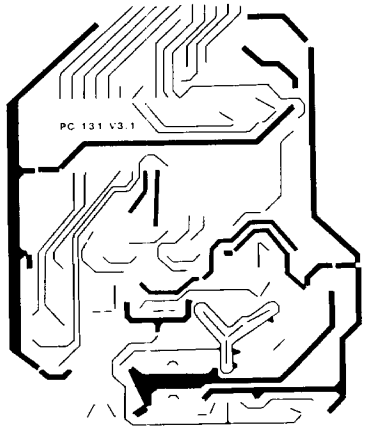
PAD MASTER COMPONENT SIDE

PC 2



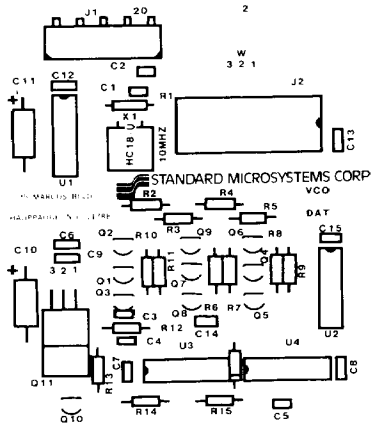
COMPONENT SIDE

PC 3



CIRCUIT SIDE

PC 4



SILK SCREEN

NOTE: The printed circuit board artwork shown above is included for illustration only. Camera ready artwork is available at no charge. Contact your SMC representative or regional sales office, and ask for Technical Note TN 6-4.

Blank PC boards (based on the illustrations above) are also available to facilitate evaluation and design. Contact your SMC representative or regional sales office for more information.