HM5164805F Series
HM5165805F Series

64 M EDO DRAM (8-Mword × 8-bit)
8 k Refresh/4 k Refresh

HITACHI

ADE-203-1057 (Z)
Preliminary
Rev. 0.0
May. 25, 1999

Description

The Hitachi HM5164805F Series, HM5165805F Series are 64M-bit dynamic RAMs organized as 8,388,608-word × 8-bit. They have realized high performance and low power by employing CMOS process technology. HM5164805F Series, HM5165805F Series offer Extended Data Out (EDO) Page Mode as a high speed access mode. They have the package variation of standard 32-pin plastic SOJ and standard 32-pin plastic TSOPII.

Features

- Single 3.3 V supply: 3.3 V ± 0.3 V
- Access time: 50 ns/60 ns (max)
- Power dissipation
  - — Active: 414 mW/378 mW (max) (HM5164805F Series)
    : 486 mW/414 mW (max) (HM5165805F Series)
  - — Standby : 1.8 mW (max) (CMOS interface)
    : TBD (L-version)
- EDO page mode capability
- Refresh cycles
  - — RAS-only refresh
    8192 cycles /64 ms (HM5164805F, HM5164805FL)
    4096 cycles /64 ms (HM5165805F, HM5165805FL)
  - — CBR/Hidden refresh
    4096 cycles /64 ms (HM5164805F, HM5164805FL, HM5165805F, HM5165805FL)

Preliminary: The specification of this device are subject to change without notice. Please contact your nearest Hitachi's Sales Dept. regarding specification.

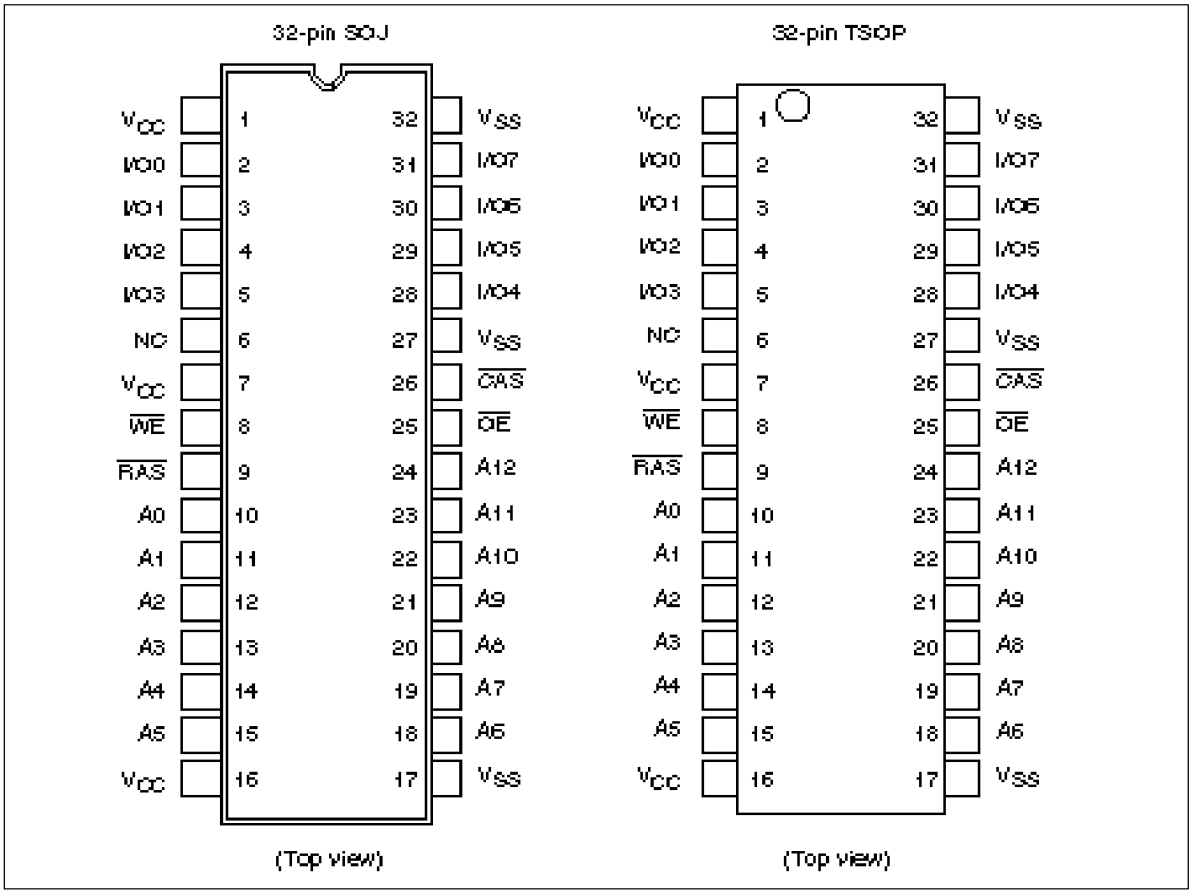
Hitachi semiconductor

- 4 variations of refresh
  - — RAS-only refresh
  - — CAS-before-RAS refresh
  - — Hidden refresh
  - — Self refresh (L-version)
- Battery backup operation (L-version)

Ordering Information

Type No.	Access time	Package
HM5164805FJ-5	50 ns	400-mil 32-pin plastic SOJ (CP-32DC)
HM5164805FJ-6	60 ns	
HM5164805FLJ-5	50 ns	
HM5164805FLJ-6	60 ns	
HM5165805FJ-5	50 ns	
HM5165805FJ-6	60 ns	
HM5165805FLJ-5	50 ns	
HM5165805FLJ-6	60 ns	
HM5164805FTT-5	50 ns	400-mil 32-pin plastic TSOP II (TTP-32DC)
HM5164805FTT-6	60 ns	
HM5164805FLTT-5	50 ns	
HM5164805FLTT-6	60 ns	
HM5165805FTT-5	50 ns	
HM5165805FTT-6	60 ns	
HM5165805FLTT-5	50 ns	
HM5165805FLTT-6	60 ns	

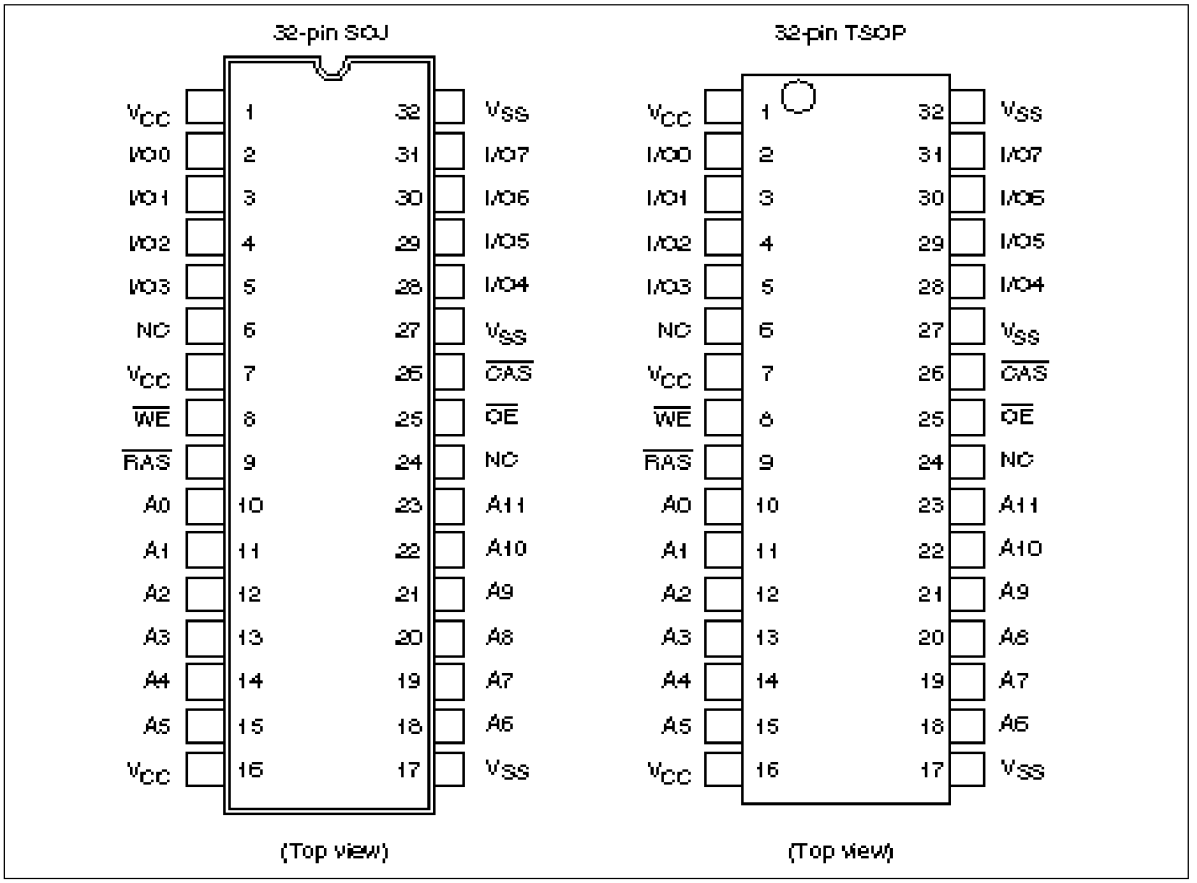
Pin Arrangement (HM5164805F Series)



Pin Description

Pin name	Function
A0 to A12	Address input — Row/Refresh address A0 to A12 — Column address A0 to A9
I/O0 to I/O7	Data input/output
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable
$\overline{OE}$	Output enable
V_{CC}	Power supply
V_{SS}	Ground
NC	No connection

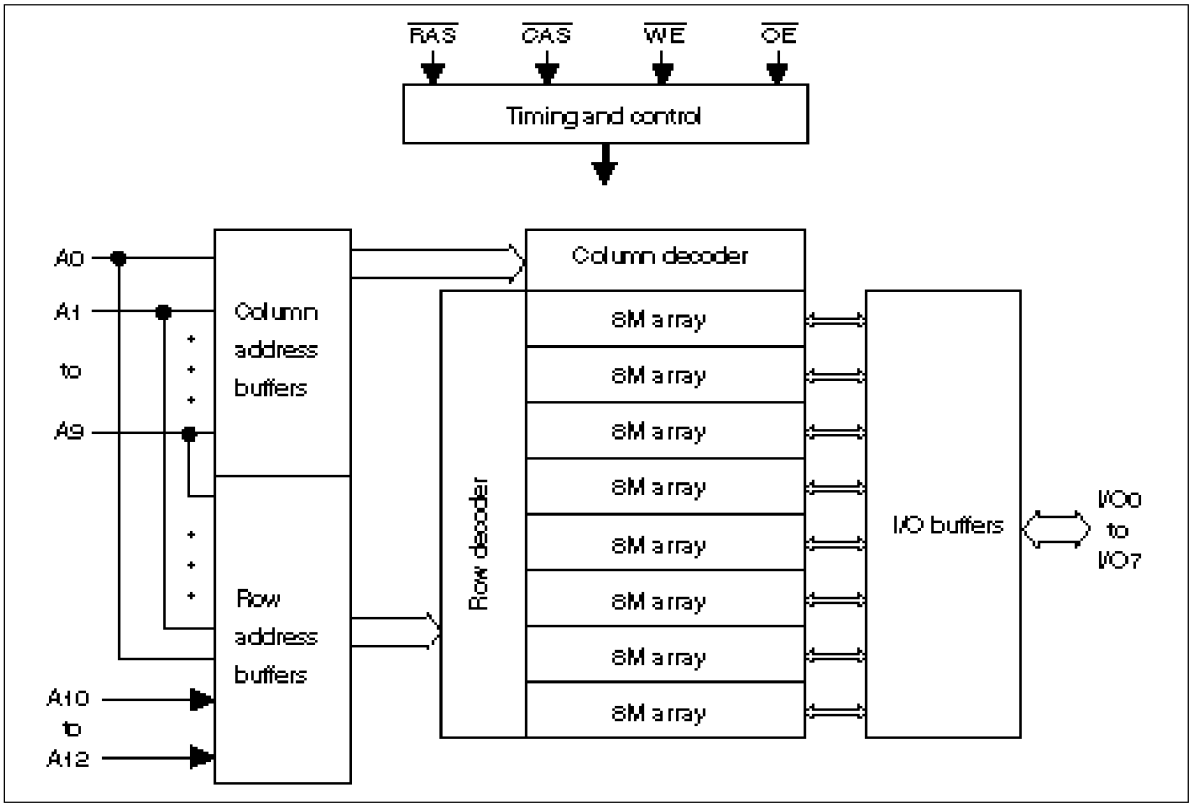
Pin Arrangement (HM5165805F Series)



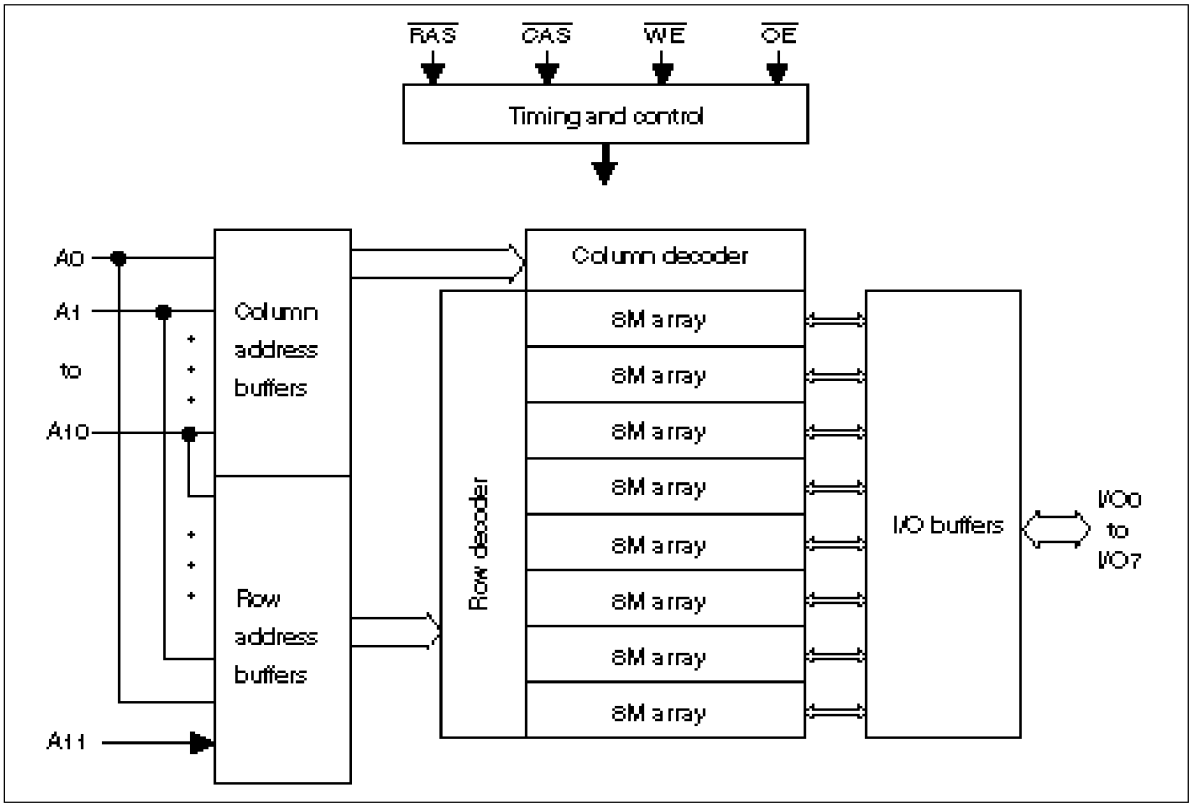
Pin Description

Pin name	Function
A0 to A11	Address input — Row/Refresh address A0 to A11 — Column address A0 to A10
I/O0 to I/O7	Data input/output
RAS	Row address strobe
CAS	Column address strobe
WE	Write enable
OE	Output enable
V_{CC}	Power supply
V_{SS}	Ground
NC	No connection

Block Diagram (HM5164805F Series)



Block Diagram (HM5165805F Series)



Operation Table

RAS	CAS	WE	OE	I/O 0 to I/O 7	Operation
H	×	×	×	High-Z	Standby
L	L	H	L	Dout	Read cycle
L	L	L*2	×	Din	Early write cycle
L	L	L*2	H	Din	Delayed write cycle
L	L	H to L	L to H	Dout/Din	Read-modify-write cycle
L	H	×	×	High-Z	RAS-only refresh cycle
H to L	L	H	×	High-Z	CAS-before-RAS refresh cycle or Self refresh cycle (L-version)
L	L	H	H	High-Z	Read cycle (Output disabled)

Notes: 1. H: V_{IH} (inactive), L: V_{IL} (active), ×: V_{IH} or V_{IL}
2. $t_{WCS} \geq 0$ ns: Early write cycle
$t_{WCS} < 0$ ns: Delayed write cycle

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Terminal voltage on any pin relative to V_{SS}	V_T	–0.5 to V_{CC} + 0.5 (4.6 V (max))	V
Power supply voltage relative to V_{SS}	V_{CC}	–0.5 to +4.6	V
Short circuit output current	Iout	50	mA
Power dissipation	P_T	1.0	W
Storage temperature	Tstg	–55 to +125	°C

DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply voltage	V_{CC}	3.0	3.3	3.6	V	1, 2
	V_{SS}	0	0	0	V	2
Input high voltage	V_{IH}	2.0	—	V_{CC} + 0.3	V	1
Input low voltage	V_{IL}	–0.3	—	0.8	V	1
Ambient temperature range	Ta	0	—	70	C	

Notes: 1. All voltage referred to V_{SS}.
2. The supply voltage with all V_{CC} pins must be on the same level. The supply voltage with all V_{SS} pins must be on the same level.

DC Characteristics (HM5164805F Series)

		HM5164805F					
		-5		-6			
Parameter	Symbol	Min	Max	Min	Max	Unit	Test conditions
Operating current*1, *2	I_{CC1}	—	115	—	105	mA	t_{RC} = min
Standby current	I_{CC2}	—	2	—	2	mA	TTL interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH} Dout = High-Z
		—	0.5	—	0.5	mA	CMOS interface $\overline{RAS}$, $\overline{CAS}$ V_{CC} – 0.2 V Dout = High-Z
Standby current (L-version)	I_{CC2}	—	TBD	—	TBD	µA	CMOS interface $\overline{RAS}$, $\overline{CAS}$ V_{CC} – 0.2 V Dout = High-Z
$\overline{RAS}$-only refresh current*2	I_{CC3}	—	115	—	105	mA	t_{RC} = min
Standby current*1	I_{CC5}	—	5	—	5	mA	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL} Dout = enable
$\overline{CAS}$-before-$\overline{RAS}$ refresh current	I_{CC6}	—	115	—	105	mA	t_{RC} = min
EDO page mode current*1, *3	I_{CC7}	—	110	—	100	mA	$\overline{RAS}$ = V_{IL} , $\overline{CAS}$ cycle, t_{HPC} = t_{HPC} min
Battery backup current*4 (Standby with CBR refresh) (L-version)	I_{CC10}	—	TBD	—	TBD	µA	CMOS interface Dout = High-Z CBR refresh: t_{RC} = 15.6 µs t_{RAS} 0.3 µs
Self refresh mode current (L-version)	I_{CC11}	—	TBD	—	TBD	µA	CMOS interface $\overline{RAS}$, $\overline{CAS}$ 0.2 V Dout = High-Z
Input leakage current	I_{LI}	–5	5	–5	5	µA	0 V Vin V_{CC} + 0.3 V
Output leakage current	I_{LO}	–5	5	–5	5	µA	0 V Vout V_{CC} Dout = disable
Output high voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	V	High Iout = –2 mA
Output low voltage	V_{OL}	0	0.4	0	0.4	V	Low Iout = 2 mA

Notes: 1. I_{CC} depends on output load condition when the device is selected. I_{CC} max is specified at the output open condition.
2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.
3. Measured with one sequential address change per EDO cycle, t_{HPC}.
4. V_{IH} V_{CC} – 0.2 V, 0 V V_{IL} 0.2 V.

(HM5165805F Series)

		HM5165805F					
				-6			
Parameter		**Min**	**Max**		**Max**	**Unit**	
Operating current*[1, 2]	I	—		—		mA	t = min
Standby current	CC2		2		2	mA	RAS, = V_{IH}
		—		—		mA	CMOS interface , CAS V_{CC} – 0.2 V
Standby current (L-version)	CC2	—	TBD		TBD	µA	RAS, V_{CC} – 0.2 V Dout = High-Z
RAS-only refresh current*[2]	I_{CC3}		135		115	mA	RC = min
[1]	I	—		—		mA	RAS IH, = V_{IL}
CAS-before- refresh current	CC6		135		115	mA	RC = min
[1, *]	I_{CC7}	—	110		100	mA	= V_{IL} CAS cycle, HPC = t min
Battery backup current* (Standby with CBR refresh) (L-version)	CC10		TBD		TBD	µA	Dout = High-Z CBR refresh: t = 15.6 µs 0.3 µs RAS
(L-version)	I	—		—		µA	CMOS interface , CAS 0.2 V Dout = High-Z
Input leakage current	I_{LI}	5	5	–5	5	µA	Vin V_{CC}
Output leakage current	I	–	5	5	5		0 V Vout CC Dout = disable
	V_{OH}		V_{CC}		V_{CC}		High Iout = 2 mA
Output low voltage	OL	0		0	0.4		Low Iout = 2 mA

Notes: I_{CC} CC max is specified at the

2. Address can be changed onc RAS = V .
3. HPC.

V_{IH} V_{CC} – 0.2 V, 0 V V_{IL} 0.2 V.

Capacitance (Ta = 25 C, V_{CC} = 3.3 V ± 0.3 V)

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address)	C_{I1}	—	5	pF	1
Input capacitance (Clocks)	C_{I2}	—	7	pF	1
Output capacitance (Data-in, Data-out)	$C_{I/O}$	—	7	pF	1, 2

Notes : 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{RAS}$ and $\overline{CAS}$ = V_{IH} to disable Dout.

AC Characteristics

= 3.3 V ± 0.3 V, V_{SS} [1, *] [*19]

- Input rise and fall time: 2 ns
  Input pulse levels: V_{IL} = 0 V, V = 3.0 V
- Input timing reference levels: 0.8 V, 2.0 V

- Output load: 1 TTL gate + C_L (100 pF) (Including scope and jig)

Read, Write, Read-Modify-Write and Refresh Cycles (Common parameters)

		HM5164805F/HM5165805F					
		-5		-6			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Random read or write cycle time	t_{RC}	84	—		—	ns	
RAS precharge time	t_{RP}	30	—		—	ns	
CAS precharge time	t_{CP}	8	—		—	ns	
RAS pulse width	t_{RAS}	50	10000	60	10000	ns	
CAS pulse width	t_{CAS}	8	10000	10	10000	ns	
Row address setup time	t_{ASR}	0	—		—	ns	
Row address hold time	t_{RAH}	8	—		—	ns	
Column address setup time	t_{ASC}	0	—		—	ns	
Column address hold time	t_{CAH}	8	—		—	ns	
RAS to CAS delay time	t_{RCD}	12	37	14	45	ns	3
RAS to column address delay time	t_{RAD}	10	25	12	30	ns	4
RAS hold time	t_{RSH}	13	—		—	ns	
CAS hold time	t_{CSH}	35	—		—	ns	
CAS to RAS precharge time	t_{CRP}	5	—		—	ns	
OE to Din delay time	t_{OED}	13	—		—	ns	5
OE delay time from Din	t_{DZO}	0	—		—	ns	6
CAS delay time from Din	t_{DZC}	0	—		—	ns	6
Transition time (rise and fall)	t_T	2	50	2	50	ns	7

Read Cycle

Parameter			HM5164805F/HM5165805F -6 Min	-6 Max	-7 Max	Unit	
Access time from RAS		t_{RAC}		50	60	ns	
Access time from CAS		t_{CAC}		13	15	ns	
Access time from address		t_{AA}	—		—	ns	9, 11, 17
	OE	t_{OAC}	—		—	ns	9
		t_{RCS}		—	—		
Read command hold time to CAS		t_{RCH}	0	—	0	ns	12
	RAS	t_{RRH}	50		60	ns	
Read command hold time to		t_{RRH}		—	—		12
Column address to	lead time	t_{RAL}	25		30	ns	
Column address to	lead time	t_{CAL}	15		18	ns	
CAS		t_{CLZ}		—	—		
Output data hold time		t_{OH}	3		3	ns	21
	OE	t_{OEH}	3		3	ns	
Output buffer turn-off time		t_{OFF}		13	15	ns	
Output buffer turn-off to OE		t_{OEZ}		13	15	ns	
CAS to Din delay time		t_{CDD}	13	—	15	ns	5
	RAS	t_{DZC}	3		3	ns	21
	RAS	t_{DZC}	—		—	ns	13, 21
	WE	t_{DZC}	—		—	ns	13
to Din delay time		t_{DZO}	13		15	ns	
RAS		t_{RDD}		—	—		

Write Cycle

Parameter	Symbol	HM5164805F/HM5165805F -5 Min	-5 Max	-6 Min	-6 Max	Unit	Notes
Write command setup time	t_{WCS}	0	—	0	—	ns	14
Write command hold time	t_{WCH}	8		10		ns	
Write command pulse width	WP	8	—	10		ns	
Write command to lead time	t	13		15		ns	
Write command to lead time	t	8		10		ns	
Data-in setup time	DS	0	—	0		ns	15
	t_{DH}		—		—		15

Read-Modify-Write Cycle

	Symbol	-5 Min	-5 Max	-6 Min	-6 Max		Notes
Read-modify-write cycle time	RWC	116	—	140		ns	
RAS WE delay time	RWD	67	—	79		ns	14
to WE	t_{CWD}		—		—		14
Column address to delay time	t	42		49		ns	14
hold time from WE	OEH		—		—		

Refresh Cycle

Parameter		HM5164805F/HM5165805F -5 Min	-5 Max	-6 Min	-6 Max	Unit
CAS setup time (CBR refresh cycle)	CSR	5	—	5		ns
CAS	t_{CHR}		—		—	
WE setup time (CBR refresh cycle)	WRP	0	—	0		ns
WE	t_{WRH}		—		—	
RAS precharge to hold time	t	5		5		ns

EDO Page Mode Cycle

	Symbol	-5 Min		-6 Min	-6 Max		Notes
EDO page mode cycle time	HPC	20	—	25		ns	20
RAS pulse width	RASP		100000		100000	ns	
Access time from CAS	t_{CPA}	—	28		35	ns	
RAS hold time from precharge	t	28		35		ns	
Output data hold time from low	t	3		3		ns	9, 22
hold time referred OE	COL	8	—	10		ns	
CAS OE setup time	COP	5	—	5		ns	
Read command hold time from precharge	t	28		35		ns	
Write pulse width during precharge	t	8		10		ns	
OE	t_{OEP}		—		—		

EDO Page Mode Read-Modify-Write Cycle

Parameter		HM5164805F/HM5165805F -6 Min	Max		-6 Max	Unit	
EDO page mode read-modify-write cycle time	HPRWC	57	—	68		ns	
WE CAS precharge	CPW	45	—	54		ns	14

(HM5164805F Series)

Parameter		Max	Unit
Refresh period	t	64	ms

Refresh (HM5165805F Series)

	Symbol	Max	Notes
Refresh period	REF	64	4096 cycles

(L-version)

		HM5164805FL/HM5165805FL				
		-6				
Parameter		Min	Max		Max	Unit
RAS pulse width (self refresh)	t_{RASS}	100	—	100		µs	25
precharge time (self refresh)	t	90		110		ns	25
hold time (self refresh)	t	–	—	–50		ns	

Notes: AC measurements assume t_T

2. An initial pause of 200 µs is required after power up followed by a minimum of eight initialization RAS-only refresh or -before-RAS
3. Operation with the t (max) limit insures that t_{RAC} $_{RCD}$ (max) is specified as $_{RCD}$ is greater than the specified t (max) limit, than the access time is controlled exclusively by t .
4. $_{RAD}$ (max) limit insures that t (max) can be met, t_{RAD} a reference point only; if t_{RAD} $_{RAD}$ (max) limit, then access time is $_{AA}$.

   Either t_{OED} $_{CDD}$ must be satisfied.

   Either t_{DZO} $_{DZC}$ must be satisfied.

   V_{IH} $_{IL}$ (max) are reference levels for measuring timing of input signals. Also, transition t $_{IH}$ (min) and V (max).
8. $_{RCD}$ (max) and t_{RAD} t_{RAD} (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
9. Measured with a load circuit equivalent to 1 TTL loads and 100 pF.
10. Assumes that t_{RCD} t (max) and t_{RCD} $_{CAC}$ + t_{AA}
11. Assumes that t t_{RAD} $_{RCD}$ + t (max) t_{RAD} $_{AA}$ (max).

    Either t_{RCH} $_{RRH}$ must be satisfied for a read cycles.

    t_{OFF} $_{OEZ}$ (max), t (max) and t_{OFR} the open circuit condition and are not referred to output voltage levels.
14. $_{WCS}$, t , t_{CWD} $_{AWD}$ and t are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if t t_{WCS} and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if t_{RWD} t_{RWD} (min), t_{CWD} t (min), and t_{AWD} t_{AWD} (min), or t_{CWD} t (min), t_{AWD} t_{AWD} (min) and t_{CPW} t (min), the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the
15. t and t_{DH} CAS leading edge in early write cycles and to leading edge in delayed write or read-modify-write cycles.

    t_{RASP} RAS pulse width in EDO page mode cycles.

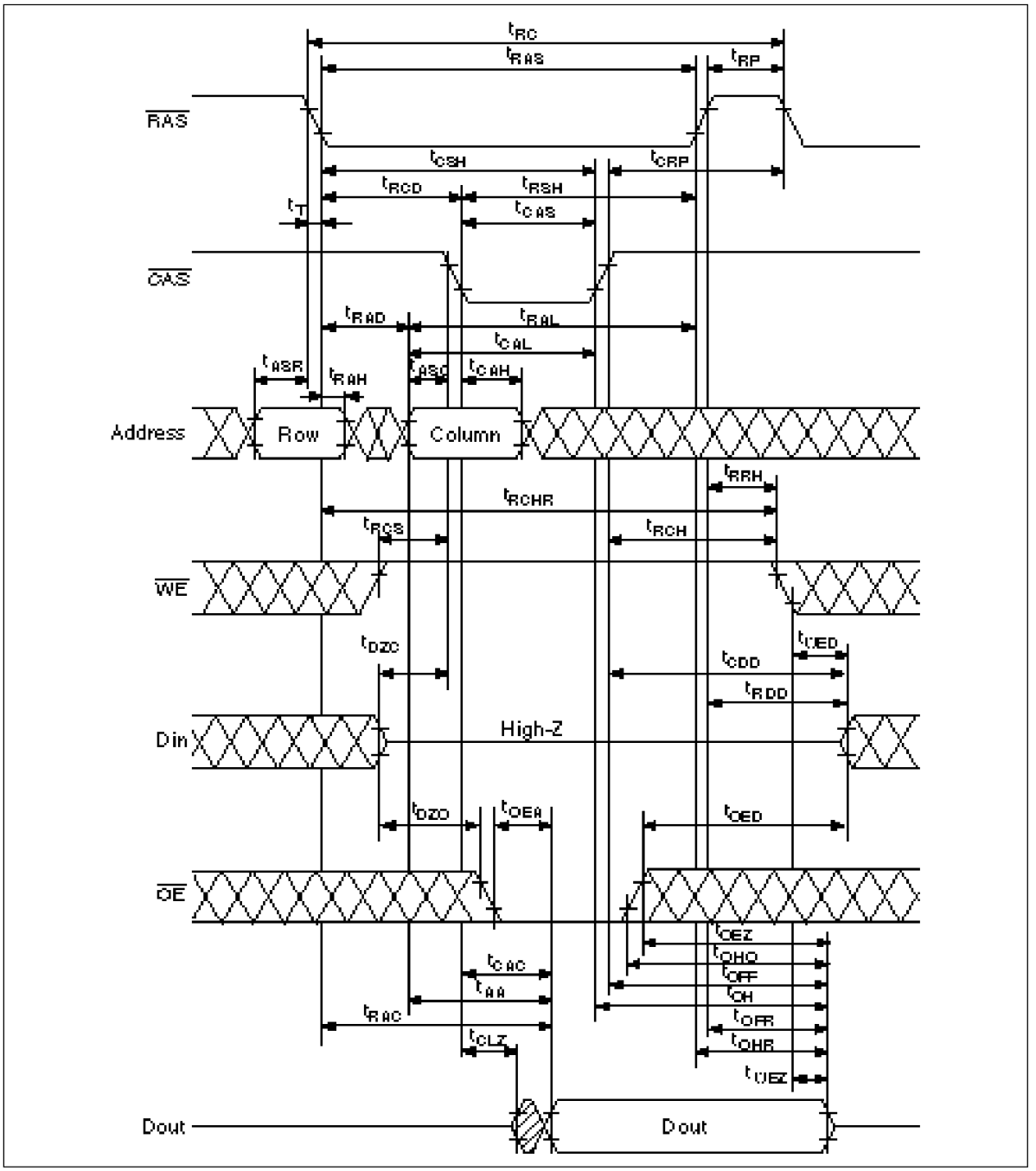
    Access time is determined by the longest among t_{AA} $_{CAC}$ and t .
18. OE must disable output buffer prior to applying data
19. When output buffers are enabled once, sustain the low impedance state until valid data is

    large V_{CC} $_{SS}$ line noise, which causes to degrade V min/V_{IL}

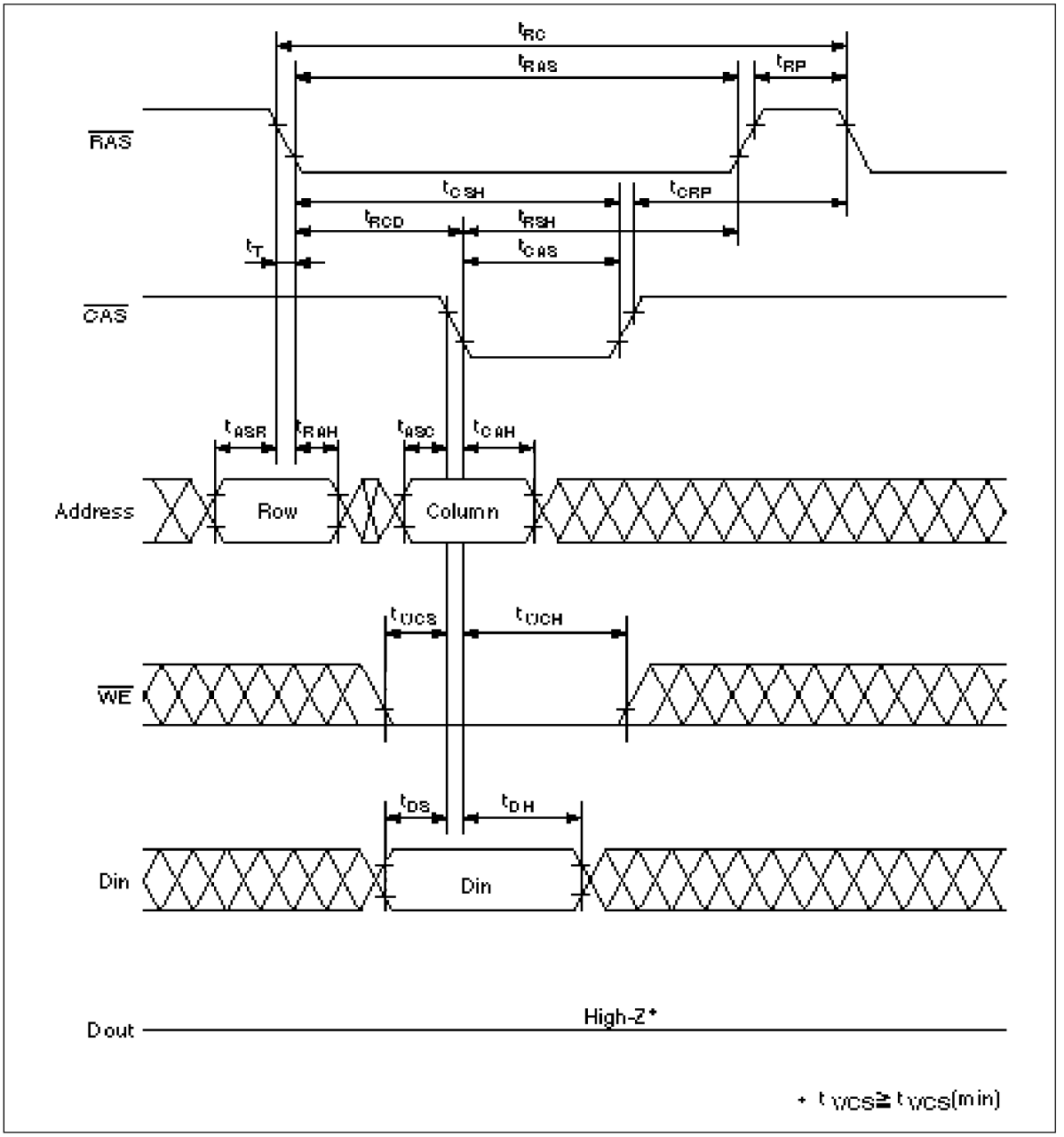
20. t_{HPC} (min) can be achieved during a series of EDO page mode write cycles or EDO page mode read cycles. If both write and read operation are mixed in a EDO page mode RAS cycle (EDO page mode mix cycle (1), (2)), minimum value of CAS cycle (t_{CAS} + t_{CP} + 2 t_T) becomes greater than the specified t_{HPC} (min) value. The value of CAS cycle time of mixed EDO page mode is shown in EDO page mode mix cycle (1) and (2).
21. Data output turns off and becomes high impedance from later rising edge of RAS and CAS. Hold time and turn off time are specified by the timing specifications of later rising edge of RAS and CAS between t_{OHR} and t_{OH} and between t_{OFR} and t_{OFF}.
22. t_{DOH} defines the time at which the output level go cross. V_{OL} = 0.8 V, V_{OH} = 2.0 V of output timing reference level.
23. Before and after self refresh mode, execute CBR refresh to all refresh addresses in or within 64 ms period on the condition a and b below.
    a. Enter self refresh mode within 15.6 µs after either burst refresh or distributed refresh at equal interval to all refresh addresses are completed.
    b. Start burst refresh or distributed refresh at equal interval to all refresh addresses within 15.6µs after exiting from self refresh mode.
24. In case of entering from RAS-only-refresh, it is necessary to execute CBR refresh before and after self refresh mode according as note 23.
25 At t_{RASS} > 100 µs, self refresh mode is activated, and not activated at t_{RASS} < 10 µs. It is undefined within the range of 10 µs t_{RASS} 100 µs. For t_{RASS} 10 µs, it is necessary to satisfy t_{RPS}.
26. XXX: H or L (H: V_{IH} (min) V_{IN} V_{IH} (max), L: V_{IL} (min) V_{IN} V_{IL} (max))
    ///////: Invalid Dout
    When the address, clock and input pins are not described on timing waveforms, their pins must be applied V_{IH} or V_{IL}.

Timing Waveforms*[26]

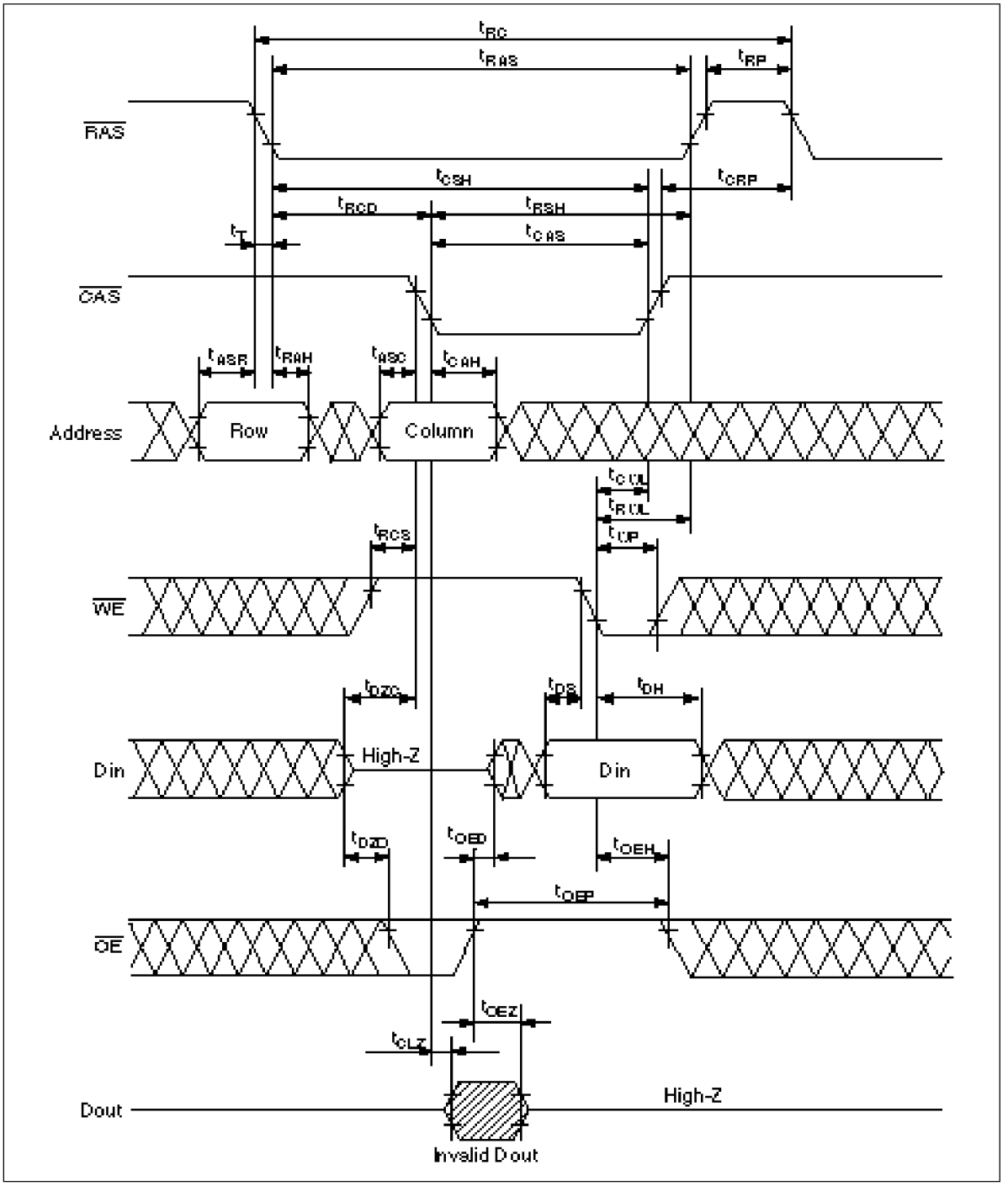
Read Cycle



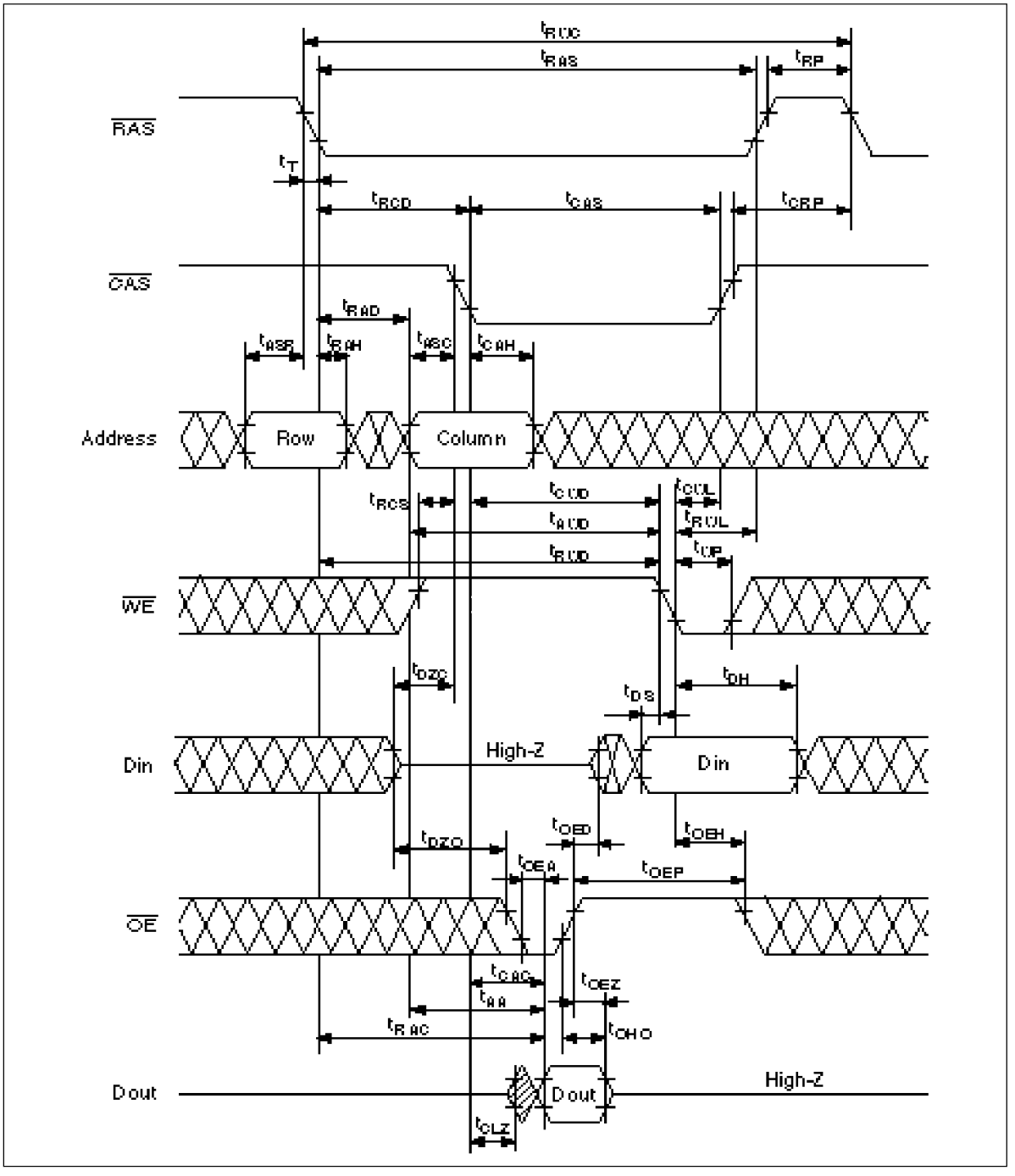
Early Write Cycle



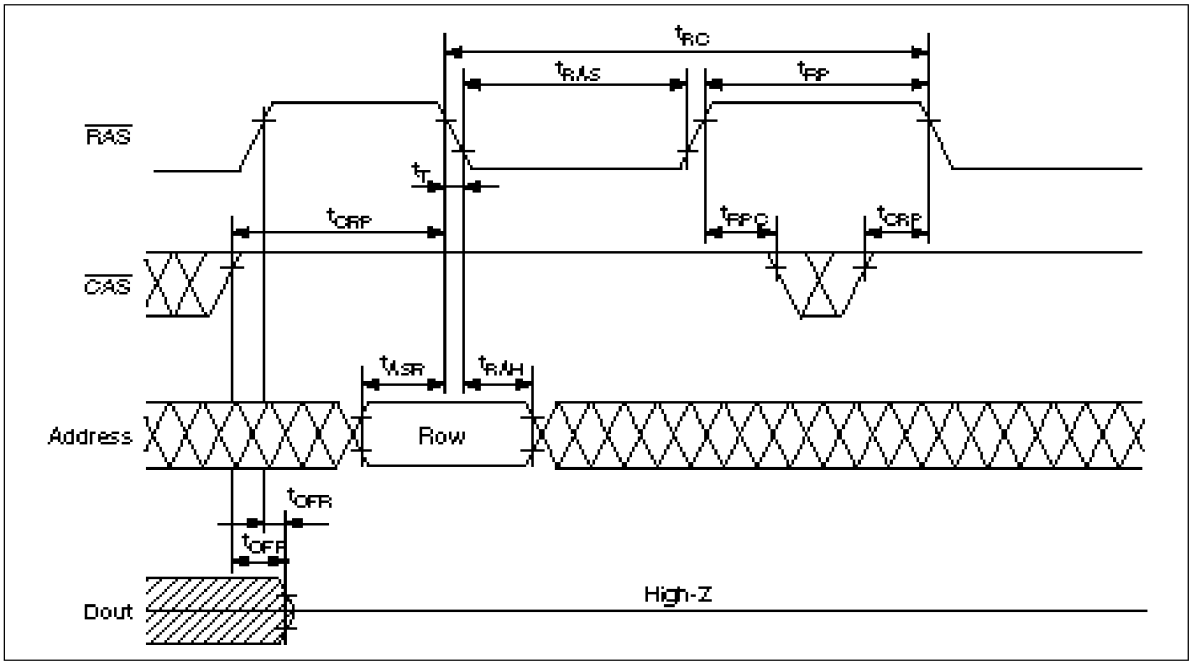
Delayed Write Cycle [18]



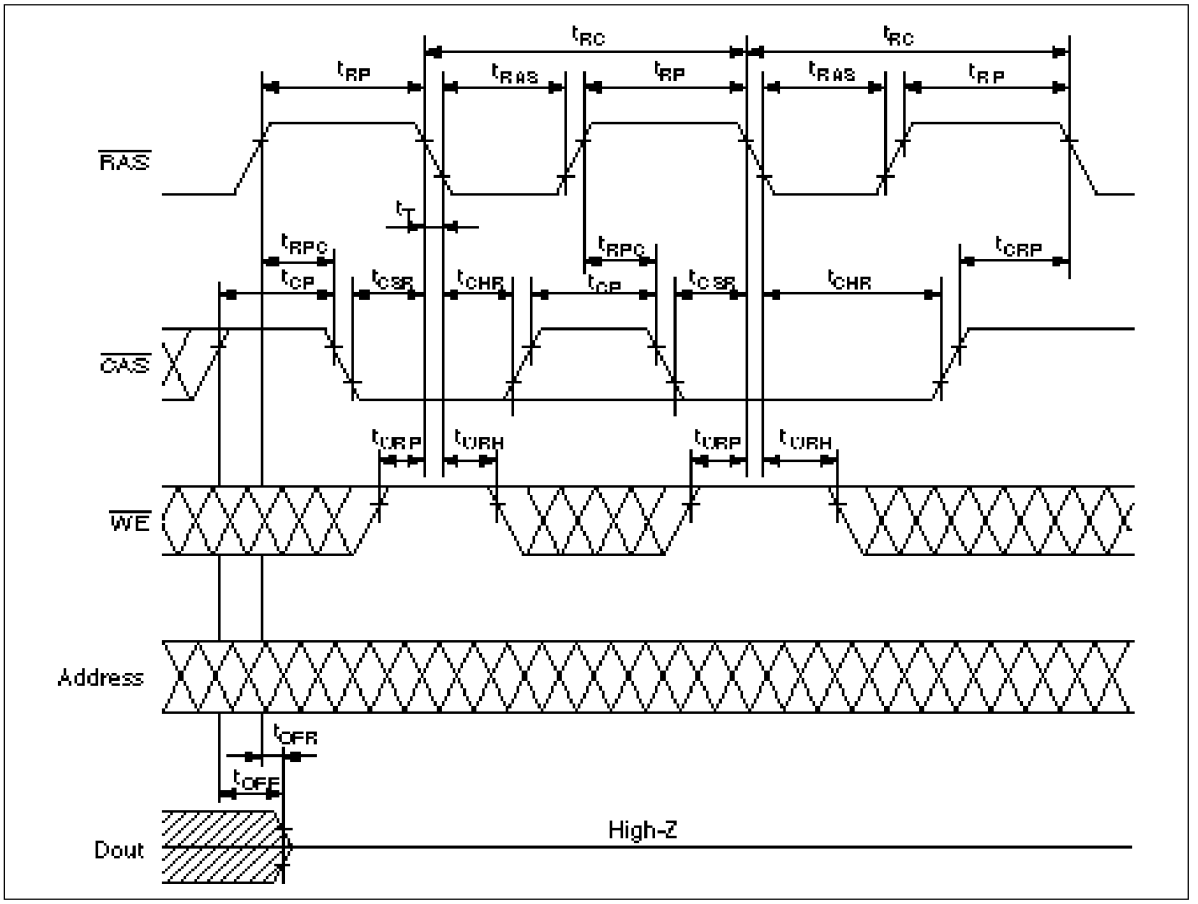
Read-Modify-Write Cycle [18]



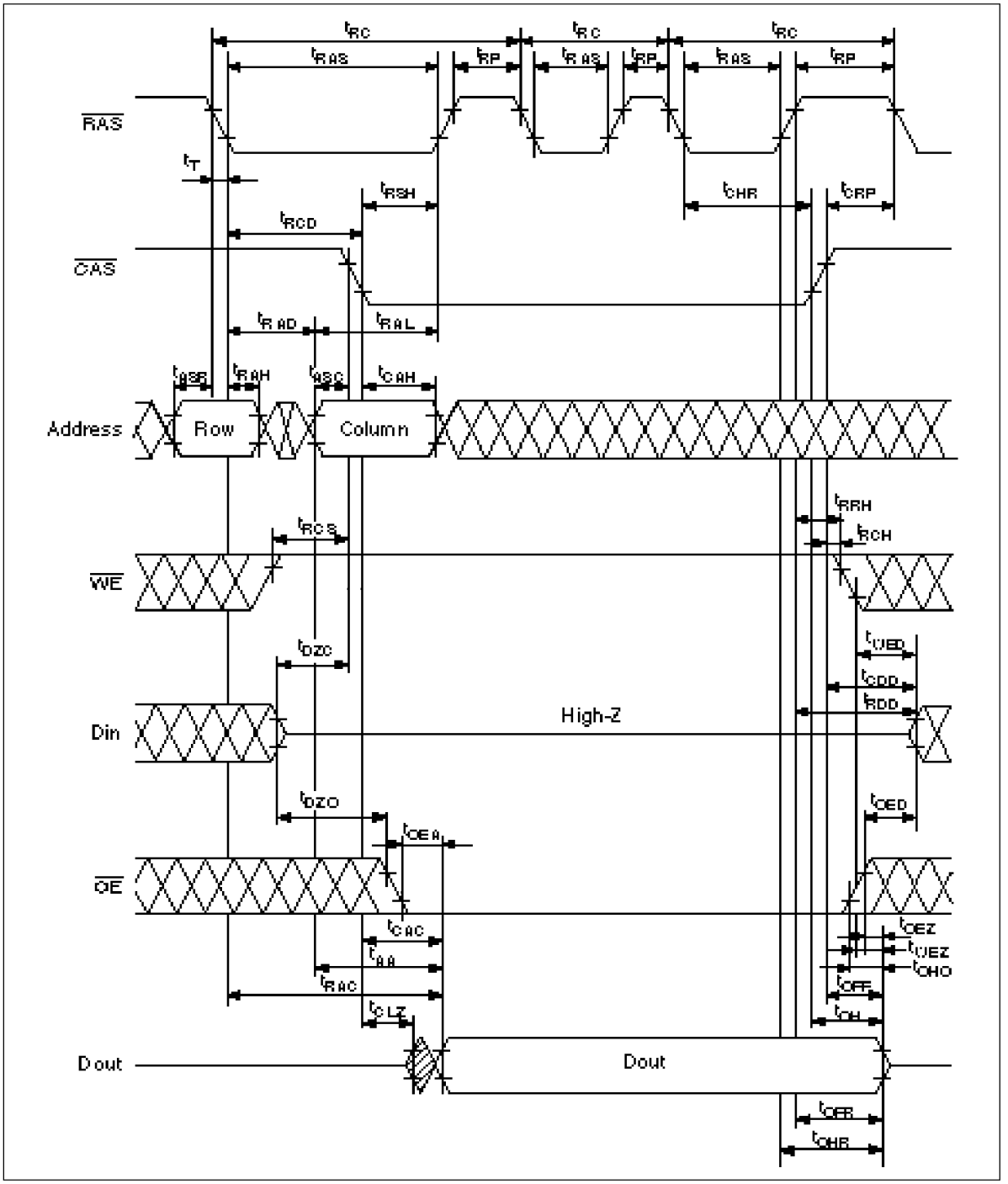
RAS-Only Refresh Cycle



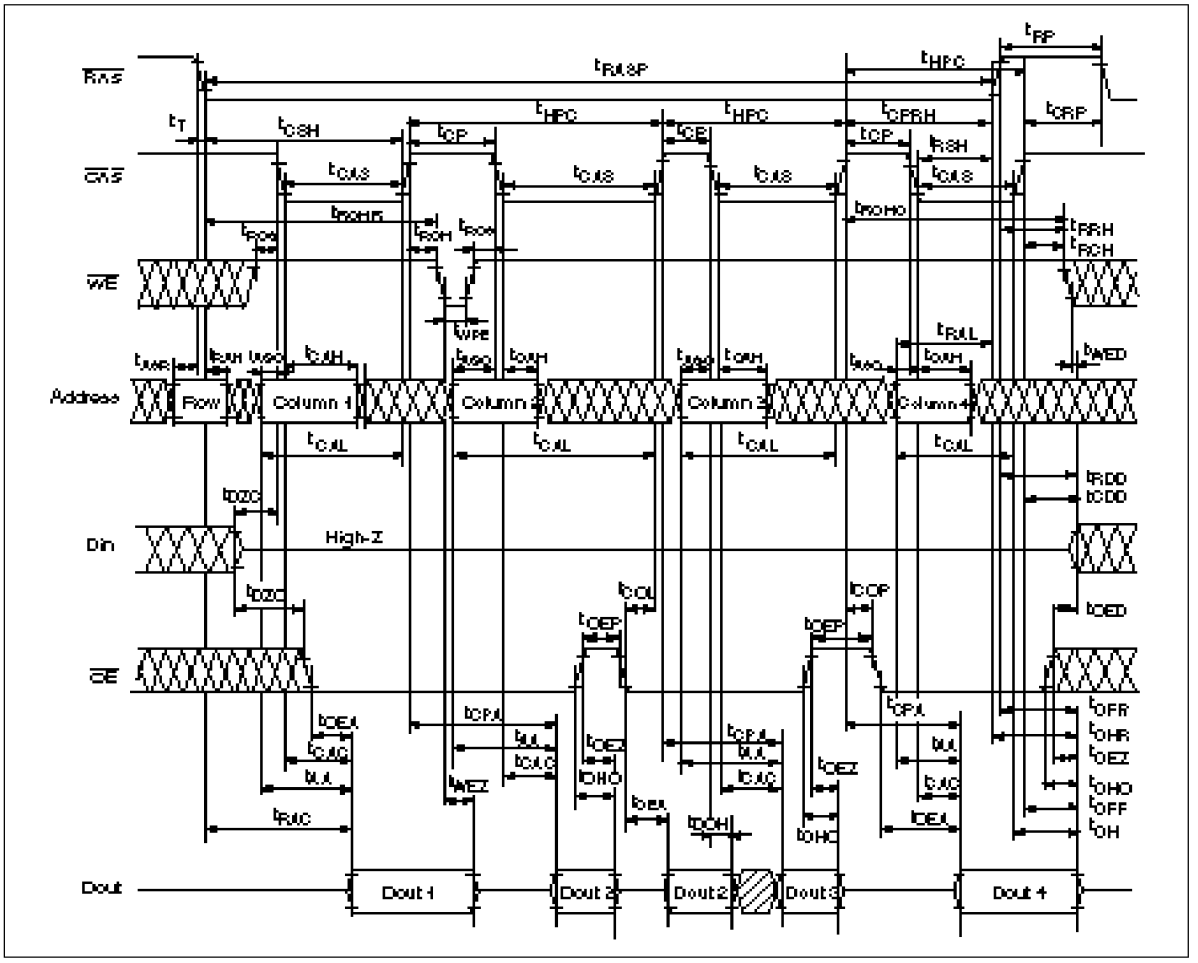
CAS-Before-RAS Refresh Cycle



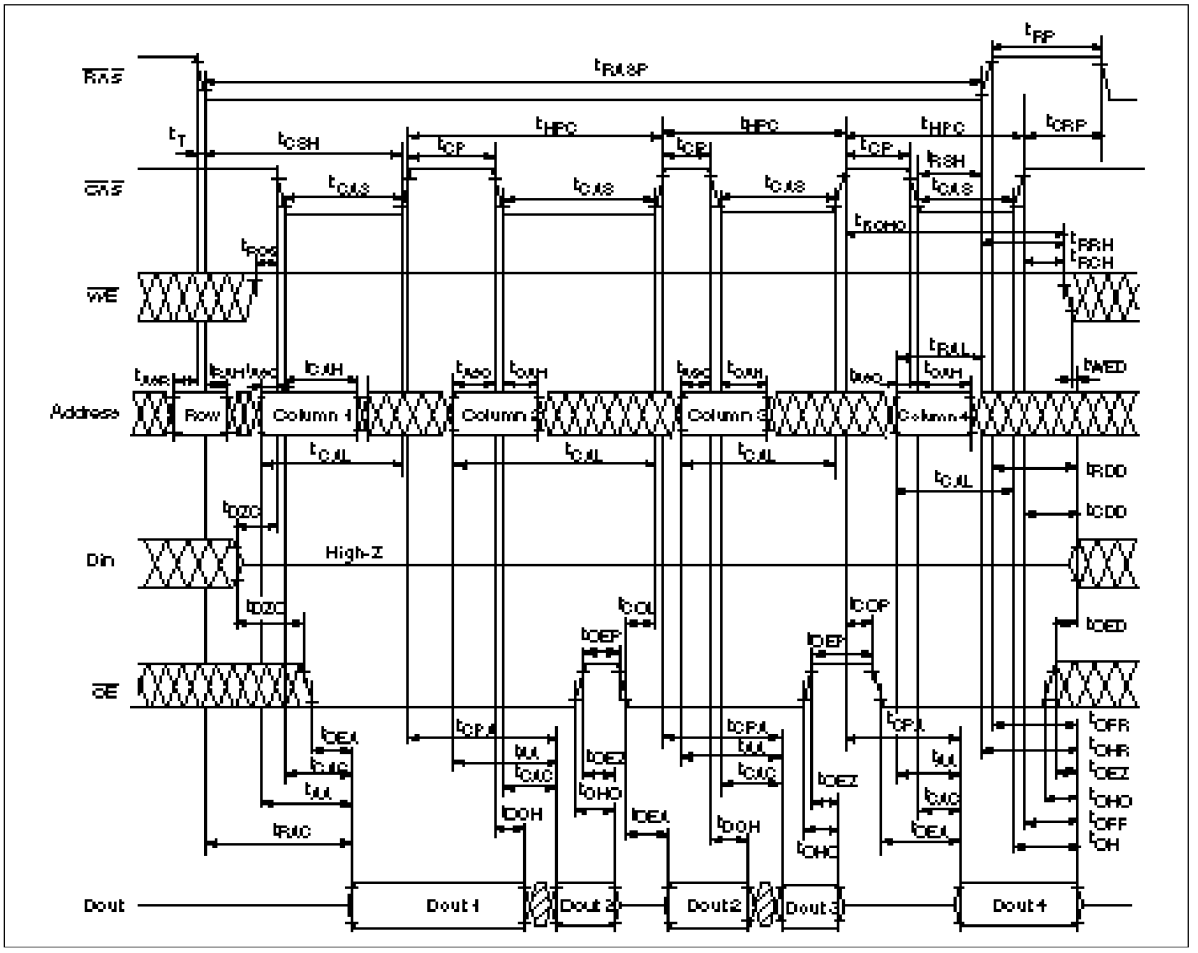
Hidden Refresh Cycle



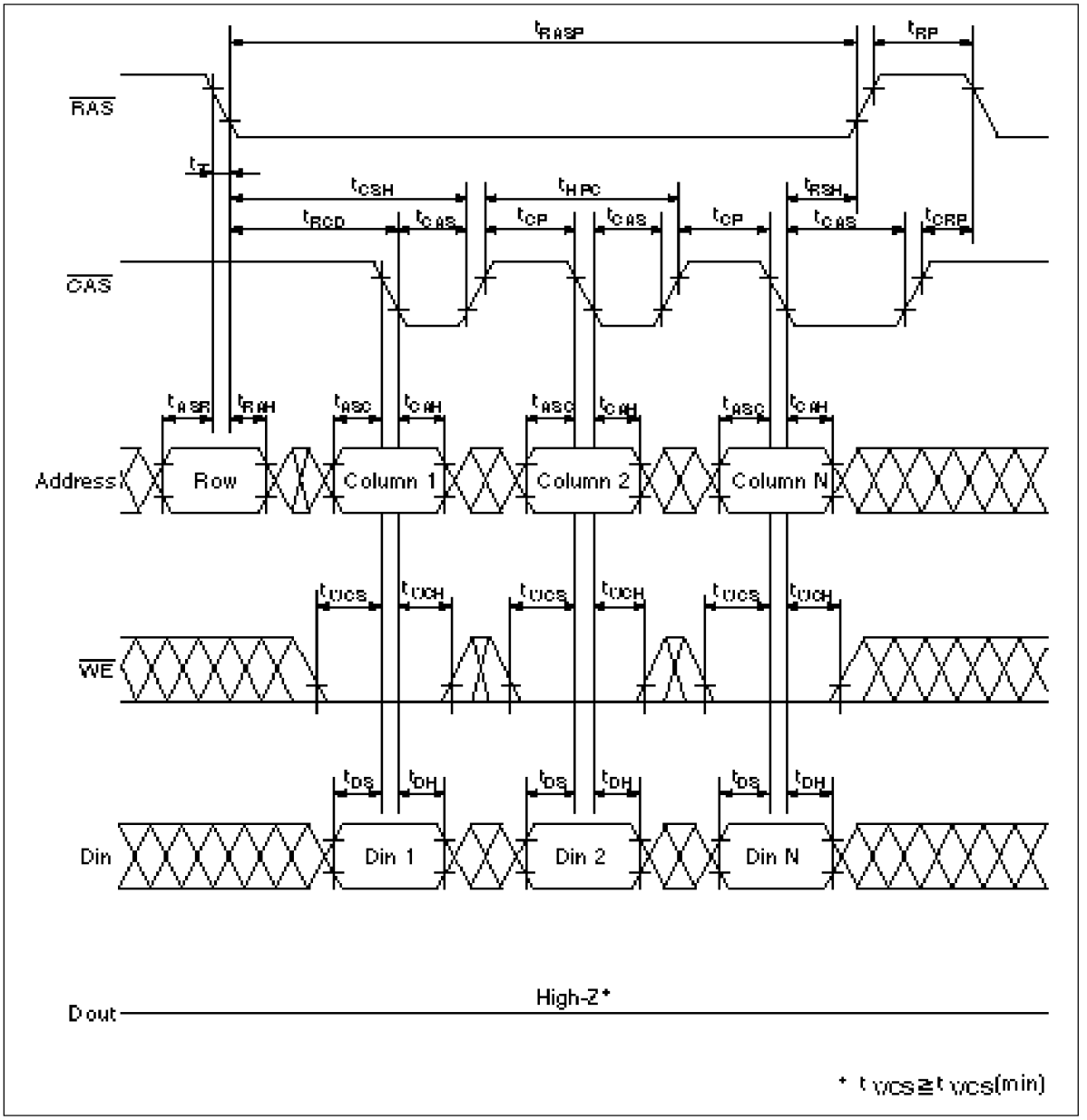
EDO Page Mode Read Cycle (1)



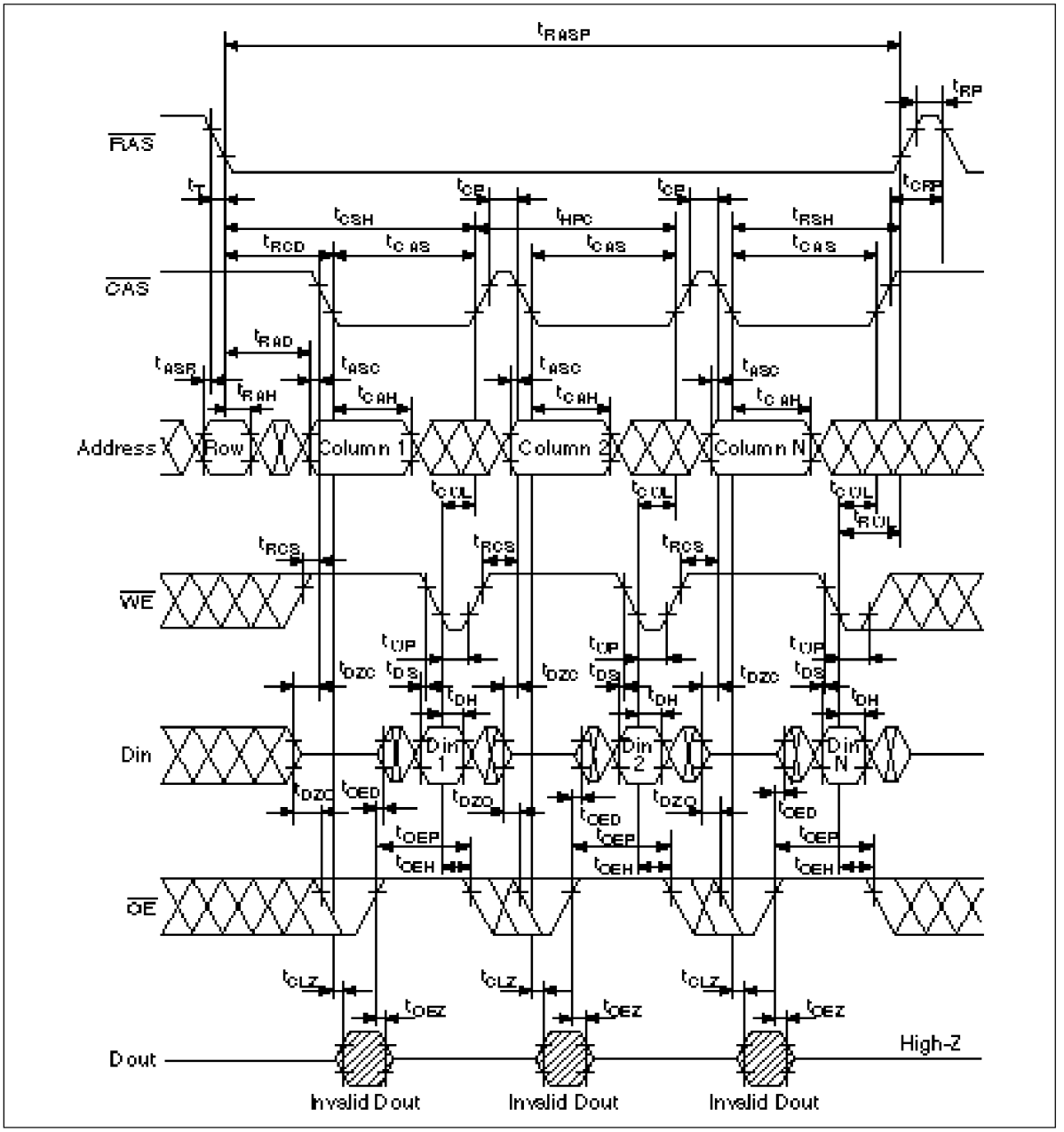
EDO Page Mode Read Cycle (2)



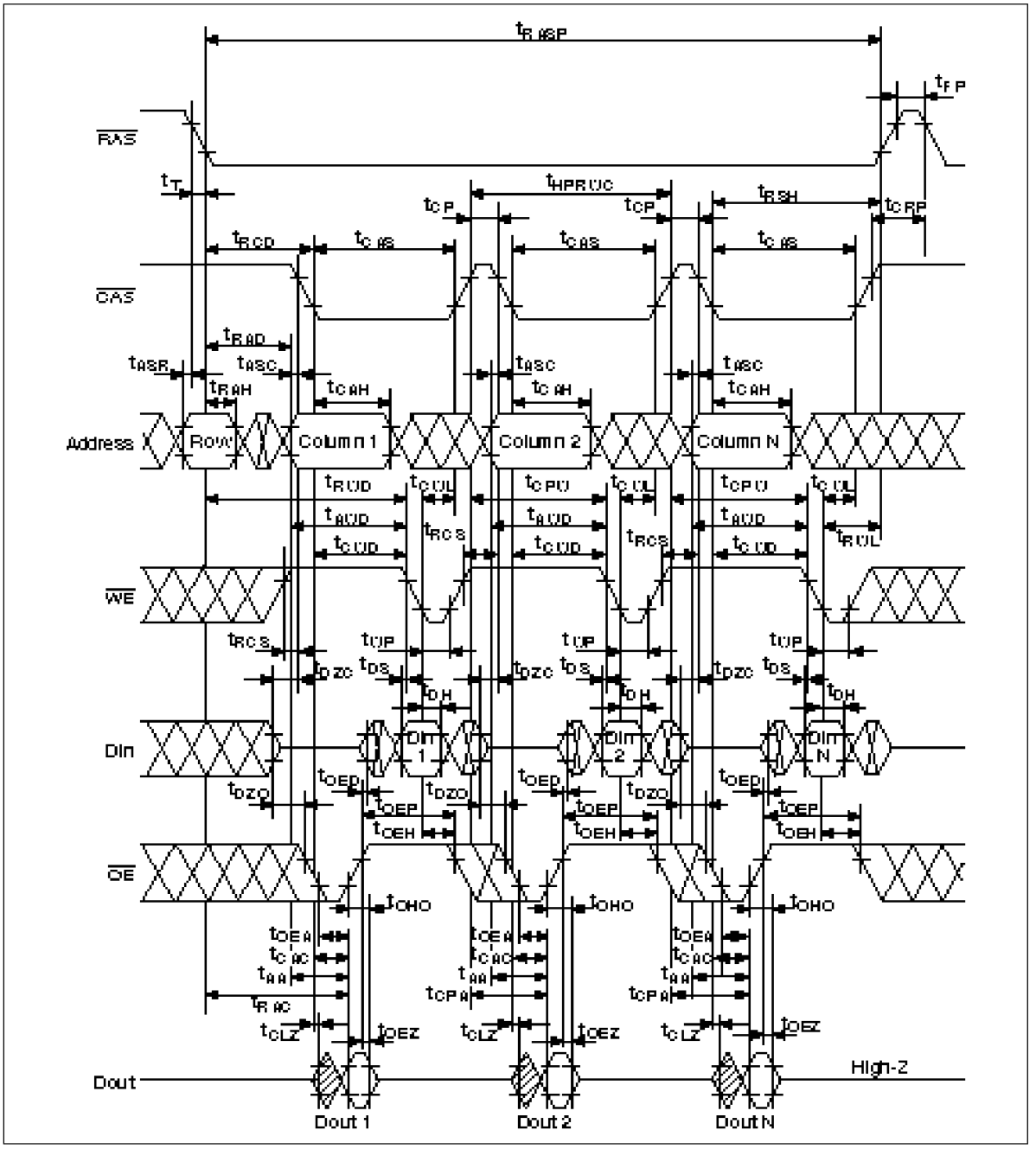
EDO Page Mode Early Write Cycle



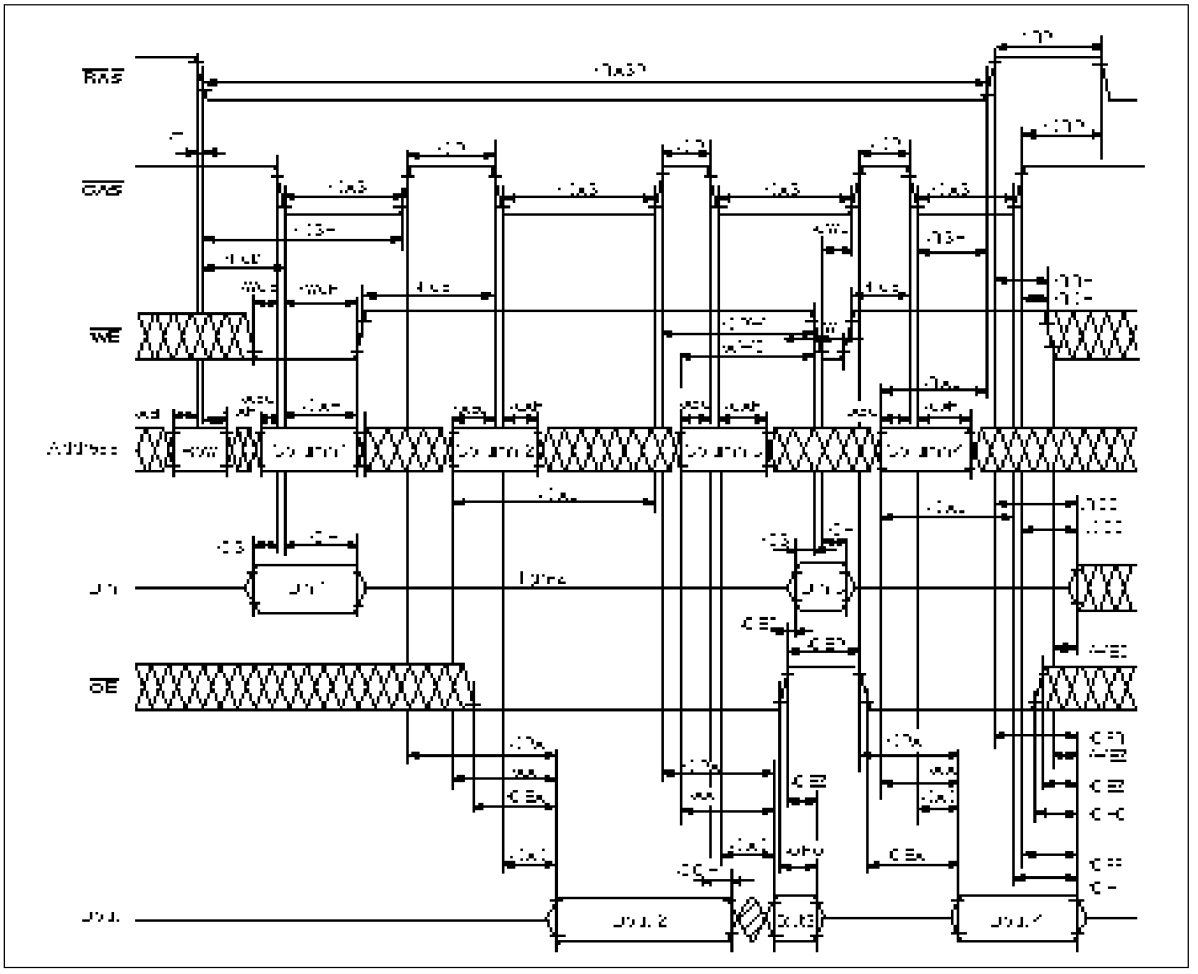
EDO Page Mode Delayed Write Cycle[*18]



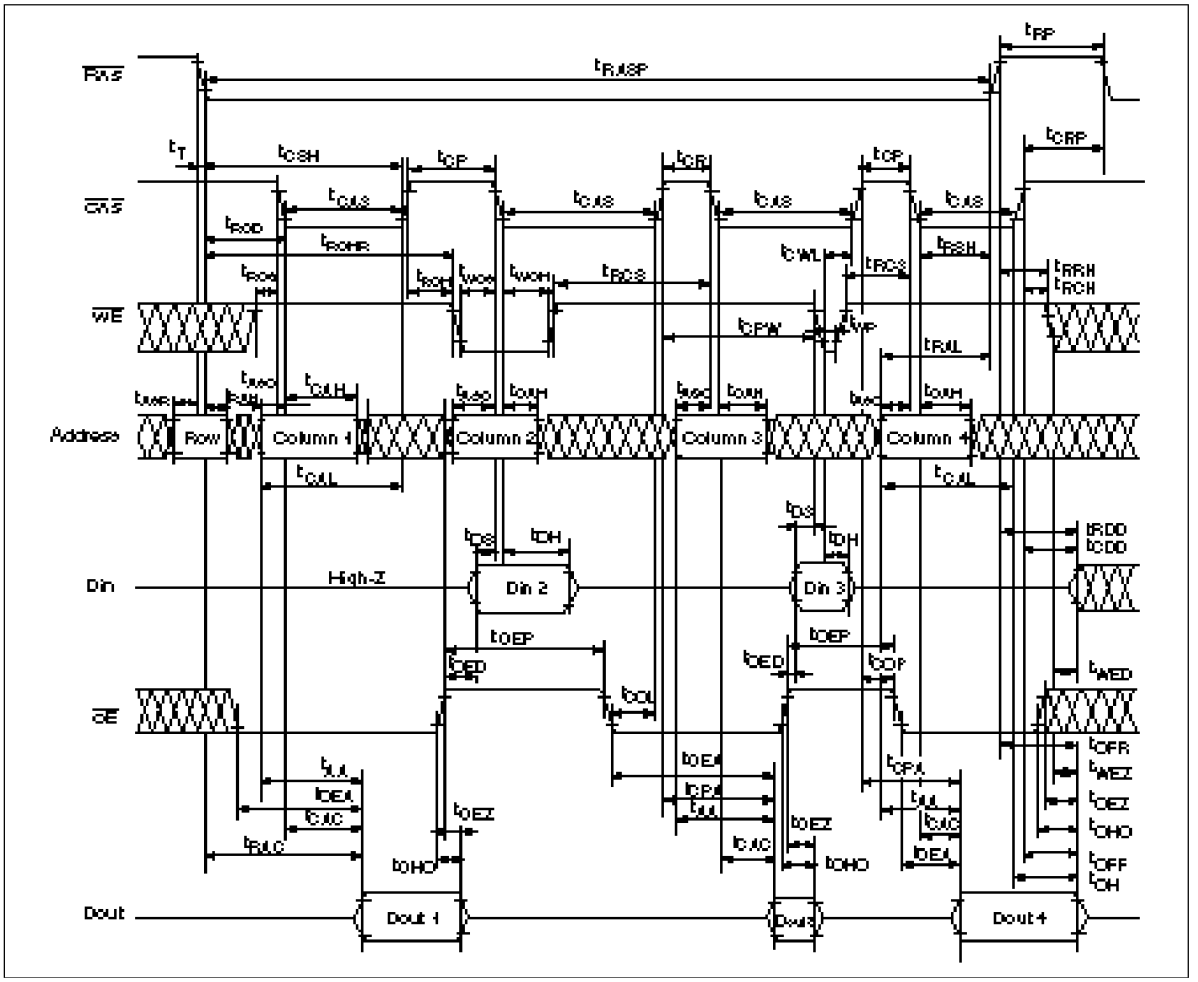
EDO Page Mode Read-Modify-Write Cycle[*18]



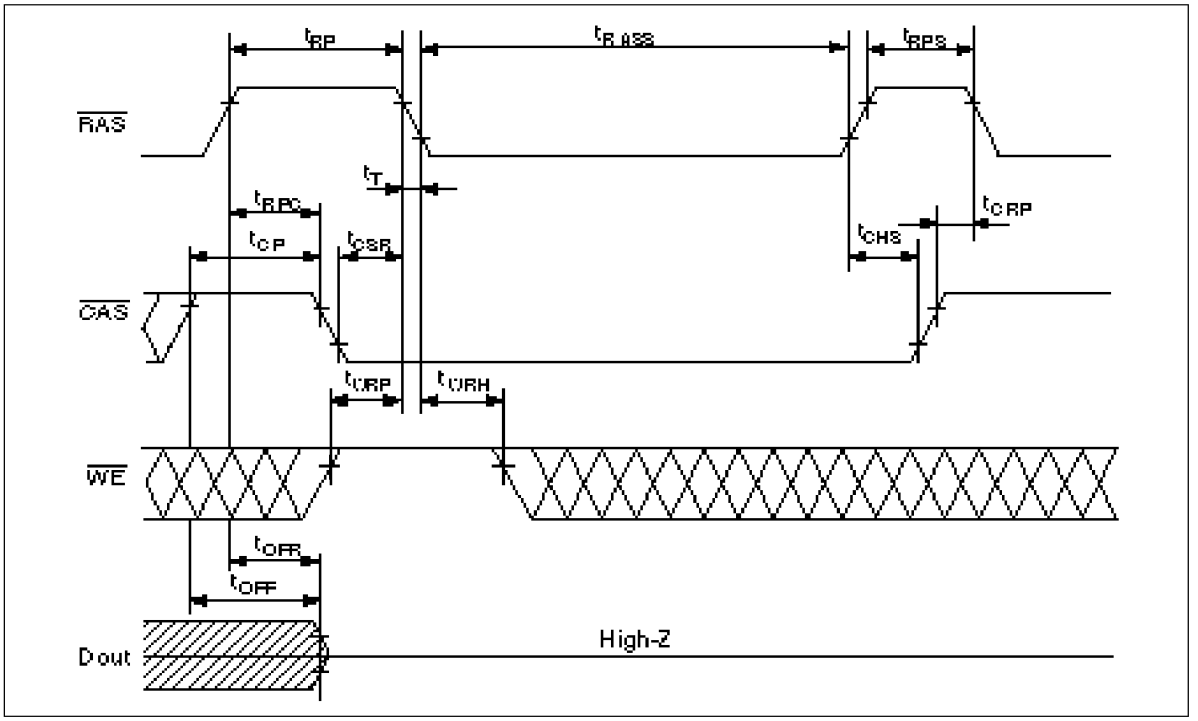
EDO Page Mode Mix Cycle (1)*[20]



EDO Page Mode Mix Cycle (2) *[20]

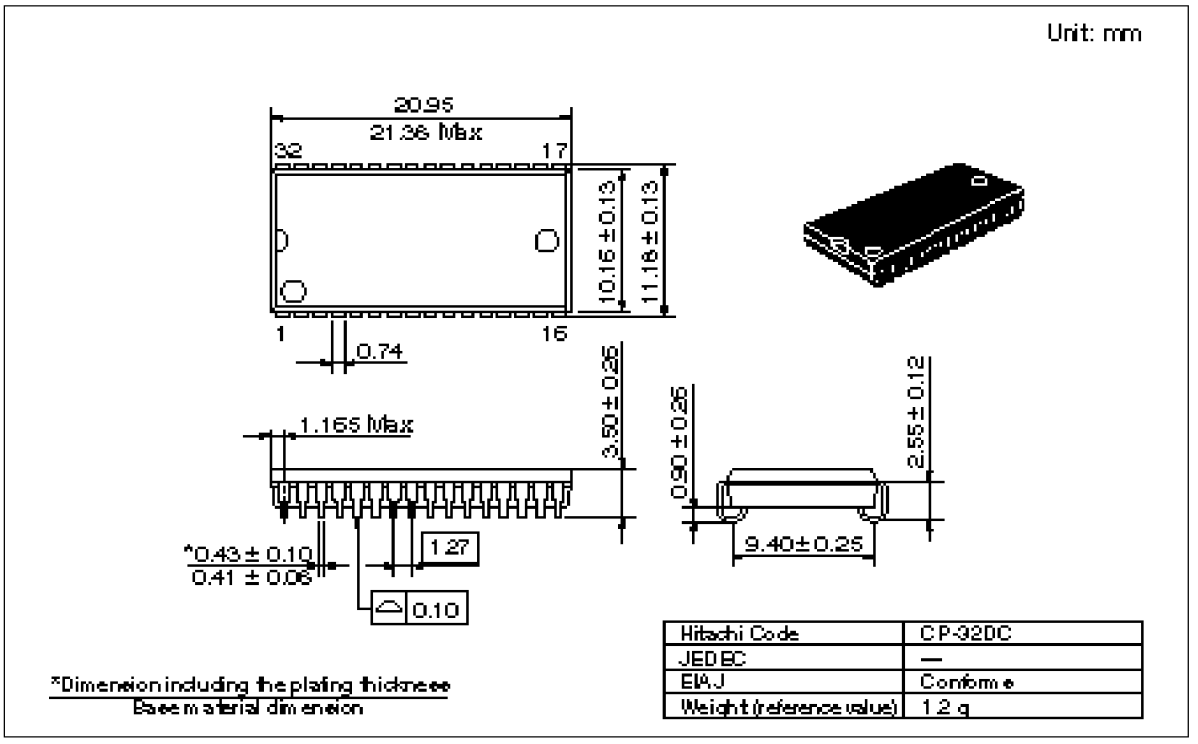


Self Refresh Cycle (L-version)* [23, 24, 25]



Package Dimensions

HM5164805FJ/ FLJ Series
HM5165805FJ/ FLJ Series (CP-32DC)



HM5164805FTT/FLTT Series
HM5165805FTT/FLTT Series (TTP-32DC)