



HV72

Product Objective Specification

40-Channel Symmetric Row Driver

Ordering Information

Device	Package Options			
	80-Lead Ceramic Gullwing	64-Lead 3-Sided Plastic Gullwing	Die in wafer pack	80-Lead Ceramic Gullwing (MIL-STD-883 Processed*)
HV7225	HV7225DG	HV7225PG	HV7225X	RBHV7225DG

* For Hi-Rel process flows, refer to page 5-3 of the Databook.

Features

- ☐ Processed with HVCMOS® technology
- ☐ Symmetric row drive (reduces latent imaging in ACTFEL displays)
- ☐ Output voltage up to 250V
- ☐ Low-power level shifting
- ☐ Source/Sink current 100mA (max.)
- ☐ Shift Register Speed 4MHz
- ☐ Pin-programmable shift direction (DIR, SHIFT)
- ☐ Hi-Rel processing available

Absolute Maximum Ratings

Supply voltage, V_{DD}^1	-0.5V to +7V	
Supply voltage, V_{PP}	-0.5V to +275V	
Logic input levels	-0.5V to $V_{DD} + 0.5V$	
Continuous total power dissipation ²	Ceramic	1500mW
	Plastic	1200mW
Storage temperature range	-65°C to +150°C	
Lead temperature 1.6mm (1/16 inch) from case for 10 seconds	260°C	

Notes: 1. All voltages are referenced to GND.

2. For operation above 25°C ambient, derate linearly to 70°C at 12mW/°C.

General Description

The HV72 is a low-voltage serial to high-voltage parallel converter with push-pull outputs. It is especially suitable for use as a symmetric row driver in AC thin-film electroluminescent (ACTFEL) displays. For packaged parts, a DIR pin controls the direction of data shift through the device. When DIR is at logic high, D_{IOA} is Data-in and D_{IOB} is Data-out, data is shifted from HV_{OUT1} to HV_{OUT40} . When DIR is grounded, D_{IOB} is Data-in and D_{IOA} is Data-out, the data is then shifted from HV_{OUT40} to HV_{OUT1} . The POL and OE pins perform the polarity select and output enable function respectively. Data is loaded on the low to high transition of the clock. A logic high will cause the output to swing to V_{PP} if POL is high, or to GND if POL is low. All outputs will be in High-Z state if OE is at logic high. Data output buffers are provided for cascading devices.

There are two output pin configurations, Option A and B. When the SHIFT pin is logic low, the device operates in Option A; when the SHIFT pin is logic high, the device operates in Option B.

Electrical Characteristics

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(over recommended operating conditions of $V_{DD} = 5V$, $V_{PP} = 250V$, and $T_A = 25^\circ C$ unless noted)

DC Characteristics

Symbol	Parameter	Min	Max	Units	Conditions
I_{DD}	V_{DD} supply current		10	mA	$f_{CLK} = 4MHz$
I_{pp}	High voltage supply current		1.0	mA	All outputs low or High-Z ($-40^\circ C$ to $85^\circ C$)
I_{DDQ}	Quiescent V_{DD} supply current		100	μA	All $V_{IN} = GND$ or V_{DD} ($-40^\circ C$ to $+80^\circ C$)
V_{OH}	High-level output	HV_{OUT}	200	V	$I_O = -70mA$ ($-50mA$) ²
V_{OL}		Data out	4.5	V	$I_O = -500\mu A$
	Low-level output	HV_{OUT}	50	V	$I_O = 70mA$ ($-50mA$) ²
		Data out	0.5	V	$I_O = 500\mu A$
	High-level logic input current		1	μA	$V_{IH} = V_{DD}$
I_{IL}	Low-level logic input current		-1	μA	$V_{IL} = 0V$

Notes:

1. Only one output can be turned on at a time.
2. Over military temperature range.

AC Characteristics

Symbol	Parameter	Min	Max	Units	Conditions
f_{CLK}	Clock frequency		4	MHz	
$t_{W(H/L)}$	Pulse width - clock high or low	125		ns	
t_{SUD}	Data set-up time before clock rises	50		ns	
t_{HD}	Data hold time after clock rises	50		ns	
t_{SUC}	HV_{OUT} delay from clock rises		600	ns	
t_{SUE}	HV_{OUT} delay from output enable rises		500	ns	
t_{SUP}	HV_{OUT} delay from polarity falls		500	ns	
t_{HC}	HV_{OUT} delay from clock rises		600	ns	
t_{HE}	HV_{OUT} delay from enable falls		500	ns	
t_{HP}	HV_{OUT} delay from polarity rises		500	ns	
t_{DHL}	Delay time clock to data output falls		160	ns	$C_L = 15pF$
t_{DLH}	Delay time clock to data output rises		160	ns	$C_L = 15pF$
t_{ONF}	HV_{OUT} fall time		2	μs	$C_L = 330pF$ $R_L = 10 k\Omega$
t_{ONR}	HV_{OUT} rise time		2	μs	$C_L = 330 pF$ $R_L = 10 k\Omega$
t_{POW}	Polarity pulse width	3		μs	
t_{OEW}	Output enable pulse width	3		μs	

Recommended Operating Conditions

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Symbol	Parameter	Min	Max	Units
V_{DD}	Logic supply voltage	4.5	5.5	V
V_{PP}	High voltage supply†	0	250	V
V_{IH}	High-level input voltage	$0.7 V_{DD}$	V_{DD}	V
V_{IL}	Low-level input voltage	0	$0.2 V_{DD}$	V
f_{CLK}	Clock frequency		4	MHz
I_O	High voltage output current		± 70	mA
T_A	Operating free-air temperature	-40	+85	°C
	Military Hi-Rel (RB)	-55	+125	°C

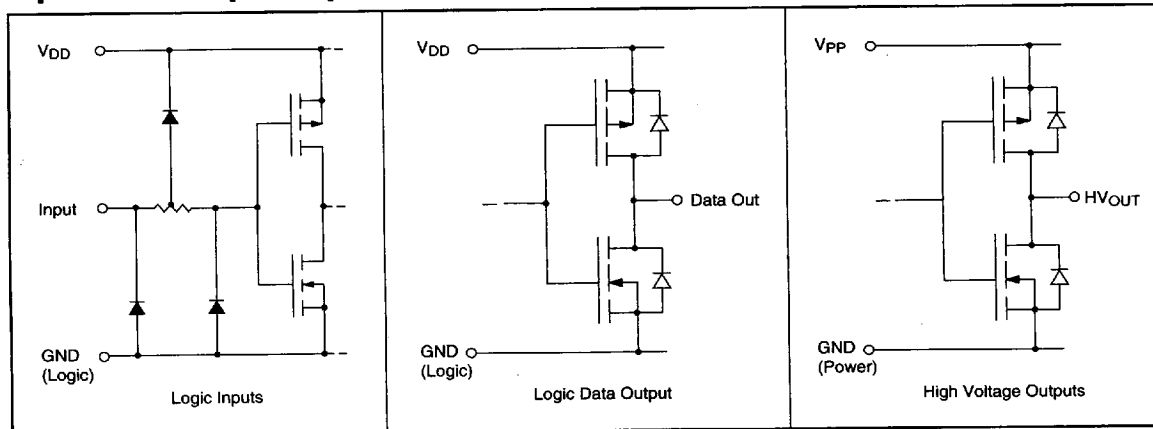
Notes:† Output will not switch at $V_{PP} = 0V$.

Power-up sequence should be the following:

1. Connect ground.
2. Apply V_{DD} .
3. Set all inputs (Data, CLK, Enable, etc.) to a known state.
4. Apply V_{PP} .

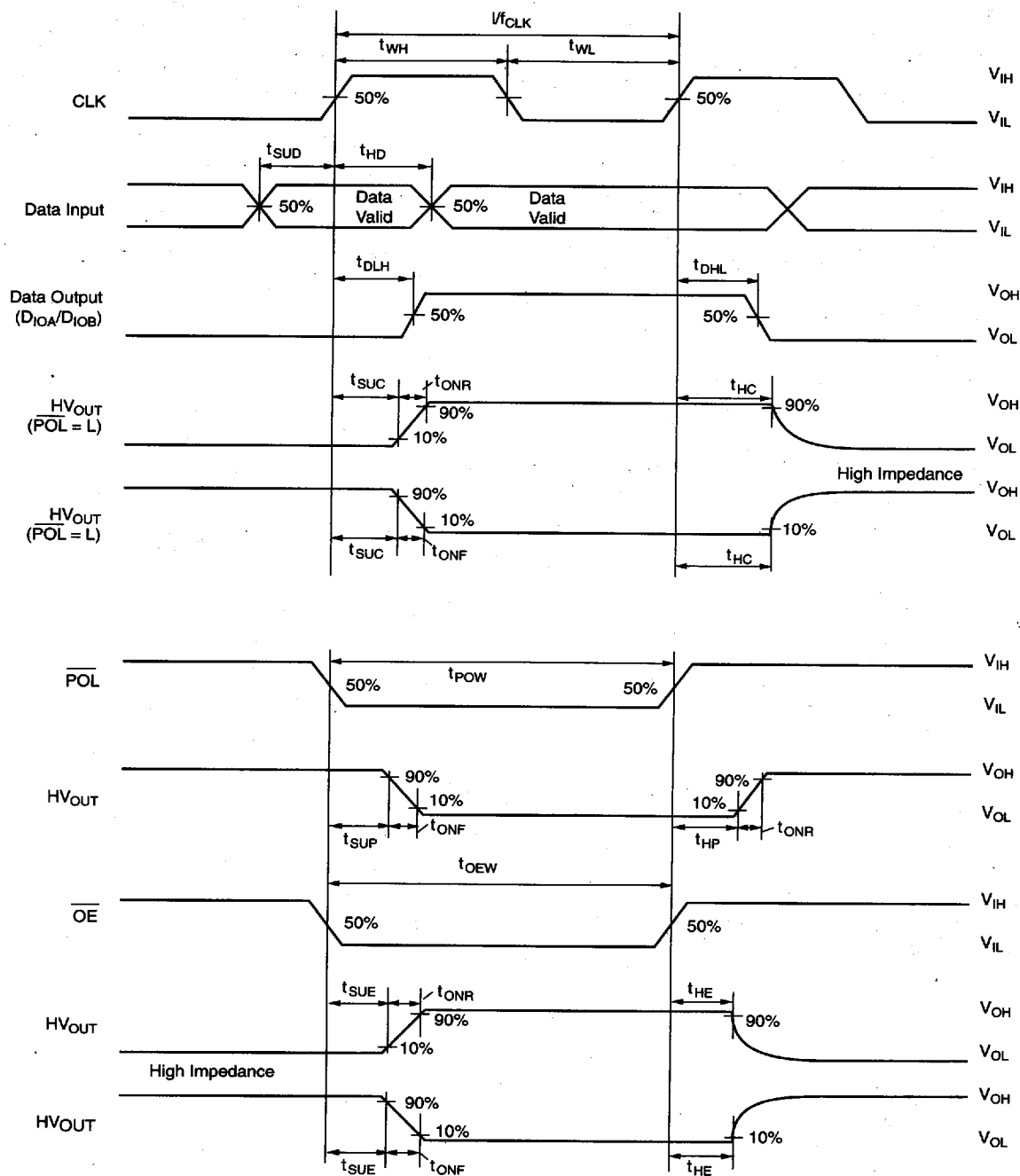
Power-down sequence should be the reverse of the above.

Input and Output Equivalent Circuits

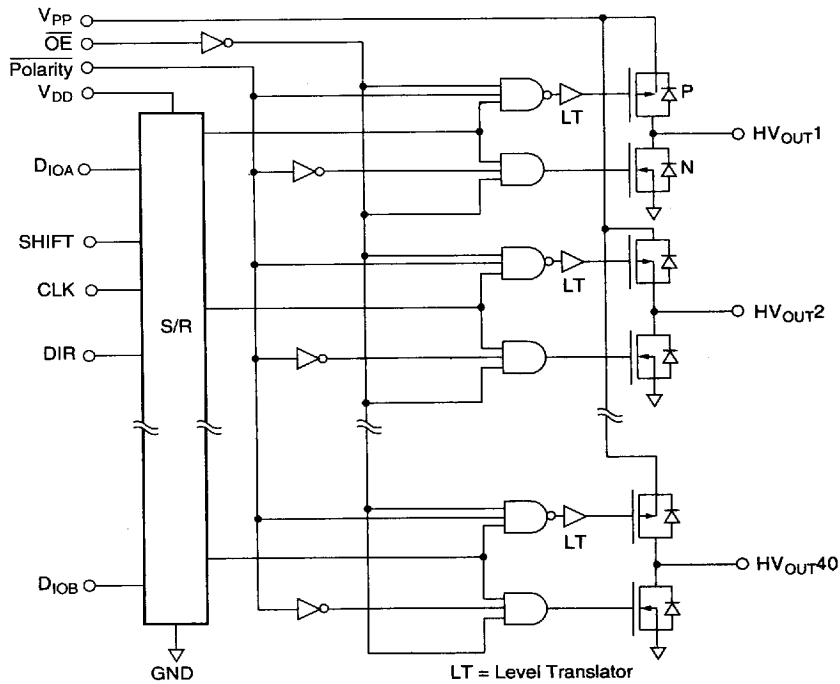


Switching Waveforms

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Functional Block Diagram SUPERTEX INC



Function Table

I/O Relations	Inputs					Outputs		
	CLK	DIR	Data	POL	OE	Shift Reg	HV Outputs	Data Out
O/P HIGH	X	X	H	H	L	*	H	*
O/P OFF	X	X	L	X	L	*	HIGH-Z	*
O/P LOW	X	X	H	L	L	*	L	*
O/P OFF	X	X	X	X	H	*	All O/P HIGH-Z	*
Load S/R, Set DIR	↑	H	X	X	X	$Q_n \rightarrow Q_{n+1}$	*	Q40
	↑	L	X	X	X	$Q_n \rightarrow Q_{n-1}$	*	Q1
I/O Relation	X	H	D _{IOA}	X	X	*	*	D _{IOB}
	X	L	D _{IOB}	X	X	*	*	D _{IOA}

Notes:

H = logic high level, L = logic low level, X = irrelevant, ↑ = low to high transition
* = dependent on previous state and whether an O/P or S/R command occurred

Pin Configurations

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Option A:

Pin	Function	Pin	Function
1	HV _{OUT} 1/40	33	NC
2	HV _{OUT} 2/39	34	D _{IOB}
3	HV _{OUT} 3/38	35	OE
4	HV _{OUT} 4/37	36	NC
5	HV _{OUT} 5/36	37	POL
6	HV _{OUT} 6/35	38	NC
7	HV _{OUT} 7/34	39	V _{DD}
8	HV _{OUT} 8/33	40	NC
9	HV _{OUT} 9/32	41	GND (Logic)
10	HV _{OUT} 10/31	42	GND (Power)
11	HV _{OUT} 11/30	43	NC
12	HV _{OUT} 12/29	44	V _{PP}
13	HV _{OUT} 13/28	45	HV _{OUT} 21/20
14	HV _{OUT} 14/27	46	HV _{OUT} 22/19
15	HV _{OUT} 15/26	47	HV _{OUT} 23/18
16	HV _{OUT} 16/25	48	HV _{OUT} 24/17
17	HV _{OUT} 17/24	49	HV _{OUT} 25/16
18	HV _{OUT} 18/23	50	HV _{OUT} 26/15
19	HV _{OUT} 19/22	51	HV _{OUT} 27/14
20	HV _{OUT} 20/21	52	HV _{OUT} 28/13
21	V _{PP}	53	HV _{OUT} 29/12
22	NC	54	HV _{OUT} 30/11
23	GND (Power)	55	HV _{OUT} 31/10
24	GND (Logic)	56	HV _{OUT} 32/9
25	DIR	57	HV _{OUT} 33/8
26	V _{DD}	58	HV _{OUT} 34/7
27	CLK	59	HV _{OUT} 35/6
28	NC	60	HV _{OUT} 36/5
29	SHIFT	61	HV _{OUT} 37/4
30	NC	62	HV _{OUT} 38/3
31	D _{IOA}	63	HV _{OUT} 39/2
32	NC	64	HV _{OUT} 40/1

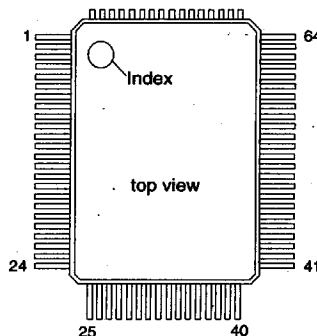
Note: Pin designation for DIR H/L, SHIFT = L.
 Example: For DIR = H, pin 1 is HV_{OUT}1.
 For DIR = L, pin 1 is HV_{OUT}40.
 Pins 65–80 are NC (ceramic only).

Option B:

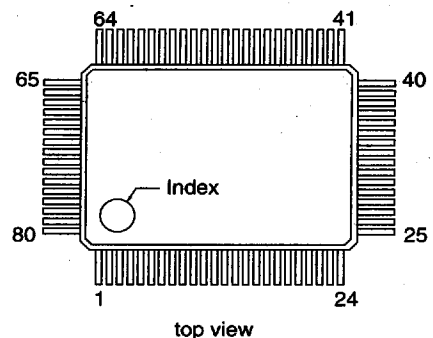
Pin	Function	Pin	Function
1	HV _{OUT} 20/21	33	NC
2	HV _{OUT} 19/22	34	D _{IOB}
3	HV _{OUT} 18/23	35	OE
4	HV _{OUT} 17/24	36	NC
5	HV _{OUT} 16/25	37	POL
6	HV _{OUT} 15/26	38	NC
7	HV _{OUT} 14/27	39	V _{DD}
8	HV _{OUT} 13/28	40	NC
9	HV _{OUT} 12/29	41	GND (Logic)
10	HV _{OUT} 11/30	42	GND (Power)
11	HV _{OUT} 10/31	43	NC
12	HV _{OUT} 9/32	44	V _{PP}
13	HV _{OUT} 8/33	45	HV _{OUT} 40/1
14	HV _{OUT} 7/34	46	HV _{OUT} 39/2
15	HV _{OUT} 6/35	47	HV _{OUT} 38/3
16	HV _{OUT} 5/36	48	HV _{OUT} 37/4
17	HV _{OUT} 4/37	49	HV _{OUT} 36/5
18	HV _{OUT} 3/38	50	HV _{OUT} 35/6
19	HV _{OUT} 2/39	51	HV _{OUT} 34/7
20	HV _{OUT} 1/40	52	HV _{OUT} 33/8
21	V _{PP}	53	HV _{OUT} 32/9
22	NC	54	HV _{OUT} 31/10
23	GND (Power)	55	HV _{OUT} 30/11
24	GND (Logic)	56	HV _{OUT} 29/12
25	DIR	57	HV _{OUT} 28/13
26	V _{DD}	58	HV _{OUT} 27/14
27	CLK	59	HV _{OUT} 26/15
28	NC	60	HV _{OUT} 25/16
29	SHIFT	61	HV _{OUT} 24/17
30	NC	62	HV _{OUT} 23/18
31	D _{IOA}	63	HV _{OUT} 22/19
32	NC	64	HV _{OUT} 21/20

Note: Pin designation for DIR L/H, SHIFT = H.
 Example: For DIR = L, pin 1 is HV_{OUT}20.
 For DIR = H, pin 1 is HV_{OUT}21.
 Pins 65–80 are NC (ceramic only).

Package Outline



3-sided Plastic QFP 64-pin Gullwing Package



80-Pin Ceramic QFP Gullwing Package