Supertex inc. HV72

Product Objective Specification

40-Channel Symmetric Row Driver T-52-13-05

Ordering Information

Device	Package Options			
	64-Lead 3-Sided Ceramic Gullwing	64-Lead 3-Sided Plastic Gullwing	Die in waffle pack	64-Lead 3-Sided Ceramic Gullwing (MIL-STD-883 Processed*)
HV7225	HV7225DJ	HV7225PJ	HV7225X	RBHV7225DJ

* For Hi-Rel process flows, refer to page 5-3 of the Databook.

Features

- Processed with HVCMOS® technology
- Symmetric row drive (reduces latent imaging in ACTFEL displays)
- Output voltages up to 250V
- Low-power level shifting
- Source/Sink current 100mA (max.)
- Shift Register Speed 4MHz
- Pin-programmable shift direction
- Hi-Rel processing available

General Description

The HV72 is a low-voltage serial to high-voltage parallel converter with push-pull outputs. It is especially suitable for use as a symmetric row driver in AC thin-film electroluminescent (ACTFEL) displays. The HV72 offers 40 output lines, a direction (DIR) pin to give CW or CCW shift register loading, output enable (OE), and polarity (POL) control. After DATA INPUT is entered (on the falling edge of CLOCK), a logic high will cause the output to swing to V_{PP} if POL is high, or to GND if POL is low.

Absolute Maximum Ratings

Supply voltage, V_{DD}[1]		-0.3V to +6V
Supply voltage, V_{PP}		-0.3V to +250V
Logic input levels		-0.3V to V_{DD} +0.3V
Ground currrent[2]		1.5A
Continuous total power dissipation[3]:	Ceramic	1500mW
	Plastic	1200mW
Storage temperature range		-65°C to +150°C
Lead temperature 1.6mm (1/16 inch) from case for 10 seconds		260°C

Notes:
1. All voltages are referenced to GND.
2. Duty cycle is limited by the total power dissipated in the package.
3. For operation above 25°C ambient, derate linearly to 72°C at 12mW/°C.

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Electrical Characteristics

(over recommended operating conditions of V_{DD} = 5V, V_{PP} = 230V, and T_A = 25°C unless noted)

DC Characteristics

Symbol	Parameter		Min	Max	Units	Conditions
I_{DD}	V_{DD} supply current			10	mA	f_{CLK} = 4MHz
I_{PP}	High voltage supply current			4	mA	1 Output high[1]
				100	µA	All Outputs low or High-Z
				750	µA	All Outputs low or High-Z (125°C)
I_{DDQ}	Quiescent V_{DD} supply current			100	µA	All V_{IN} = GND or V_{DD}
V_{OH}	High-level output	HV_{OUT}	200		V	I_O= -70mA
		Data out	11		V	I_O= -500µA
V_{OL}	Low-level output	HV_{OUT}		30	V	I_O= 70mA
		Data out		1	V	I_O= 500µA
I_{IH}	High-level logic input current			1	µA	V_{IH} = 12V
I_{IL}	Low-level logic input current			-1	µA	V_{IL} = 0V

Note1 The total number of ON outputs times the duty cycle must not exceed the allowable package power disspation.

AC Characteristics (V_{DD} = 12V, T_A = 25°C)

Symbol	Parameter	Min	Max	Units	Conditions
f_{CLK}	Clock frequency		4	MHz	
t_W	Pulse duration clock high or low	125		ns	
t_{SUD}	Data set-up time before falling clock	100		ns	
t_{HD}	Data hold time after falling clock	100		ns	
t_{SUC}	Setup time clock low before V_{PP}↑ or GND↓	300		ns	
t_{SUE}	Setup time enable high before V_{PP}↑ or GND↓	300		ns	
t_{SUP}	Setup time polarity high or low before V_{PP}↑ or GND↓	300		ns	
t_{HC}	Hold time clock high after V_{PP}↑ or GND↓	500		ns	
t_{HE}	Hold time enable high after V_{PP}↑ or GND↓	300		ns	
t_{HP}	Hold time polarity high or low after V_{PP}↑ or GND↓	300		ns	
t_{DHL}	Delay time high to low level output from clock		150	ns	C_L = 10pF
t_{DLH}	Delay time low to high level output from clock		200	ns	C_L = 10pF
t_{THL}	Transition time high to low level serial output		200	ns	C_L = 15pF
t_{TLH}	Transition time low to high level serial output		100	ns	C_L = 15pF
t_{ONH}	High level turn-on time Q outputs from enable		500	ns	I_O = -50 mA, V_{OH} =195V R_L = 2 kΩ to 95V
t_{ONL}	Low level turn-on time Q outputs from enable		500	ns	I_O = 50 mA, V_{OH} =130V R_L = 2 kΩ to 30V
t_{OFFH}	High level turn-off time Q outputs from enable		1000	ns	I_O = -50 mA, V_{OH} =195V R_L = 2 kΩ to 95V
t_{OFFL}	Low level turn-off time Q outputs from enable		500	ns	I_O = 50 mA, V_{OH} =130V R_L = 2 kΩ to 30V
dv/dt	Slew rate, V_{PP} or GND		45	V/µs	With one active output driving a 4.7 nF load to V_{PP} or GND

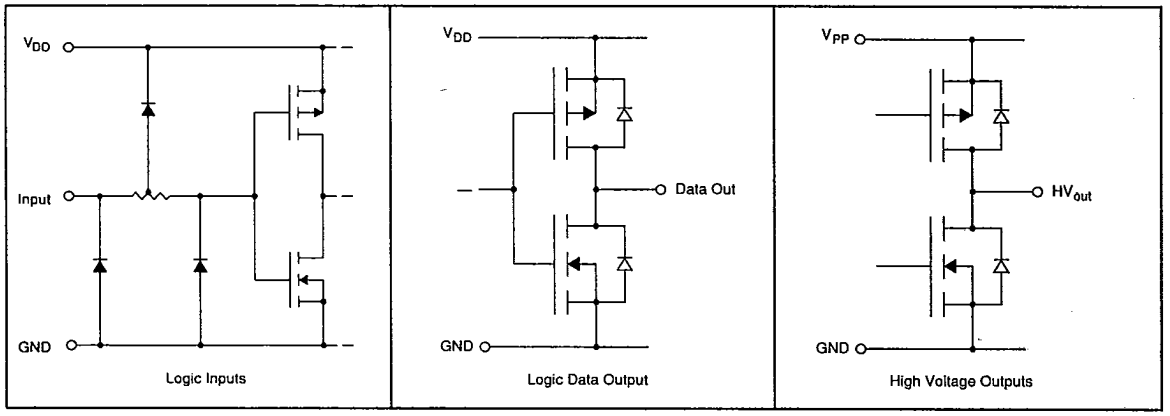
Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{DD}	Logic supply voltage		4.5	5.5	V
V_{PP}	High voltage supply			230	V
V_{IH}	High-level input voltage	V_{DD} = 4.5V	3.5		V
V_{IL}	Low-level input voltage	V_{DD} = 4.5V		1	V
f_{CLK}	Clock frequency			4	MHz
T_A	Operating free-air temperature	Commercial	0	+70	°C
		Military Hi-Rel (RB)	-55	+125	°C

Note:
Power-up sequence should be the following:
1. Connect ground.
2. Apply V_{DD}.
3. Set all inputs (Data, CLK, Enable, etc.) to a known state.
4. Apply V_{PP}.

Power-down sequence should be the reverse of the above.

Input and Output Equivalent Circuits



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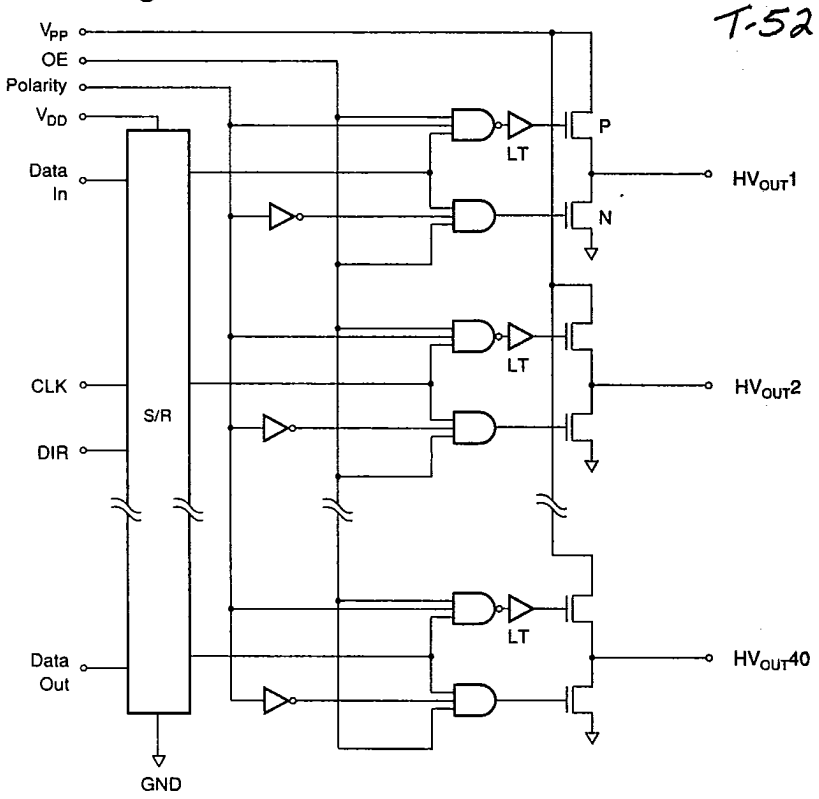
Functional Block Diagram



LT = Level Translator

Function Table

I/O Relations	Inputs					Outputs		
	CLK	DIR	Data	POL	OE	Shift Reg	HV Outputs	Data Out
O/P HIGH	X	X	H	H	H	*	H	
O/P OFF	X	X	L	H	H	*	HIGH-Z	*
O/P LOW	X	X	H	L	H	*	L	*
O/P OFF	X	X	L	L	H	*	HIGH-Z	*
O/P OFF	X	X	X	X	L	*	All O/P HIGH-Z	*
Load S/R, set DIR	↓	L	X	X	X	$Q_n \rightarrow Q_{n+1}$	*	Q_{40}
	↓	H	X	X	X	$Q_n \rightarrow Q_{n-1}$	*	Q_1
I/O Relation	X	L	D_{IOB}	X	X	*	*	D_{IOA}
	X	H	D_{IOA}	X	X	*	*	D_{IOB}

Notes:
H = logic high level, L = logic low level, X = irrelevant, ↓ = high-to-low transition,
$Q_1 = HV_{out}$ 1, $Q_n = HV_{out}$ (n), etc.
* = dependent on previous state and whether an O/P or S/R command occured.

Pin Configurations

HV72
64-pin 3-sided Gullwing

Pin	Function	Pin	Function
1	$HV_{OUT}1/40$	33	NC
2	$HV_{OUT}2/39$	34	D_{IOB}
3	$HV_{OUT}3/38$	35	OE
4	$HV_{OUT}4/37$	36	NC
5	$HV_{OUT}5/36$	37	POL
6	$HV_{OUT}6/35$	38	NC
7	$HV_{OUT}7/34$	39	V_{DD}
8	$HV_{OUT}8/33$	40	NC
9	$HV_{OUT}9/32$	41	GND(Logic)
10	$HV_{OUT}10/31$	42	GND(Power)
11	$HV_{OUT}11/30$	43	NC
12	$HV_{OUT}12/29$	44	V_{PP}
13	$HV_{OUT}13/28$	45	$HV_{OUT}21/20$
14	$HV_{OUT}14/27$	46	$HV_{OUT}22/19$
15	$HV_{OUT}15/26$	47	$HV_{OUT}23/18$
16	$HV_{OUT}16/25$	48	$HV_{OUT}24/17$
17	$HV_{OUT}17/24$	49	$HV_{OUT}25/16$
18	$HV_{OUT}18/23$	50	$HV_{OUT}26/15$
19	$HV_{OUT}19/22$	51	$HV_{OUT}27/14$
20	$HV_{OUT}20/21$	52	$HV_{OUT}28/13$
21	V_{PP}	53	$HV_{OUT}29/12$
22	NC	54	$HV_{OUT}30/11$
23	GND(Power)	55	$HV_{OUT}31/10$
24	GND(Logic)	56	$HV_{OUT}32/9$
25	DIR	57	$HV_{OUT}33/8$
26	V_{DD}	58	$HV_{OUT}34/7$
27	CK	59	$HV_{OUT}35/6$
28	NC	60	$HV_{OUT}36/5$
29	NC	61	$HV_{OUT}37/4$
30	NC	62	$HV_{OUT}38/3$
31	D_{IOA}	63	$HV_{OUT}39/2$
32	NC	64	$HV_{OUT}40/1$

Note:
Pin designation for DIR H/L
Example: For DIR = H, pin 1 is HV_{OUT} 1
For DIR = L, pin 1 is HV_{OUT} 40

Package Outline

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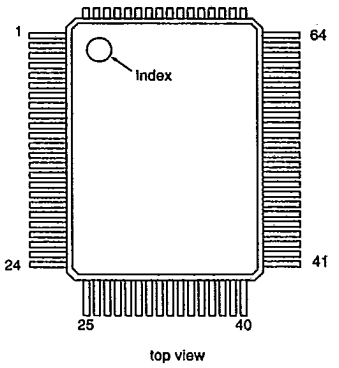

3-sided Plastic QFP 64-pin Gullwing Package

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