FUJITSU SEMICONDUCTOR
DATA SHEET

DS04-21382-1E

ASSP DTS

Bi-CMOS

Dual Serial Input PLL Frequency Synthesizer

MB15F63UL

■ DESCRIPTION

MB15F63UL has a 2000 MHz PLL frequency synthesizer with a high-speed frequency switching function based on the Fractional-N PLL (Phase Locked Loop), and 600 MHz Integer-N PLL frequency synthesizer which enables pulse swallow operation. Encased in a subminiature package (thin-BCC20), MB15F63UL has successfully achieved a small thin external form (BCC20 package dimensions: 3.50 mm × 3.50 mm × 0.60 mm). MB15F63UL is suitable for use in digital mobile communication devices such as GSM.

■ FEATURES

- High frequency operation : 100 MHz to 1800 MHz (RF : 2.7 V ≤ Vcc < 2.9 V) /
  100 MHz to 2000 MHz (RF : 2.9 V ≤ Vcc ≤ 3.3 V)
  50 MHz to 600 MHz (IF)
- Fractional-N function : Modulo 1048576 (ΣΔ method)
  : Fractional-N, enabling high-speed PLL lock-up and low phase noise
- Low voltage operation : Vcc = 2.7 V to 3.3 V
- Ultra Low power supply current : 6.1 mA Typ (RF) +1.4 mA (IF) Vcc = 3.0 V, Ta = + 25 °C, in locking state
- Direct power saving function : Power supply current in power saving mode
  (controllable in external pin) 0.1 μA Typ (Vcc = 3.0 V, Ta = + 25 °C)
  10 μA Max (Vcc = 3.0 V)
- Internal automatic switch changeover circuit (changeover time selectable)
  Bit function to update the changeover time
- Constant-current charge pump circuit capable of switching control of the current value through serial data control or internal changeover circuit :
  For steady-state operation: 94 μA
  For high-speed changeover: 4.5 mA

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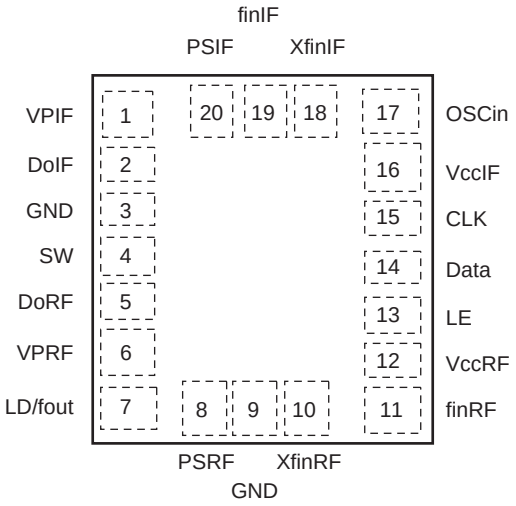
- Open-drain NMOS switch that can be turned on and off from the internal changeover circuit
- Prescaler division ratio : 2000 MHz prescaler (16/17/20/21) /600 MHz prescaler (8/9, 16/17)
- 29-bit shift register input control
- Serial input 14-bit programmable reference divider : Binary 6-bit 1 to 63 (RF side) / Binary 14-bit swallow counter 3 to 16383 (IF side)
- Serial input programmable divider consisting of :
  Binary 4-bit swallow counter 0 to 15 (RF side) / Binary 7-bit swallow counter 0 to 127 (IF side)
  Binary 7-bit programmable counter 5 to 127 (RF side) /Binary 11-bit swallow counter 3 to 2047 (IF side)
- On-chip phase control for phase comparator
- Built-in digital locking detector circuit to detect PLL locking and unlocking
- Extended operating temperature : Ta = –40 °C to +85 °C

■ PIN ASSIGNMENTS

(TOP VIEW)

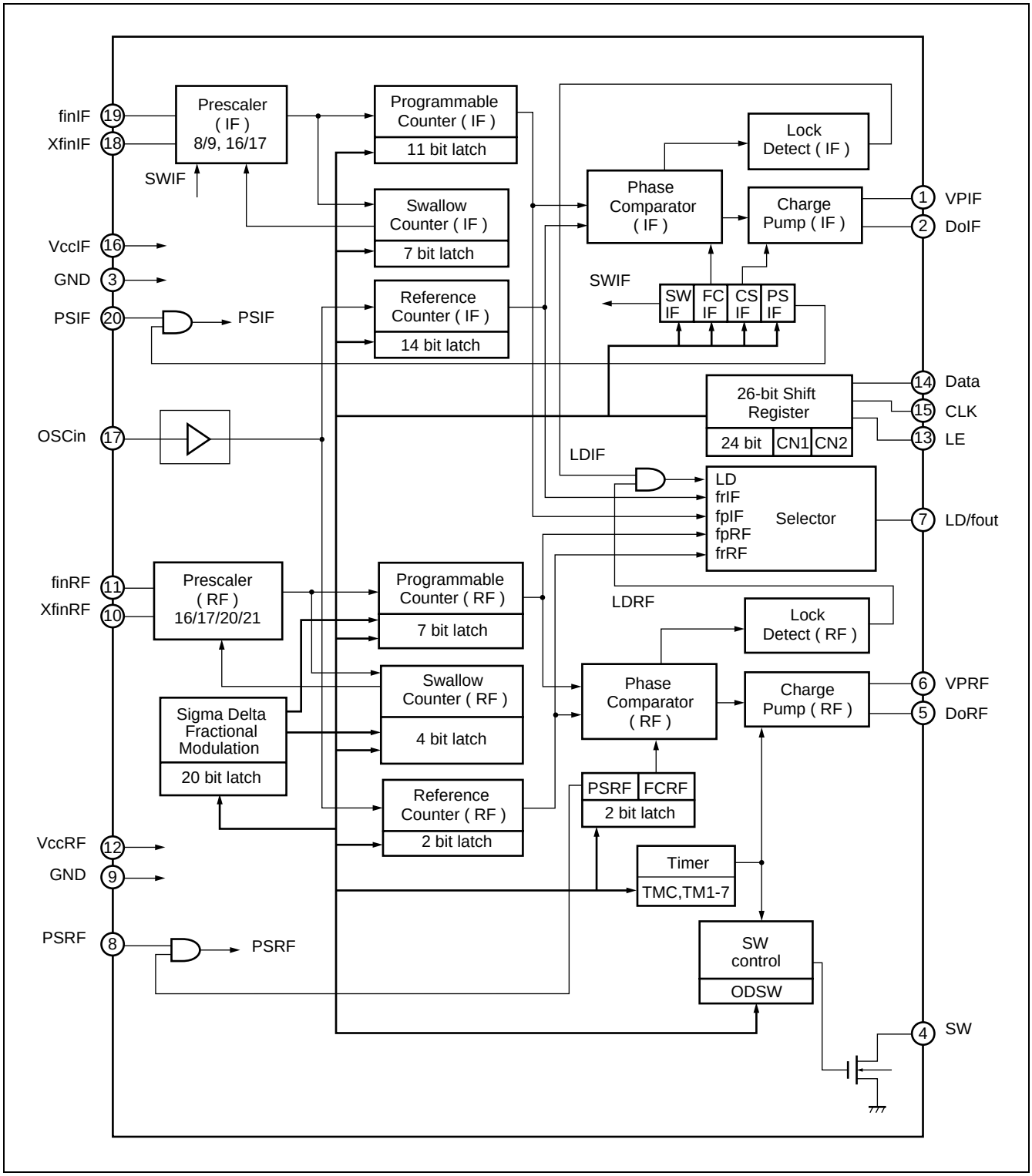


(LCC-20P-M06)

■ PIN DESCRIPTIONS

Pin no.	Pin name	I/O	Descriptions
1	VPIF	—	Charge pump power supply for the IF-PLL
2	DoIF	O	Charge pump output for the IF-PLL
3	GND	—	Ground pin
4	SW	O	Open-drain switch pin for changing over the high-speed mode filter
5	DoRF	O	Charge pump output for the RF-PLL
6	VPRF	—	Power supply for the RF-PLL charge pump
7	LD/fout	O	Lock detect signal output (LD) /phase comparator monitoring output (fout) pin. The output signal is selected by LDS bit in a serial data. LDS bit = “H” : outputs fout signal/LDS bit = “L” : outputs LD signal
8	PSRF	I	Power saving mode control for the RF-PLL section. This pin must be set at “L” when the power supply is started up. (Open is prohibited.) PS = “H” : Normal mode/PS = “L” : Power saving mode
9	GND	—	Ground pin
10	XfinRF	I	Prescaler complimentary input pin for the RF-PLL section. This pin should be grounded via a capacitor.
11	finRF	I	Prescaler input pin for the RF-PLL. Connection to an external VCO should be via AC coupling.
12	VccRF	—	Power supply pin for the RF-PLL
13	LE	I	Load enable signal input pin (with the schmitt trigger circuit) When LE is set “H”, data in the shift register is transferred to the corresponding latch according to the control bit in a serial data.
14	Data	I	Serial data input pin (with the schmitt trigger circuit) Data is transferred to the corresponding latch (IF-ref. counter, IF-prog. counter, RF-ref. counter, RF-prog. counter) according to the control bit in a serial data.
15	CLK	I	Clock input pin for the 29-bit shift register (with the schmitt trigger circuit) One bit data is shifted into the shift register on a rising edge of the clock.
16	VccIF	—	Power supply pin for the IF-PLL
17	OSCin	I	The programmable reference divider input pin. TCXO should be connected with an AC coupling capacitor.
18	XfinIF	I	Prescaler complimentary input for the IF-PLL section. This pin should be grounded via a capacitor.
19	finIF	I	Prescaler input pin for the IF-PLL. Connection to an external VCO should be AC coupling.
20	PSIF	I	Power saving mode control pin for the IF-PLL section. This pin must be set at “L” when the power supply is started up. (Open is prohibited.) PS bit = “H” : Normal mode/PS bit = “L” : Power saving mode

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Rating		Unit
			Min	Max	
Power supply voltage		Vcc	− 0.5	+ 3.6	V
		Vp	Vcc	3.6	V
Input voltage		V_I	− 0.5	Vcc + 0.5	V
Output voltage	LD/fout	V_O	GND	Vcc	V
	Do	V_{DO}	GND	Vp	V
Storage temperature		Tstg	− 55	+125	°C

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Rating			Unit
		Min	Typ	Max	
Power supply voltage	Vcc	2.7	3.0	3.3	V
	Vp	Vcc	—	3.3	V
Input voltage	V_I	GND	—	Vcc	V
Operating temperature	Ta	−40	—	+85	°C

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

(Vcc = 2.7 V to 3.3 V, Ta = –40 °C to +85 °C)

Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
Power supply current		Icc_{IF}*1	IF-PLL section	—	1.4	3.0	mA
		Icc_{RF}*2	RF-PLL section	—	6.1	10.0	mA
Power saving current		Ips_{IF}*10	IF-PLL section	—	0.1*9	10	µA
		Ips_{RF}*10	RF-PLL section	—	0.1*9	10	µA
Operating frequency	fin_{IF}*3	fin_{IF}	IF-PLL section	50	—	600	MHz
	fin_{RF}*3	fin_{RF}	RF-PLL section (2.7 V ≤ Vcc < 2.9 V)	100	—	1800	MHz
			RF-PLL section (2.9 V ≤ Vcc ≤ 3.3 V)	100	—	2000	MHz
	OSCin	fosc	Reference counter setting value : R = 1	5	—	20	MHz
			Reference counter setting value : 2 ≤ R ≤ 63	5	—	40	MHz
Input sensitivity	fin_{IF}	$Pfin_{IF}$	IF-PLL section 50 Ω termination	–15	—	+2	dBm
	fin_{RF}	$Pfin_{RF}$	RF-PLL section 50 Ω termination (fin = 200 MHz to 2000 MHz)	–15	—	+2	dBm
			RF-PLL section 50 Ω termination (fin = 100 MHz to 200 MHz)	–10	—	+2	
Input available voltage	OSCin	V_{OSC}	—	0.5	—	1.5	Vp-p
Operating frequency of phase comparator		f_{MAIN_PD}	RF-PLL section	0.4	—	20	MHz
“H” level input voltage	Data, LE, CLK	V_{IH}	Schmitt trigger input	0.7 Vcc + 0.4	—	—	V
“L” level input voltage		V_{IL}	Schmitt trigger input	—	—	0.3 Vcc – 0.4	V
“H” level input voltage	PSIF, PSRF	V_{IH}	—	0.7 Vcc	—	—	V
“L” level input voltage		V_{IL}	—	—	—	0.3 Vcc	V
“H” level input current	Data, LE, CLK	I_{IH}*4	—	–1.0	—	+1.0	µA
“L” level input current		I_{IL}*4	—	–1.0	—	+1.0	µA
“H” level output voltage	LD/fout	V_{OH}	Vcc = 3.0 V, I_{OH} = –1 mA	Vcc – 0.4	—	—	V
“L” level output voltage		V_{OL}	Vcc = 3.0 V, I_{OL} = 1 mA	—	—	0.4	V

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(Vcc = 2.7 V to 3.3 V, Ta = –40 °C to +85 °C)

Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
"H" level output voltage	DoIF	V_{DOH}	VccIF = VPIF = 3.0 V, I_{DOH} = –0.5 mA	Vp – 0.4	—	—	V
"L" level output voltage	DoIF	V_{DOL}	VccIF = VPIF = 3.0 V, I_{DOL} = 0.5 mA	—	—	0.4	V
"H" level output voltage	DoRF	V_{DOH}	VccRF = VPRF = 3.0 V, I_{DOH} = –0.01 mA	Vp – 0.4	—	—	V
"L" level output voltage	DoRF	V_{DOL}	VccRF = VPRF = 3.0 V, I_{DOL} = 0.01 mA	—	—	0.4	V
High impedance cutoff current	DoIF DoRF	I_{OFF}	Vcc = Vp = 3.0 V, V_{OFF} = 0.5 V to Vcc–0.5 V	—	—	2.5	nA
"H" level output current	LD/fout	I_{OH}*4	Vcc = 3.0 V	—	—	–1.0	mA
"L" level output current	LD/fout	I_{OL}	Vcc = 3.0 V	1.0	—	—	mA
"H" level output current	DoIF	I_{DOH}*4	VccIF = VPIF = 3.0 V, VDoIF = VPIF/2 CSIF = "L", Ta = + 25 °C	–2.2	–1.5	–0.8	mA
"L" level output current	DoIF	I_{DOL}		+0.8	+1.5	+2.2	mA
"H" level output current	DoIF	I_{DOH}*4	VccIF = VPIF = 3.0 V, VDoIF = VPIF/2 CSIF = "H", Ta = + 25 °C	–8.2	–6.0	–4.1	mA
"L" level output current	DoIF	I_{DOL}		+4.1	+6.0	+8.2	mA
"H" level output current	DoRF	I_{DOH}*4	VccRF = VPRF = 3.0 V, VDoRF = VPRF/2 In steady state (locking state) : Ta = + 25 °C	–160	–94	–40	µA
"L" level output current	DoRF	I_{DOL}		+40	+94	+160	µA
"H" level output current	DoRF	I_{DOH}*4	VccRF = VPRF = 3.0 V, VDoRF = VPRF/2 channels in changeover : Ta = + 25 °C	–6.1	–4.5	–2.4	mA
"L" level output current	DoRF	I_{DOL}		+2.4	+4.5	+6.1	mA
Charge pump current rate	DoIF	I_{DOL}/I_{DOH}	I_{DOMT}*5	V_{DO} = Vp/2	—	3	—	%
	DoIF	vs. VDo	I_{DOVD}*6	0.5V ≤ V_{DO} ≤ Vcc – 0.5 V	—	10	—	%
	DoIF	vs. Ta	I_{DOTA}*7	–40 °C ≤ Ta ≤ + 85 °C, V_{DO} = Vcc/2	—	5	—	%
	DoRF	I_{DOL}/I_{DOH}	I_{DOMT}*8	V_{DO} = Vp/2	—	8.0	15.0	%
Open-drain output resistance for high-speed (SW)		Z_{SSH}	At normal mode (OFF)	100	—	—	kΩ
Open-drain output resistance for high-speed (SW)		Z_{SSH}	At high-speed mode (ON)	—	35	70	Ω

*1 : finIF = 190 MHz, fosc = 19.2 MHz, frIF = 100 kHz, V_{CC}IF = VPIF = 3.0 V, Ta = + 25 °C, in locking state.

*2 : finRF = 1600 MHz, fosc = 19.2 MHz, frRF = 19.2 MHz, V_{CC}RF = VPRF = 3.0 V, Ta = + 25 °C, in locking state.

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*3 : AC coupling. 1000 pF capacitor is connected under the condition of minimum operating frequency.

*4 : The symbol "–" means direction of current flow.

*5 : $V_{CC} = V_P = 3.0$ V, Ta = +25 °C
$(||I_3| - |I_4||) \ / \ [(|I_3| + |I_4|) \ / \ 2] \times 100\%$

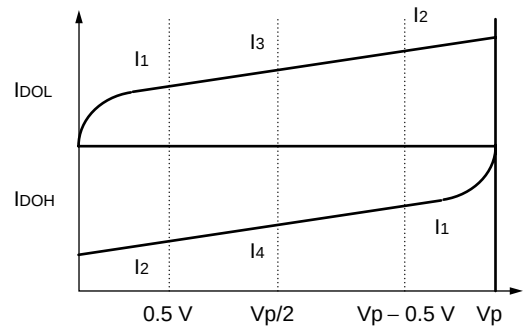
*6 : $V_{CC} = V_P = 3.0$V, Ta = +25 °C (I_{DOL}, I_{DOH} respectively)
$[(||I_2| - |I_1||) \ / \ 2] \ / \ [(|I_1| + |I_2|) \ / \ 2] \times 100\%$

*7 : $V_{CC} = V_P = 3.0$V, Ta = +25 °C (I_{DOL}, I_{DOH} respectively)
$[(||I_{DO}\ (85c)| - |I_{DO}\ (-40c)||) \ / \ 2] \ / \ [(|I_{DO}\ (85c)| + |I_{DO}\ (-40C)|) \ / \ 2] \times 100\%$

*8 : $V_{CC} = V_P = 3.0$ V, Ta = +25 °C $(||I_{DOL}| - |I_{DOH}||) \ / \ [(|I_{DOL}| + |I_{DOH}|) \ / \ 2] \times 100\%$

*9 : Power supply current at PS = GND (Data, LE and CLK are V_{IL} = GND and V_{IH} = Vcc setting.)

*10 : Power supply current at fosc = 19.2 MHz, $V_{CC} = V_P = 3.0$ V, Ta = +25 °C, PS = GND (Data, LE and CLK are V_{IL} = GND, V_{IH} = Vcc setting.)



Charge pump output potential [V]

■ FUNCTIONAL DESCRIPTION

1. Serial Data Input

Serial data is processed using the Data, Clock, and LE pins. Serial data controls the programmable reference divider and the programmable divider separately.
Binary serial data is entered through the Data pin.
One bit of data is shifted into the shift register on the rising edge of the Clock. When the LE signal pin is taken high, stored data is latched according to the control bit data.

The following table shows the shift register configuration and combinations of data transfer control bits.

LSB — Destination of serial data → — MSB

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29
0	0	R1 IF	R2 IF	R3 IF	R4 IF	R5 IF	R6 IF	R7 IF	R8 IF	R9 IF	R10 IF	R11 IF	R12 IF	R13 IF	R14 IF	CS IF	SW IF	FC IF	LD S	T1	T2	×	×	×	×	×	×	×
0	1	A1 IF	A2 IF	A3 IF	A4 IF	A5 IF	A6 IF	A7 IF	N1 IF	N2 IF	N3 IF	N4 IF	N5 IF	N6 IF	N7 IF	N8 IF	N9 IF	N10 IF	N11 IF	PS IF	×	×	×	×	×	×	×	×
1	0	F1 RF	F2 RF	F3 RF	F4 RF	F5 RF	F6 RF	F7 RF	F8 RF	F9 RF	F10 RF	F11 RF	F12 RF	F13 RF	F14 RF	F15 RF	F16 RF	F17 RF	F18 RF	F19 RF	F20 RF	A1 RF	A2 RF	A3 RF	A4 RF	N1 RF	N2 RF	N3 RF
1	1	N4 RF	N5 RF	N6 RF	N7 RF	R1 RF	R2 RF	R3 RF	R4 RF	R5 RF	R6 RF	FC RF	TM C	TM 1	TM 2	TM 3	TM 4	TM 5	TM 6	TM 7	×	OD SW	PS RF	SC	×	×	×	×

Note : Start data input with MSB first.

2. Setting data

a) Fractional-N Synthesizer in the RF-PLL section

Set each setting value for the Fractional-N Synthesizer counter, according to the following equations.

$fvco_{RF} = N_{TOTAL} \times f_{OSC} \div R$

$N_{TOTAL} = P \times N + A + 3 + F/Q$

F: Set the numerator of fractional division with its fractional portion discarded.
When value F is even-numbered as a result of the division calculation, “1” is added to F.

b) Integer-N Synthesizer in the IF-PLL section

The Integer-N Synthesizer counter is set, according to the following equations.

$fvco_{IF} = N_{TOTAL} \times f_{OSC} \div R$

$N_{TOTAL} = P \times N + A$

$fvco_{RF}/fvco_{IF}$	:	Output frequency of externally connected VCO
N_{TOTAL}	:	Total number of divisions from prescaler input to phase comparator input
fosc	:	Reference oscillation frequency (OSCin input frequency)
R	:	RF side : Setting value for binary 6-bit reference counter (1 to 63) IF side : Setting value for binary 14-bit reference counter (1 to 16383)
P	:	RF side : Division ratio for prescaler (16) IF side : Division ratio for prescaler (8, 16)
N	:	RF side : Setting value for binary 7-bit programmable counter (5 to 127) IF side : Setting value for binary 11-bit programmable counter (3 to 2047)
A	:	RF side : Setting value for binary 4-bit swallow counter (0 to 15) IF side : Setting value for binary 4-bit swallow counter (0 to 127, A < N)
F	:	Numerator of fractional division (0 to 1048575, F < Q)
Q	:	Denominator of fractional division (2^{20} = 1048576)

c) Data bit description

Bit name	Description
F1RF to F20RF	Bits for setting the fractional numerator for the RF-PLL (Setting range: 0 to 1048575) (Refer to Table 1)
A1RF to A4RF	Bits for setting the division ratio of the RF-side swallow counter (Setting range: 0 to 15) (Refer to Table 2)
N1RF to N7RF	Bits for setting the RF-side main counter (Setting range: 5 to 127) (Refer to Table 3)
R1RF to R6RF	Bits for setting the division ratio of the RF-side reference counter (Setting range: 1 to 63) (Refer to Table 4)
A1IF to A7IF	Bits for setting the division ratio of the IF-side swallow counter (Setting range: 0 to 127) (Refer to Table 5)
N1IF to N11IF	Bits for setting the IF-side main counter (Setting range: 3 to 2047) (Refer to Table 6)
R1IF to R14IF	Bits for setting the division ratio of the IF-side reference counter (Setting range: 3 to 16383) (Refer to Table 7)
TMC	Control bit for setting Speedup Mode (Refer to Table 9) TMC_bit = "0"→ disabled TMC_bit = "1"→ enabled
TM1 to TM7	Bits for setting the speedup timer (Refer to Table 8)
PSRF	Power saving bit for the RF-PLL section
FCRF	Phase switching bit for the RF-side phase comparator (Refer to Table 11)
ODSW	Control bit for the open-drain switch ODSW bit = "0"→Dynamic ODSW bit = "1"→OFF
FCIF	Phase switching bit for the IF-side phase comparator (Refer to Table 11)
CSIF	Charge pump switching bit for the IF-PLL section CSIF bit = "0"→ Icp = ±1.5mA CSIF bit = "1"→ Icp = ±6.0mA
SWIF	Bits for setting the division ratio of the IF-side prescaler SWIF = "0"→ 16/17 SWIF = "1"→ 8/9
PSIF	Power saving bit for the IF-PLL section
LDS, T1, T2	Control bits for selecting monitor function (Refer to Table 10)
SC	Bit for switching the order of ΣΔ SC bit = "0"→ 2nd order SC bit = "1"→ 3rd order
×	Dummy bit: Must be fixed to "0"

Table 1 - Fractional counter F numerator value Setting

Setting value (F)	F20 RF	F19 RF	F18 RF	F17 RF	F16 RF	F15 RF	F14 RF	F13 RF	F12 RF	F11 RF	F10 RF	F9 RF	F8 RF	F7 RF	F6 RF	F5 RF	F4 RF	F3 RF	F2 RF	F1 RF
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1
6	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0
⋮	⋮																			
1048574	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
1048575	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Table 2 - Swallow counter setting

Setting value (A)	A4 RF	A3 RF	A2 RF	A1 RF
0	0	0	0	0
1	0	0	0	1
⋮	⋮			
14	1	1	1	0
15	1	1	1	1

Table 3 - Main counter setting

Setting value (N)	N7 RF	N6 RF	N5 RF	N4 RF	N3 RF	N2 RF	N1 RF
5	0	0	0	0	1	0	1
6	0	0	0	0	1	1	0
⋮	⋮						
126	1	1	1	1	1	1	0
127	1	1	1	1	1	1	1

Table 4 - Reference counter setting

Setting value (R)	R6 RF	R5 RF	R4 RF	R3 RF	R2 RF	R1 RF
1	0	0	0	0	0	1
2	0	0	0	0	1	0
⋮	⋮					
62	1	1	1	1	1	0
63	1	1	1	1	1	1

Table 5 - Swallow counter setting

Setting value (A)	A7 IF	A6 IF	A5 IF	A4 IF	A3 IF	A2 IF	A1 IF
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
⋮	⋮						
126	1	1	1	1	1	1	0
127	1	1	1	1	1	1	1

Table 6 - Main counter setting

Setting value (N)	N11 IF	N10 IF	N9 IF	N8 IF	N7 IF	N6 IF	N5 IF	N4 IF	N3 IF	N2 IF	N1 IF
3	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	1	0	0
⋮	⋮					⋮					
2046	1	1	1	1	1	1	1	1	1	1	0
2047	1	1	1	1	1	1	1	1	1	1	1

Table 7 - Reference counter setting

Setting value (R)	R14 IF	R13 IF	R12 IF	R11 IF	R10 IF	R9 IF	R8 IF	R7 IF	R6 IF	R5 IF	R4 IF	R3 IF	R2 IF	R1 IF
3	0	0	0	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	0	0	0	1	0	0
⋮	⋮						⋮							
16382	1	1	1	1	1	1	1	1	1	1	1	1	1	0
16383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Table 8 - Speedup timer update value setting

Setting value	TM 7	TM 6	TM 5	TM 4	TM 3	TM 2	TM 1
1	0	0	0	0	0	0	1
⋮	⋮						
126	1	1	1	1	1	1	0
127	1	1	1	1	1	1	1

case) fosc = 19.2 MHz

3.3
⋮
420.0
423.3

unit:µs

Charge pump current switching time = 64/fosc × TM

Table 9 - Charge pump output current setting

Charge pump output current	TMC
± 0.094 mA fixed	0
± 4.5 mA → ± 0.094 mA switched	1

Table 10 - LD/fout output setting

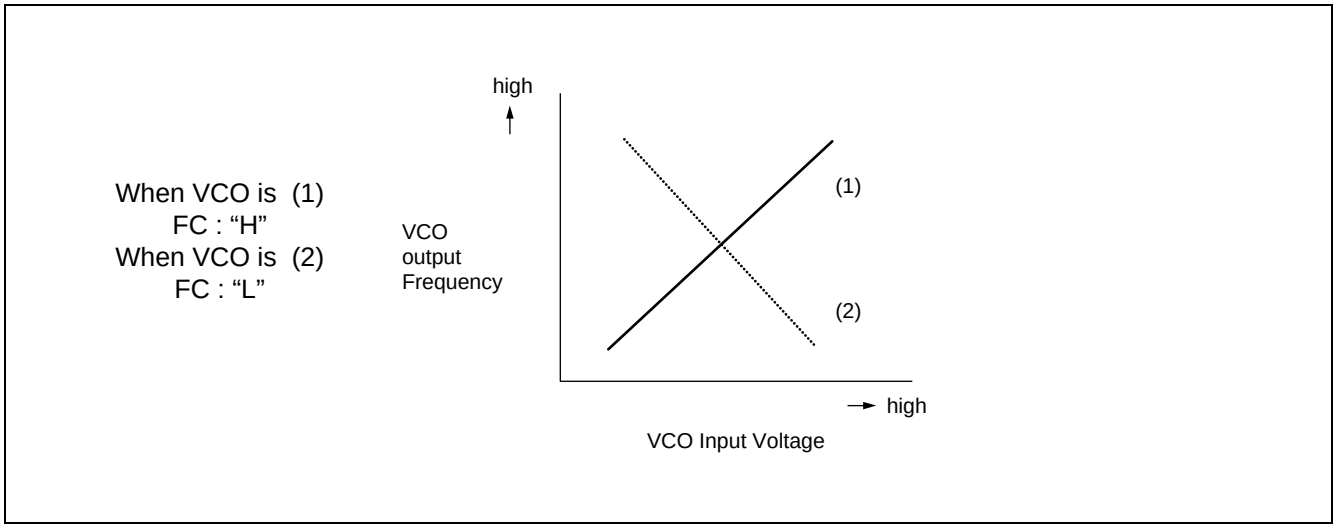
LD/fout		LDS	T1	T2	Maximum operating frequency [MHz]*
LD output		0	—	—	1800
fout	frIF	1	0	0	2000
	frRF	1	1	0	
	fpIF	1	0	1	
	fpRF	1	1	1	

* : The maximum operating frequency varies depending on the output state of the LD/fout pin (LD output or fout output).

Table 11 - Comparator polarity setting

	FC = "1"	**FC = "0"**
	Do	**Do**
fp < fr	H	L
fr < fp	L	H
fr = fp	Z	Z
VCO Polarity	(1)	(2)

Note : Set the FC bit in accordance with the low pass filter and VCO polarity, when designing a PLL frequency synthesizer.



3. Power Saving Mode (Intermittent Operation)

PSIF		IFPLL	PSRF		RFPLL
ExternalPIN	SerialData		ExternalPIN	SerialData	
0	0	Power save	0	0	Power save
0	1	Power save	0	1	Power save
1	0	Power save	1	0	Power save
1	1	Active	1	1	Active

The intermittent operation allows internal circuits to operate only when required and to stop otherwise. It is designed to control the power consumed by the entire circuit block. However, if the circuit starts operating directly from a stop state, the phase relation is undefined, even when the comparison frequency (fp) is the same as the reference frequency (fr) input to the phase comparator. As a result, the phase comparator generates excessive error signals, causing the problem of unlocking the PLL. To solve this problem, the intermittent operation control has been implemented to control fluctuations in the locked frequency by performing forcible phase adjustment at the beginning of operation.

- Operation mode

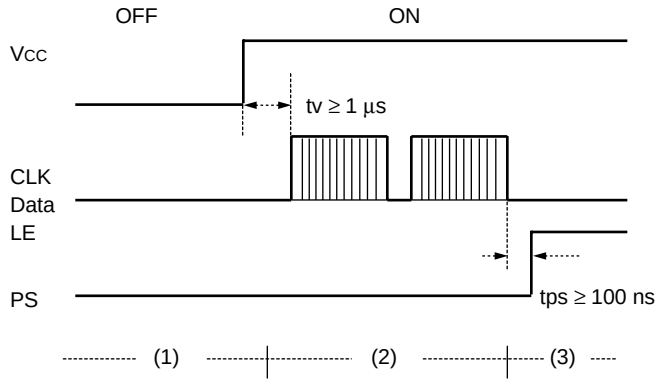
The set channel and crystal oscillator circuit are in operation and the PLL performs normal operation.

- Power save mode

This mode realizes low current consumption by stopping the circuits which will not cause any problem even when stopped. In this condition, the standard consumption current is 0.1 μA per channel with the maximum of 10 μA.

At this point, Do and LD are set to the same levels as when the PLL was locked. The Do enters a high impedance state, and the voltage input to the voltage control oscillator (VCO) remains the same as the voltage for operation mode (i.e. locked state) with the time constant of the low pass filter. Therefore, the VCO output frequency can be maintained almost at the same level as the lock frequency.

Notes :
- When power (VCC) is first applied, the device must be in power saving mode (external pin = L, due to the undefined serial data) .
- The serial data input after the power supply became stable, and then the power saving mode is released after completed the data input.

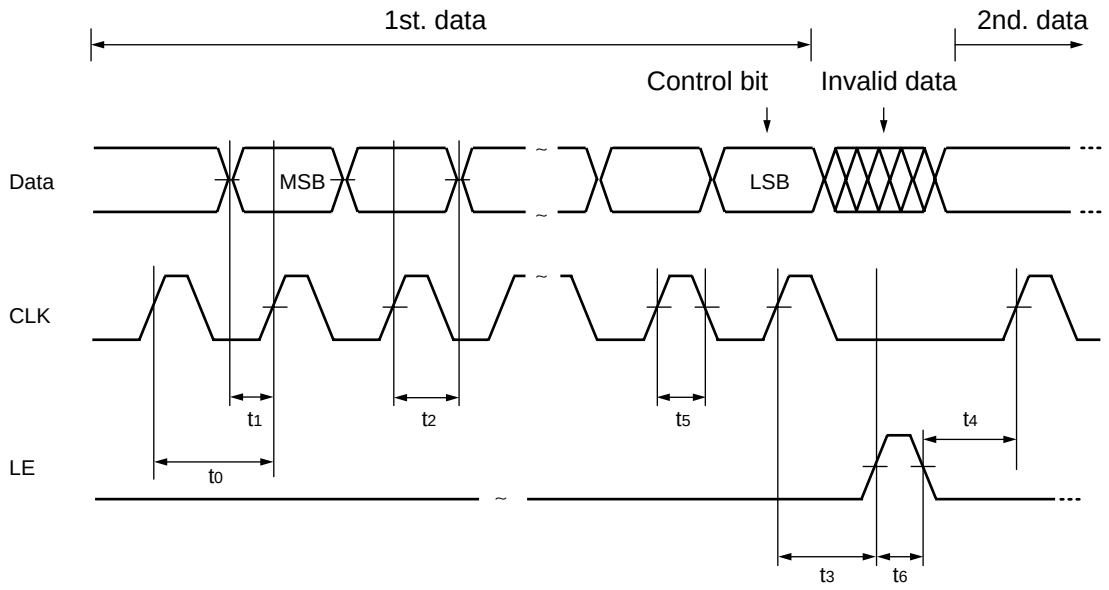


(1) PS = L (power saving mode) at Power ON
(2) Set serial data 1 μs later after power supply remains stable ($V_{CC} \geq 2.2$ V) .
(3) Release power saving mode (PS : L → H)

4. Serial Data Input Timing

Divide ratio is performed through a serial interface using the Data pin, Clock pin, and LE pin.

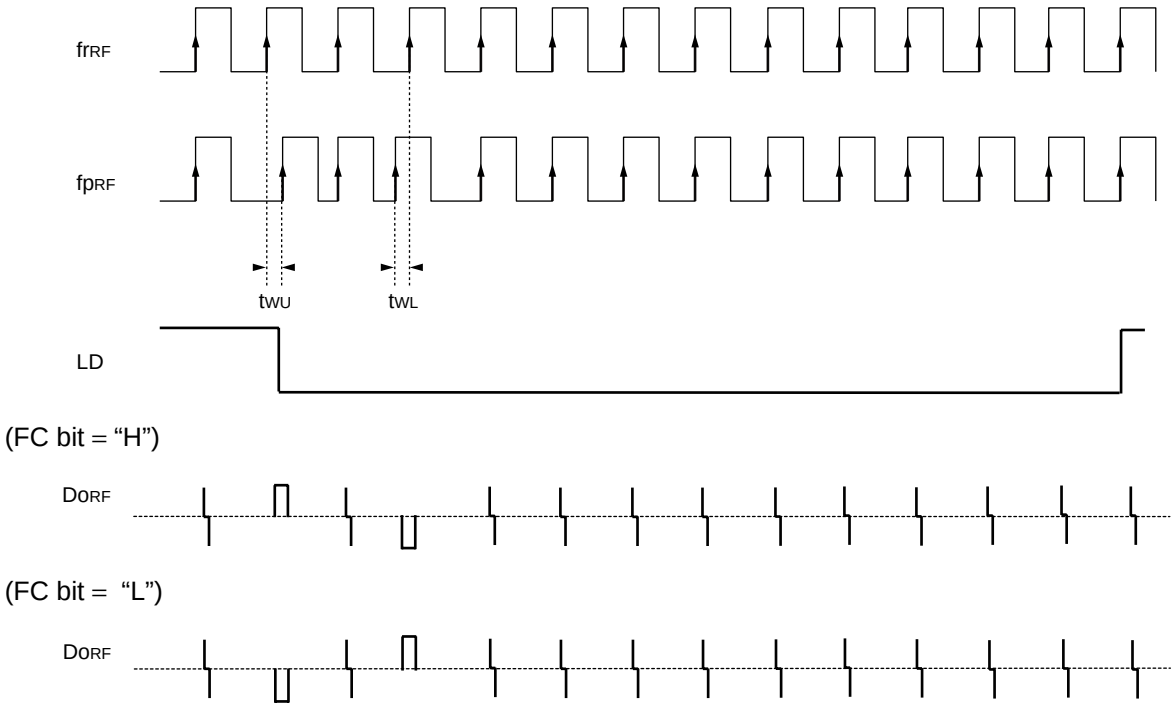
Setting data is read into the shift register at the rise of the Clock signal, and transferred to a latch at the rise of the LE signal. The following diagram shows the data input timing.



100 ns ≤ t_0, t_6 20 ns ≤ t_1, t_2, t_4 30 ns ≤ t_3, t_5

LE should be “L” when the data is transferred into the shift register.

■ PHASE COMPARATOR OUTPUT WAVEFORM



• LD Output Logic

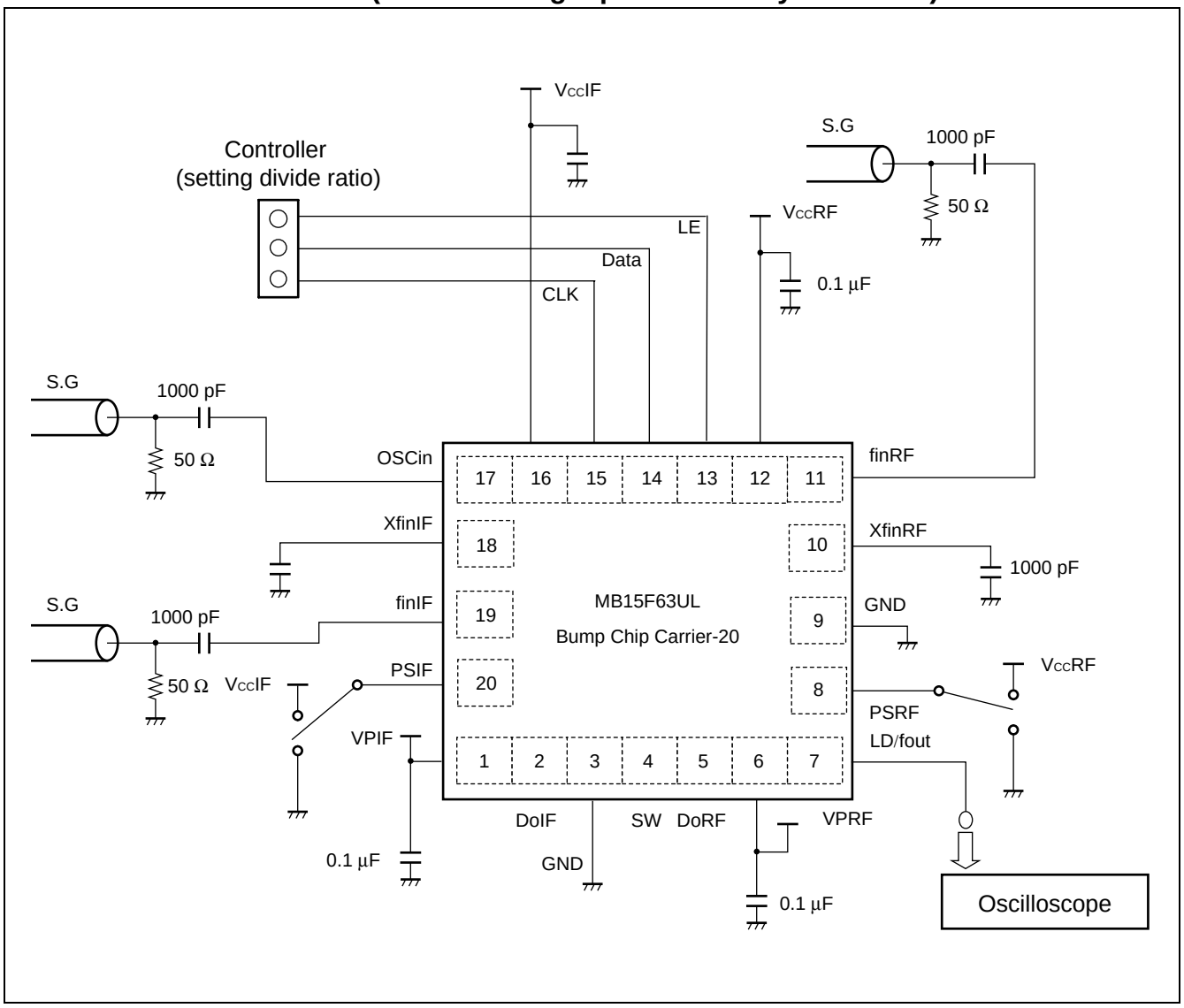
IF-PLL section	RF-PLL section	LD output
Locking state/Power saving state	Locking state/Power saving state	H
Locking state/Power saving state	Unlocking state	L
Unlocking state	Locking state/Power saving state	L
Unlocking state	Unlocking state	L

Notes :
- Phase error detection range : -2π to $+2\pi$
- Pulses on Do signal during locked state are output to prevent dead zone.

RF-PLL section :
- LD output becomes "L" when phase is t_{WU} or more. LD output becomes "H" when phase error is t_{WL} or less and continues to be so for ten cycles or more.
- t_{WU} and t_{WL} depend on fin input frequency.
  $t_{WU} \geq 1 / (fin / 16)$ [s] ex.) fin = 1629.9 MHz : $t_{WU} \geq 9.82$ ns
  $t_{WL} \leq 2 / (fin / 16)$ [s] : $t_{WL} \leq 19.63$ ns

IF-PLL section
- LD output becomes "L" when phase is t_{WU} or more. LD output becomes "H" when phase error is t_{WL} or less and continues to be so for three cycles or more.
- t_{WU} and t_{WL} depend on OSCin input frequency.
  $t_{WU} \geq 2 / fosc$ [s] ex.) fosc = 13.0 MHz : $t_{WU} \geq 153$ ns
  $t_{WL} \leq 4 / fosc$ [s] : $t_{WL} \leq 256$ ns

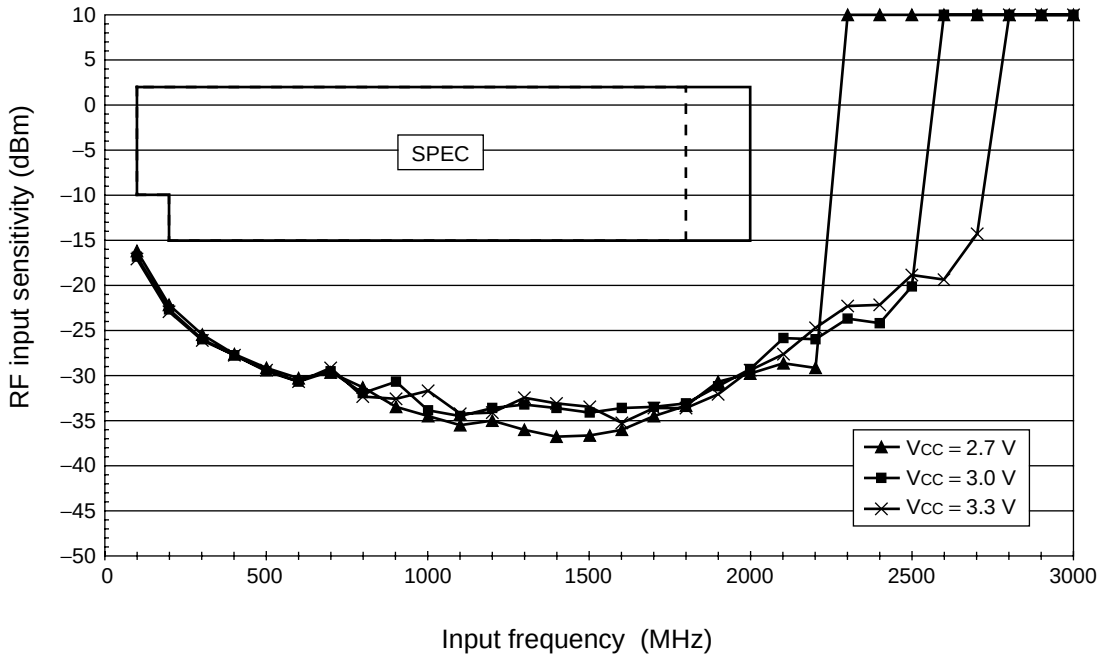
■ MEASURMENT CIRCUIT (for Measuring Input Sensitivity fin/OSCin)



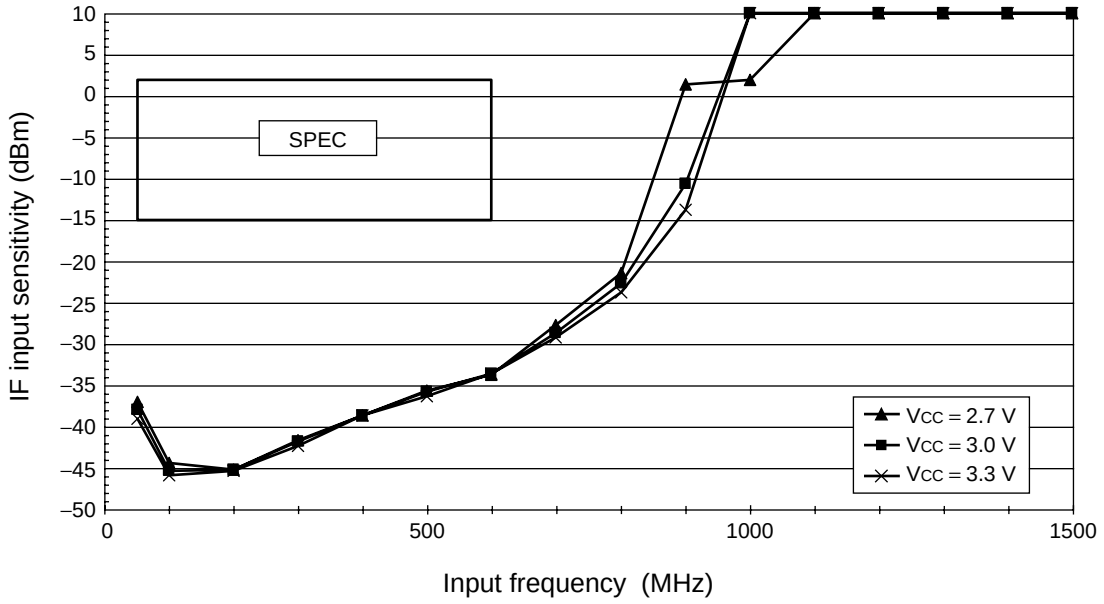
■ TYPICAL CHARACTERISTICS

1. fin Input Sensitivity

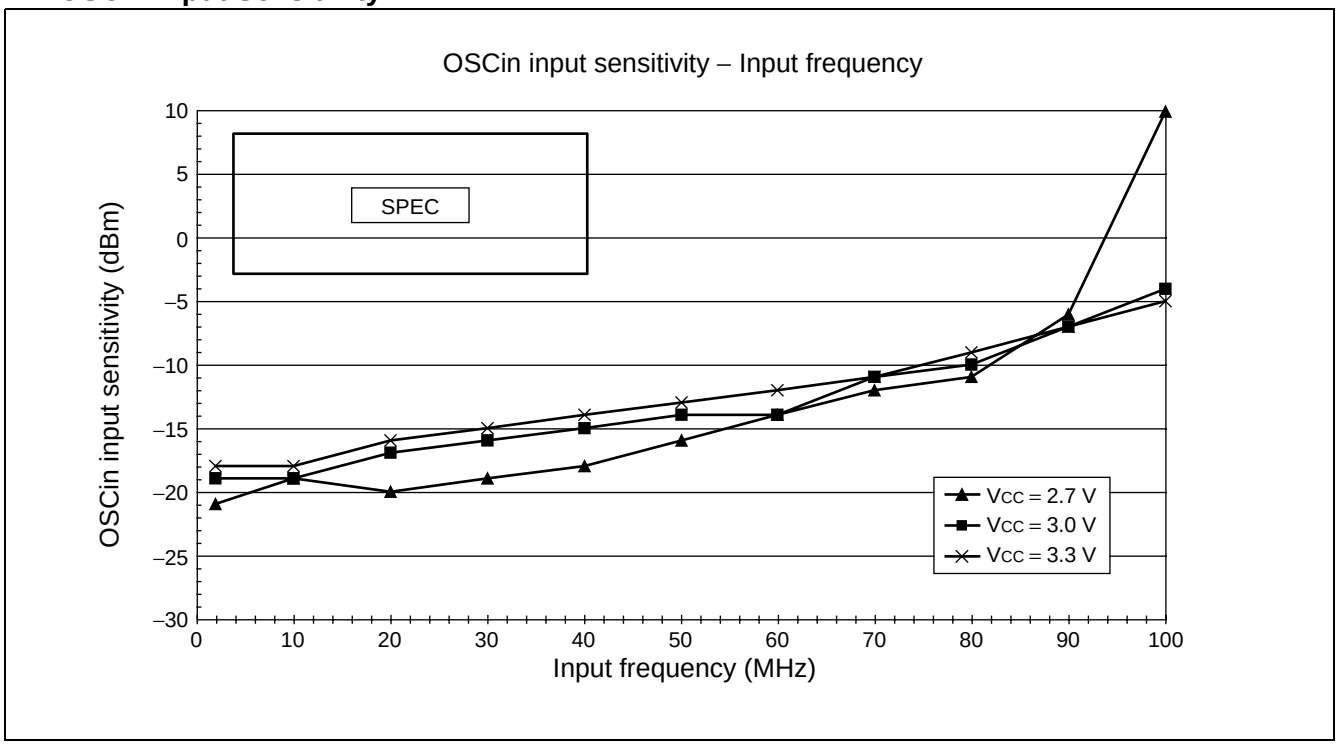
RF input sensitivity – Input frequency



IF input sensitivity – Input frequency

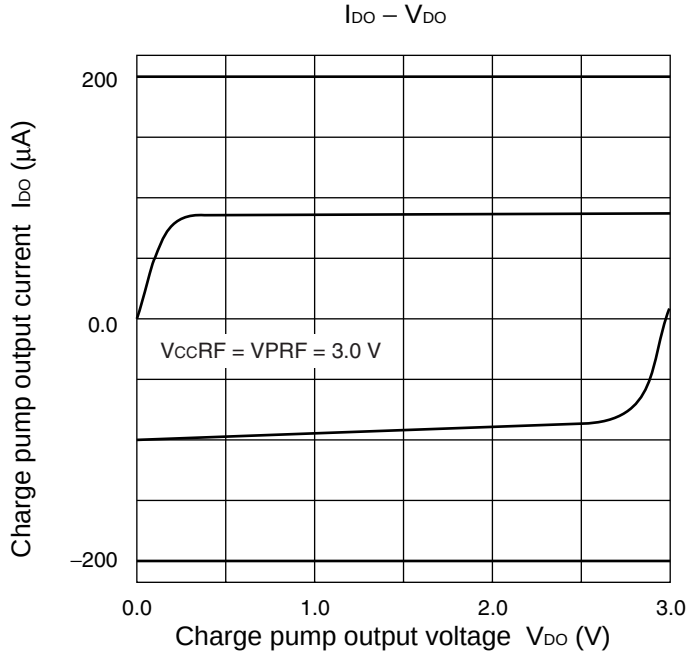


2. OSCin Input Sensitivity

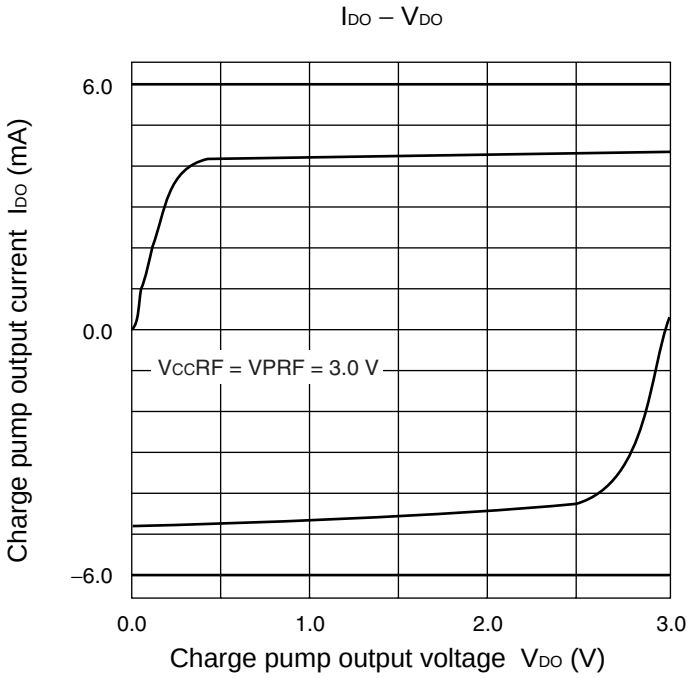


3. RF Do output current

- CP = 94 µA

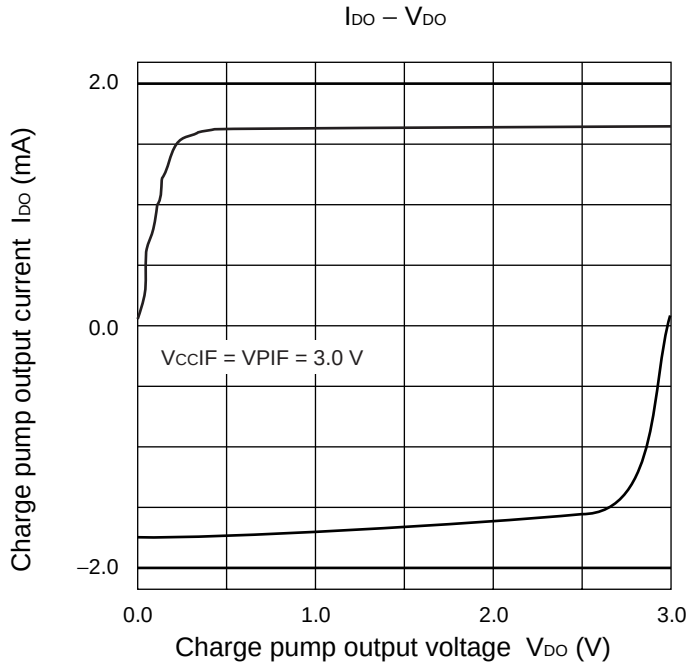


- CP = 4.5 mA

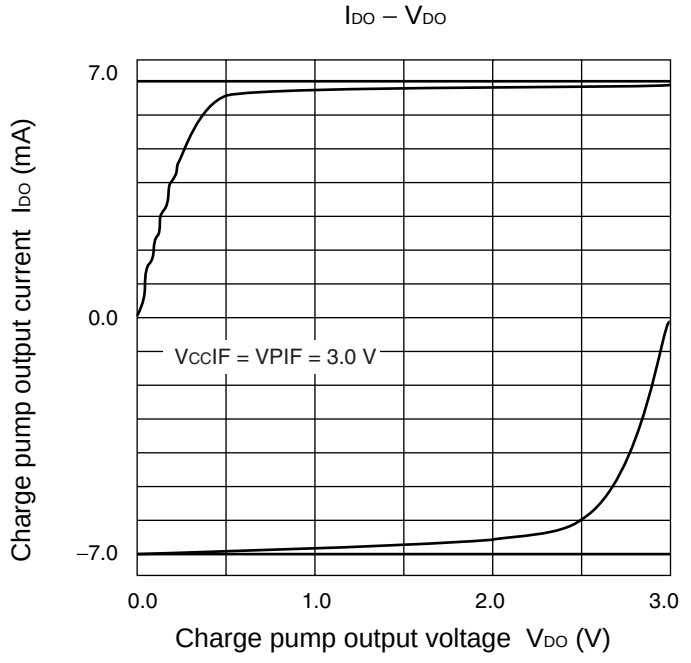


4. IF Do output current

- CP = 1.5 mA

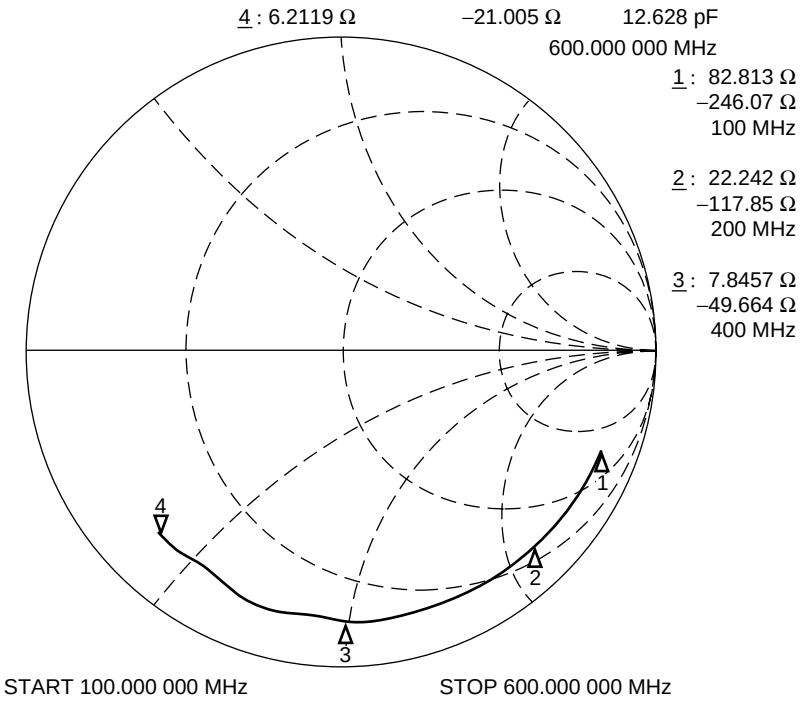


- CP = 6 mA

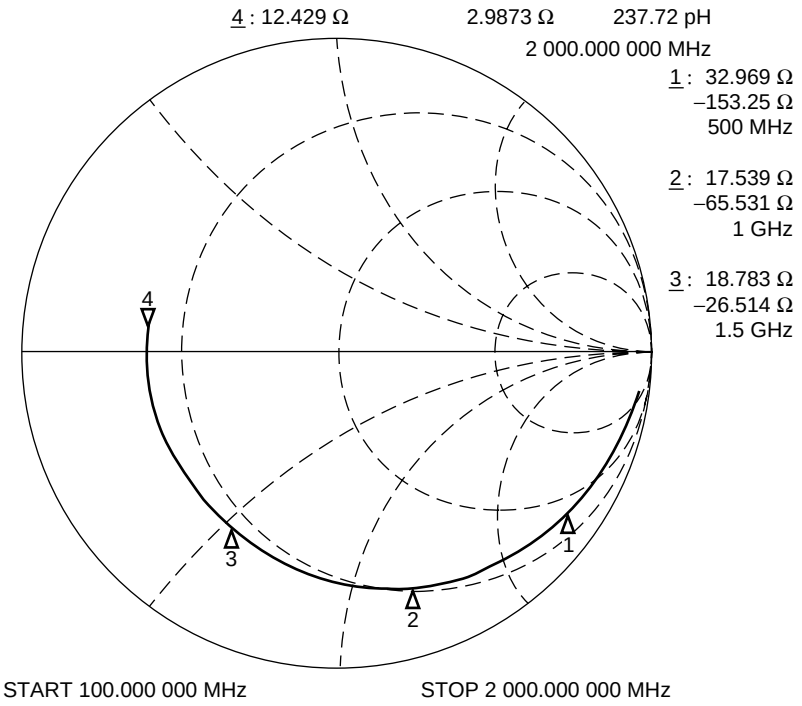


5. fin input impedance

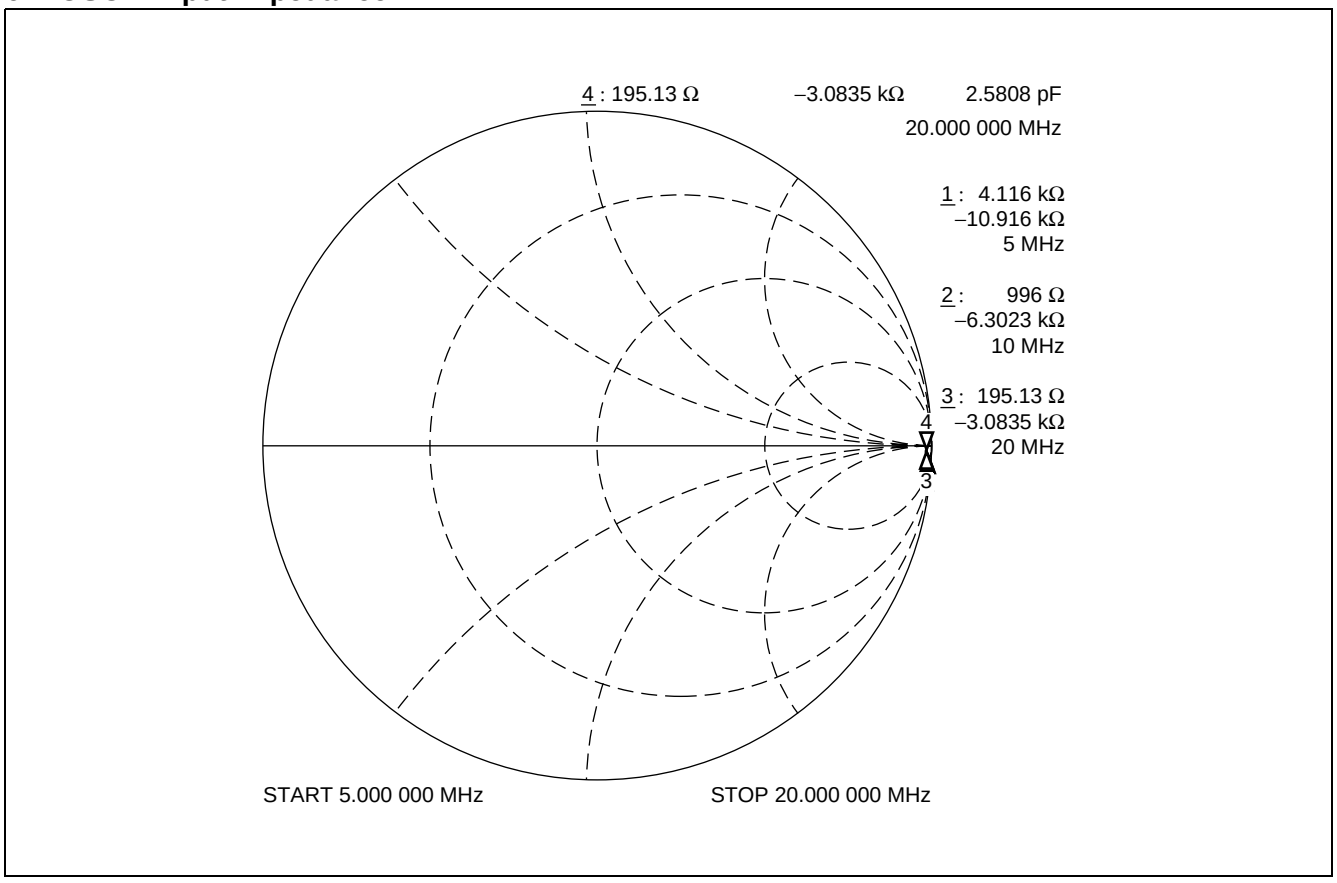
finIF input impedance



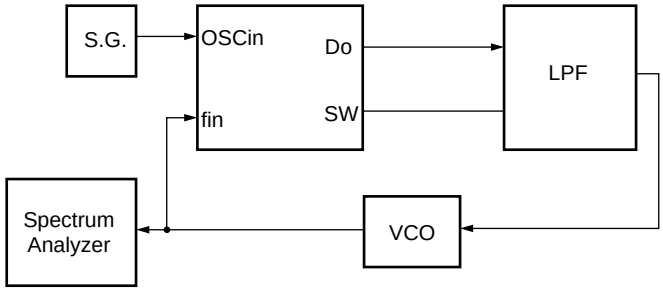
finRF input impedance



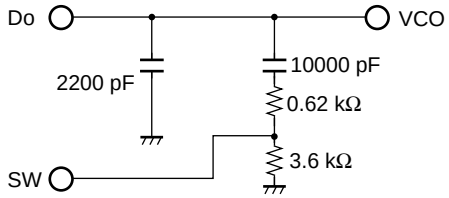
6. OSCin input impedance



■ REFERENCE INFORMATION

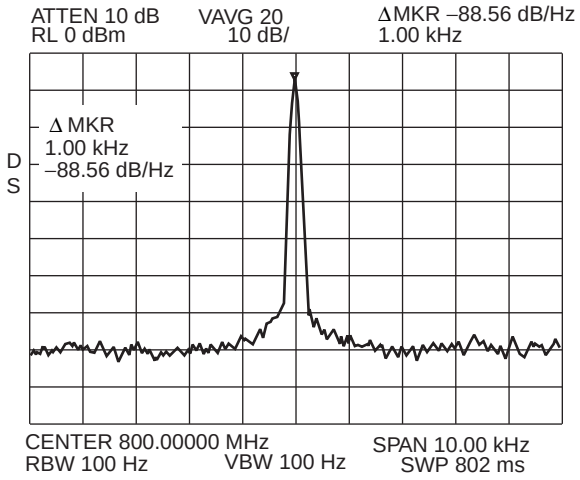


fvco = 800 MHz Vcc = Vp = 3.0 V
Kv = 25 MHz/V Vvco = 5.0 V
fr = 6.5 MHz (R = 2) Ta = + 25 °C
fosc = 13.0 MHz TMC = “1”, TM = “4”
CS = “0”, ODSW = “0”, SC = “1”, MODE = “0”

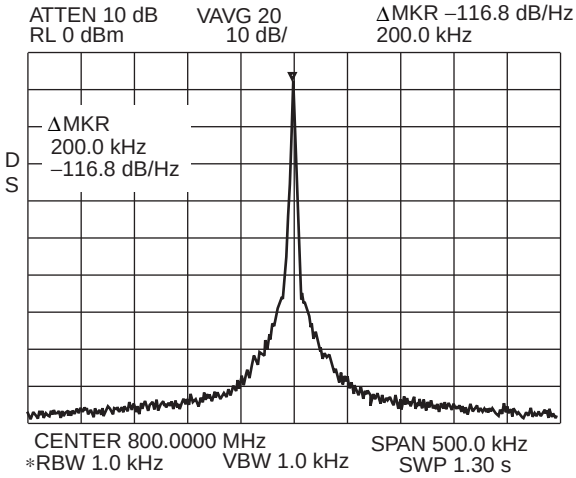


• PLL Phase Noise & Spurious Noise

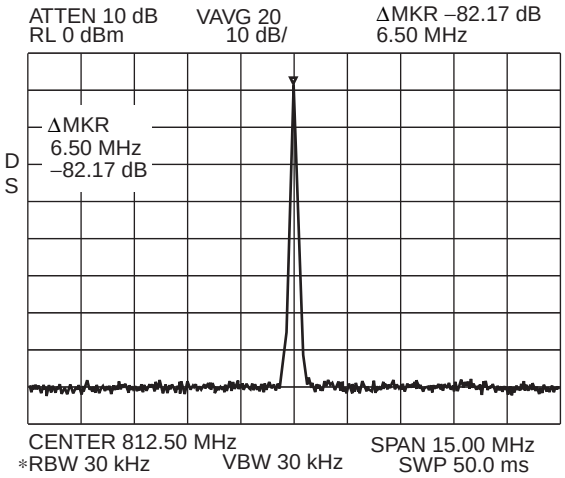
C/N 1 kHz Offset



C/N 200 kHz Offset



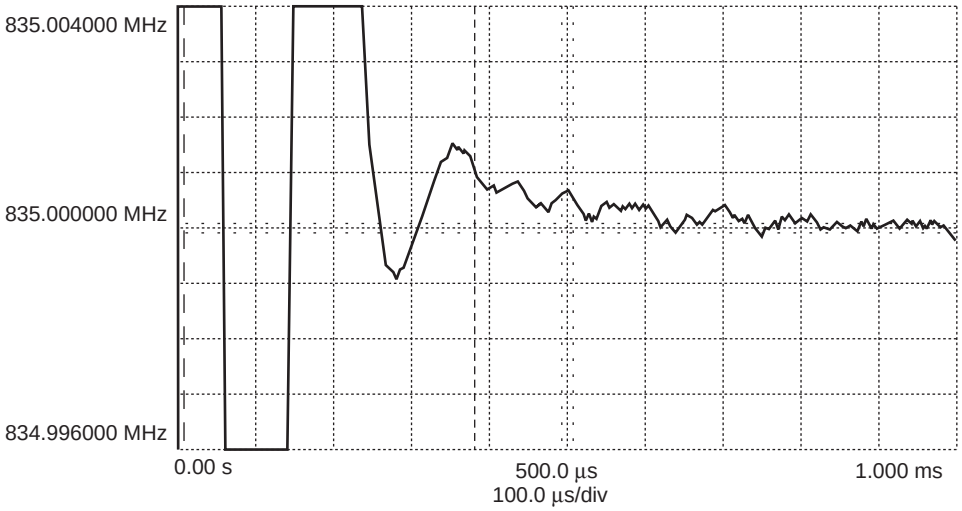
Ref. Leakage 6.5 MHz Offset



PLL Lock Up time

L : 800 MHz → H : 835 MHz ± 1 kHz

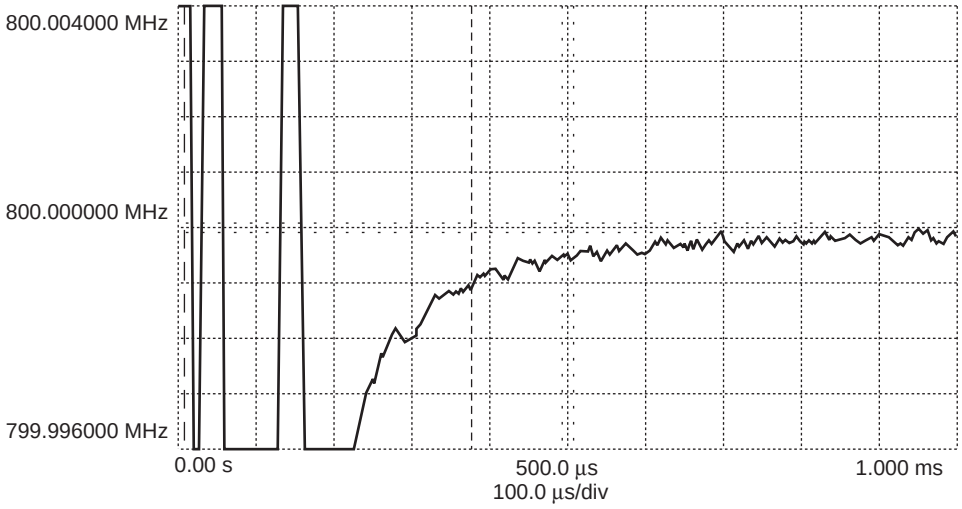
L ch → H ch 373 µs



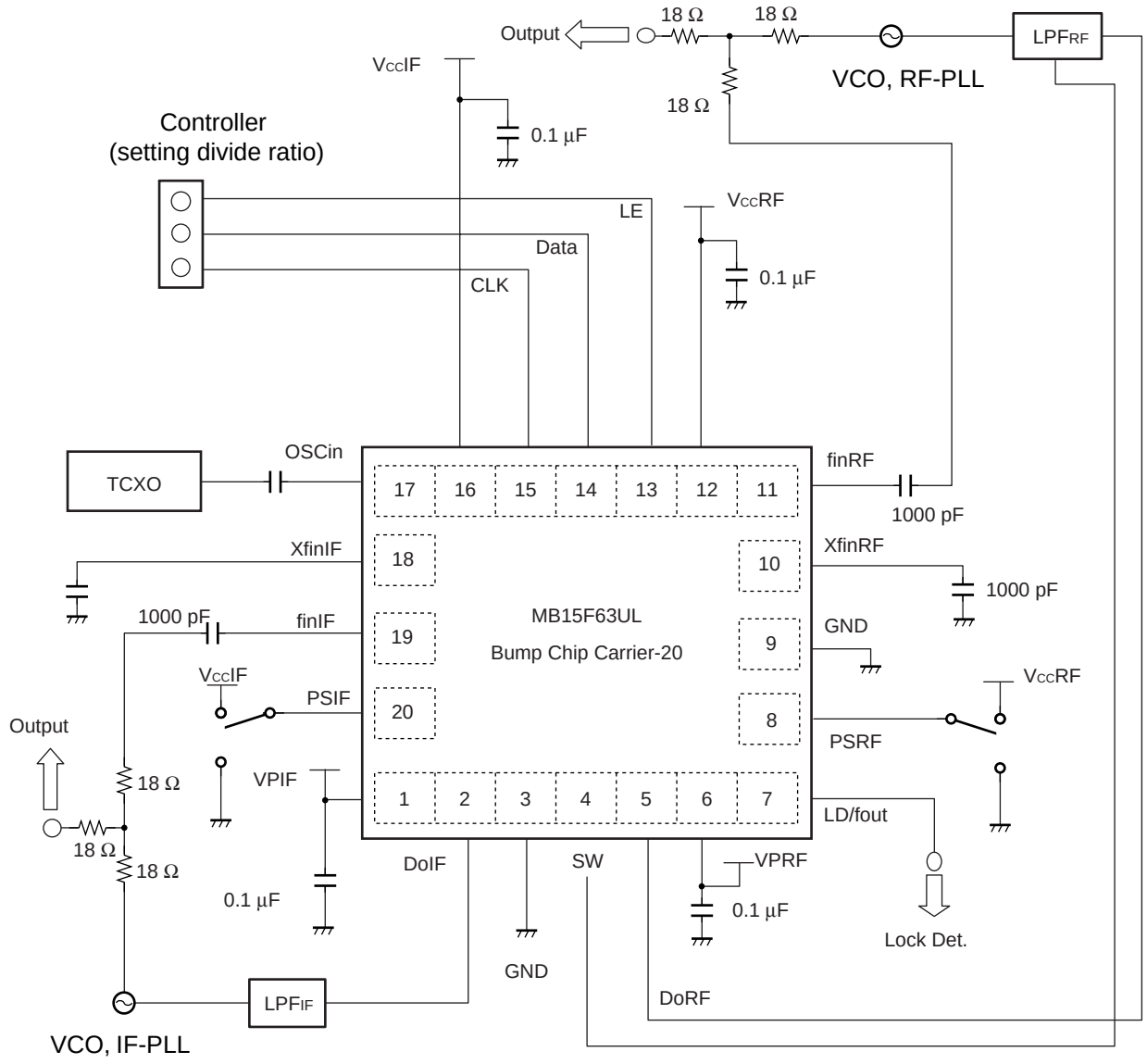
PLL Lock Up time

H : 835 MHz → L : 800 MHz ± 1 kHz

H ch → L ch 364 µs



■ APPLICATION EXAMPLE



Note : CLK, Data and LE are the built-in schmitt trigger circuits (insert a pull-down or pull-up register to prevent oscillation when open-circuit in the input) .

■ PRECAUTIONS FOR USE

The Fractional-N PLL used in the RF section is based on the ΣΔ system and has the following characteristics.

(1) Integer operation when F = 0

When F is set to “0”, the ΣΔ circuit block is stopped completely and the same operation as a normal Integer product is performed. Therefore, the most preferable noise characteristics can be achieved.

(2) Generation of spurious signals

1.Spurious signals are generated in the offset part of fp, which is a comparison frequency (equivalent of a reference leak in the integer type).

Example:

If fosc is set to 13 MHz and R is set to 2 when fvco is 800 MHz in the GSM 800 MHz band, Ntotal becomes 124 and F becomes 0. (Integer mode)
Spurious signals are generated at “fp / R = 13 MHz / 2 = 6.5 MHz” offset. (Reference leak)

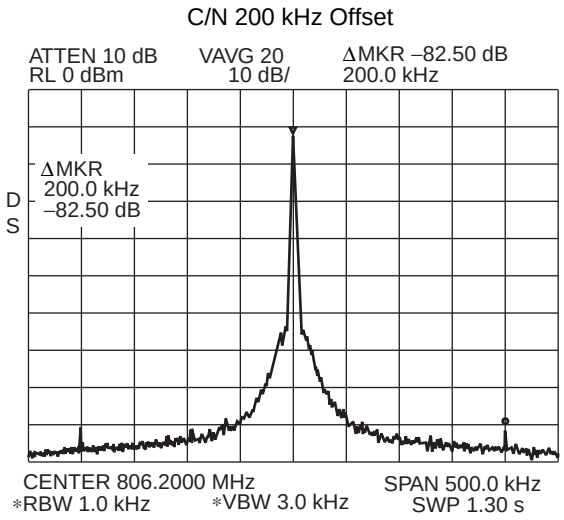
(The waveform resembles that of the reference leakage shown on Ref Leakage of “REFERENCE INFORMATION”. A filter can be used to eliminate the effects.)

2. Due to the ΣΔ circuit operation, spurious signals are generated where “F / Q × fp” or “(Q – F) / Q × fp” is located.

Example:

fosc = 13 MHz; R = 2 in GSM 800 MHz band:

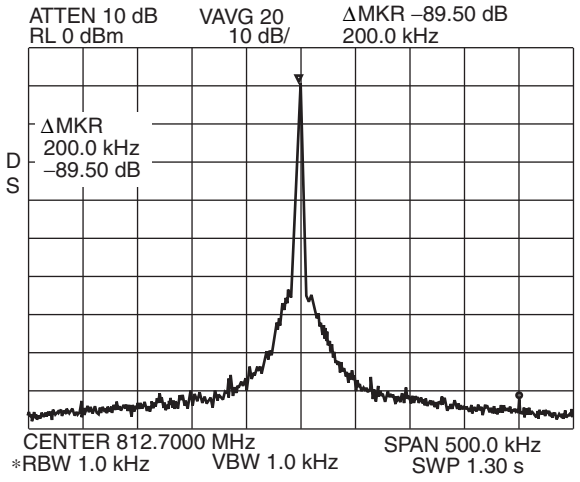
When fvco is 806.2 MHz, Ntotal becomes 142.0307692... and F becomes 32263. Consequently, spurious signals are generated at “F / Q × fp ≒ 200 kHz” offset.



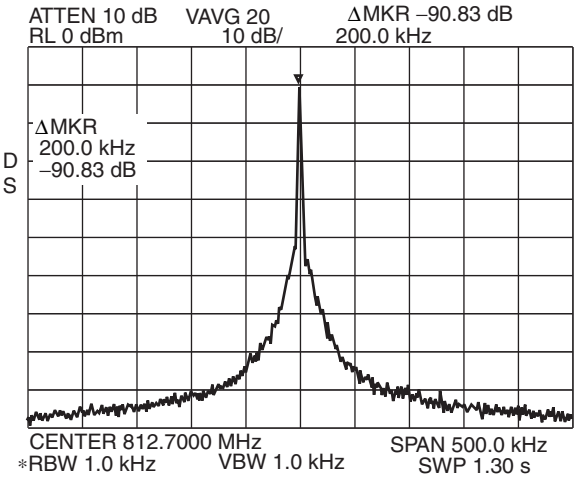
Adjusting the filter may reduce these spurious signals. Furthermore, modifying R and fr may change the setting value to avoid to generate spurious signals.
For example, when fosc = 13 MHz and R = 2, Ntotal becomes 125.0307692…, where fvco is 812.7 MHz. Therefore, F becomes 32263. Spurious signals are supposed to be generated at “F / Q × fp≒ 200 kHz” and 200 kHz offset. However, if R is changed to 3, F will become 572683 and “F / Q × fp ≒ 2.366 MHz” and spurious signals will be the outer frequencies. Therefore, the effects will not be foreseen.

Note that the problem cannot be avoided when the setting value of the swallow counter (A) is odd-numbered (also applicable to the 806.2 MHz environment, used in the above explanation).
However, the spurious signals can be reduced by changing fr (reducing it) to limit the band. Note that in this case, the comparison frequency itself changes, resulting in a change in the loop band and deterioration of CN. Therefore,each case should be handled in accordance with the system used. Some example waveforms are attached to the following.

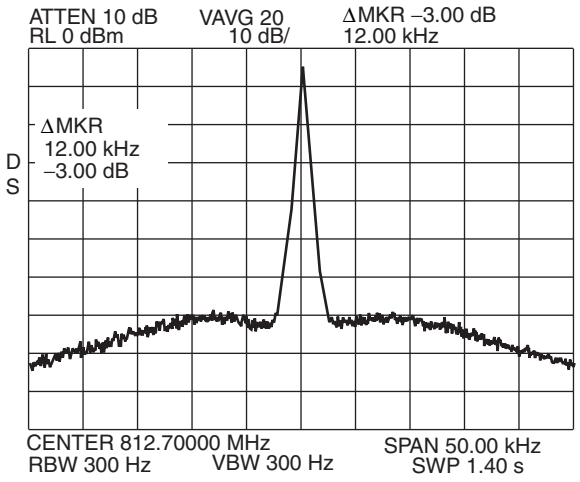
R = 2 (200 kHz offset)



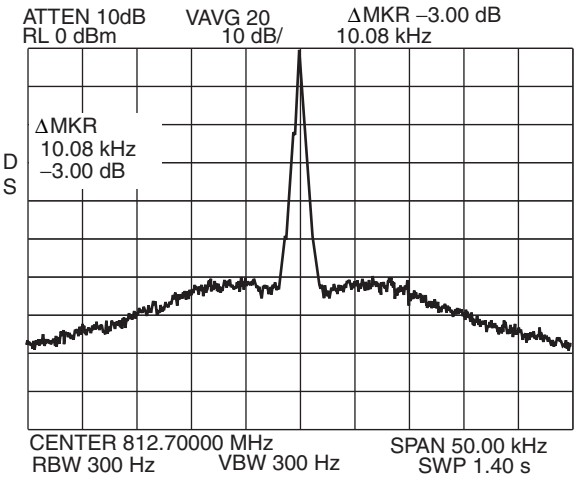
R = 3 (200kHz offset)



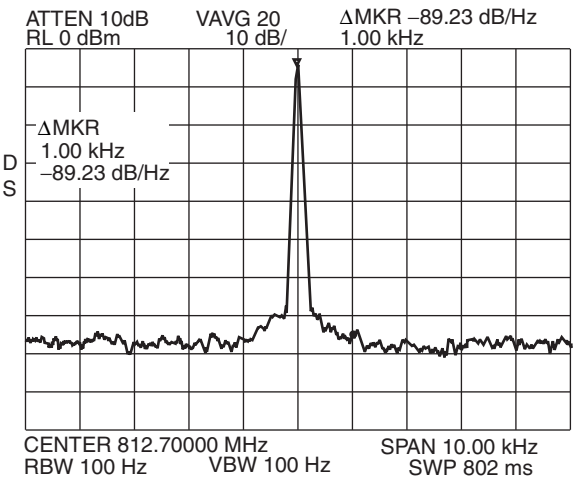
R = 2 (loop band waveform)



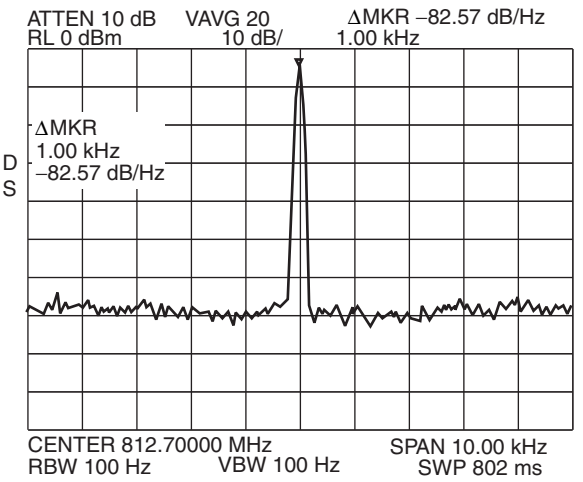
R = 3 (loop band waveform)



R = 2 (1kHz offset)



R = 3 (1kHz offset)



3. Excessive spurious signals are generated when setting a binary division such as F/Q = 1/2, 1/4, 1/8…
If it is difficult to reduce the excess level, value F can be shifted to the acceptable range of frequency differences to reduce it.

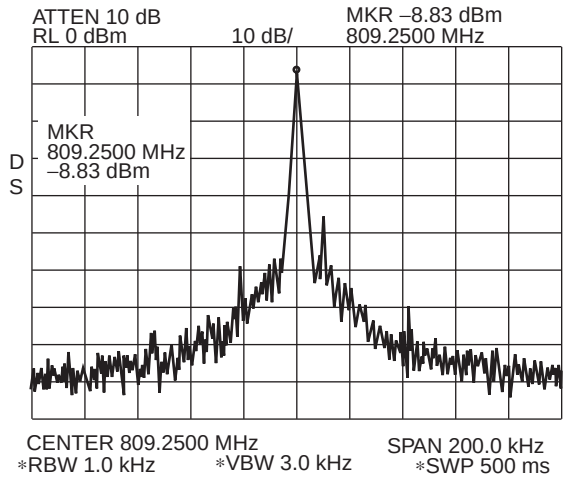
Example:

Spurious noise is generated on the entire floor when F = 524288 (F/Q = 1/2).

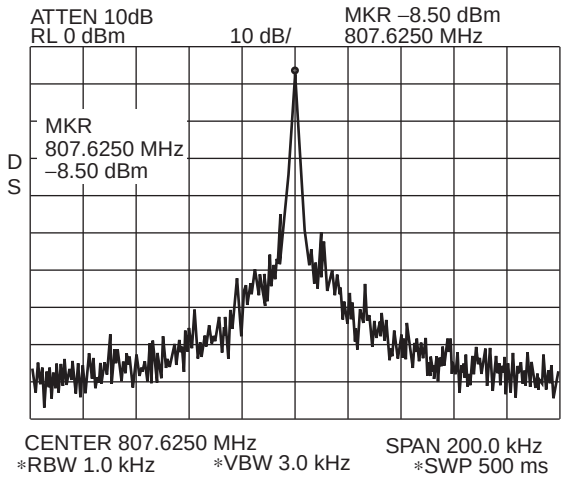
Spurious noise is generated on the entire floor when F = 262144 (F/Q = 1/4).

The following section shows examples of spurious waveforms generated in the above cases as well as examples of waveforms when 5 and 10 are added to value F.

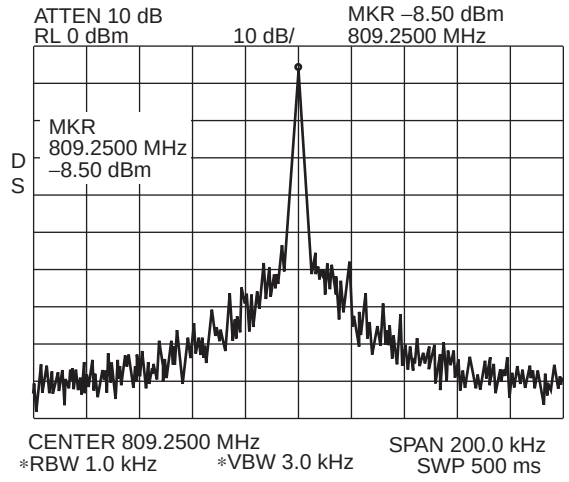
F = 524288(F/Q = 1/2)



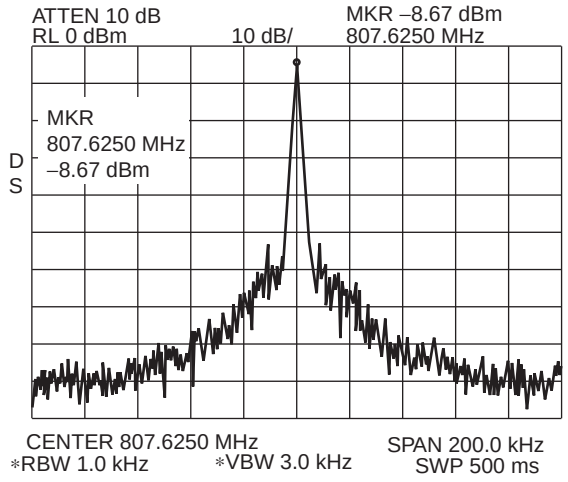
F = 262144(F/Q = 1/4)



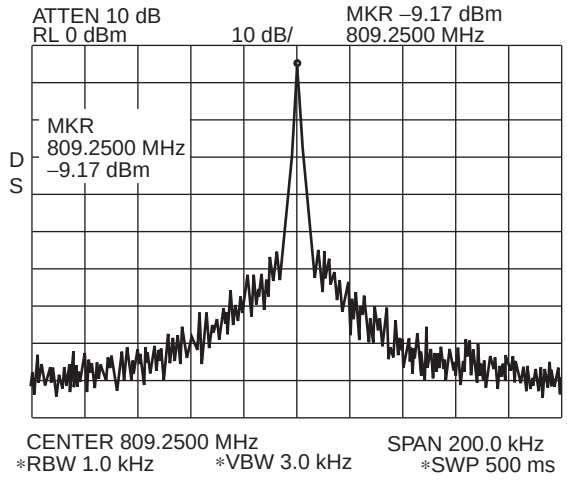
F = 524288 + 5



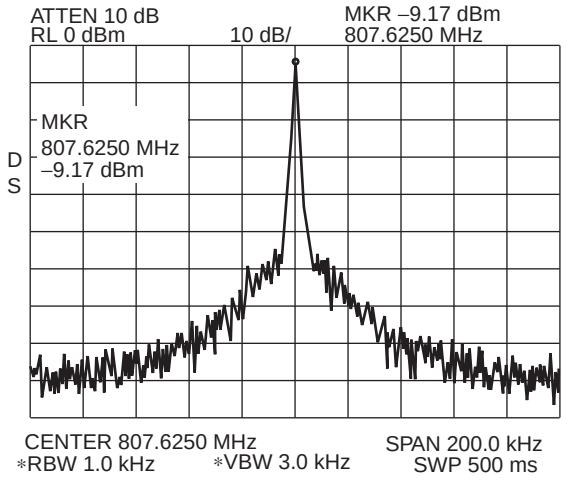
F = 262144 + 5



F = 524288 + 10



F = 262144 + 10



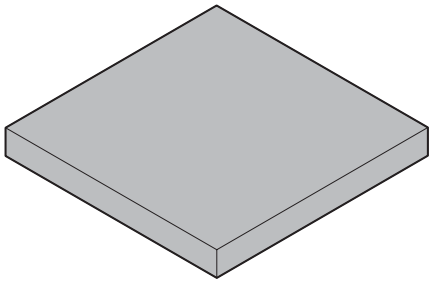
Notes : • V_{CC}RF and V_{CC}IF must be equal voltage.
Even if either RF-PLL or IF-PLL is not used, power must be supplied to V_{CC}RF and V_{CC}IF to keep them equal. It is recommended that the non-use PLL is controlled by power saving function.

• To protect against damage by electrostatic discharge, note the following handling precautions :
- Store and transport devices in conductive containers.
- Use properly grounded workstations, tools, and equipment.
- Turn off power before inserting device into or removing device from a socket.
- Protect leads with a conductive sheet when transporting a board-mounted device.

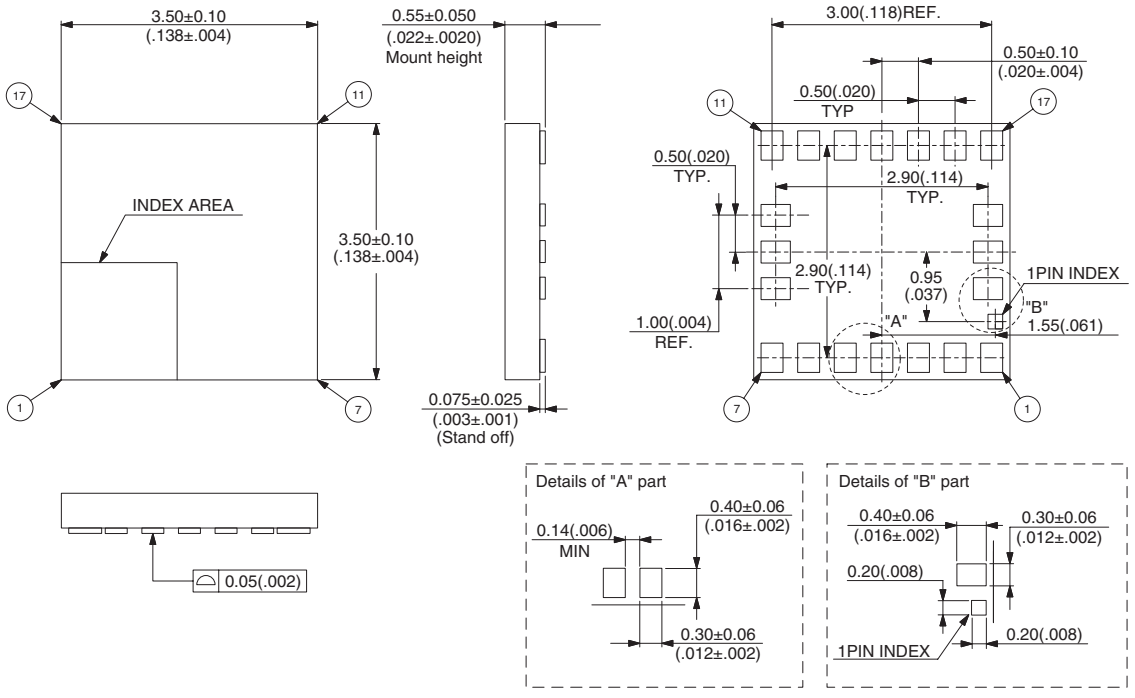
■ ORDERING INFORMATION

Part number	Package	Remarks
MB15F63ULPVA1	20-pin, Plastic BCC (LCC-20P-M06)	

■ PACKAGE DIMENSIONS

20-pin plastic BCC		
	Lead pitch	0.50 mm
	Package width × package length	3.50 mm × 3.50 mm
	Sealing method	Plastic mold
	Mounting height	0.60 mm MAX
	Weight	0.01 g
(LCC-20P-M06)		

20-pin plastic BCC
(LCC-20P-M06)



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

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If any products described in this document represent goods or technologies subject to certain restrictions on export under the Foreign Exchange and Foreign Trade Law of Japan, the prior authorization by Japanese government will be required for export of those products from Japan.

Edited Business Promotion Dept.