



# STD40NF10

N-channel 100V - 0.025Ω - 50A - DPAK  
STripFET™ II Power MOSFET

PRELIMINARY DATA

## General features

Type	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>
STD40NF10	100V	< 0.028Ω	50A

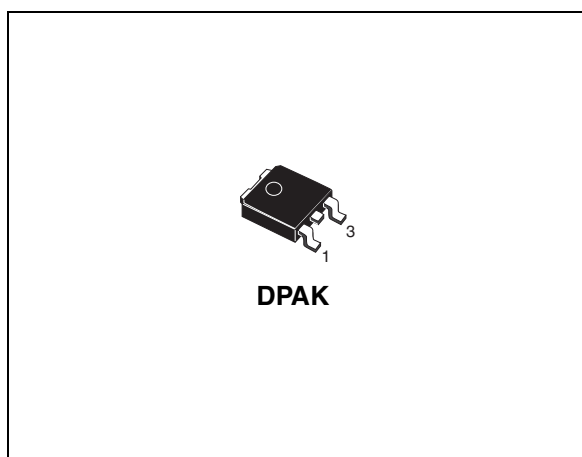
- 100% avalanche tested
- Exceptional dv/dt capability

## Description

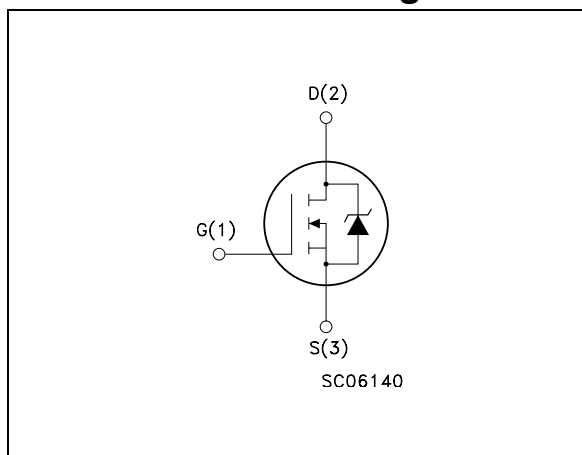
This Power MOSFET is the latest development of STMicroelectronics unique 'single feature size™' strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

## Applications

- Switching application



## Internal schematic diagram



## Order codes

Part number	Marking	Package	Packaging
STD40NF10	D40NF10	DPAK	Tape & reel

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# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage ( $V_{GS}=0$ )	100	V
$V_{GS}$	Gate-source voltage	$\pm 20$	V
$I_D$	Drain current (continuous) at $T_C = 25^\circ\text{C}$	50	A
$I_D$	Drain current (continuous) at $T_C = 100^\circ\text{C}$	35	A
$I_{DM}^{(1)}$	Drain current (pulsed)	200	A
	Derating factor	0.8	W/ $^\circ\text{C}$
$P_{TOT}$	Total dissipation at $T_C = 25^\circ\text{C}$	120	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	20	V/ns
$E_{AS}^{(3)}$	Single pulse avalanche energy	385	mJ
$T_j$ $T_{stg}$	Operating junction temperature Storage temperature	-55 to 175	$^\circ\text{C}$

1. Pulse width limited by safe operating area
2.  $I_{SD} \leq 50\text{A}$ ,  $di/dt \leq 600\text{A}/\mu\text{s}$ ,  $V_{DD} \leq V_{(BR)DSS}$ ,  $T_J < T_{JMAX}$
3. Starting  $T_j=25^\circ\text{C}$ ,  $I_D=20\text{A}$ ,  $V_{DD}=25\text{V}$

**Table 2. Thermal data**

Symbol	Parameter	Value	Unit
Rthj-case	Thermal resistance junction-case max	1.25	$^\circ\text{C}/\text{W}$
Rthj-amb	Thermal resistance junction-amb max	100	$^\circ\text{C}/\text{W}$

## 2 Electrical characteristics

( $T_{CASE}=25^{\circ}\text{C}$  unless otherwise specified)

**Table 3. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250\mu\text{A}$ , $V_{GS} = 0$	100			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = \text{Max rating}$ , $V_{DS} = \text{Max rating}$ , $T_c = 125^{\circ}\text{C}$			1 10	$\mu\text{A}$ $\mu\text{A}$
$I_{GSS}$	Gate body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 20\text{V}$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 250\mu\text{A}$	2	3	4	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{V}$ , $I_D = 25\text{A}$		0.025	0.028	$\Omega$

**Table 4. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
gfs	Forward transconductance	$V_{DS} = 15\text{V}$ , $I_D = 25\text{V}$		22		S
$C_{iss}$	Input capacitance	$V_{DS} = 25\text{V}$ , $f = 1\text{MHz}$ , $V_{GS} = 0$		2180		pF
$C_{oss}$	Output capacitance			298		pF
$C_{rss}$	Reverse transfer capacitance			83.7		pF
$Q_g$	Total gate charge	$V_{DD} = 80\text{V}$ , $I_D = 50\text{A}$		57.6	76	nC
$Q_{gs}$	Gate-source charge	$V_{GS} = 10\text{V}$		13.3		nC
$Q_{gd}$	Gate-drain charge	(see Figure 2)		17.5		nC

**Table 5. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD}=80V, I_D=25V$ $R_G=4.7\Omega, V_{GS}=10V$ <i>(see Figure 2)</i>		21		ns
$t_r$	Rise time			46		ns
$t_{d(off)}$	Turn-off delay time			54		ns
$t_f$	Fall time			13		ns

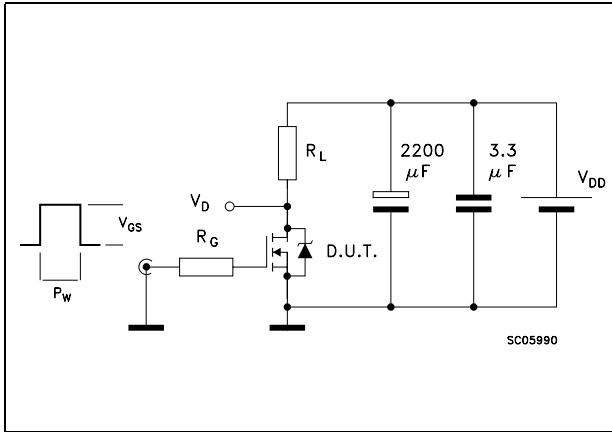
**Table 6. Source drain diode**

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
$I_{SD}$	Source-drain current				50	A
$I_{SDM}$	Source-drain current (pulsed)				200	A
$V_{SD}^{(1)}$	Forward on voltage	$I_{SD}=50A, V_{GS}=0$			1.3	V
$t_{rr}$	Reverse recovery time	$I_{SD}=50A, V_{DD}=100V$ $di/dt=25A/\mu s, T_j=150^\circ C$ <i>(see Figure 6)</i>		90		ns
$Q_{rr}$	Reverse recovery charge			333		nC
$I_{RRM}$	Reverse recovery current			7.4		A

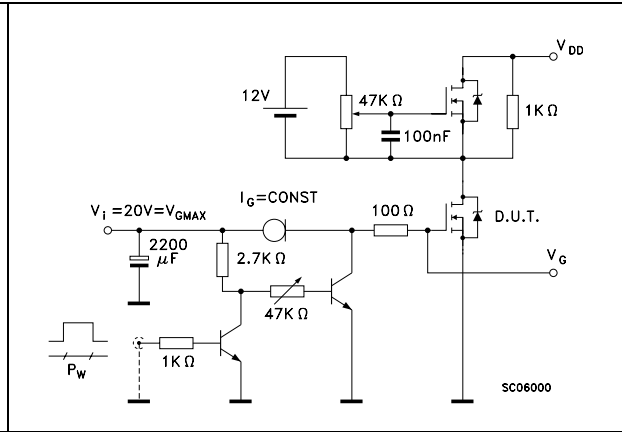
1. Pulsed: pulse duration = 300 $\mu s$ , duty cycle 1.5%

### 3 Test circuit

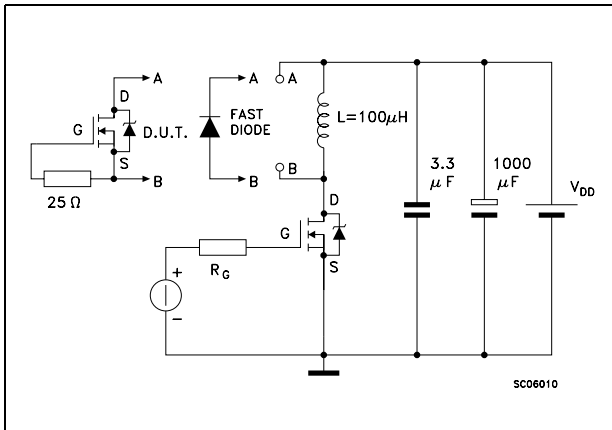
**Figure 1. Switching times test circuit for resistive load**



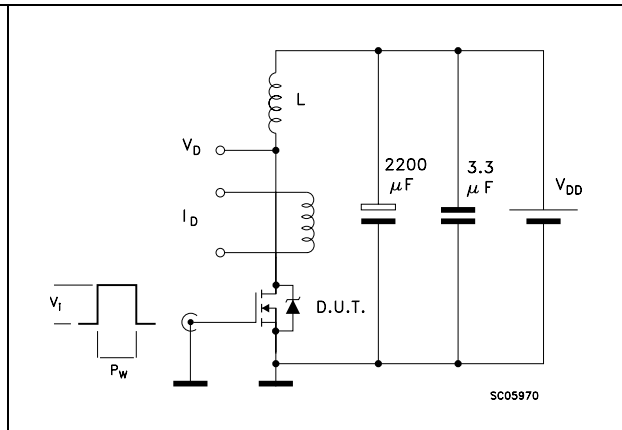
**Figure 2. Gate charge test circuit**



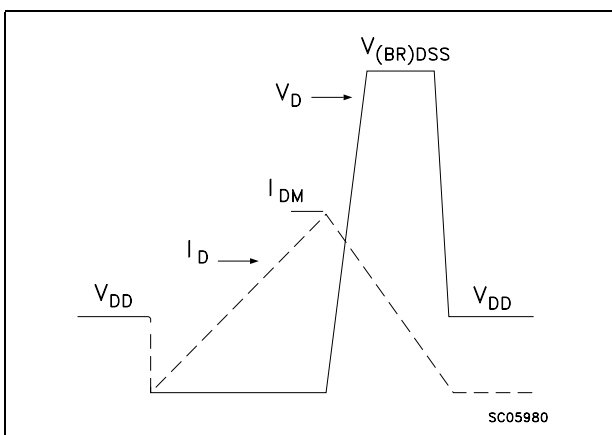
**Figure 3. Test circuit for inductive load switching and diode recovery times**



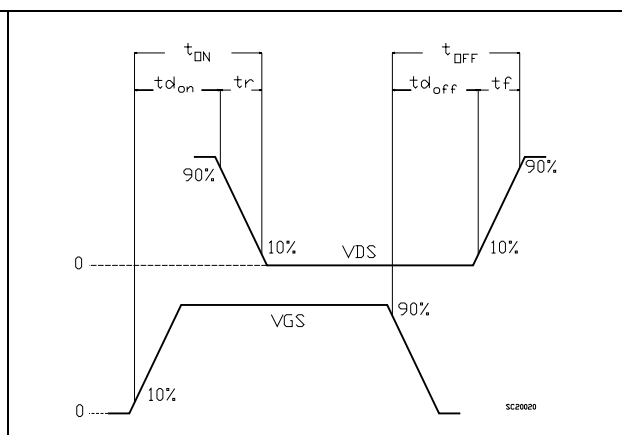
**Figure 4. Unclamped inductive load test circuit**



**Figure 5. Unclamped inductive waveform**



**Figure 6. Switching time waveform**

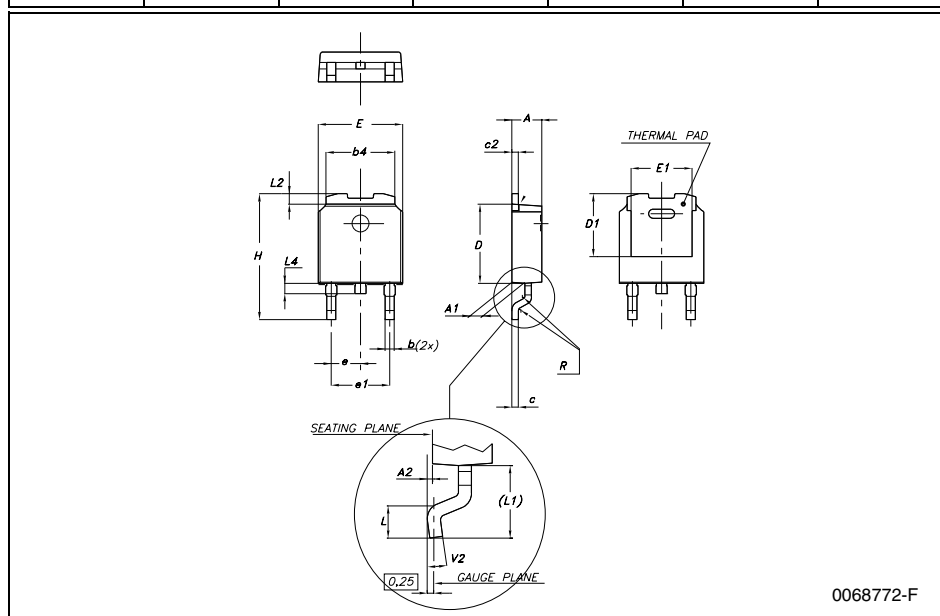


## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com)

## DPAK MECHANICAL DATA

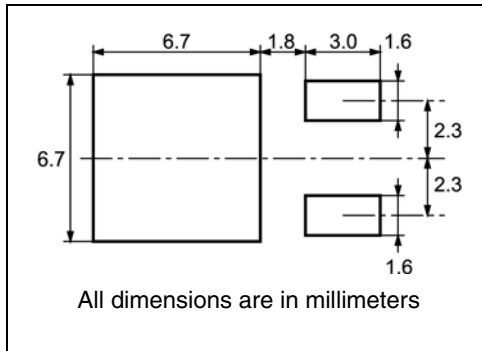
DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A2	0.03		0.23	0.001		0.009
B	0.64		0.9	0.025		0.035
b4	5.2		5.4	0.204		0.212
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
D1		5.1			0.200	
E	6.4		6.6	0.252		0.260
E1		4.7			0.185	
e		2.28			0.090	
e1	4.4		4.6	0.173		0.181
H	9.35		10.1	0.368		0.397
L	1			0.039		
(L1)		2.8			0.110	
L2		0.8			0.031	
L4	0.6		1	0.023		0.039
R		0.2			0.008	
V2	0°		8°	0°		8°



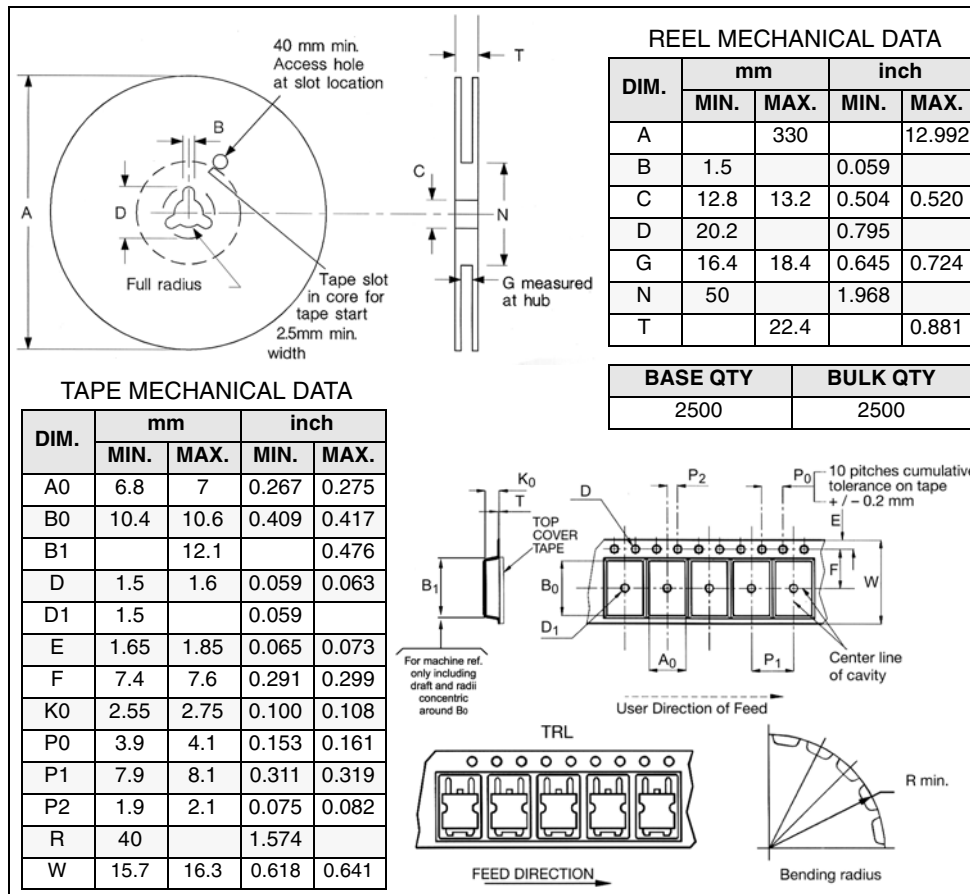


## 5 Packaging mechanical data

### DPAK FOOTPRINT



### TAPE AND REEL SHIPMENT



## 6 Revision history

**Table 7. Revision history**

Date	Revision	Changes
05-Oct-2006	1	First release

**STD40NF10**

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