

0.13 µm Cell-Based IC **CB-12 Family** L/M/H Type



Features

Cell-based IC utilizing a leading edge 0.13 μ m process technology – enabling design of a wide variety of system LSI

NEC can now offer the new CB-12 Family, a cell-based IC that is a world-first in its use of a 0.13 μ m process technology. The CB-12 Family consists of three types (L, M and H), and enables the realization of system LSI ideal for both the low static power consumption requirements of portable devices and the large-scale, high-speed requirements of the network and image processing markets.

Moreover, future plans to provide a design environment in which the three CB-12 Family transistor types can be combined will allow designers to create a highly functional system LSI that both minimizes static power consumption and realizes high-speed operation, in a reduced TAT.

- L type: Due to its leak-current suppressant transistor characteristics, this library was developed for portable devices and other such set applications in which low static power consumption is a requirement. The L-type library should be selected when backing up the circuit power supply.
- M type: This library features transistor characteristics suited to high-speed operations, making it ideal for set applications that demand high-speed processing.

Family Name	CB-12 Family			
	L Type	М Туре	Н Туре	
Technology	0.13 μ m CMOS (effective gate length 0.10 μ m), 5/7/8 aluminum layers			
Power supply voltage	1.5±0.15 V			
I/O power supply voltage	2.5±0.2 V			
	3.3±0.3 V			
Maximum number of mounted gates	26M	32M	22M	
Delay time Internal gates ^{Note}	31.7ps	20.7ps	17.1ps	
Power consumption	13nW/MHz/gate	13nW/MHz/gate	24nW/MHz/gate	
Static current consumption ratio	0.02	1	10	

H type: Notwithstanding a density inferior to that of the M type, with its ultra-high-speed operation transistor characteristics, this library is ideally suited to set applications where ultra-high-speed processing is essential.

Note Value for 2-nand power gate, fanout 2, wiring length 0 mm.

Diverse package lineup

- Tape BGA 696 pins (MAX.)
- QFP 304 pins (MAX.) (0.5 mm pitch)
- Flip-chip BGA 2000 pins (MAX.)

Testing

Large-scale circuit design-for-test supported

- Scan path test
- JTAG

Abundant macro library

Functional Cells	Compiled Macros
Logic gates	Single-port RAM
Delay gates	Dual-port RAM
Adders	ROM
Decoders	
Multiplexers	
Latches	
Flip-flops	
Shift registers	
Counters	

Cores					
Core Name	PC	Consumer	Portable Devices	Communication	Graphics
PCI controller	0				
USB ^{Note}	0				
IEEE1394 ^{Note}	0	0			
V8xx CPU		0	0		
VR4xxx CPU		0	0		
V30MZ [™]		0	0		
MPEG2 (decoder)		0			
A/D, D/A		0			
Modem codec		0			
DSP (SPX, OAK/Pine)	0	0	0		
ARM CPU		0	0		
ATM (25 MHz, 155 MHz)				0	
Ethernet [™] 10/100 Base PHY, MAC				0	
RAC (Rambus [™] ASIC Core cell)					0
2D, 3D accelerator					0

I/O Buffers
LVTTL
Low-noise buffers
3-state buffers
Open-drain buffers

DPLL (up to 250 MHz)
APLL (up to 500 MHz)
Multipliers
UART
Register file
DRAM
Flash memory
Scan block
JTAG

High-Speed I/O				
PCI	(Peripheral Component Interconnect)			
HSTL	(High-Speed Transceiver Logic)			
pECL	(Pseudo Emitter Coupled Logic)			
SSTL	(Stub Series Terminated Transfer Logic)			
LVDS	(Low Voltage Differential Signaling)			
USB ^{Note} (Universal Serial Bus)				
IEEE1394 ^{Note}				
AGP	(Accelerated Graphics Port)			
GTL+	(Gunning Transceiver Logic Plus)			

Note Under development

Remark The release schedule differs depending on the macro, so please contact NEC for details.

Electrical Specifications

12 mA type TDOPAC25NN12

3 mA type TDOPAC33NN03

6 mA type TDOPAC33NN06

9 mA type TDOPAC33NN09

12 mA type TDOPAC33NN12

18 mA type TDOPAC33NN18

24 mA type TDOPAC33NN24

3.3 V buffer

Operating ambient temperature

Storage temperature

			_	
Parameter		Symbol	Conditions	Ratings
Power supply	1.5 V system	Vdd		-0.5 to +2.0
voltage	2.5 V system			-0.5 to +3.6
	3.3 V system			-0.5 to +4.6
I/O voltage 2.5 V buffer		Vı/Vo	VI/Vo < VDD +0.3V	-0.5 to +3.6
	3.3 V buffer		VI/Vo < VDD +0.5V	-0.5 to +4.6
Output current 2.5 V buffer		lo		
	2 mA type TDOPAC25NN02		lol = 2 mA	9
	4 mA type TDOPAC25NN04		lol = 4 mA	17
	6 mA type TDOPAC25NN06		lol = 6 mA	38
	9 mA type TDOPAC25NN09		lol = 9 mA	49

IoL = 12 mA

 $I_{OL} = 3 \text{ mA}$

IOL = 6 mA

lo∟=9 mA

IoL = 12 mA

IoL = 18 mA

lo∟ = 24 mA

Absolute maximum ratings

Unit

V

V V

V V

mΑ mΑ mΑ mΑ

mΑ

mΑ

mΑ

mΑ

mΑ

mΑ

mΑ

°C

°C

63

10

19

27

41

53

67

-40 to +85

-65 to +150

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

ΤA

Tstg

Remark Be sure to confirm the power supply voltage before applying either 2.5 V or 3.3 V to the I/O pins.

AC characteristics –

The following ratings are applicable for a power supply voltage of 1.5 V.

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Toggle frequency (L type)	ftog	Internal toggle F/F (fanout 1)		1.9		GHz
Toggle frequency (M type)				3.1		GHz
Toggle frequency (H type)				5.7		GHz
Propagation delay time	t PD	2.5 V input buffer		249		ps
(2.5 V buffer)		Fanout 1, wiring length = 30 μ m, tr, tf = 0.1 ns				
		2.5 V output buffer (12 mA)		1187		ps
		C∟ = 15 pF				
Propagation delay time		3.3 V input buffer		207		ps
(3.3 V buffer)		Fanout 1, wiring length = 30 μ m, tr, tf = 0.1 ns				
		3.3 V output buffer (24 mA)		995		ps
		CL = 15 pF				
Propagation delay time		Fanout 1, standard wiring length		41.3		ps
(internal gates: L type)		Fanout 1, standard wiring length		30.8		ps
		(Power gate)				
Propagation delay time		Fanout 1, standard wiring length		27.1		ps
(internal gates: M type)		Fanout 1, standard wiring length		19.9		ps
		(Power gate)				
Propagation delay time		Fanout 1, standard wiring length		17.1		ps
(internal gates: H type)		Fanout 1, standard wiring length				ps
		(Power gate)				
Output rise time	tro	2.5 V output buffer (12 mA)		841		ps
		CL = 15 pF; 10 to 90%				
		3.3 V output buffer (18 mA)		944		ps
		CL = 15 pF; 10 to 90%				
Output fall time	t _{fo}	2.5 V output buffer (12 mA)		673		ps
		CL = 15 pF; 10 to 90%				
		3.3 V output buffer (18 mA)		637		ps
		CL = 15 pF; 10 to 90%				

Remark Blank spaces in the table above indicate values under study.

Design Environment

NEC provides OPENCAD[™] CB12_KIT as the ideal design environment for the CB-12 Family. OPENCAD CB12_KIT includes a number of tools, from amongst which the customer can select those best-suited to their environment.

Function	NEC Tools	Commercial Tools	I/F Data
Function simulator	_	Verilog-XL [™]	
		NC-Verilog™	
		ModelSim™ EE	
		ModelSim SE/VHDL	
		VCS™	
Circuit diagram editor	Vdraw™	_	Function description language
Logic synthesis	_	Design Compiler®	Verilog™ HDL/VHDL
Floor planner	ace_floorplan	_	
Gate-level simulator Note 1	V.sim™	Verilog-XL	• Netlist
		NC-Verilog	PWC/EDIF(2.0.0)/Verilog HDL
		ModelSim EE	
		ModelSim SE/VHDL	Test pattern ALBA/LOGPAT
		VCS	
STA ^{Note 1}	Tiara	PrimeTime®	• Delay data SDF
Format verification	_	Formality®	
		Tuxedo™-Lec	Timing constraint file
Placement and routing	_	Silicon Ensemble ^{TM Note 2}	
Design-for-test	NEC_SCAN	TestCompiler™(DFT)	
	TESTACT	DFTAdvisor™(DFT)	
		Testgen™(ATPG)	
		FastScan™(ATPG)	
		TetraMAX™(ATPG)	

Notes 1. Sign-off tool

2. Tool not supported in the HP[™] version

Remark Platform: SUN[™](Solaris[™])/HP(HP-UX[™])

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