203 592.

FINAL

COM'L: -4/5/7/B/B-2/A, D/2 MIL: -10/12/B/B-2/A/B-4

# PAL16R8 Family

## 20-Pin TTL Programmable Array Logic

Advanced Micro Devices

## DISTINCTIVE CHARACTERISTICS

- As fast as 4.5 ns maximum propagation delay
- Popular 20-pin architectures: 16L8, 16R8, 16R6, 16R4
- Programmable replacement for high-speed TTL logic
- Register preload for testability
- Power-up reset for initialization
- Extensive third-party software and programmer support through FusionPLD partners
- 20-Pin DIP and PLCC packages save space
- 28-Pin PLCC-4 package provides ultra-clean high-speed signals

## GENERAL DESCRIPTION

The PAL16R8 Family (PAL16L8, PAL16R8, PAL16R6, PAL16R4) includes the PAL16R8-5/4 Series which provides the highest speed in the 20-pin TTL PAL device family, making the series ideal for high-performance applications. The PAL16R8 Family is provided with standard 20-pin DIP and PLCC pinouts and a 28-pin PLCC pinout. The 28-pin PLCC pinout contains seven extra ground pins interleaved between the outputs to reduce noise and increase speed.

The devices provide user-programmable logic for replacing conventional SSI/MSI gates and flip-flops at a reduced chip count.

The family allows the systems engineer to implement the design on-chip, by opening fuse links to configure AND and OR gates within the device, according to the desired logic function. Complex interconnections between gates, which previously required time-consuming layout, are lifted from the PC board and placed on silicon, where they can be easily modified during prototyping or production.

The PAL device implements the familiar Boolean logic transfer function, the sum of products. The PAL device is a programmable AND array driving a fixed OR array. The AND array is programmed to create custom product terms, while the OR array sums selected terms at the outputs.

In addition, the PAL device provides the following options:

— Variable input/output pin ratio

— Programmable three-state outputs

— Registers with feedback

Product terms with all connections opened assume the logical HIGH state; product terms connected to both true and complement of any single input assume the logical LOW state. Registers consist of D-type flip-flops that are loaded on the LOW-to-HIGH transition of the clock. Unused input pins should be tied to $V_{CC}$ or GND.

The entire PAL device family is supported by the FusionPLD partners. The PAL family is programmed on conventional PAL device programmers with appropriate personality and socket adapter modules. Once the PAL device is programmed and verified, an additional connection may be opened to prevent pattern readout. This feature secures proprietary circuits.

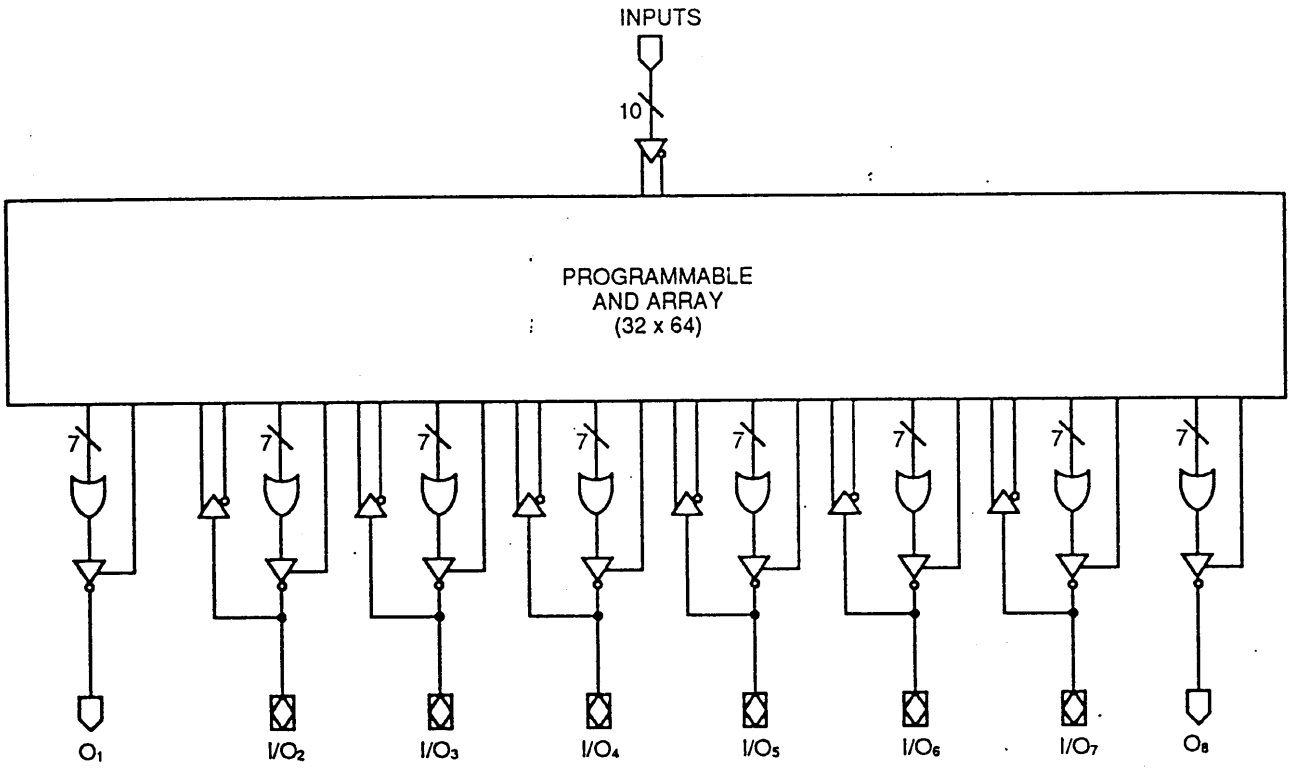
## PRODUCT SELECTOR GUIDE

| Device | Dedicated Inputs | Outputs | Product Terms/ Output | Feedback | Enable |
|---|---|---|---|---|---|
| PAL16L8 | 10 | 6 comb.<br>2 comb. | 7<br>7 | I/O<br>– | prog.<br>prog. |
| PAL16R8 | 8 | 8 reg. | 8 | reg. | pin |
| PAL16R6 | 8 | 6 reg.<br>2 comb. | 8<br>7 | reg.<br>I/O | pin<br>prog. |
| PAL16R4 | 8 | 4 reg.<br>4 comb. | 8<br>7 | reg.<br>I/O | pin<br>prog. |

Publication# 16492 Rev. C Amendment/0
Issue Date: October 1994

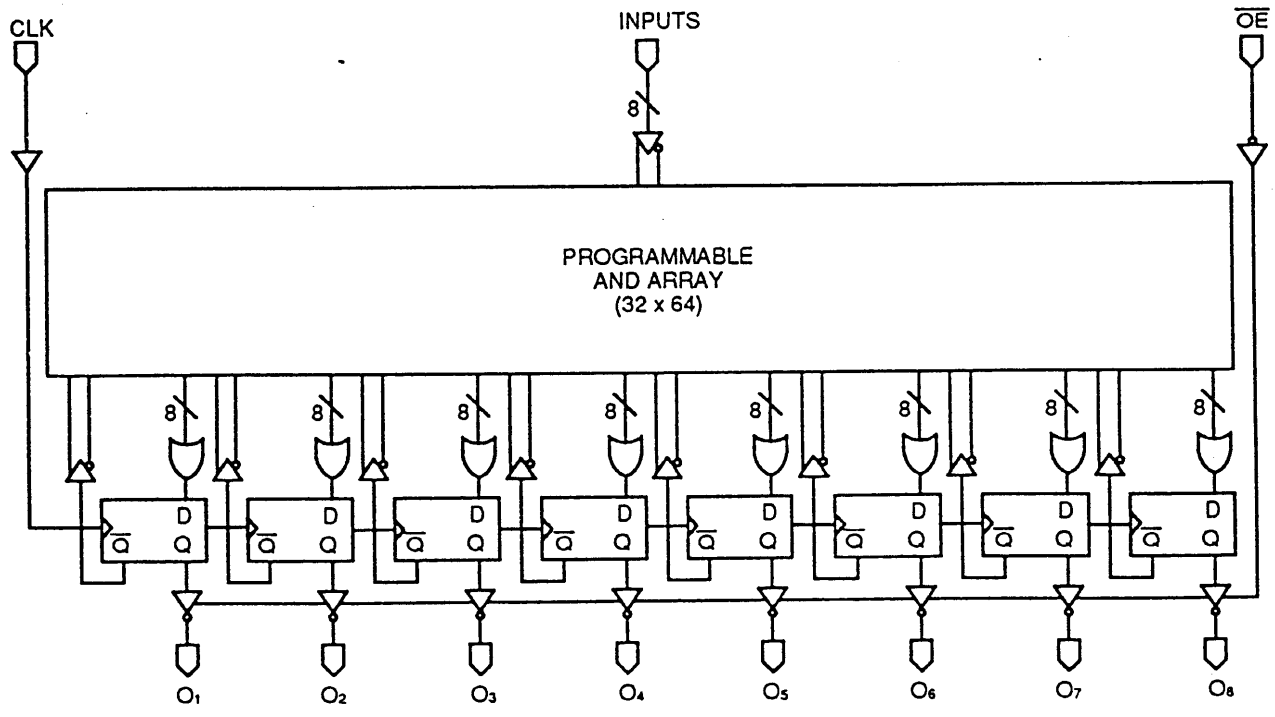
## BLOCK DIAGRAMS

**PAL16L8**




16492C-1

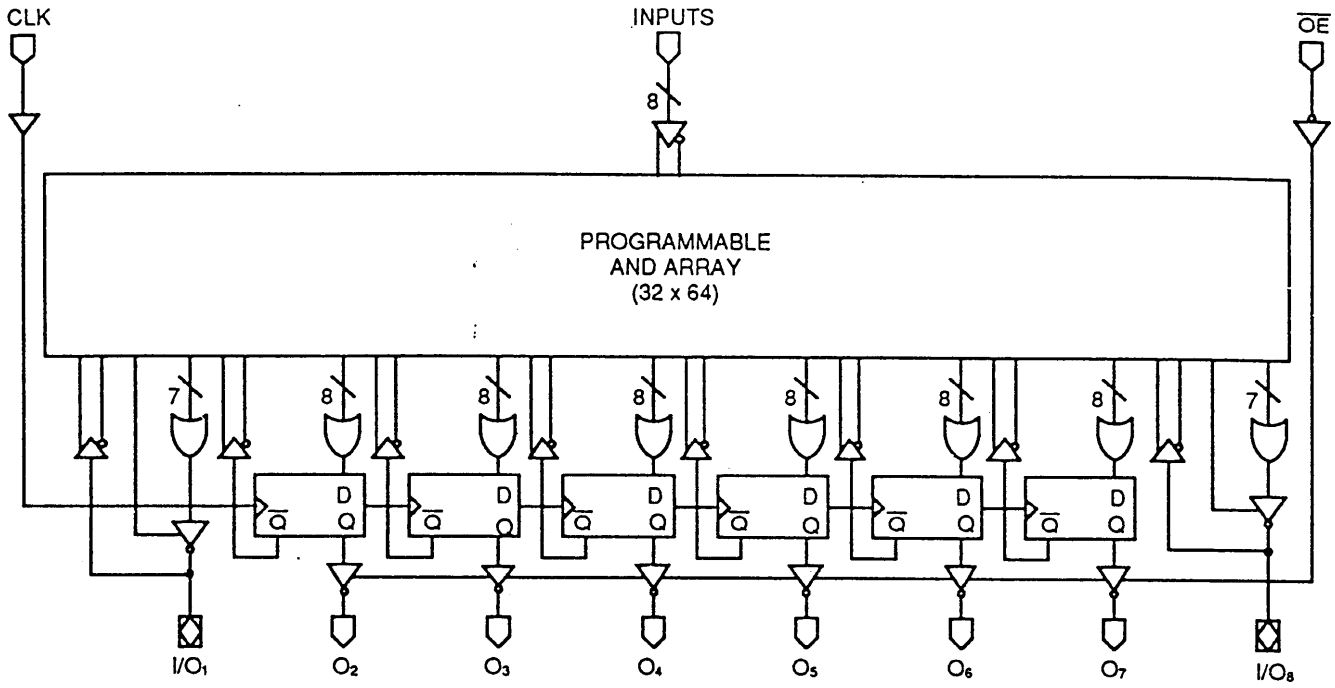
**PAL16R8**




16492C-2

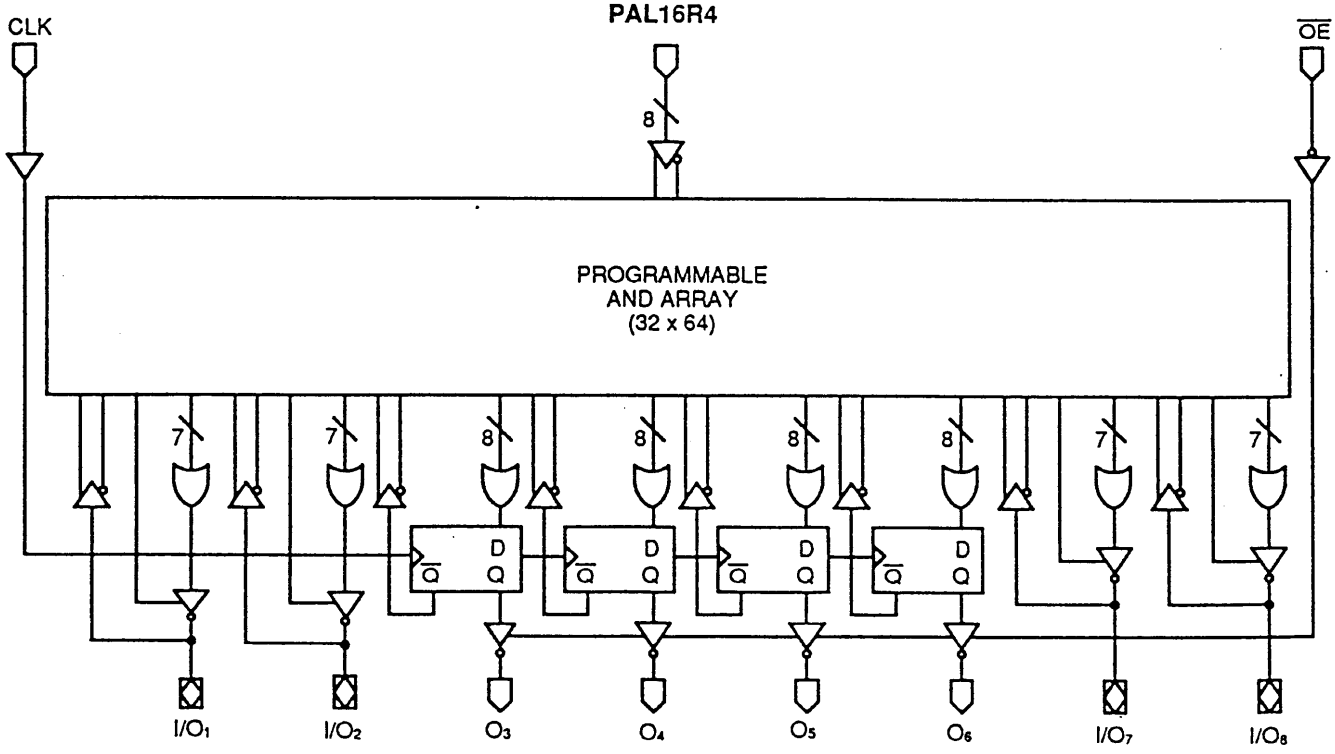
## BLOCK DIAGRAMS

### PAL16R6




16492C-3

### PAL16R4

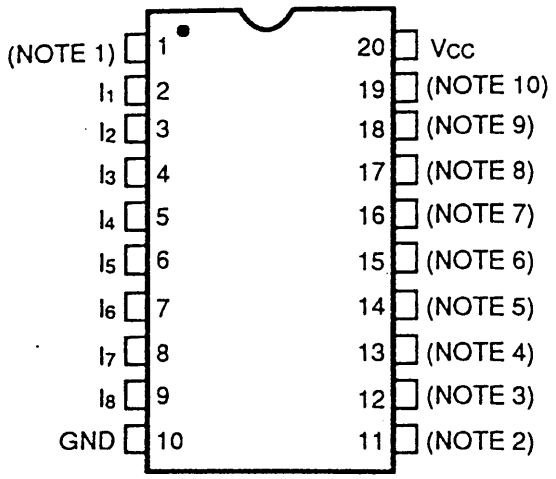



16492C-4

## CONNECTION DIAGRAMS

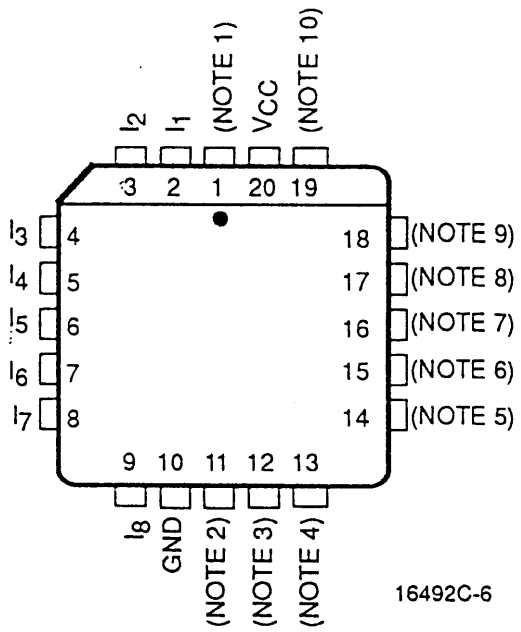
### Top View

#### DIP



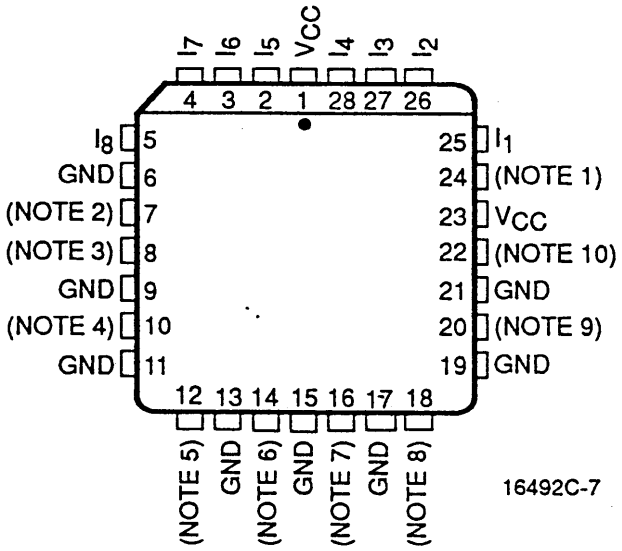

16492C-5

#### 20-Pin PLCC




16492C-6

#### 28-Pin PLCC




16492C-7

### PIN DESIGNATIONS

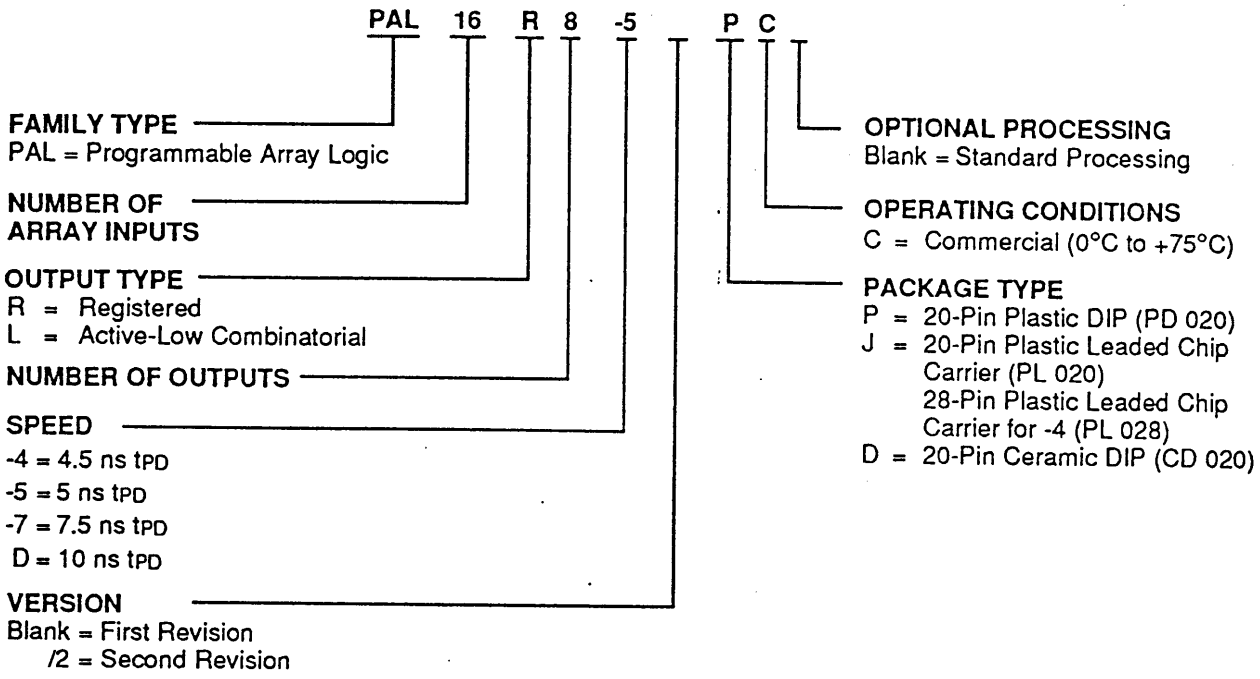
| | | |
|---|---|---|
| CLK | = | Clock |
| GND | = | Ground |
| I | = | Input |
| I/O | = | Input/Output |
| $\overline{O}$ | = | Output |
| $\overline{OE}$ | = | Output Enable |
| Vcc | = | Supply Voltage |

*Note:*
*Pin 1 is marked for orientation.*

| Note | 16L8 | 16R8 | 16R6 | 16R4 |
|---|---|---|---|---|
| 1 | $I_0$ | CLK | CLK | CLK |
| 2 | $I_9$ | $\overline{OE}$ | $\overline{OE}$ | $\overline{OE}$ |
| 3 | $O_1$ | $O_1$ | $I/O_1$ | $I/O_1$ |
| 4 | $I/O_2$ | $O_2$ | $O_2$ | $I/O_2$ |
| 5 | $I/O_3$ | $O_3$ | $O_3$ | $O_3$ |
| 6 | $I/O_4$ | $O_4$ | $O_4$ | $O_4$ |
| 7 | $I/O_5$ | $O_5$ | $O_5$ | $O_5$ |
| 8 | $I/O_6$ | $O_6$ | $O_6$ | $O_6$ |
| 9 | $I/O_7$ | $O_7$ | $O_7$ | $I/O_7$ |
| 10 | $O_8$ | $O_8$ | $I/O_8$ | $I/O_8$ |

# ORDERING INFORMATION
## Commercial Products

AMD programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:




| Valid Combinations | |
|---|---|
| PAL16L8 | -5PC, -5JC, -4JC |
| PAL16R8 | |
| PAL16R6 | |
| PAL16R4 | |
| PAL16L8-7 | PC, JC, DC |
| PAL16R8-7 | |
| PAL16R6-7 | |
| PAL16R4-7 | |
| PAL16L8D/2 | PC, JC |
| PAL16R8D/2 | |
| PAL16R6D/2 | |
| PAL16R4D/2 | |

**Valid Combinations**

Valid Combinations lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

# ORDERING INFORMATION
## Commercial Products (MMI Marking Only)

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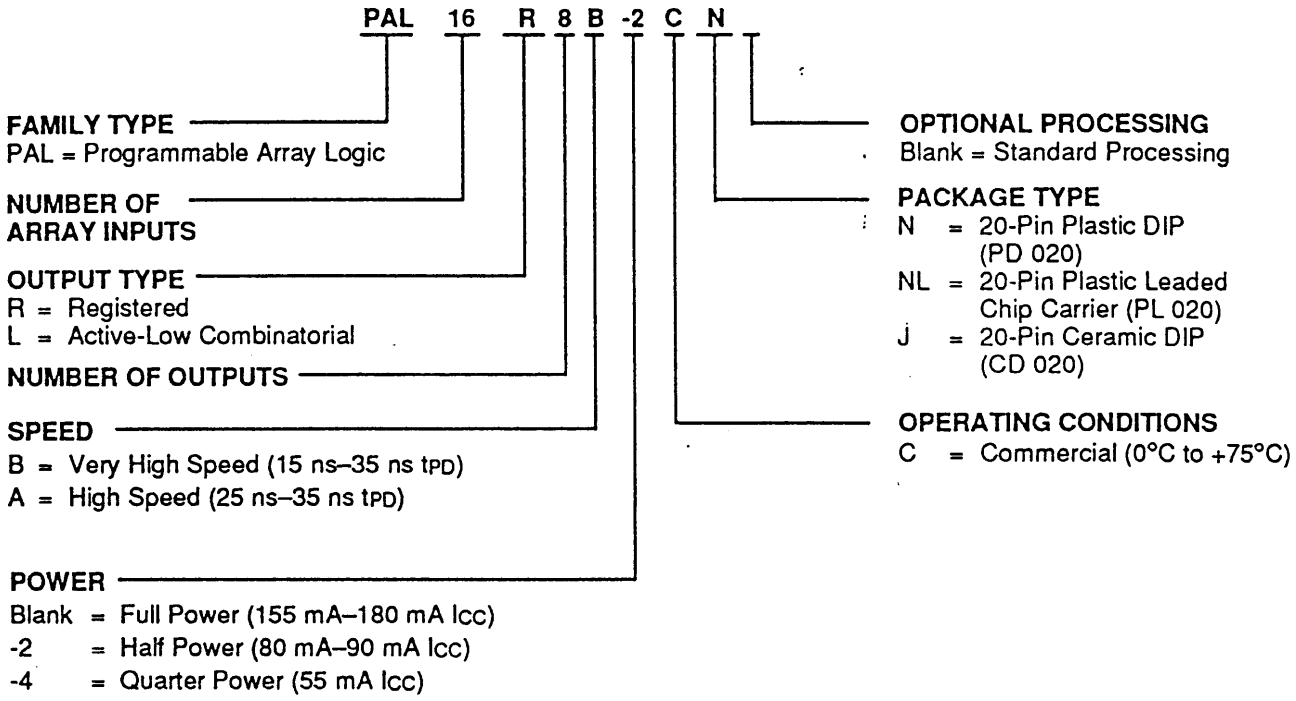



| Valid Combinations | | |
|---|---|---|
| PAL16L8 | B, B-2, A, B-4 | CN, CNL, CJ |
| PAL16R8 | | |
| PAL16R6 | | |
| PAL16R4 | | |

**Valid Combinations**

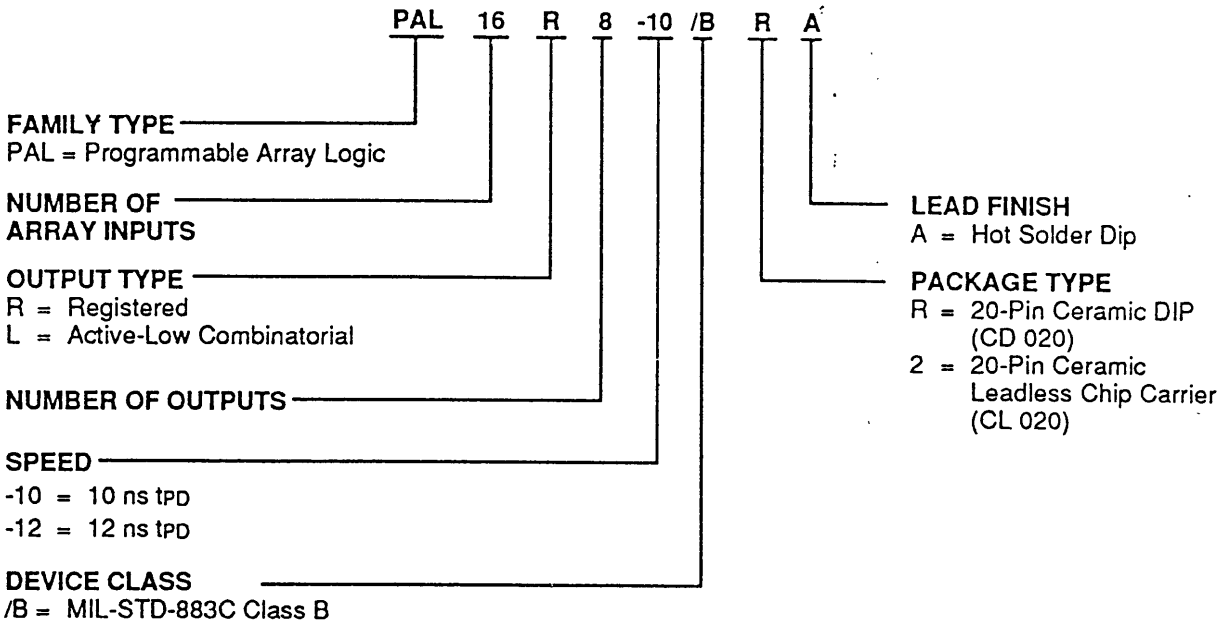
Valid Combinations lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

***Note:*** *Marked with MMI logo.*

# ORDERING INFORMATION

## APL Products

AMD programmable logic products for Aerospace and Defense applications are available with several ordering options. APL (Approved Products List) products are fully compliant with MIL-STD-883 requirements. The order number (Valid Combination) is formed by a combination of:




| Valid Combinations | | |
|---|---|---|
| PAL16L8 | -10, -12 | /BRA, /B2A |
| PAL16R8 | | |
| PAL16R6 | | |
| PAL16R4 | | |

### Valid Combinations

Valid Combinations lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

### Military Burn-In

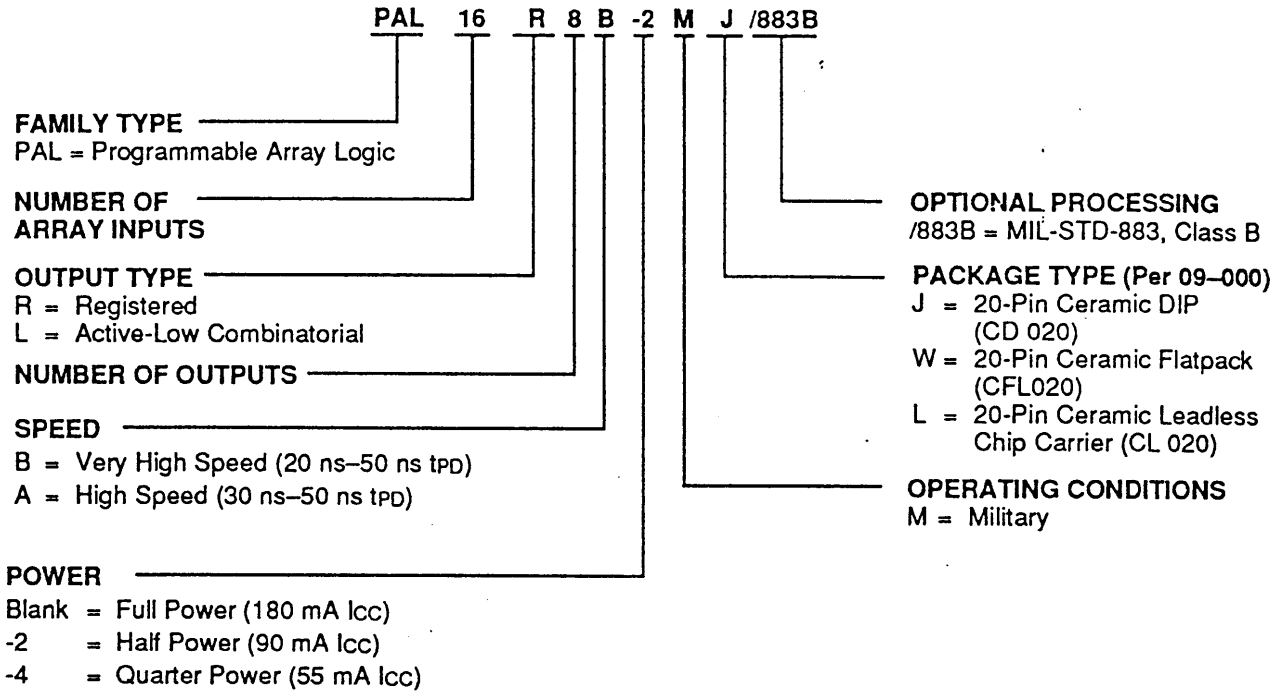
Military burn-in is in accordance with the current revision of MIL-STD-883, Test Methods 1015, Conditions A through E. Test conditions are selected at AMD's option.

### Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

# ORDERING INFORMATION
## APL Products (MMI Marking Only)

AMD programmable logic products for Aerospace and Defense applications are available with several ordering options. APL (Approved Products List) products are fully compliant with MIL-STD-883 requirements. The order number (Valid Combination) is formed by a combination of:




| Valid Combinations | | |
|---|---|---|
| PAL16L8 | B, B-2, A, B-4 | MJ/883B, MW/883B, ML/883B |
| PAL16R8 | | |
| PAL16R6 | | |
| PAL16R4 | | |

### Valid Combinations

Valid Combinations lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

*Note: Marked with MMI logo.*

### Military Burn-In

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Methods 1015, Conditions A through E. Test conditions are selected at AMD's option.

### Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

## FUNCTIONAL DESCRIPTION

### Standard 20-Pin PAL Family

The standard bipolar 20-pin PAL family devices have common electrical characteristics and programming procedures. Four different devices are available, including both registered and combinatorial devices. All parts are produced with a fuse link at each input to the AND gate array, and connections may be selectively removed by applying appropriate voltages to the circuit. Utilizing an easily-implemented programming algorithm, these products can be rapidly programmed to any customized pattern. Extra test words are preprogrammed during manufacturing to ensure extremely high field programming yields, and provide extra test paths to achieve excellent parametric correlation.

### Pinouts

The PAL16R8 Family is available in the standard 20-pin DIP and PLCC pinouts and the PAL16R8-4 Series is available in the new 28-pin PLCC pinout. The 28-pin PLCC pinout gives the designer the cleanest possible signal with only 4.5 ns delay.

The PAL16R8-4 pinout has been designed to minimize the noise that can be generated by high-speed signals. Because of its inherently shorter leads, the PLCC package is the best package for use in high-speed designs. The short leads and multiple ground signals reduce the effective lead inductance, minimizing ground bounce. Placing the ground pins between the outputs optimizes the ground bounce protection, and also isolates the outputs from each other, eliminating cross-talk. This pinout can reduce the effective propagation delay by as much as 20% from a standard DIP pinout. Design files for PAL16R8-4 Series devices are written as if the device had a standard 20-pin DIP pinout for most design software packages.

### Variable Input/Output Pin Ratio

The registered devices have eight dedicated input lines, and each combinatorial output is an I/O pin. The PAL16L8 has ten dedicated input lines and six of the eight combinatorial outputs are I/O pins. Buffers for device inputs have complementary outputs to provide user-programmable input signal polarity. Unused input pins should be tied to Vcc or GND.

### Programmable Three-State Outputs

Each output has a three-state output buffer with three-state control. On combinatorial outputs, a product term controls the buffer, allowing enable and disable to be a function of any product of device inputs or output feedback. The combinatorial output provides a bidirectional I/O pin and may be configured as a dedicated input if the output buffer is always disabled. On registered outputs, an input pin controls the enabling of the three-state outputs.

### Registers with Feedback

Registered outputs are provided for data storage and synchronization. Registers are composed of D-type flip-flops that are loaded on the LOW-to-HIGH transition of the clock input.

### Register Preload

The register on the AMD marked 16R8, 16R6, and 16R4 devices can be preloaded from the output pins to facilitate functional testing of complex state machine designs. This feature allows direct loading of arbitrary states, making it unnecessary to cycle through long test vector sequences to reach a desired state. In addition, transitions from illegal states can be verified by loading illegal states and observing proper recovery.

### Power-Up Reset

All flip-flops power-up to a logic LOW for predictable system initialization. Outputs of the PAL16R8 Family will be HIGH due to the active-low outputs. The Vcc rise must be monotonic and the reset delay time is 1000 ns maximum.

### Security Fuse

After programming and verification, a PAL16R8 Family design can be secured by programming the security fuse. Once programmed, this fuse defeats readback of the internal programmed pattern by a device programmer, securing proprietary designs from competitors. When the security fuse is programmed, the array will read as if every fuse is programmed.

### Quality and Testability

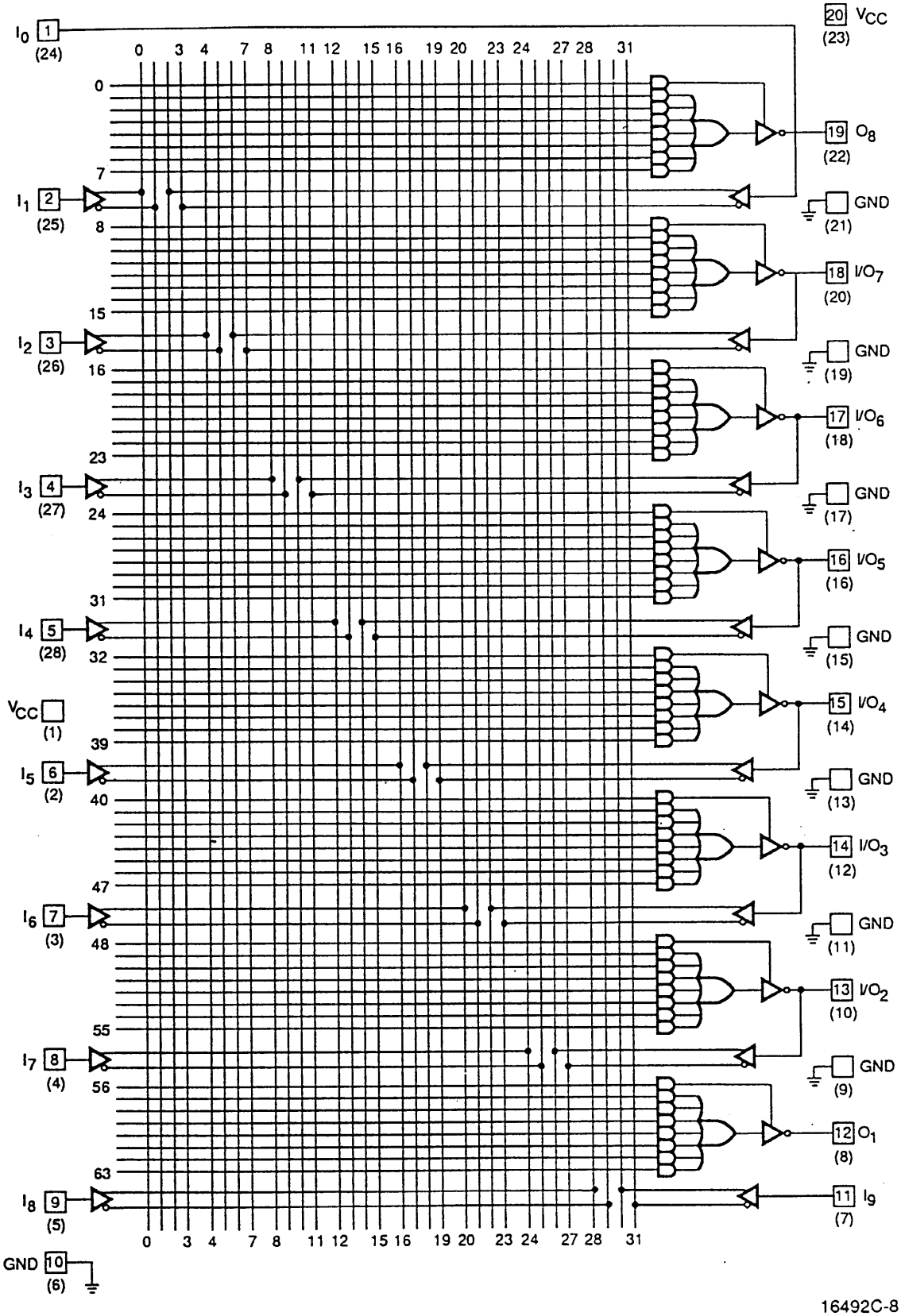
The PAL16R8 Family offers a very high level of built-in quality. Extra programmable fuses provide a means of verifying performance of all AC and DC parameters. In addition, this verifies complete programmability and functionality of the device to provide the highest programming yields and post-programming functional yields in the industry.

### Technology

The PAL16R8-5, -7 and D/2 are fabricated with AMD's oxide isolated bipolar process. The array connections are formed with highly reliable PtSi fuses. The PAL16R8B, B-2, A and B-4 series are fabricated with AMD's advanced trench-isolated bipolar process. The array connections are formed with proven TiW fuses for reliable operation. These processes reduce parasitic capacitances and minimum geometries to provide higher performance.

## LOGIC DIAGRAM
## DIP and 20-Pin PLCC (28-Pin PLCC) Pinouts

### 16L8 (-4)

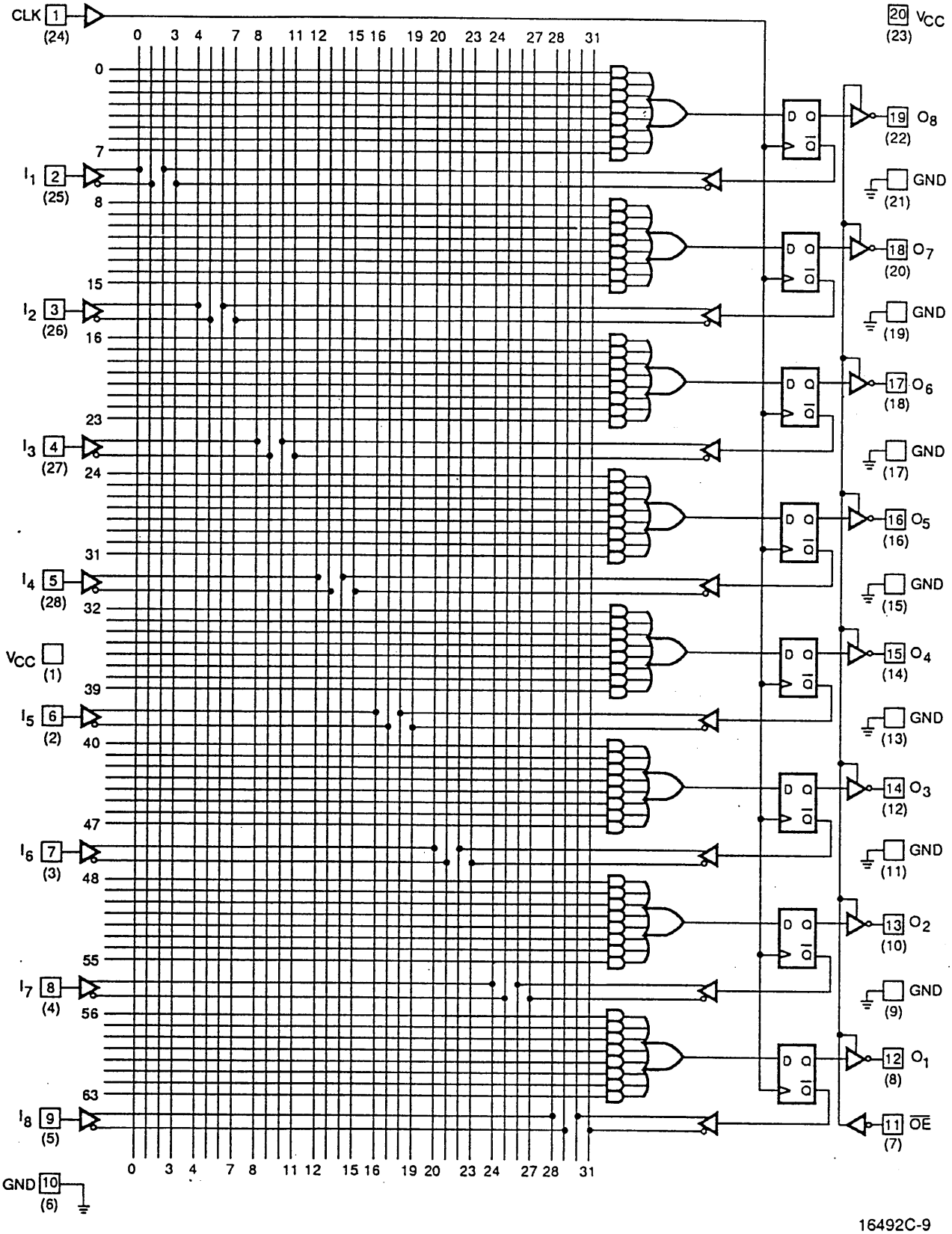



16492C-8

## LOGIC DIAGRAM

'DIP and 20-Pin PLCC (28-Pin PLCC) Pinouts

### 16R8 (-4)

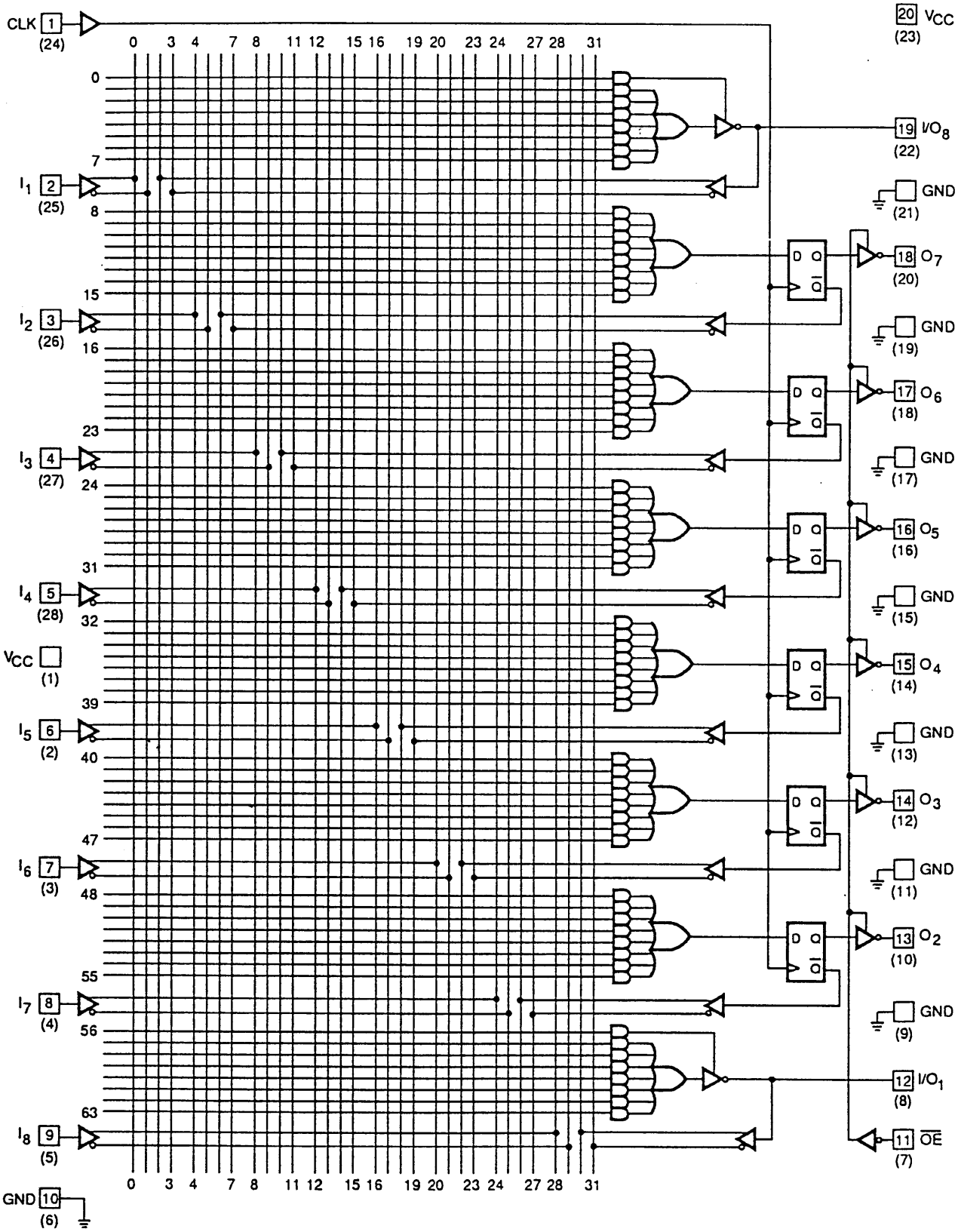



16492C-9

## LOGIC DIAGRAM

### DIP and 20-Pin PLCC (28-Pin PLCC) Pinouts

16R6 (-4)

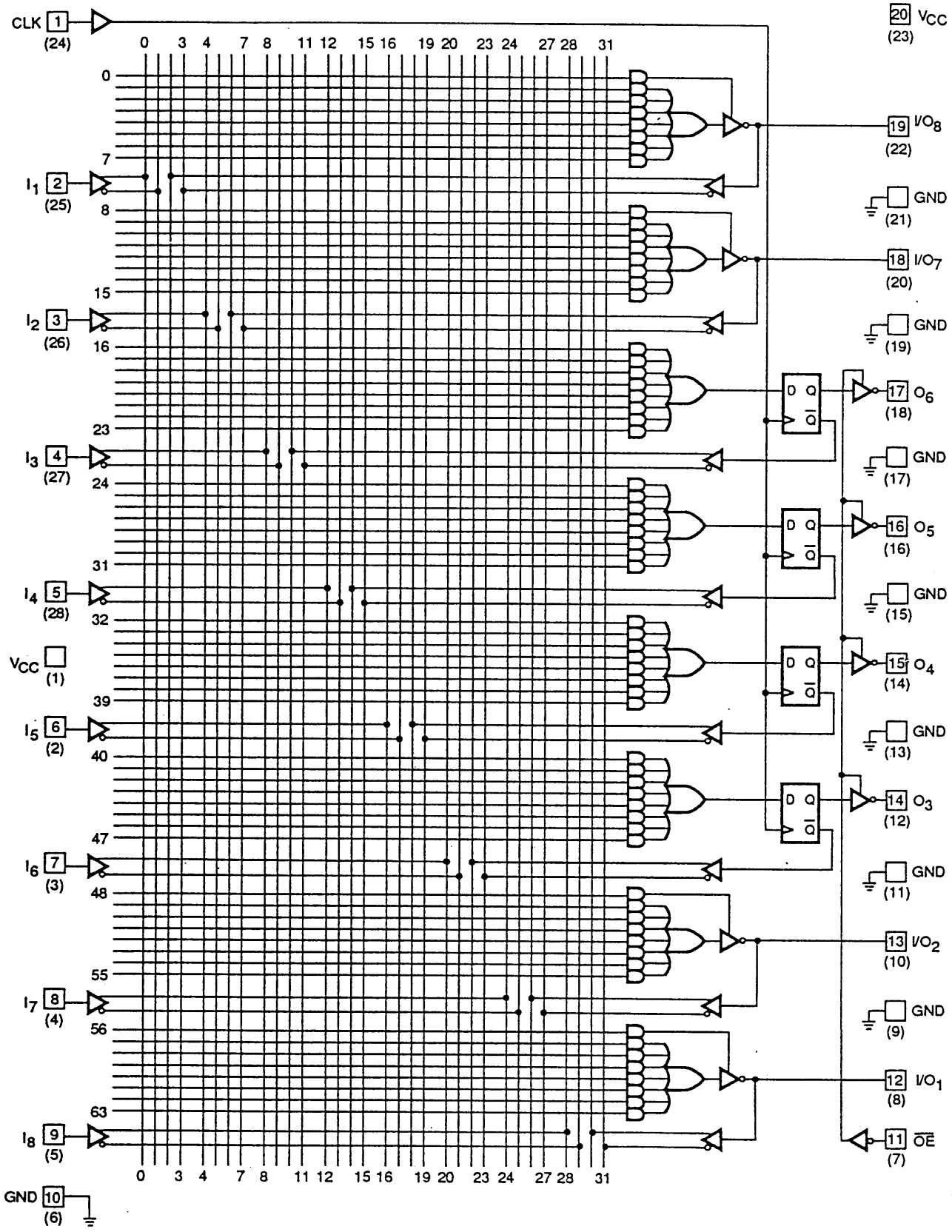



16492C-10

## LOGIC DIAGRAM

### DIP and 20-Pin PLCC (28-Pin PLCC) Pinouts

16R4 (-4)




16492C-11

## ABSOLUTE MAXIMUM RATINGS

Ambient Temperature with Power Applied ..... −65°C to +150°C

Storage Temperature ..... −55°C to +125°C

Supply Voltage with Respect to Ground ..... −0.5 V to + 7.0 V

DC Input Voltage ..... −1.2 V to Vcc + 0.5 V

DC Input Current ..... −30 mA to + 5 mA

DC Output or I/O Pin Voltage ..... −0.5 V to Vcc + 0.5 V

Static Discharge Voltage ..... 2001 V

*Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.*

## OPERATING RANGES

### Commercial (C) Devices

Ambient Temperature ($T_A$) Operating in Free Air ..... 0°C to +75°C

Supply Voltage (Vcc) with Respect to Ground ..... +4.75 V to +5.25 V

*Operating ranges define those limits between which the functionality of the device is guaranteed.*

## DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

| Parameter Symbol | Parameter Description | Test Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $I_{OH}$ = −3.2 mA $V_{IN}$ = $V_{IH}$ or $V_{IL}$, Vcc = Min | 2.4 | | V |
| $V_{OL}$ | Output LOW Voltage | $I_{OL}$ = 24 mA $V_{IN}$ = $V_{IH}$ or $V_{IL}$, Vcc = Min | | 0.5 | V |
| $V_{IH}$ | Input HIGH Voltage | Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1) | 2.0 | | V |
| $V_{IL}$ | Input LOW Voltage | Guaranteed Input Logical LOW Voltage for all Inputs (Note 1) | | 0.8 | V |
| $V_I$ | Input Clamp Voltage | $I_{IN}$ = −18 mA, Vcc = Min | | −1.2 | V |
| $I_{IH}$ | Input HIGH Current | $V_{IN}$ = 2.7 V, Vcc = Max (Note 2) | | 25 | µA |
| $I_{IL}$ | Input LOW Current | $V_{IN}$ = 0.4 V, Vcc = Max (Note 2) | | −250 | µA |
| $I_I$ | Maximum Input Current | $V_{IN}$ = 5.5 V, Vcc = Max | | 1 | mA |
| $I_{OZH}$ | Off-State Output Leakage Current HIGH | $V_{OUT}$ = 2.7 V, Vcc = Max, $V_{IN}$ = $V_{IH}$ or $V_{IL}$ (Note 2) | | 100 | µA |
| $I_{OZL}$ | Off-State Output Leakage Current LOW | $V_{OUT}$ = 0.4 V, Vcc = Max, $V_{IN}$ = $V_{IH}$ or $V_{IL}$ (Note 2) | | −100 | µA |
| $I_{SC}$ | Output Short-Circuit Current | $V_{OUT}$ = 0.5 V, Vcc = Max (Note 3) | −30 | −130 | mA |
| $I_{CC}$ | Supply Current | $V_{IN}$ = 0 V, Outputs Open ($I_{OUT}$ = 0 mA), Vcc = Max | | 210 | mA |

***Notes:***

1. *These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.*
2. *I/O pin leakage is the worst case of $I_{IL}$ and $I_{OZL}$ (or $I_{IH}$ and $I_{OZH}$).*
3. *Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. $V_{OUT}$ = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

## CAPACITANCE (Note 1)

| Parameter Symbol | Parameter Description | | Test Conditions | | Typ | Unit |
|---|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | CLK, $\overline{OE}$ | $V_{IN}$ = 2.0 V | $V_{CC}$ = 5.0 V | 8 | pF |
| | | $I_1$–$I_8$ | | $T_A$ = 25°C | 5 | |
| $C_{OUT}$ | Output Capacitance | | $V_{OUT}$ = 2.0 V | f = 1 MHz | 8 | |

***Note:***

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

## SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

| Parameter Symbol | Parameter Description | | | | -5 | | -4 | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | Min (Note 3) | Max | Min (Note 3) | Max | |
| $t_{PD}$ | Input or Feedback to Combinatorial Output | | | 16L8, 16R8, 16R4 | 1 | 5 | 1 | 4.5 | ns |
| $t_S$ | Setup Time from Input or Feedback to Clock | | | 16R8, 16R6, 16R4 | 4.5 | | 4.5 | | ns |
| $t_H$ | Hold Time | | | | 0 | | 0 | | ns |
| $t_{CO}$ | Clock to Output | | | | 1 | 4.0 | 1 | 3.5 | ns |
| $t_{SKEWR}$ | Skew Between Registered Outputs (Note 4) | | | | | 1 | | 0.5 | ns |
| | | | | | | | | | |
| $t_{WL}$ | Clock Width | LOW | | | 4 | | 4 | | ns |
| $t_{WH}$ | | HIGH | | | 4 | | 4 | | ns |
| $f_{MAX}$ | Maximum Frequency (Note 5) | External Feedback | 1/($t_S$ + $t_{CO}$) | | 117 | | 125 | | MHz |
| | | Internal Feedback ($f_{CNT}$) | | | 125 | | 125 | | MHz |
| | | No Feedback | 1/($t_{WH}$ + $t_{WL}$) | | 125 | | 125 | | MHz |
| $t_{PZX}$ | $\overline{OE}$ to Output Enable | | | | 1 | 6.5 | 1 | 6.5 | ns |
| $t_{PXZ}$ | $\overline{OE}$ to Output Disable | | | | 1 | 5 | 1 | 5 | ns |
| $t_{EA}$ | Input to Output Enable Using Product Term Control | | | 16L8, 16R6, 16R4 | 2 | 6.5 | 2 | 6.5 | ns |
| $t_{ER}$ | Input to Output Disable Using Product Term Control | | | | 2 | 5 | 2 | 5 | ns |

***Notes:***

2. *See Switching Test Circuit for test conditions.*
3. *Output delay minimums for $t_{PD}$, $t_{CO}$, $t_{PZX}$, $t_{PXZ}$, $t_{EA}$, and $t_{ER}$ are defined under best case conditions. Future process improvements may alter these values; therefore, minimum values are recommended for simulation purposes only.*
4. *Skew testing takes into account pattern and switching direction differences between outputs.*
5. *These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where the frequency may be affected.*

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage with Respect to Ground ..... −0.5 V to + 7.0 V

DC Input Voltage ..... −1.2 V to + 7.0 V

DC Input Current ..... −30 mA to + 5 mA

DC Output or I/O Pin Voltage ..... −0.5 V to $V_{CC}$ + 0.5 V

Static Discharge Voltage ..... 2001 V

*Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.*

## OPERATING RANGES

**Commercial (C) Devices**

Ambient Temperature ($T_A$) Operating in Free Air ..... 0°C to +75°C

Supply Voltage ($V_{CC}$) with Respect to Ground ..... +4.75 V to +5.25 V

*Operating ranges define those limits between which the functionality of the device is guaranteed.*

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| $V_{OL}$ | Output LOW Voltage | $I_{OL}$ = 24 mA $V_{IN}$ = $V_{IH}$ or $V_{IL}$ $V_{CC}$ = Min | | 0.5 | V |
| $V_{IH}$ | Input HIGH Voltage | Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1) | 2.0 | | V |
| $V_{IL}$ | Input LOW Voltage | Guaranteed Input Logical LOW Voltage for all Inputs (Note 1) | | 0.8 | V |
| $V_I$ | Input Clamp Voltage | $I_{IN}$ = −18 mA, $V_{CC}$ = Min | | −1.2 | V |
| $I_{IH}$ | Input HIGH Current | $V_{IN}$ = 2.7 V, $V_{CC}$ = Max (Note 2) | | 25 | µA |
| $I_{IL}$ | Input LOW Current | $V_{IN}$ = 0.4 V, $V_{CC}$ = Max (Note 2) | | −250 | µA |
| $I_I$ | Maximum Input Current | $V_{IN}$ = 5.5 V, $V_{CC}$ = Max | | 1 | mA |
| $I_{OZH}$ | Off-State Output Leakage Current HIGH | $V_{OUT}$ = 2.7 V, $V_{CC}$ = Max $V_{IN}$ = $V_{IH}$ or $V_{IL}$ (Note 2) | | 100 | µA |
| $I_{OZL}$ | Off-State Output Leakage Current LOW | $V_{OUT}$ = 0.4 V, $V_{CC}$ = Max $V_{IN}$ = $V_{IH}$ or $V_{IL}$ (Note 2) | | −100 | µA |
| $I_{SC}$ | Output Short-Circuit Current | $V_{OUT}$ = 0.5 V, $V_{CC}$ = Max (Note 3) | −30 | −130 | mA |
| $I_{CC}$ | Supply Current | $V_{IN}$ = 0 V, Outputs Open ($I_{OUT}$ = 0 mA) $V_{CC}$ = Max | | 180 | mA |

***Notes:***

1. *These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.*
2. *I/O pin leakage is the worst case of $I_{IL}$ and $I_{OZL}$ (or $I_{IH}$ and $I_{OZH}$).*
3. *Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. $V_{OUT}$ = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

## CAPACITANCE (Note 1)

| Parameter Symbol | Parameter Description | Test Conditions | | Typ | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 2.0 V | $V_{CC}$ = 5.0 V<br>$T_A$ = 25°C<br>f = 1 MHz | 5 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = 2.0 V | | 8 | |

***Note:***

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

## SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

| Parameter Symbol | Parameter Description | | | | Min (Note 3) | Max | Unit |
|---|---|---|---|---|---|---|---|
| $t_{PD}$ | Input or Feedback to Combinatorial Output | | | 16L8, 16R6, 16R4 | 3 | 7.5 | ns |
| | | 1 Output Switching | | | 3 | 7 | |
| $t_S$ | Setup Time from Input or Feedback to Clock | | | 16R8, 16R6, 16R4 | 7 | | ns |
| $t_H$ | Hold Time | | | | 0 | | ns |
| $t_{CO}$ | Clock to Output | | | | 1 | 6.5 | ns |
| $t_{SKEW}$ | Skew Between Registered Outputs (Note 4) | | | | | 1 | ns |
| $t_{WL}$ | Clock Width | LOW | | | 5 | | ns |
| $t_{WH}$ | | HIGH | | | 5 | | ns |
| $f_{MAX}$ | Maximum Frequency (Note 5) | External Feedback | $1/(t_S + t_{CO})$ | | 74 | | MHz |
| | | Internal Feedback ($f_{CNT}$) | | | 100 | | MHz |
| | | No Feedback | $1/(t_{WH} + t_{WL})$ | | 100 | | MHz |
| $t_{PZX}$ | $\overline{OE}$ to Output Enable | | | | 1 | 8 | ns |
| $t_{PXZ}$ | $\overline{OE}$ to Output Disable | | | | 1 | 8 | ns |
| $t_{EA}$ | Input to Output Enable Using Product Term Control | | | 16L8, 16R6, 16R4 | 3 | 10 | ns |
| $t_{ER}$ | Input to Output Disable Using Product Term Control | | | | 3 | 10 | ns |

***Notes:***

2. *See Switching Test Circuit for test conditions.*
3. *Output delay minimums for $t_{PD}$, $t_{CO}$, $t_{PZX}$, $t_{PXZ}$, $t_{EA}$, and $t_{ER}$ are defined under best case conditions. Future process improvements may alter these values; therefore, minimum values are recommended for simulation purposes only.*
4. *Skew is measured with all outputs switching in the same direction.*
5. *These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where the frequency may be affected.*

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage with Respect to Ground ..... −0.5 V to + 7.0 V

DC Input Voltage ..... −1.5 V to + 5.5 V

DC Output or I/O Pin Voltage ..... −0.5 V to + 5.5 V

Static Discharge Voltage ..... 2001 V

*Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.*

## OPERATING RANGES

**Commercial (C) Devices**

Ambient Temperature ($T_A$) Operating in Free Air ..... 0°C to +75°C

Supply Voltage ($V_{CC}$) with Respect to Ground ..... +4.75 V to +5.25 V

*Operating ranges define those limits between which the functionality of the device is guaranteed.*

## DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

| Parameter Symbol | Parameter Description | Test Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $I_{OH}$ = −3.2 mA $V_{IN}$ = $V_{IH}$ or $V_{IL}$ $V_{CC}$ = Min | 2.4 | | V |
| $V_{OL}$ | Output LOW Voltage | $I_{OL}$ = 24 mA $V_{IN}$ = $V_{IH}$ or $V_{IL}$ $V_{CC}$ = Min | | 0.5 | V |
| $V_{IH}$ | Input HIGH Voltage | Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1) | 2.0 | | V |
| $V_{IL}$ | Input LOW Voltage | Guaranteed Input Logical LOW Voltage for all Inputs (Note 1) | | 0.8 | V |
| $V_I$ | Input Clamp Voltage | $I_{IN}$ = −18 mA, $V_{CC}$ = Min | | −1.5 | V |
| $I_{IH}$ | Input HIGH Current | $V_{IN}$ = 2.4 V, $V_{CC}$ = Max (Note 2) | | 25 | µA |
| $I_{IL}$ | Input LOW Current | $V_{IN}$ = 0.4 V, $V_{CC}$ = Max (Note 2) | | −250 | µA |
| $I_I$ | Maximum Input Current | $V_{IN}$ = 5.5 V, $V_{CC}$ = Max | | 100 | µA |
| $I_{OZH}$ | Off-State Output Leakage Current HIGH | $V_{OUT}$ = 2.4 V, $V_{CC}$ = Max $V_{IN}$ = $V_{IH}$ or $V_{IL}$ (Note 2) | | 100 | µA |
| $I_{OZL}$ | Off-State Output Leakage Current LOW | $V_{OUT}$ = 0.4 V, $V_{CC}$ = Max $V_{IN}$ = $V_{IH}$ or $V_{IL}$ (Note 2) | | −100 | µA |
| $I_{SC}$ | Output Short-Circuit Current | $V_{OUT}$ = 0.5 V, $V_{CC}$ = Max (Note 3) | −30 | −130 | mA |
| $I_{CC}$ | Supply Current | $V_{IN}$ = 0 V, Outputs Open ($I_{OUT}$ = 0 mA) $V_{CC}$ = Max | | 180 | mA |

***Notes:***

1. *These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.*
2. *I/O pin leakage is the worst case of $I_{IL}$ and $I_{OZL}$ (or $I_{IH}$ and $I_{OZH}$).*
3. *Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. $V_{OUT}$ = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

## CAPACITANCE (Note 1)

| Parameter Symbol | Parameter Description | Test Conditions | | Typ | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 2.0 V | $V_{CC}$ = 5.0 V, $T_A$ = 25°C, f = 1 MHz | 5 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = 2.0 V | | 8 | |

***Note:***

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

## SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

| Parameter Symbol | Parameter Description | | | | Min (Note 3) | Max | Unit |
|---|---|---|---|---|---|---|---|
| $t_{PD}$ | Input or Feedback to Combinatorial Output | | | 16L8, 16R6, 16R4 | 3 | 10 | ns |
| $t_S$ | Setup Time from Input or Feedback to Clock | | | 16R8, 16R6, 16R4 | 10 | | ns |
| $t_H$ | Hold Time | | | | 0 | | ns |
| $t_{CO}$ | Clock to Output | | | | 3 | 7 | ns |
| $t_{WL}$ | Clock Width | LOW | | | 8 | | ns |
| $t_{WH}$ | | HIGH | | | 8 | | ns |
| $f_{MAX}$ | Maximum Frequency (Note 4) | External Feedback | $1/(t_S + t_{CO})$ | | 58.8 | | MHz |
| | | Internal Feedback ($f_{CNT}$) | | | 60 | | MHz |
| | | No Feedback | $1/(t_{WH} + t_{WL})$ | | 62.5 | | MHz |
| $t_{PZX}$ | $\overline{OE}$ to Output Enable | | | | 2 | 10 | ns |
| $t_{PXZ}$ | $\overline{OE}$ to Output Disable | | | | 2 | 10 | ns |
| $t_{EA}$ | Input to Output Enable Using Product Term Control | | | 16L8, 16R6, 16R4 | 3 | 10 | ns |
| $t_{ER}$ | Input to Output Disable Using Product Term Control | | | | 3 | 10 | ns |

***Notes:***

2. *See Switching Test Circuit for test conditions.*
3. *Output delay minimums for $t_{PD}$, $t_{CO}$, $t_{PZX}$, $t_{PXZ}$, $t_{EA}$, and $t_{ER}$ are defined under best case conditions. Future process improvements may alter these values; therefore, minimum values are recommended for simulation purposes only.*
4. *These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where the frequency may be affected.*

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage with Respect to Ground ..... −0.5 V to +7.0 V

DC Input Voltage ..... −1.5 V to Vcc + 0.5 V

DC Output or I/O Pin Voltage ..... −0.5 V to Vcc + 0.5 V

*Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.*

## OPERATING RANGES

**Commercial (C) Devices**

Ambient Temperature ($T_A$) Operating in Free Air ..... 0°C to +75°C

Supply Voltage ($V_{CC}$) with Respect to Ground ..... +4.75 V to +5.25 V

*Operating ranges define those limits between which the functionality of the device is guaranteed.*

## DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

| Parameter Symbol | Parameter Description | Test Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $I_{OH}$ = −3.2 mA, $V_{IN}$ = $V_{IH}$ or $V_{IL}$, $V_{CC}$ = Min | 2.4 | | V |
| $V_{OL}$ | Output LOW Voltage | $I_{OL}$ = 24 mA, $V_{IN}$ = $V_{IH}$ or $V_{IL}$, $V_{CC}$ = Min | | 0.5 | V |
| $V_{IH}$ | Input HIGH Voltage | Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1) | 2.0 | | V |
| $V_{IL}$ | Input LOW Voltage | Guaranteed Input Logical LOW Voltage for all Inputs (Note 1) | | 0.8 | V |
| $V_I$ | Input Clamp Voltage | $I_{IN}$ = −18 mA, $V_{CC}$ = Min | | −1.2 | V |
| $I_{IH}$ | Input HIGH Current | $V_{IN}$ = 2.4 V, $V_{CC}$ = Max (Note 2) | | 25 | µA |
| $I_{IL}$ | Input LOW Current | $V_{IN}$ = 0.4 V, $V_{CC}$ = Max (Note 2) | | −250 | µA |
| $I_I$ | Maximum Input Current | $V_{IN}$ = 5.5 V, $V_{CC}$ = Max | | 100 | µA |
| $I_{OZH}$ | Off-State Output Leakage Current HIGH | $V_{OUT}$ = 2.4 V, $V_{CC}$ = Max, $V_{IN}$ = $V_{IH}$ or $V_{IL}$ (Note 2) | | 100 | µA |
| $I_{OZL}$ | Off-State Output Leakage Current LOW | $V_{OUT}$ = 0.4 V, $V_{CC}$ = Max, $V_{IN}$ = $V_{IH}$ or $V_{IL}$ (Note 2) | | −100 | µA |
| $I_{SC}$ | Output Short-Circuit Current | $V_{OUT}$ = 0.5 V, $V_{CC}$ = Max (Note 3) | −30 | −130 | mA |
| $I_{CC}$ | Supply Current | $V_{IN}$ = 0 V, Outputs Open ($I_{OUT}$ = 0 mA), $V_{CC}$ = Max | | 180 | mA |

***Notes:***

1. *These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.*
2. *I/O pin leakage is the worst case of $I_{IL}$ and $I_{OZL}$ (or $I_{IH}$ and $I_{OZH}$).*
3. *Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. $V_{OUT}$ = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

## CAPACITANCE (Note 1)

| Parameter Symbol | Parameter Description | Test Conditions | | Typ | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 2.0 V | $V_{CC}$ = 5.0 V, $T_A$ = 25°C, f = 1 MHz | 8 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = 2.0 V | | 9 | |

***Note:***

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

## SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

| Parameter Symbol | Parameter Description | | | | Min | Max | Unit |
|---|---|---|---|---|---|---|---|
| $t_{PD}$ | Input or Feedback to Combinatorial Output | | | 16L8, 16R6, 16R4 | | 15 | ns |
| ts | Setup Time from Input or Feedback to Clock | | | 16R8, 16R6, 16R4 | 15 | | ns |
| $t_H$ | Hold Time | | | | 0 | | ns |
| tco | Clock to Output or Feedback | | | | | 12 | ns |
| $t_{WL}$ | Clock Width | LOW | | | 10 | | ns |
| $t_{WH}$ | | HIGH | | | 10 | | ns |
| $f_{MAX}$ | Maximum Frequency (Note 3) | External Feedback | 1/(ts + tco) | | 37 | | MHz |
| | | No Feedback | 1/($t_{WH}$ + $t_{WL}$) | | 50 | | MHz |
| $t_{PZX}$ | $\overline{OE}$ to Output Enable | | | | | 15 | ns |
| $t_{PXZ}$ | $\overline{OE}$ to Output Disable | | | | | 15 | ns |
| $t_{EA}$ | Input to Output Enable Using Product Term Control | | | 16R8, 16R6, 16R4 | | 15 | ns |
| $t_{ER}$ | Input to Output Disable Using Product Term Control | | | | | 15 | ns |

***Notes:***

2. *See Switching Test Circuit for test conditions.*
3. *These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.*

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage with Respect to Ground ..... −0.5 V to +7.0 V

DC Input Voltage ..... −1.5 V to $V_{CC}$ + 0.5 V

DC Output or I/O Pin Voltage ..... −0.5 V to $V_{CC}$ + 0.5 V

*Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.*

## OPERATING RANGES

### Commercial (C) Devices

Ambient Temperature ($T_A$) Operating in Free Air ..... 0°C to +75°C

Supply Voltage ($V_{CC}$) with Respect to Ground ..... +4.75 V to +5.25 V

*Operating ranges define those limits between which the functionality of the device is guaranteed.*

## DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

| Parameter Symbol | Parameter Description | Test Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $I_{OH}$ = −3.2 mA $V_{IN}$ = $V_{IH}$ or $V_{IL}$ $V_{CC}$ = Min | 2.4 | | V |
| $V_{OL}$ | Output LOW Voltage | $I_{OL}$ = 24 mA $V_{IN}$ = $V_{IH}$ or $V_{IL}$ $V_{CC}$ = Min | | 0.5 | V |
| $V_{IH}$ | Input HIGH Voltage | Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1) | 2.0 | | V |
| $V_{IL}$ | Input LOW Voltage | Guaranteed Input Logical LOW Voltage for all Inputs (Note 1) | | 0.8 | V |
| $V_I$ | Input Clamp Voltage | $I_{IN}$ = −18 mA, $V_{CC}$ = Min | | −1.2 | V |
| $I_{IH}$ | Input HIGH Current | $V_{IN}$ = 2.7 V, $V_{CC}$ = Max (Note 2) | | 25 | µA |
| $I_{IL}$ | Input LOW Current | $V_{IN}$ = 0.4 V, $V_{CC}$ = Max (Note 2) | | −100 | µA |
| $I_I$ | Maximum Input Current | $V_{IN}$ = 5.5 V, $V_{CC}$ = Max | | 100 | µA |
| $I_{OZH}$ | Off-State Output Leakage Current HIGH | $V_{OUT}$ = 2.7 V, $V_{CC}$ = Max $V_{IN}$ = $V_{IH}$ or $V_{IL}$ (Note 2) | | 100 | µA |
| $I_{OZL}$ | Off-State Output Leakage Current LOW | $V_{OUT}$ = 0.4 V, $V_{CC}$ = Max $V_{IN}$ = $V_{IH}$ or $V_{IL}$ (Note 2) | | −100 | µA |
| $I_{SC}$ | Output Short-Circuit Current | $V_{OUT}$ = 0.5 V, $V_{CC}$ = Max (Note 3) | −30 | −130 | mA |
| $I_{CC}$ | Supply Current | $V_{IN}$ = 0 V, Outputs Open ($I_{OUT}$ = 0 mA) $V_{CC}$ = Max | | 90 | mA |

***Notes:***

1. *These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.*
2. *I/O pin leakage is the worst case of $I_{IL}$ and $I_{OZL}$ (or $I_{IH}$ and $I_{OZH}$).*
3. *Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. $V_{OUT}$ = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

## CAPACITANCE (Note 1)

| Parameter Symbol | Parameter Description | Test Conditions | | Typ | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 2.0 V | $V_{CC}$ = 5.0 V<br>$T_A$ = 25°C<br>f = 1 MHz | 7 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = 2.0 V | | 7 | |

***Note:***

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

## SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

| Parameter Symbol | Parameter Description | | | | Min | Max | Unit |
|---|---|---|---|---|---|---|---|
| $t_{PD}$ | Input or Feedback to Combinatorial Output | | | 16L8, 16R6, 16R4 | | 25 | ns |
| $t_S$ | Setup Time from Input or Feedback to Clock | | | 16R8, 16R6, 16R4 | 25 | | ns |
| $t_H$ | Hold Time | | | | 0 | | ns |
| $t_{CO}$ | Clock to Output | | | | | 15 | ns |
| $t_{WL}$ | Clock Width | LOW | | | 15 | | ns |
| $t_{WH}$ | | HIGH | | | 15 | | ns |
| $f_{MAX}$ | Maximum Frequency (Note 4) | External Feedback | $1/(t_S + t_{CO})$ | | 25 | | MHz |
| | | Internal Feedback ($f_{CNT}$) | | | 28.5 | | MHz |
| | | No Feedback | $1/(t_{WH} + t_{WL})$ | | 33 | | MHz |
| $t_{PZX}$ | $\overline{OE}$ to Output Enable | | | | | 20 | ns |
| $t_{PXZ}$ | $\overline{OE}$ to Output Disable | | | | | 20 | ns |
| $t_{EA}$ | Input to Output Enable Using Product Term Control | | | 16R8, 16R6, 16R4 | | 25 | ns |
| $t_{ER}$ | Input to Output Disable Using Product Term Control | | | | | 25 | ns |

***Notes:***

2. *See Switching Test Circuit for test conditions.*
3. *Calculated from measured $f_{MAX}$ internal.*
4. *These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.*

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage with Respect to Ground ..... −0.5 V to + 7.0 V

DC Input Voltage ..... −1.5 V to $V_{CC}$ + 0.5 V

DC Output or I/O Pin Voltage ..... −0.5 V to $V_{CC}$ + 0.5 V

*Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.*

## OPERATING RANGES

**Commercial (C) Devices**

Ambient Temperature ($T_A$) Operating in Free Air ..... 0°C to +75°C

Supply Voltage ($V_{CC}$) with Respect to Ground ..... +4.75 V to +5.25 V

*Operating ranges define those limits between which the functionality of the device is guaranteed.*

## DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

| Parameter Symbol | Parameter Description | | Test Conditions | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | | $I_{OH}$ = −3.2 mA $V_{IN}$ = $V_{IH}$ or $V_{IL}$ $V_{CC}$ = Min | 2.4 | | V |
| $V_{OL}$ | Output LOW Voltage | | $I_{OL}$ = 24 mA $V_{IN}$ = $V_{IH}$ or $V_{IL}$ $V_{CC}$ = Min | | 0.5 | V |
| $V_{IH}$ | Input HIGH Voltage | | Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1) | 2.0 | | V |
| $V_{IL}$ | Input LOW Voltage | | Guaranteed Input Logical LOW Voltage for all Inputs (Note 1) | | 0.8 | V |
| $V_I$ | Input Clamp Voltage | | $I_{IN}$ = −18 mA, $V_{CC}$ = Min | | −1.2 | V |
| $I_{IH}$ | Input HIGH Current | | $V_{IN}$ = 2.7 V, $V_{CC}$ = Max (Note 2) | | 25 | µA |
| $I_{IL}$ | Input LOW Current | | $V_{IN}$ = 0.4 V, $V_{CC}$ = Max (Note 2) | | −250 | µA |
| $I_I$ | Maximum Input Current | | $V_{IN}$ = 5.5 V, $V_{CC}$ = Max | | 100 | µA |
| $I_{OZH}$ | Off-State Output Leakage Current HIGH | | $V_{OUT}$ = 2.7 V, $V_{CC}$ = Max $V_{IN}$ = $V_{IH}$ or $V_{IL}$ (Note 2) | | 100 | µA |
| $I_{OZL}$ | Off-State Output Leakage Current LOW | | $V_{OUT}$ = 0.4 V, $V_{CC}$ = Max $V_{IN}$ = $V_{IH}$ or $V_{IL}$ (Note 2) | | −100 | µA |
| $I_{SC}$ | Output Short-Circuit Current | | $V_{OUT}$ = 0.5 V, $V_{CC}$ = Max (Note 3) | −30 | −130 | mA |
| $I_{CC}$ | Supply Current | 16L8 | $V_{IN}$ = 0 V, Outputs Open ($I_{OUT}$ = 0 mA) $V_{CC}$ = Max | | 155 | mA |
| | | 16R8/6/4 | | | 180 | |

***Notes:***

1. *These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.*
2. *I/O pin leakage is the worst case of $I_{IL}$ and $I_{OZL}$ (or $I_{IH}$ and $I_{OZH}$).*
3. *Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. $V_{CC}$ = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

## CAPACITANCE (Note 1)

| Parameter Symbol | Parameter Description | Test Conditions | | Typ | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 2.0 V | $V_{CC}$ = 5.0 V<br>$T_A$ = 25°C<br>f = 1 MHz | 7 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = 2.0 V | | 7 | |

***Note:***

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

## SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

| Parameter Symbol | Parameter Description | | | | Min | Max | Unit |
|---|---|---|---|---|---|---|---|
| $t_{PD}$ | Input or Feedback to Combinatorial Output | | | 16L8, 16R6, 16R4 | | 25 | ns |
| $t_S$ | Setup Time from Input or Feedback to Clock | | | 16R8, 16R6, 16R4 | 25 | | ns |
| $t_H$ | Hold Time | | | | 0 | | ns |
| $t_{CO}$ | Clock to Output | | | | | 15 | ns |
| $t_{WL}$ | Clock Width | LOW | | | 15 | | ns |
| $t_{WH}$ | | HIGH | | | 15 | | ns |
| $f_{MAX}$ | Maximum Frequency (Note 4) | External Feedback | $1/(t_S + t_{CO})$ | | 25 | | MHz |
| | | Internal Feedback ($f_{CNT}$) | | | 28.5 | | MHz |
| | | No Feedback | $1/(t_{WH} + t_{WL})$ | | 33 | | MHz |
| $t_{PZX}$ | $\overline{OE}$ to Output Enable | | | | | 20 | ns |
| $t_{PXZ}$ | $\overline{OE}$ to Output Disable | | | | | 20 | ns |
| $t_{EA}$ | Input to Output Enable Using Product Term Control | | | 16R8, 16R6, 16R4 | | 25 | ns |
| $t_{ER}$ | Input to Output Disable Using Product Term Control | | | | | 25 | ns |

***Notes:***

2. *See Switching Test Circuit for test conditions.*
3. *Calculated from measured $f_{MAX}$ internal.*
4. *These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.*

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage with Respect to Ground ..... −0.5 V to +7.0 V

DC Input Voltage ..... −1.5 V to +5.5 V

DC Output or I/O Pin Voltage ..... 5.5 V

*Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.*

## OPERATING RANGES

### Commercial (C) Devices

Ambient Temperature ($T_A$) Operating in Free Air ..... 0°C to +75°C

Supply Voltage ($V_{CC}$) with Respect to Ground ..... +4.75 V to +5.25 V

*Operating ranges define those limits between which the functionality of the device is guaranteed.*

## DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

| Parameter Symbol | Parameter Description | Test Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $I_{OH}$ = −1 mA $V_{IN}$ = $V_{IH}$ or $V_{IL}$ $V_{CC}$ = Min | 2.4 | | V |
| $V_{OL}$ | Output LOW Voltage | $I_{OL}$ = 8 mA $V_{IN}$ = $V_{IH}$ or $V_{IL}$ $V_{CC}$ = Min | | 0.5 | V |
| $V_{IH}$ | Input HIGH Voltage | Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1) | 2.0 | | V |
| $V_{IL}$ | Input LOW Voltage | Guaranteed Input Logical LOW Voltage for all Inputs (Note 1) | | 0.8 | V |
| $V_I$ | Input Clamp Voltage | $I_{IN}$ = −18 mA, $V_{CC}$ = Min | | −1.5 | V |
| $I_{IH}$ | Input HIGH Current | $V_{IN}$ = 2.4 V, $V_{CC}$ = Max (Note 2) | | 25 | µA |
| $I_{IL}$ | Input LOW Current | $V_{IN}$ = 0.4 V, $V_{CC}$ = Max (Note 2) | | −250 | µA |
| $I_I$ | Maximum Input Current | $V_{IN}$ = 5.5 V, $V_{CC}$ = Max | | 100 | µA |
| $I_{OZH}$ | Off-State Output Leakage Current HIGH | $V_{OUT}$ = 2.4 V, $V_{CC}$ = Max $V_{IN}$ = $V_{IH}$ or $V_{IL}$ (Note 2) | | 100 | µA |
| $I_{OZL}$ | Off-State Output Leakage Current LOW | $V_{OUT}$ = 0.4 V, $V_{CC}$ = Max $V_{IN}$ = $V_{IH}$ or $V_{IL}$ (Note 2) | | −100 | µA |
| $I_{SC}$ | Output Short-Circuit Current | $V_{OUT}$ = 0.5 V, $V_{CC}$ = Max (Note 3) | −30 | −250 | mA |
| $I_{CC}$ | Supply Current | $V_{IN}$ = 0 V, Outputs Open ($I_{OUT}$ = 0 mA) $V_{CC}$ = Max | | 55 | mA |

***Notes:***

1. *These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.*
2. *I/O pin leakage is the worst case of $I_{IL}$ and $I_{OZL}$ (or $I_{IH}$ and $I_{OZH}$).*
3. *Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. $V_{OUT}$ = 0.5 V as been chosen to avoid test problems caused by tester ground degradation.*

## SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 1)

| Parameter Symbol | Parameter Description | | | | Min | Max | Unit |
|---|---|---|---|---|---|---|---|
| $t_{PD}$ | Input or Feedback to Combinatorial Output | | | 16L8, 16R6, 16R4 | | 35 | ns |
| $t_S$ | Setup Time from Input or Feedback to Clock | | | 16R8, 16R6, 16R4 | 35 | | ns |
| $t_H$ | Hold Time | | | | 0 | | ns |
| $t_{CO}$ | Clock to Output or Feedback | | | | | 25 | ns |
| $t_{WL}$ | Clock Width | LOW | | | 25 | | ns |
| $t_{WH}$ | | HIGH | | | 25 | | ns |
| $f_{MAX}$ | Maximum Frequency (Note 2) | External Feedback | $1/(t_S + t_{CO})$ | | 16 | | MHz |
| | | No Feedback | $1/(t_{WH} + t_{WL})$ | | 20 | | MHz |
| $t_{PZX}$ | $\overline{OE}$ to Output Enable | | | | | 25 | ns |
| $t_{PXZ}$ | $\overline{OE}$ to Output Disable | | | | | 25 | ns |
| $t_{EA}$ | Input to Output Enable Using Product Term Control | | | 16L8, 16R6, 16R4 | | 35 | ns |
| $t_{ER}$ | Input to Output Disable Using Product Term Control | | | | | 35 | ns |

***Notes:***

1. *See Switching Test Circuit for test conditions.*
2. *These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.*

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage with Respect to Ground ..... −0.5 V to +7.0 V

DC Input Voltage ..... −1.2 V to +5.5 V

DC Input Current ..... −30 mA to +5 mA

DC Output or I/O Pin Voltage ..... −0.5 V to $V_{CC}$ + 0.5 V

Static Discharge Voltage ..... 2001 V

*Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ. Absolute Maximum Ratings are for system design reference; parameters given are not tested.*

## OPERATING RANGES

**Military (M) Devices (Note 1)**

Ambient Temperature ($T_A$) Operating in Free Air ..... −55°C Min

Operating Case ($T_C$) Temperature ..... 125°C Max

Supply Voltage ($V_{CC}$) with Respect to Ground ..... +4.50 V to +5.50 V

***Note:***

*1. Military products are tested at $T_C$ = +25°C, +125°C, and −55°C, per MIL-STD-883.*

*Operating ranges define those limits between which the functionality of the device is guaranteed.*

## DC CHARACTERISTICS over MILITARY operating ranges unless otherwise specified (Note 2)

| Parameter Symbol | Parameter Description | Test Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $I_{OH}$ = −2 mA $V_{IN}$ = $V_{IH}$ or $V_{IL}$ $V_{CC}$ = Min | 2.4 | | V |
| $V_{OL}$ | Output LOW Voltage | $I_{OL}$ = 12 mA $V_{IN}$ = $V_{IH}$ or $V_{IL}$ $V_{CC}$ = Min | | 0.5 | V |
| $V_{IH}$ | Input HIGH Voltage | Guaranteed Input Logical HIGH Voltage for all Inputs (Note 3) | 2.0 | | V |
| $V_{IL}$ | Input LOW Voltage | Guaranteed Input Logical LOW Voltage for all Inputs (Note 3) | | 0.8 | V |
| $V_I$ | Input Clamp Voltage | $I_{IN}$ = −18 mA, $V_{CC}$ = Min | | −1.2 | V |
| $I_{IH}$ | Input HIGH Current | $V_{IN}$ = 2.7 V, $V_{CC}$ = Max (Note 4) | | 25 | µA |
| $I_{IL}$ | Input LOW Current | $V_{IN}$ = 0.4 V, $V_{CC}$ = Max (Note 4) | | −250 | µA |
| $I_I$ | Maximum Input Current | $V_{IN}$ = 5.5 V, $V_{CC}$ = Max | | 1 | mA |
| $I_{OZH}$ | Off-State Output Leakage Current HIGH | $V_{OUT}$ = 2.7 V, $V_{CC}$ = Max $V_{IN}$ = $V_{IH}$ or $V_{IL}$ (Note 4) | | 100 | µA |
| $I_{OZL}$ | Off-State Output Leakage Current LOW | $V_{OUT}$ = 0.4 V, $V_{CC}$ = Max $V_{IN}$ = $V_{IH}$ or $V_{IL}$ (Note 4) | | −100 | µA |
| $I_{SC}$ | Output Short-Circuit Current | $V_{OUT}$ = 0.5 V, $V_{CC}$ = Max (Note 5) | −30 | −130 | mA |
| $I_{CC}$ | Supply Current | $V_{IN}$ = 0 V, Outputs Open ($I_{OUT}$ = 0 mA) $V_{CC}$ = Max | | 200 | mA |

***Notes:***

*2. For APL Products, Group A, Subgroups 1, 2, and 3 are tested per MIL-STD-883, Method 5005, unless otherwise noted.*

*3. $V_{IL}$ and $V_{IH}$ are input conditions of output tests and are not themselves directly tested. $V_{IL}$ and $V_{IH}$ are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.*

*4. I/O pin leakage is the worst case of $I_{IL}$ and $I_{OZL}$ (or $I_{IH}$ and $I_{OZH}$).*

*5. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. $V_{OUT}$ = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

## CAPACITANCE (Note 1)

| Parameter Symbol | Parameter Description | | Test Conditions | | Typ | Unit |
|---|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | Corner Pins | $V_{IN}$ = 2.0 V | $V_{CC}$ = 5.0 V, $T_A$ = 25°C, f = 1 MHz | 10 | pF |
| | | Middle Pins | | | 5 | |
| $C_{OUT}$ | Output Capacitance | | $V_{OUT}$ = 2.0 V | | 9 | |

***Note:***

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

## SWITCHING CHARACTERISTICS over MILITARY operating ranges (Note 2)

| Parameter Symbol | Parameter Description | | | | -10 | | -12 | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | Min (Note 3) | Max | Min (Note 3) | Max | |
| $t_{PD}$ | Input or Feedback to Combinatorial Output | | | 16L8, 16R6, 16R4 | 3 | 10 | 3 | 12 | ns |
| $t_S$ | Setup Time from Input or Feedback to Clock | | | 16R8, 16R6, 16R4 | 10 | | 10 | | ns |
| $t_H$ | Hold Time | | | | 0 | | 0 | | ns |
| $t_{CO}$ | Clock to Output | | | | 3 | 9 | 3 | 11 | ns |
| $t_{SKEW}$ | Skew Between Registered Outputs (Note 4) | | | | | 1 | | 1 | ns |
| $t_{WL}$ | Clock Width | LOW | | | 8 | | 8 | | ns |
| $t_{WH}$ | | HIGH | | | 8 | | 8 | | ns |
| $f_{MAX}$ | Maximum Frequency (Note 5) | External Feedback | $1/(t_S + t_{CO})$ | | 52.6 | | 47.6 | | MHz |
| | | Internal Feedback ($f_{CNT}$) | | | 60.6 | | 60.6 | | MHz |
| | | No Feedback | $1/(t_{WH} + t_{WL})$ | | 62.5 | | 62.5 | | MHz |
| $t_{PZX}$ | $\overline{OE}$ to Output Enable (Note 5) | | | | 3 | 10 | 3 | 12 | ns |
| $t_{PXZ}$ | $\overline{OE}$ to Output Disable (Note 5) | | | | 3 | 10 | 3 | 12 | ns |
| $t_{EA}$ | Input to Output Enable Using Product Term Control (Note 5) | | | 16L8, 16R6, 16R4 | 3 | 10 | 3 | 12 | ns |
| $t_{ER}$ | Input to Output Disable Using Product Term Control (Note 5) | | | | 3 | 10 | 3 | 12 | ns |

***Notes:***

2. *See Switching Test Circuit for test conditions. For APL products Group A, Subgroups 9, 10, and 11 are tested per MIL-STD-883, Method 5005, unless otherwise noted.*
3. *Minimum value for $t_{PD}$, $t_{CO}$, $t_{PZX}$, $t_{PXZ}$, $t_{EA}$, and $t_{ER}$ parameters should be used for simulation purposes only and are not tested.*
4. *Skew is measured with all outputs switching in the same direction.*
5. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.*

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage with Respect to Ground ..... −0.5 V to +7.0 V

DC Input Voltage ..... −1.5 V to +5.5 V

DC Output or I/O Pin Voltage ..... 5.5 V

*Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ. Absolute Maximum Ratings are for system design reference; parameters given are not tested.*

## OPERATING RANGES

**Military (M) Devices (Note 1)**

Ambient Temperature ($T_A$) Operating in Free Air ..... −55°C Min

Operating Case ($T_C$) Temperature ..... 125°C Max

Supply Voltage ($V_{CC}$) with Respect to Ground ..... +4.50 V to +5.50 V

***Note:***

*1. Military products are tested at $T_C$ = +25°C, +125°C, and −55°C, per MIL-STD-883.*

*Operating ranges define those limits between which the functionality of the device is guaranteed.*

## DC CHARACTERISTICS over MILITARY operating ranges unless otherwise specified (Note 2)

| Parameter Symbol | Parameter Description | Test Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $I_{OH}$ = −2 mA $V_{IN}$ = $V_{IH}$ or $V_{IL}$ $V_{CC}$ = Min | 2.4 | | V |
| $V_{OL}$ | Output LOW Voltage | $I_{OL}$ = 12 mA $V_{IN}$ = $V_{IH}$ or $V_{IL}$ $V_{CC}$ = Min | | 0.5 | V |
| $V_{IH}$ | Input HIGH Voltage | Guaranteed Input Logical HIGH Voltage for all Inputs (Note 3) | 2.0 | | V |
| $V_{IL}$ | Input LOW Voltage | Guaranteed Input Logical LOW Voltage for all Inputs (Note 3) | | 0.8 | V |
| $V_I$ | Input Clamp Voltage | $I_{IN}$ = −18 mA, $V_{CC}$ = Min | | −1.5 | V |
| $I_{IH}$ | Input HIGH Current | $V_{IN}$ = 2.4 V, $V_{CC}$ = Max (Note 4) | | 25 | µA |
| $I_{IL}$ | Input LOW Current | $V_{IN}$ = 0.4 V, $V_{CC}$ = Max (Note 4) | | −250 | µA |
| $I_I$ | Maximum Input Current | $V_{IN}$ = 5.5 V, $V_{CC}$ = Max | | 1 | mA |
| $I_{OZH}$ | Off-State Output Leakage Current HIGH | $V_{OUT}$ = 2.4 V, $V_{CC}$ = Max $V_{IN}$ = $V_{IH}$ or $V_{IL}$ (Note 4) | | 100 | µA |
| $I_{OZL}$ | Off-State Output Leakage Current LOW | $V_{OUT}$ = 0.4 V, $V_{CC}$ = Max $V_{IN}$ = $V_{IH}$ or $V_{IL}$ (Note 4) | | −100 | µA |
| $I_{SC}$ | Output Short-Circuit Current | $V_{OUT}$ = 0.5 V, $V_{CC}$ = Max (Note 5) | −30 | −130 | mA |
| $I_{CC}$ | Supply Current | $V_{IN}$ = 0 V, Outputs Open ($I_{OUT}$ = 0 mA) $V_{CC}$ = Max | | 180 | mA |

***Notes:***

*2. For APL Products, Group A, Subgroups 1, 2, and 3 are tested per MIL-STD-883, Method 5005, unless otherwise noted.*

*3. $V_{IL}$ and $V_{IH}$ are input conditions of output tests and are not themselves directly tested. $V_{IL}$ and $V_{IH}$ are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.*

*4. I/O pin leakage is the worst case of $I_{IL}$ and $I_{OZL}$ (or $I_{IH}$ and $I_{OZH}$).*

*5. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. $V_{OUT}$ = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

## CAPACITANCE (Note 1)

| Parameter Symbol | Parameter Description | Test Conditions | | Typ | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 2.0 V | $V_{CC}$ = 5.0 V, $T_A$ = 25°C, f = 1 MHz | 9 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = 2.0 V | | 10 | |

***Note:***

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

## SWITCHING CHARACTERISTICS over MILITARY operating ranges (Note 2)

| Parameter Symbol | Parameter Description | | | | Min | Max | Unit |
|---|---|---|---|---|---|---|---|
| $t_{PD}$ | Input or Feedback to Combinatorial Output | | | 16L8, 16R6, 16R4 | | 20 | ns |
| $t_S$ | Setup Time from Input or Feedback to Clock | | | 16L8, 16R6, 16R4 | 20 | | ns |
| $t_H$ | Hold Time | | | | 0 | | ns |
| $t_{CO}$ | Clock to Output or Feedback | | | | | 15 | ns |
| $t_{WL}$ | Clock Width | LOW | | | 12 | | ns |
| $t_{WH}$ | | HIGH | | | 12 | | ns |
| $f_{MAX}$ | Maximum Frequency (Note 3) | External Feedback | $1/(t_S + t_{CO})$ | | 28.5 | | MHz |
| | | No Feedback | $1/(t_{WH} + t_{WL})$ | | 41.6 | | MHz |
| $t_{PZX}$ | $\overline{OE}$ to Output Enable (Note 4) | | | | | 20 | ns |
| $t_{PXZ}$ | $\overline{OE}$ to Output Disable (Note 4) | | | | | 20 | ns |
| $t_{EA}$ | Input to Output Enable Using Product Term Control (Note 4) | | | 16L8, 16R6, 16R4 | | 25 | ns |
| $t_{ER}$ | Input to Output Disable Using Product Term Control (Note 4) | | | | | 20 | ns |

***Notes:***

2. *See Switching Test Circuit for test conditions. For APL products Group A, Subgroups 9, 10, and 11 are tested per MIL-STD-883, Method 5005, unless otherwise noted.*
3. *These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.*
4. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.*

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage with Respect to Ground ..... −0.5 V to +7.0 V

DC Input Voltage ..... −1.5 V to +5.5 V

DC Output or I/O Pin Voltage ..... 5.5 V

*Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ. Absolute Maximum Ratings are for system design reference; parameters given are not tested.*

## OPERATING RANGES

**Military (M) Devices (Note 1)**

Ambient Temperature ($T_A$) Operating in Free Air ..... −55°C Min

Operating Case ($T_C$) Temperature ..... 125°C Max

Supply Voltage ($V_{CC}$) with Respect to Ground ..... +4.50 V to +5.50 V

***Note:***

1. *Military products are tested at $T_C$ = +25°C, +125°C, and −55°C, per MIL-STD-883.*

*Operating ranges define those limits between which the functionality of the device is guaranteed.*

## DC CHARACTERISTICS over MILITARY operating ranges unless otherwise specified (Note 2)

| Parameter Symbol | Parameter Description | Test Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $I_{OH}$ = −2 mA $V_{IN}$ = $V_{IH}$ or $V_{IL}$ $V_{CC}$ = Min | 2.4 | | V |
| $V_{OL}$ | Output LOW Voltage | $I_{OL}$ = 12 mA $V_{IN}$ = $V_{IH}$ or $V_{IL}$ $V_{CC}$ = Min | | 0.5 | V |
| $V_{IH}$ | Input HIGH Voltage | Guaranteed Input Logical HIGH Voltage for all Inputs (Note 3) | 2.0 | | V |
| $V_{IL}$ | Input LOW Voltage | Guaranteed Input Logical LOW Voltage for all Inputs (Note 3) | | 0.8 | V |
| $V_I$ | Input Clamp Voltage | $I_{IN}$ = −18 mA, $V_{CC}$ = Min | | −1.5 | V |
| $I_{IH}$ | Input HIGH Current | $V_{IN}$ = 2.4 V, $V_{CC}$ = Max (Note 4) | | 25 | µA |
| $I_{IL}$ | Input LOW Current | $V_{IN}$ = 0.4 V, $V_{CC}$ = Max (Note 4) | | −250 | µA |
| $I_I$ | Maximum Input Current | $V_{IN}$ = 5.5 V, $V_{CC}$ = Max | | 1 | mA |
| $I_{OZH}$ | Off-State Output Leakage Current HIGH | $V_{OUT}$ = 2.4 V, $V_{CC}$ = Max $V_{IN}$ = $V_{IH}$ or $V_{IL}$ (Note 4) | | 100 | µA |
| $I_{OZL}$ | Off-State Output Leakage Current LOW | $V_{OUT}$ = 0.4 V, $V_{CC}$ = Max $V_{IN}$ = $V_{IH}$ or $V_{IL}$ (Note 4) | | −100 | µA |
| $I_{SC}$ | Output Short-Circuit Current | $V_{OUT}$ = 0.5 V, $V_{CC}$ = Max (Note 5) | −30 | −130 | mA |
| $I_{CC}$ | Supply Current | $V_{IN}$ = 0 V, Outputs Open ($I_{OUT}$ = 0 mA) $V_{CC}$ = Max | | 90 | mA |

***Notes:***

2. *For APL Products, Group A, Subgroups 1, 2, and 3 are tested per MIL-STD-883, Method 5005, unless otherwise noted.*
3. *$V_{IL}$ and $V_{IH}$ are input conditions of output tests and are not themselves directly tested. $V_{IL}$ and $V_{IH}$ are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.*
4. *I/O pin leakage is the worst case of $I_{IL}$ and $I_{OZL}$ (or $I_{IH}$ and $I_{OZH}$).*
5. *Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. $V_{OUT}$ = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

## CAPACITANCE (Note 1)

| Parameter Symbol | Parameter Description | Test Conditions | | Typ | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 2.0 V | $V_{CC}$ = 5.0 V<br>$T_A$ = 25°C<br>f = 1 MHz | 7 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = 2.0 V | | 7 | |

***Note:***

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

## SWITCHING CHARACTERISTICS over MILITARY operating ranges (Note 2)

| Parameter Symbol | Parameter Description | | | | Min | Max | Unit |
|---|---|---|---|---|---|---|---|
| $t_{PD}$ | Input or Feedback to Combinatorial Output | | | 16L8, 16R6, 16R4 | | 30 | ns |
| $t_S$ | Setup Time from Input or Feedback to Clock | | | 16L8, 16R6, 16R4 | 30 | | ns |
| $t_H$ | Hold Time | | | | 0 | | ns |
| $t_{CO}$ | Clock to Output or Feedback | | | | | 20 | ns |
| $t_{WL}$ | Clock Width | LOW | | | 20 | | ns |
| $t_{WH}$ | | HIGH | | | 20 | | ns |
| $f_{MAX}$ | Maximum Frequency (Note 3) | External Feedback | $1/(t_S + t_{CO})$ | | 20 | | MHz |
| | | No Feedback | $1/(t_{WH} + t_{WL})$ | | 25 | | MHz |
| $t_{PZX}$ | $\overline{OE}$ to Output Enable (Note 4) | | | | | 25 | ns |
| $t_{PXZ}$ | $\overline{OE}$ to Output Disable (Note 4) | | | | | 25 | ns |
| $t_{EA}$ | Input to Output Enable Using Product Term Control (Note 4) | | | 16L8, 16R6, 16R4 | | 30 | ns |
| $t_{ER}$ | Input to Output Disable Using Product Term Control (Note 4) | | | | | 30 | ns |

***Notes:***

2. *See Switching Test Circuit for test conditions. For APL products Group A, Subgroups 9, 10, and 11 are tested per MIL-STD-883, Method 5005, unless otherwise noted.*
3. *These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.*
4. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.*

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage with Respect to Ground ..... −0.5 V to + 7.0 V

DC Input Voltage ..... −1.5 V to + 5.5 V

DC Output or I/O Pin Voltage ..... 5.5 V

*Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ. Absolute Maximum Ratings are for system design reference; parameters given are not tested.*

## OPERATING RANGES

**Military (M) Devices (Note 1)**

Ambient Temperature ($T_A$) Operating in Free Air ..... −55°C Min

Operating Case ($T_C$) Temperature ..... 125°C Max

Supply Voltage ($V_{CC}$) with Respect to Ground ..... +4.50 V to +5.50 V

***Note:***

*1. Military products are tested at $T_C$ = +25°C, +125°C, and −55°C, per MIL-STD-883.*

*Operating ranges define those limits between which the functionality of the device is guaranteed.*

## DC CHARACTERISTICS over MILITARY operating ranges unless otherwise specified (Note 2)

| Parameter Symbol | Parameter Description | Test Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $I_{OH}$ = −2 mA $V_{IN}$ = $V_{IH}$ or $V_{IL}$, $V_{CC}$ = Min | 2.4 | | V |
| $V_{OL}$ | Output LOW Voltage | $I_{OL}$ = 12 mA $V_{IN}$ = $V_{IH}$ or $V_{IL}$, $V_{CC}$ = Min | | 0.5 | V |
| $V_{IH}$ | Input HIGH Voltage | Guaranteed Input Logical HIGH Voltage for all Inputs (Note 3) | 2.0 | | V |
| $V_{IL}$ | Input LOW Voltage | Guaranteed Input Logical LOW Voltage for all Inputs (Note 3) | | 0.8 | V |
| $V_I$ | Input Clamp Voltage | $I_{IN}$ = −18 mA, $V_{CC}$ = Min | | −1.5 | V |
| $I_{IH}$ | Input HIGH Current | $V_{IN}$ = 2.4 V, $V_{CC}$ = Max (Note 4) | | 25 | µA |
| $I_{IL}$ | Input LOW Current | $V_{IN}$ = 0.4 V, $V_{CC}$ = Max (Note 4) | | −250 | µA |
| $I_I$ | Maximum Input Current | $V_{IN}$ = 5.5 V, $V_{CC}$ = Max | | 1 | mA |
| $I_{OZH}$ | Off-State Output Leakage Current HIGH | $V_{OUT}$ = 2.4 V, $V_{CC}$ = Max, $V_{IN}$ = $V_{IH}$ or $V_{IL}$ (Note 4) | | 100 | µA |
| $I_{OZL}$ | Off-State Output Leakage Current LOW | $V_{OUT}$ = 0.4 V, $V_{CC}$ = Max, $V_{IN}$ = $V_{IH}$ or $V_{IL}$ (Note 4) | | −100 | µA |
| $I_{SC}$ | Output Short-Circuit Current | $V_{OUT}$ = 0.5 V, $V_{CC}$ = Max (Note 5) | −30 | −130 | mA |
| $I_{CC}$ | Supply Current | $V_{IN}$ = 0 V, Outputs Open ($I_{OUT}$ = 0 mA), $V_{CC}$ = Max | | 180 | mA |

***Notes:***

*2. For APL Products, Group A, Subgroups 1, 2, and 3 are tested per MIL-STD-883, Method 5005, unless otherwise noted.*

*3. $V_{IL}$ and $V_{IH}$ are input conditions of output tests and are not themselves directly tested. $V_{IL}$ and $V_{IH}$ are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.*

*4. I/O pin leakage is the worst case of $I_{IL}$ and $I_{OZL}$ (or $I_{IH}$ and $I_{OZH}$).*

*5. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. $V_{OUT}$ = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

## CAPACITANCE (Note 1)

| Parameter Symbol | Parameter Description | Test Conditions | | Typ | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 2.0 V | $V_{CC}$ = 5.0 V, $T_A$ = 25°C, f = 1 MHz | 7 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = 2.0 V | | 7 | |

***Note:***

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

## SWITCHING CHARACTERISTICS over MILITARY operating ranges (Note 2)

| Parameter Symbol | Parameter Description | | | | Min | Max | Unit |
|---|---|---|---|---|---|---|---|
| $t_{PD}$ | Input or Feedback to Combinatorial Output | | | 16L8, 16R6, 16R4 | | 30 | ns |
| $t_S$ | Setup Time from Input or Feedback to Clock | | | 16L8, 16R6, 16R4 | 30 | | ns |
| $t_H$ | Hold Time | | | | 0 | | ns |
| $t_{CO}$ | Clock to Output or Feedback | | | | | 20 | ns |
| $t_{WL}$ | Clock Width | LOW | | | 20 | | ns |
| $t_{WH}$ | | HIGH | | | 20 | | ns |
| $f_{MAX}$ | Maximum Frequency (Note 3) | External Feedback | $1/(t_S + t_{CO})$ | | 20 | | MHz |
| | | No Feedback | $1/(t_{WH} + t_{WL})$ | | 25 | | MHz |
| $t_{PZX}$ | $\overline{OE}$ to Output Enable (Note 4) | | | | | 25 | ns |
| $t_{PXZ}$ | $\overline{OE}$ to Output Disable (Note 4) | | | | | 25 | ns |
| $t_{EA}$ | Input to Output Enable Using Product Term Control (Note 4) | | | 16L8, 16R6, 16R4 | | 30 | ns |
| $t_{ER}$ | Input to Output Disable Using Product Term Control (Note 4) | | | | | 30 | ns |

***Notes:***

2. *See Switching Test Circuit for test conditions. For APL products Group A, Subgroups 9, 10, and 11 are tested per MIL-STD-883, Method 5005, unless otherwise noted.*
3. *These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.*
4. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.*

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage with Respect to Ground ..... −0.5 V to + 7.0 V

DC Input Voltage ..... −1.5 V to + 5.5 V

DC Output or I/O Pin Voltage ..... 5.5 V

*Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ. Absolute Maximum Ratings are for system design reference; parameters given are not tested.*

## OPERATING RANGES

**Military (M) Devices (Note 1)**

Ambient Temperature ($T_A$) Operating in Free Air ..... −55°C Min

Operating Case ($T_C$) Temperature ..... 125°C Max

Supply Voltage ($V_{CC}$) with Respect to Ground ..... +4.50 V to +5.50 V

***Note:***

*1. Military products are tested at $T_C$ = +25°C, +125°C, and −55°C, per MIL-STD-883.*

*Operating ranges define those limits between which the functionality of the device is guaranteed.*

## DC CHARACTERISTICS over MILITARY operating ranges unless otherwise specified (Note 2)

| Parameter Symbol | Parameter Description | Test Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $I_{OH}$ = −1 mA $V_{IN}$ = $V_{IH}$ or $V_{IL}$ $V_{CC}$ = Min | 2.4 | | V |
| $V_{OL}$ | Output LOW Voltage | $I_{OL}$ = 4 mA $V_{IN}$ = $V_{IH}$ or $V_{IL}$ $V_{CC}$ = Min | | 0.5 | V |
| $V_{IH}$ | Input HIGH Voltage | Guaranteed Input Logical HIGH Voltage for all Inputs (Note 3) | 2.0 | | V |
| $V_{IL}$ | Input LOW Voltage | Guaranteed Input Logical LOW Voltage for all Inputs (Note 3) | | 0.8 | V |
| $V_I$ | Input Clamp Voltage | $I_{IN}$ = −18 mA, $V_{CC}$ = Min | | −1.5 | V |
| $I_{IH}$ | Input HIGH Current | $V_{IN}$ = 2.4 V, $V_{CC}$ = Max (Note 4) | | 25 | µA |
| $I_{IL}$ | Input LOW Current | $V_{IN}$ = 0.4 V, $V_{CC}$ = Max (Note 4) | | −250 | µA |
| $I_I$ | Maximum Input Current | $V_{IN}$ = 5.5 V, $V_{CC}$ = Max | | 1 | mA |
| $I_{OZH}$ | Off-State Output Leakage Current HIGH | $V_{OUT}$ = 2.4 V, $V_{CC}$ = Max $V_{IN}$ = $V_{IH}$ or $V_{IL}$ (Note 4) | | 100 | µA |
| $I_{OZL}$ | Off-State Output Leakage Current LOW | $V_{OUT}$ = 0.4 V, $V_{CC}$ = Max $V_{IN}$ = $V_{IH}$ or $V_{IL}$ (Note 4) | | −100 | µA |
| $I_{SC}$ | Output Short-Circuit Current | $V_{OUT}$ = 0.5 V, $V_{CC}$ = Max (Note 5) | −30 | −250 | mA |
| $I_{CC}$ | Supply Current | $V_{IN}$ = 0 V, Outputs Open ($I_{OUT}$ = 0 mA) $V_{CC}$ = Max | | 55 | mA |

***Notes:***

*2. For APL Products, Group A, Subgroups 1, 2, and 3 are tested per MIL-STD-883, Method 5005, unless otherwise noted.*

*3. $V_{IL}$ and $V_{IH}$ are input conditions of output tests and are not themselves directly tested. $V_{IL}$ and $V_{IH}$ are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.*

*4. I/O pin leakage is the worst case of $I_{IL}$ and $I_{OZL}$ (or $I_{IH}$ and $I_{OZH}$).*

*5. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. $V_{OUT}$ = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

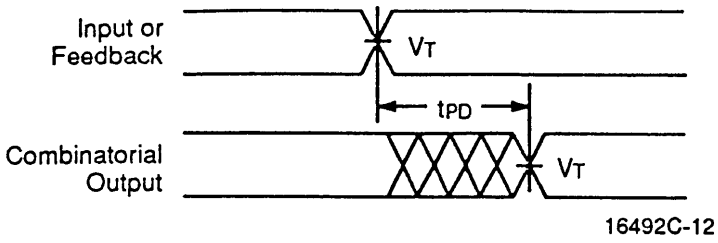
## SWITCHING CHARACTERISTICS over MILITARY operating ranges (Note 1)

| Parameter Symbol | Parameter Description | | | | Min | Max | Unit |
|---|---|---|---|---|---|---|---|
| $t_{PD}$ | Input or Feedback to Combinatorial Output | | | 16L8, 16R6, 16R4 | | 50 | ns |
| $t_S$ | Setup Time from Input or Feedback to Clock | | | 16L8, 16R6, 16R4 | 50 | | ns |
| $t_H$ | Hold Time | | | | 0 | | ns |
| $t_{CO}$ | Clock to Output or Feedback | | | | | 25 | ns |
| $t_{WL}$ | Clock Width | LOW | | | 25 | | ns |
| $t_{WH}$ | | HIGH | | | 25 | | ns |
| $f_{MAX}$ | Maximum Frequency (Note 2) | External Feedback | $1/(t_S + t_{CO})$ | | 13.3 | | MHz |
| | | No Feedback | $1/(t_{WH} + t_{WL})$ | | 20 | | MHz |
| $t_{PZX}$ | $\overline{OE}$ to Output Enable (Note 3) | | | | | 25 | ns |
| $t_{PXZ}$ | $\overline{OE}$ to Output Disable (Note 3) | | | | | 25 | ns |
| $t_{EA}$ | Input to Output Enable Using Product Term Control (Note 3) | | | 16L8, 16R6, 16R4 | | 45 | ns |
| $t_{ER}$ | Input to Output Disable Using Product Term Control (Note 3) | | | | | 45 | ns |

***Notes:***

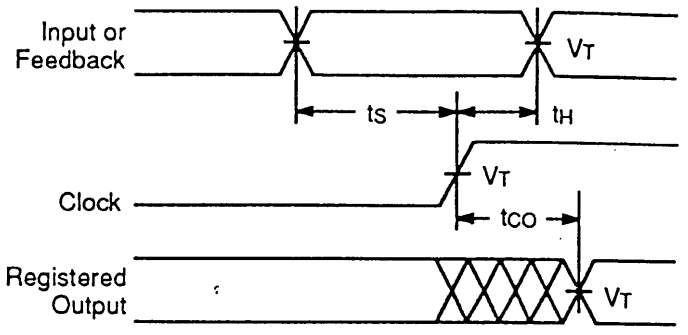
1. *See Switching Test Circuit for test conditions. For APL products Group A, Subgroups 9, 10, and 11 are tested per MIL-STD-883, Method 5005, unless otherwise noted.*
2. *These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.*
3. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.*

## SWITCHING WAVEFORMS



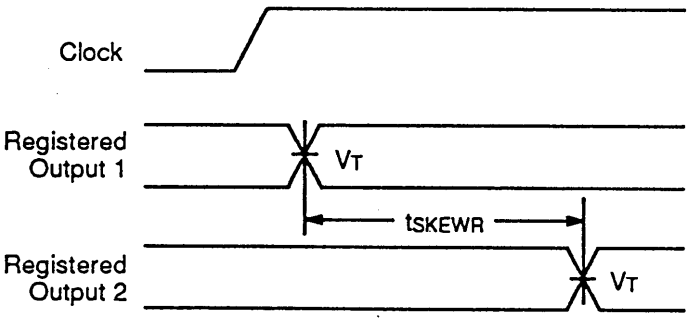

16492C-12

**Combinatorial Output**



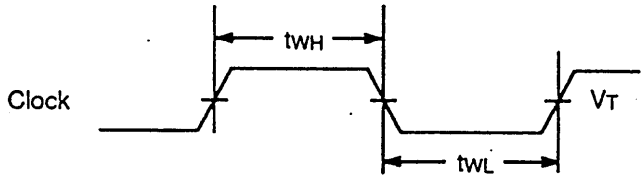

16492C-13

**Registered Output**



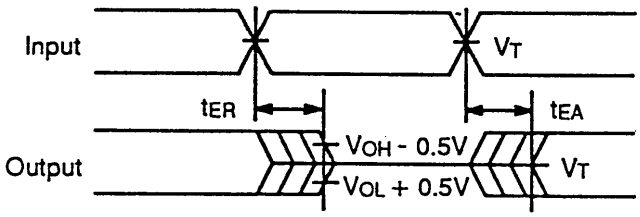

16492C-14

**Registered Output Skew**



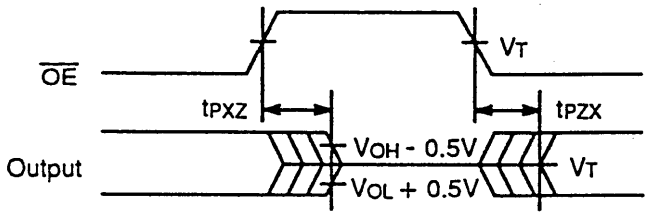

16492C-15

**Clock Width**




16492C-16

**Input to Output Disable/Enable**




16492C-17

**$\overline{OE}$ to Output Disable/Enable**

***Notes:***

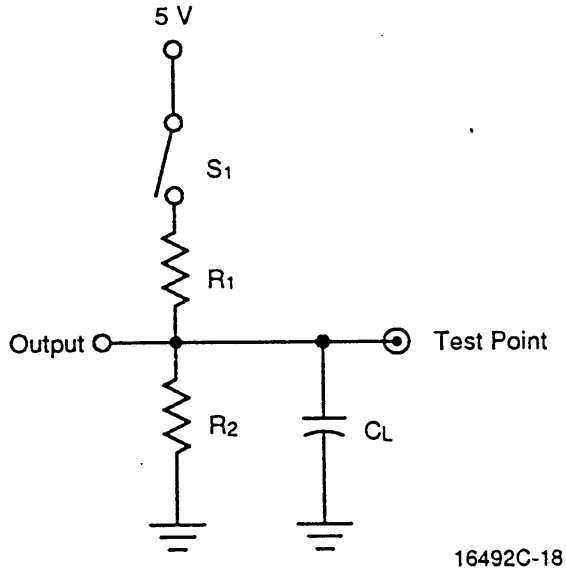
1. *$V_T$ = 1.5 V*
2. *Input pulse amplitude 0 V to 3.0 V*
3. *Input rise and fall times 2 ns–3 ns typical.*

## KEY TO SWITCHING WAVEFORMS

| WAVEFORM | INPUTS | OUTPUTS |
|---|---|---|
| ——— | Must be Steady | Will be Steady |
| ——— | | |
| ⟋⟋⟋ | May Change from H to L | Will be Changing from H to L |
| ⟋⟋⟋ | May Change from L to H | Will be Changing from L to H |
| ⟋⟍⟋⟍ | Don't Care, Any Change Permitted | Changing, State Unknown |
| ⟋⟍ ⟋⟍ | Does Not Apply | Center Line is High-Impedance "Off" State |

KS000010-PAL

## SWITCHING TEST CIRCUIT

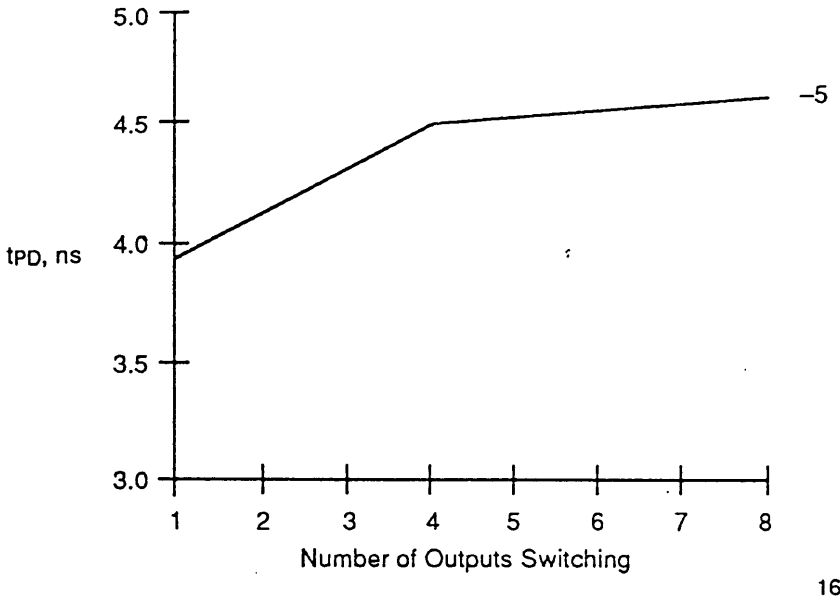



16492C-18

| Specification | $S_1$ | $C_L$ | Commercial | | Military | | Measured Output Value |
|---|---|---|---|---|---|---|---|
| | | | $R_1$ | $R_2$ | $R_1$ | $R_2$ | |
| $t_{PD}$, $t_{CO}$ | Closed | 50 pF | All but B-4: 200 Ω | All but B-4: 390 Ω | All but B-4: 390 Ω | All but B-4: 750 Ω | 1.5 V |
| $t_{PZX}$, $t_{EA}$ | Z → H: Open<br>Z → L: Closed | | | | | | |
| $t_{PXZ}$, $t_{ER}$ | H → Z: Open<br>L → Z: Closed | 5 pF | B-4: 800 Ω | B-4: 1.56 kΩ | B-4: 800 Ω | B-4: 1.56 kΩ | H → Z: $V_{OH}$ – 0.5 V<br>L → Z: $V_{OL}$ + 0.5 V |

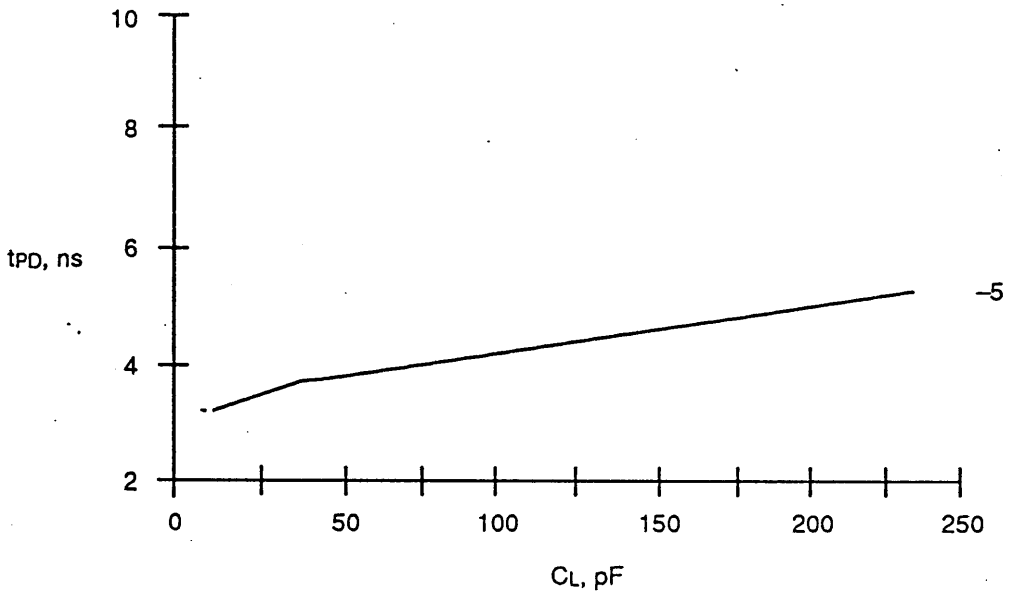
## MEASURED SWITCHING CHARACTERISTICS for the PAL16R8-5

$V_{CC}$ = 4.75 V, $T_A$ = 75°C (Note 1)




16492C-19

**$t_{PD}$ vs. Number of Outputs Switching**




16492C-20

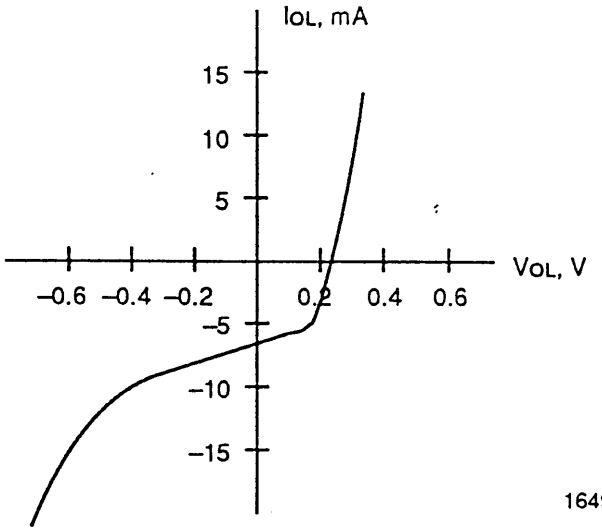
**$t_{PD}$ vs. Load Capacitance**
**$V_{CC}$ = 5.25 V, $T_A$ = 25°C**

***Note:***

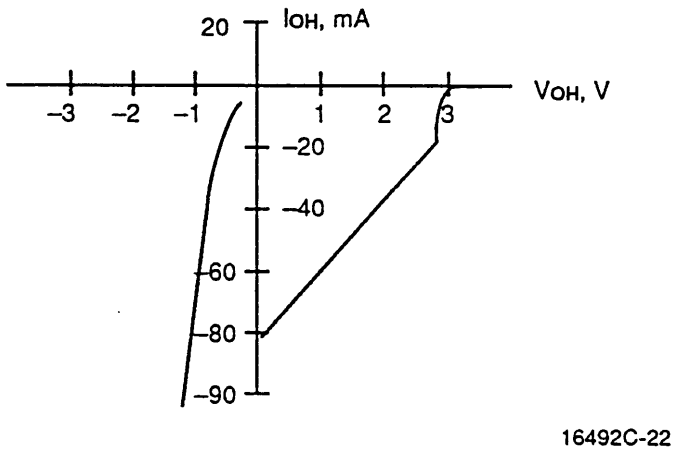
1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where $t_{PD}$ may be affected.*

## CURRENT VS. VOLTAGE (I-V) CHARACTERISTICS for the PAL16R8-4/5

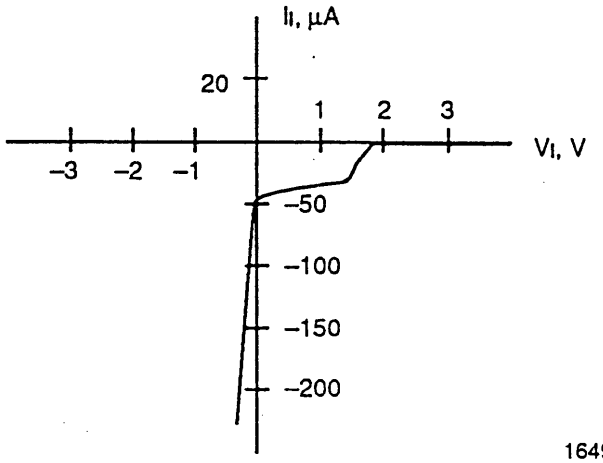
$V_{CC}$ = 5.0 V, $T_A$ = 25°C




**Output, LOW**



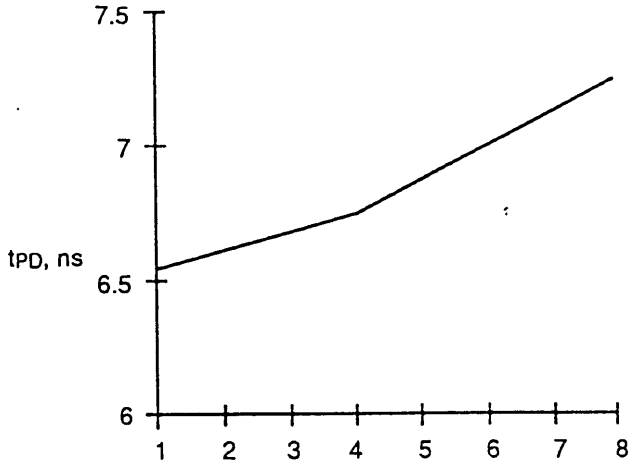

**Output, HIGH**




**Input**

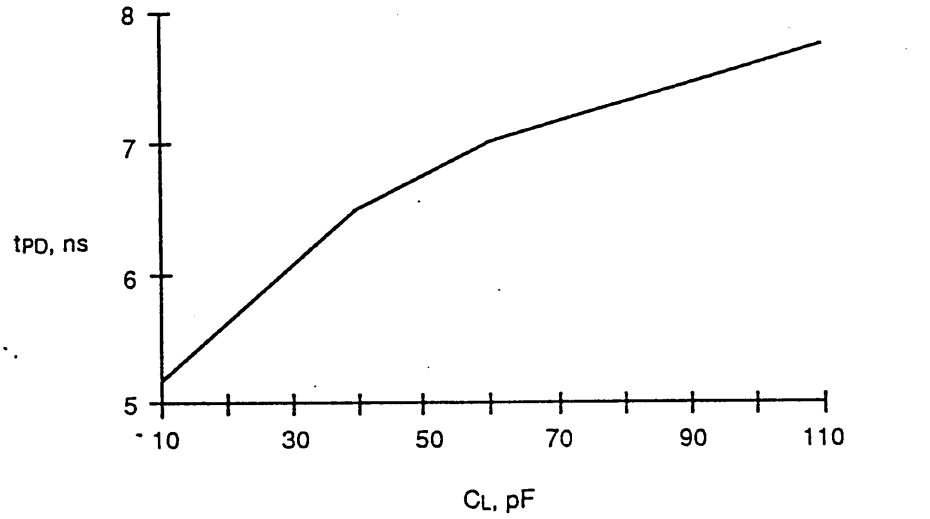
## MEASURED SWITCHING CHARACTERISTICS for the PAL16R8-7

$V_{CC}$ = 4.75 V, $T_A$ = 75°C (Note 1)




16492C-24

**$t_{PD}$ vs. Number of Outputs Switching**




16492C-25

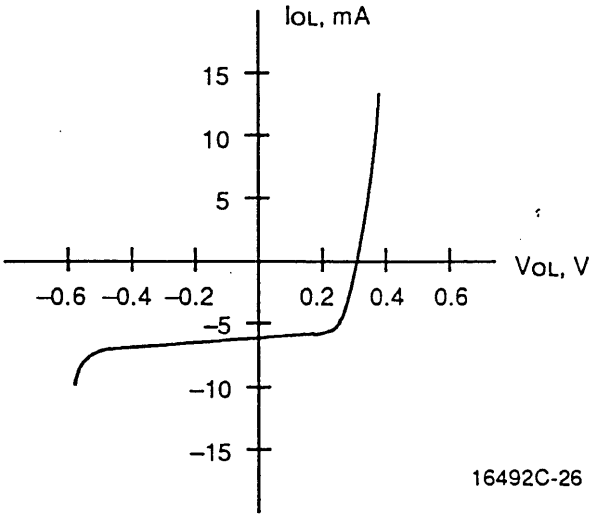
**$t_{PD}$ vs. Load Capacitance**

***Note:***

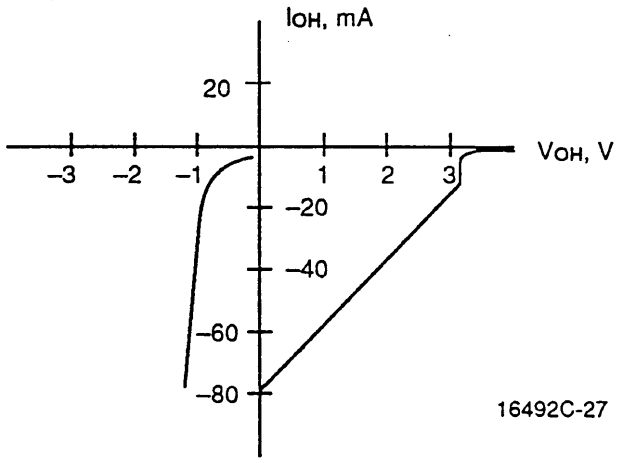
1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where $t_{PD}$ may be affected.*

## CURRENT VS. VOLTAGE (I-V) CHARACTERISTICS for the PAL16R8-7

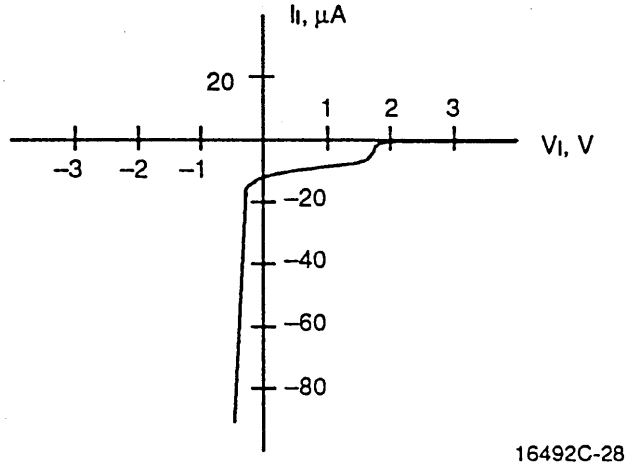
$V_{CC}$ = 5.0 V, $T_A$ = 25°C




**Output, LOW**

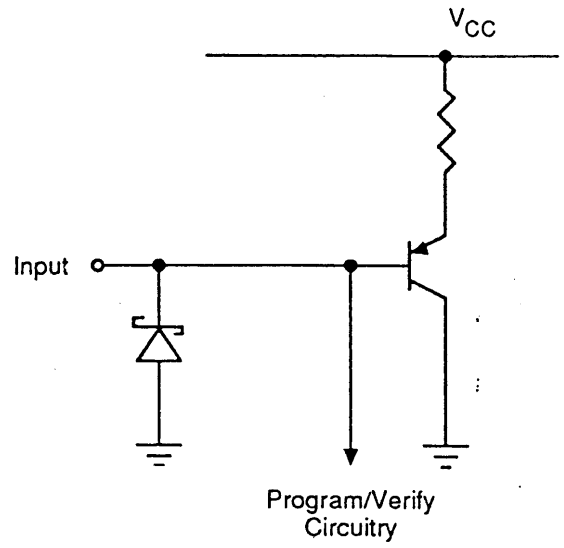



**Output, HIGH**

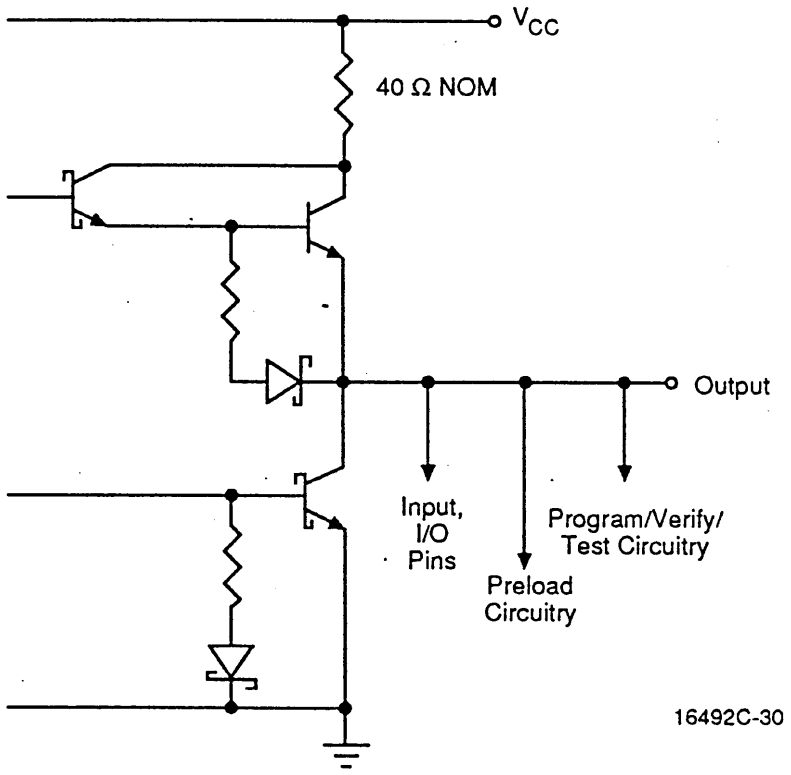



**Input**

## TPUT EQUIVALENT SCHEMATICS




**Typical Input**



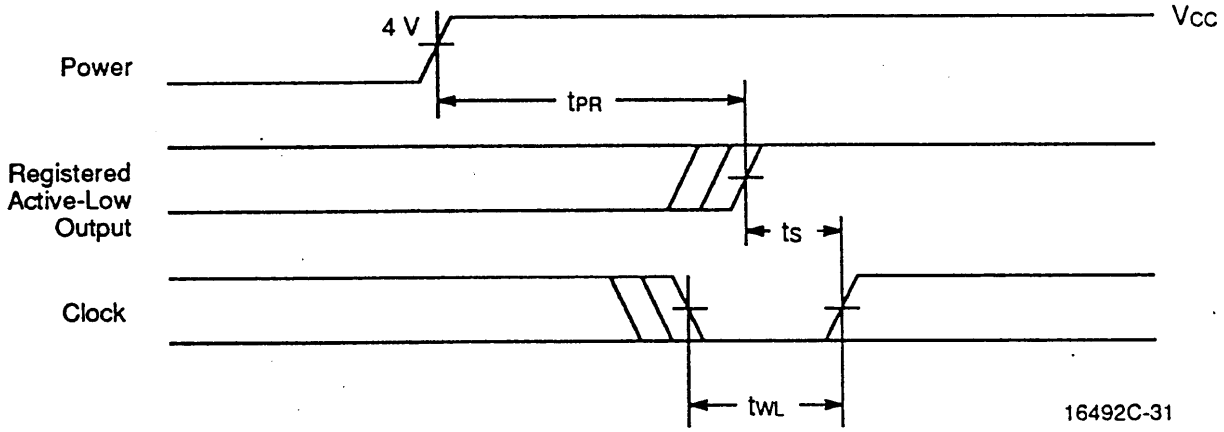

**Typical Output**

## POWER-UP RESET

The power-up reset feature ensures that all flip-flops will be reset to LOW after the device has been powered up. The output state will be HIGH due to the inverting output buffer. This feature is valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the synchronous operation of the power-up reset and the wide range of ways Vcc can rise to its steady state, two conditions are required to ensure a valid power-up reset. These conditions are:

- The Vcc rise must be monotonic.
- Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

| Parameter Symbol | Parameter Description | Max | Unit |
|---|---|---|---|
| $t_{PR}$ | Power-Up Reset Time | 1000 | ns |
| $t_S$ | Input or Feedback Setup Time | See Switching Characteristics | |
| $t_{WL}$ | Clock Width LOW | | |




**Power-Up Reset Waveform**