Octal transceiver with dual enable, non-inverting (3-State) 54ABT623

FEATURES

- Octal bidirectional bus interface
- 3-State buffers
- Output capability: +48mA/-24mA
- Latch-up protection exceeds 500mA per JEDEC JC40.2 Std 17
- ESD protection exceeds 2000V per MIL STD 883C Method 3015.6 and 200V per Machine Model

DESCRIPTION

The 54ABT623 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 54ABT573 device is an octal transceiver featuring non-inverting 3-State bus compatible outputs in both send and receive directions. The 54ABT623 is designed for asynchronous two-way communication between data busses.

The control function implementation allows for maximum flexibility in timing. This device allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the logic levels at the Enable inputs ($\overline{OEBA}$ and OEAB). The Enable inputs can be used to disable the device so that the busses are effectively isolated. The dual-enable configuration gives the 54ABT623 the capability to store data by simultaneously enabling $\overline{OEBA}$ and OEAB. Each output reinforces its input in this transceiver configuration. Thus when both control inputs are enabled and all other data sources to the two sets of bus lines are at high impedance, both sets of bus liens (16 in all) will remain at their last states.

ORDERING INFORMATION

DESCRIPTION	ORDER CODE	PACKAGE DESIGNATOR*
20-Pin Ceramic DIP	54ABT623/BRA	GDIP1-T20
20-Pin Ceramic LLCC	54ABT623/B2A	CQCC2-N20

* MIL-STD 1835 or Appendix A of 1995 Military Data Handbook

FUNCTION TABLE

INPUTS		INPUTS/OUTPUTS	
$\overline{OEBA}$	OEAB	An	Bn
L	L	A = B	Inputs
H	H	Inputs	B = A
H	L	Z	Z
L	H	A = B	B = A

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	OEAB	Output enable input
2, 3, 4, 5 6, 7, 8, 9	A0 - A7	Data inputs/outputs (A side)
18, 17, 16, 15, 14, 13, 12, 11	B0 - B7	Data inputs/outputs (B side)
19	$\overline{OEBA}$	Output Enable input
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

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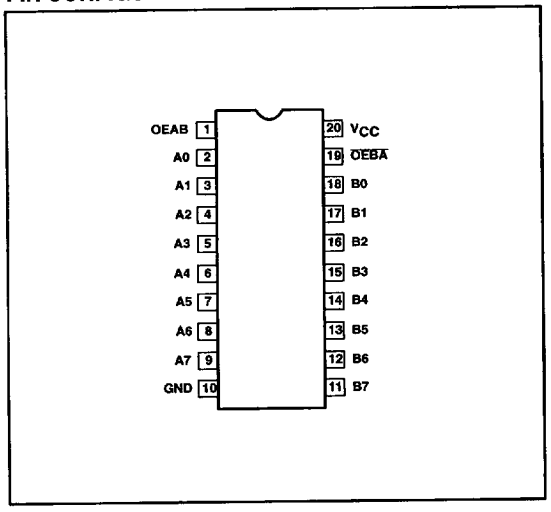
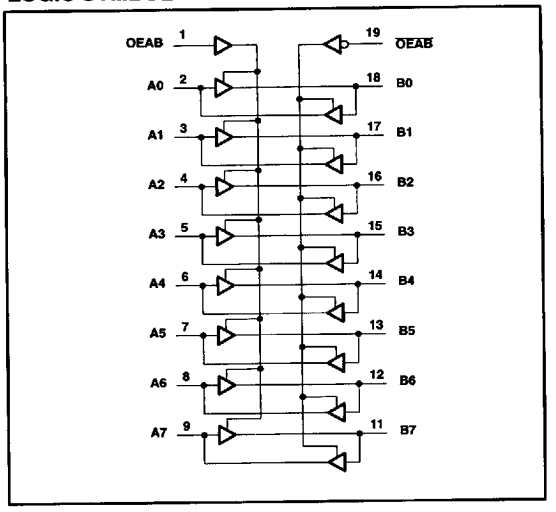
54ABT623

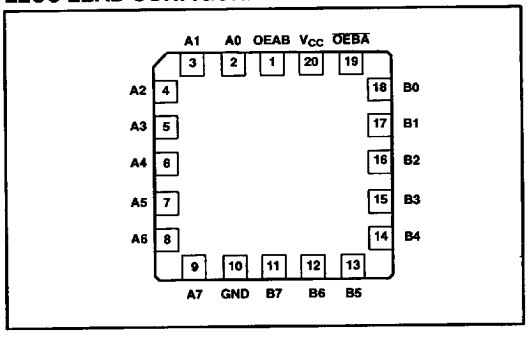
PIN CONFIGURATION



LOGIC SYMBOL



LLCC LEAD CONFIGURATION



ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage range		-0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	-18	mA
V_I	DC input voltage range[3]		-1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_O	DC output voltage range[3]	Output in Off or High state	-0.5 to +5.5	V
I_{OUT}	DC output current	Output in Low state	96	mA
T_{STG}	Storage temperature range		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level input voltage		0.8	V
I_{OH}	High-level output current		-24	mA
I_{OL}	Low-level output current		48	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	-55	+125	°C

DC ELECTRICAL CHARACTERISTICS

Unless otherwise stated; V_{CC} = MAX, $V_I = V_{IL}$ or V_{IH}, t_{amb} = -55°C to +125°C.

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS		UNIT
				T_{amb} = -55 to +125°C		
				MIN	MAX	
V_{IK}	Input clamp voltage		V_{CC} = 4.5V, I_{IK} = -18mA		-1.2	V
V_{OH}	High-level output to voltage		V_{CC} = 4.5V; I_{OH} = -3mA	2.5		V
			V_{CC} = 4.5V; I_{OH} = -24mA	2.0		V
V_{OL}	Low-level output voltage		V_{CC} = 4.5V; I_{OL} = 48mA		0.55	V
I_I	Input leakage current	Control pins	V_I = GND or V_{CC}		±1.0	µA
		Data pins[6]	V_I = GND or V_{CC}		±100	
$I_{IH} + I_{OZH}$	3-State output High current		V_O = 2.7V, $V_I = V_{IL}$ or 3.0V		50	µA
$I_{IL} + I_{OZL}$	3-State output Low current		V_O = 0.5V, $V_I = V_{IL}$ or 3.0V		-50	µA
I_O	Short-circuit output current[4]		V_O = 2.5V, V_I = GND or V_{CC}	-50	-180	mA
I_{CCH}	Quiescent supply current		Outputs High, V_I = GND or V_{CC}		250	µA
I_{CCL}			Outputs Low, V_I = GND or V_{CC}		30	mA
I_{CCZ}			Outputs 3-State, V_I = GND or V_{CC}		250	µA
ΔI_{CC}	Additional supply current per input pin[5]		Outputs enabled, one input at 3.4V, other inputs at V_{CC} or GND		1.5	mA
			Outputs 3-State, one input at 3.4V, other inputs at V_{CC} or GND		50	µA
			Outputs 3-State, one enable input at 3.4V, other inputs at V_{CC} or GND		1.5	mA

AC ELECTRICAL CHARACTERISTICS

GND = 0V, $t_R = t_F = 2.5ns$, $C_L = 50pF$, $R_L = 500\Omega$

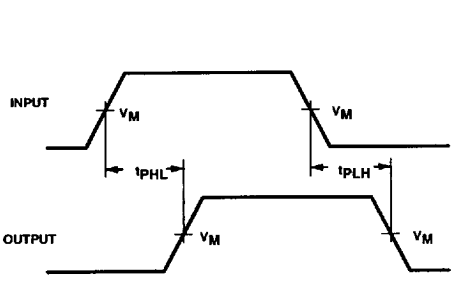
SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V			T_{amb} = -55°C to +125°C, V_{CC} = +5.0V ± 0.5%		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	Waveform 1	1.0 1.0	2.8 2.9	4.1 4.2	1.0 1.0	5.0 5.0	ns ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	Waveform 2	1.7 1.7	4.8 4.9	6.5 6.5	1.0 1.0	8.5 8.5	ns ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	Waveform 2	1.7 1.7	5.0 5.0	6.5 6.5	1.0 1.0	8.5 8.5	ns ns

NOTES:

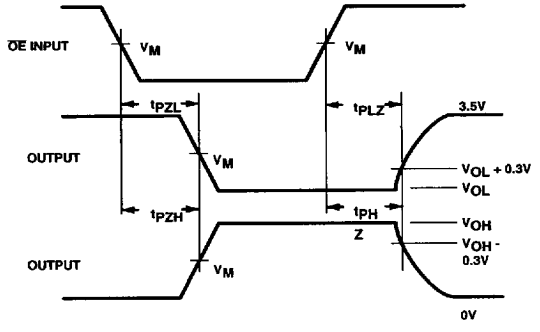
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
4. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
5. This is the increase in supply current for each input at 3.4V.
6. Input leakage on transceiver data pins also includes I_{OZH} or I_{OZL} current from the output circuitry.

AC WAVEFORMS

V_M = 1.5V, V_{IN} = GND to 3.0V

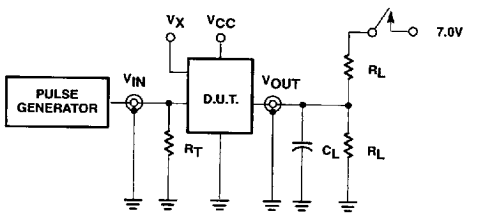


Waveform 1. Waveforms Showing the Input to Output Propagation Delays

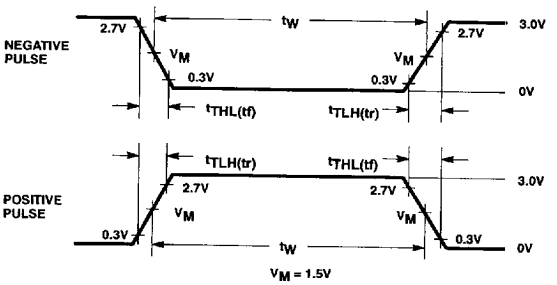


Waveform 2. Waveforms Showing the 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



Input Pulse Definitions

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	closed / open

INPUT PULSE CHARACTERISTICS				
Family	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54ABT	1MHz	500ns	≤2.5ns	≤2.5ns

DEFINITIONS:

R_L = Load Resistor; see AC Characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.