

9-bit D-type flip-flop with reset and enable (3-State)

74ABT823

FEATURES

- High speed parallel registers with positive edge-triggered D-type flip-flops
- Ideal where high speed, light loading, or increased fan-in are required with MOS microprocessors
- Output capability: +64mA/-32mA
- Latch-up protection exceeds 500mA per Jedec Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model
- Power-up 3-State
- Power-up Reset

DESCRIPTION

The 74ABT823 Bus interface Register is designed to eliminate the extra packages required to buffer existing registers and provide extra data width for wider data/address paths of buses carrying parity.

The 74ABT823 is a 9-bit wide buffered register with Clock Enable (CE) and Master Reset (MR) which are ideal for parity bus interfacing in high microprogrammed systems.

The register is fully edge-triggered. The state of each D input, one set-up time before the Low-to-High clock transition is transferred to the corresponding flip-flop's Q output.

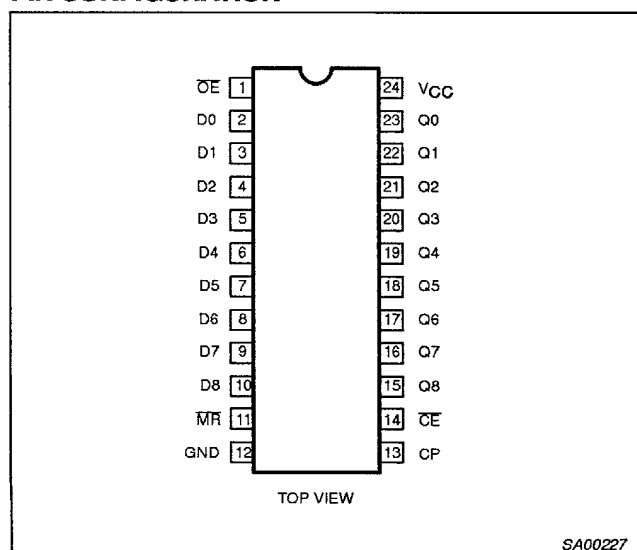
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS $T_{amb} = 25^{\circ}\text{C}$; $GND = 0V$	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay CP to Qn	$C_L = 50\text{pF}$; $V_{CC} = 5V$	4.4	ns
C_{IN}	Input capacitance	$V_I = 0V$ or V_{CC}	4	pF
C_{OUT}	Output capacitance	Outputs disabled; $V_O = 0V$ or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs disabled; $V_{CC} = 5.5V$	500	nA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
24-Pin Plastic DIP	-40°C to $+85^{\circ}\text{C}$	74ABT823 N	74ABT823 N	SOT222-1
24-Pin plastic SO	-40°C to $+85^{\circ}\text{C}$	74ABT823 D	74ABT823 D	SOT137-1
24-Pin Plastic SSOP Type II	-40°C to $+85^{\circ}\text{C}$	74ABT823 DB	74ABT823 DB	SOT340-1
24-Pin Plastic TSSOP Type I	-40°C to $+85^{\circ}\text{C}$	74ABT823 PW	74ABT823PW DH	SOT355-1

PIN CONFIGURATION



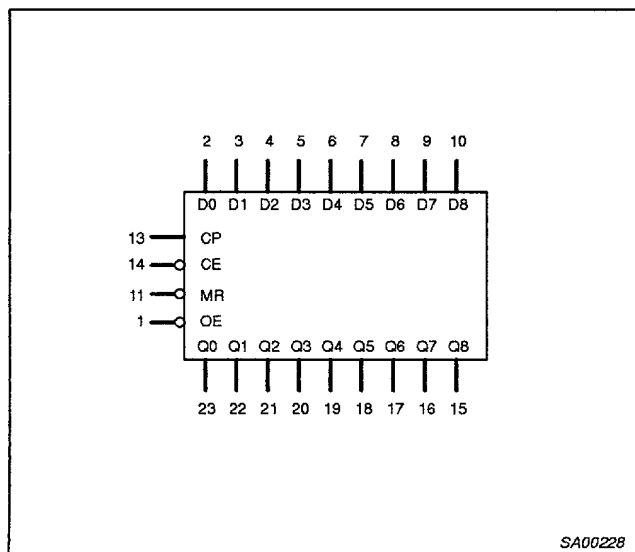
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	OE	Output enable input (active-Low)
2, 3, 4, 5, 6, 7, 8, 9, 10	D0-D8	Data inputs
23, 22, 21, 20, 19, 18, 17, 16, 15	Q0-Q8	Data outputs
13	CP	Clock pulse input (active rising edge)
14	CE	Clock enable input (active-Low)
11	MR	Master reset input (active-Low)
12	GND	Ground (0V)
24	V_{CC}	Positive supply voltage

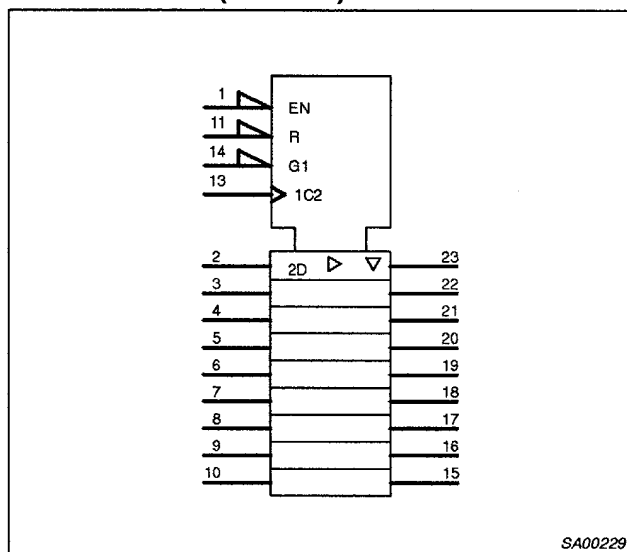
9-bit D-type flip-flop with reset and enable (3-State)

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LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



FUNCTION TABLE

INPUTS					OUTPUTS	OPERATING MODE
OE	MR	CE	CP	Dn	Q0 - Q8	
L	L	X	X	X	L	Clear
L	H	L	↑	h	H	Load and read data
L	H	L	↑	l	L	
L	H	H	↑	X	NC	Hold
H	X	X	X	X	Z	High impedance

H = High voltage level

h = High voltage level one set-up time prior to the Low-to-High clock transition

L = Low voltage level

l = Low voltage level one set-up time prior to the Low-to-High clock transition

NC = No change

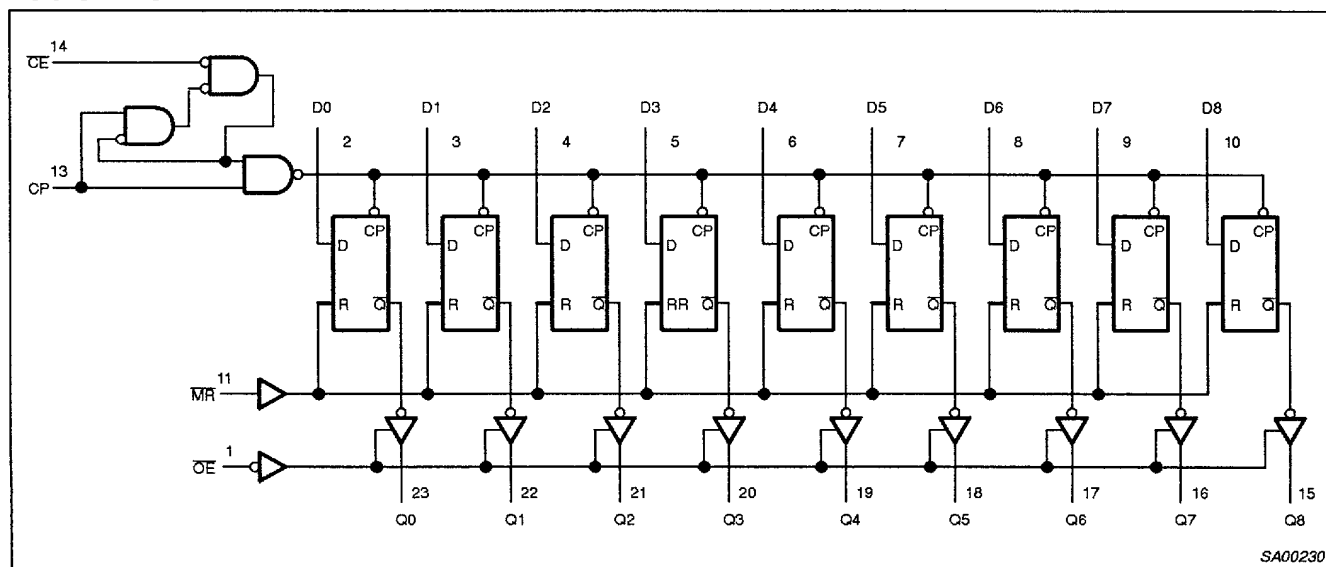
X = Don't care

Z = High impedance "off" state

↑ = Low to High clock transition

↑ = Not a Low-to-High clock transition

LOGIC DIAGRAM



9-bit D-type flip-flop with reset and enable (3-State)

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ABSOLUTE MAXIMUM RATINGS^{1, 2}

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	-18	mA
V_I	DC input voltage ³		-1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_{OUT}	DC output voltage ³	output in Off or High state	-0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		-65 to 150	°C

NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level input voltage		0.8	V
I_{OH}	High-level output current		-32	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	°C

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DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T _{amb} = +25°C			T _{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
V _{IK}	Input clamp voltage	V _{CC} = 4.5V; I _{IK} = -18mA		-0.9	-1.2		-1.2	V
V _{OH}	High-level output voltage	V _{CC} = 4.5V; I _{OH} = -3mA; V _I = V _{IL} or V _{IH}	2.5	2.9		2.5		V
		V _{CC} = 5.0V; I _{OH} = -3mA; V _I = V _{IL} or V _{IH}	3.0	3.4		3.0		V
		V _{CC} = 4.5V; I _{OH} = -32mA; V _I = V _{IL} or V _{IH}	2.0	2.4		2.0		V
V _{OL}	Low-level output voltage	V _{CC} = 4.5V; I _{OL} = 64mA; V _I = V _{IL} or V _{IH}		0.42	0.55		0.55	V
V _{RST}	Power-up output low voltage ³	V _{CC} = 5.5V; I _O = 1mA; V _I = GND or V _{CC}		0.13	0.55		0.55	V
I _I	Input leakage current	V _{CC} = 5.5V; V _I = GND or 5.5V		±0.01	±1.0		±1.0	μA
I _{OFF}	Power-off leakage current	V _{CC} = 0.0V; V _O or V _I ≤ 4.5V		±5.0	±100		±100	μA
I _{PU} /I _{PD}	Power-up/down 3-State output current ⁴	V _{CC} = 2.0V; V _O = 0.5V; V _{OE} = V _{CC} ; V _I = GND or V _{CC}		±5.0	±50		±50	μA
I _{OZH}	3-State output High current	V _{CC} = 5.5V; V _O = 2.7V; V _I = V _{IL} or V _{IH}		5.0	50		50	μA
I _{OZL}	3-State output Low current	V _{CC} = 5.5V; V _O = 0.5V; V _I = V _{IL} or V _{IH}		-5.0	-50		-50	μA
I _{CEX}	Output High leakage current	V _{CC} = 5.5V; V _O = 5.5V; V _I = GND or V _{CC}		5.0	50		50	μA
I _O	Output current ¹	V _{CC} = 5.5V; V _O = 2.5V	-50	-100	-180	-50	-180	mA
I _{CCH}	Quiescent supply current	V _{CC} = 5.5V; Outputs High, V _I = GND or V _{CC}		0.5	250		250	μA
I _{CCL}		V _{CC} = 5.5V; Outputs Low, V _I = GND or V _{CC}		27	34		34	mA
I _{CCZ}		V _{CC} = 5.5V; Outputs 3-State; V _I = GND or V _{CC}		0.5	250		250	μA
ΔI _{CC}	Additional supply current per input pin ²	V _{CC} = 5.5V; one input at 3.4V, other inputs at V _{CC} or GND		0.5	1.5		1.5	mA

NOTES:

- Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
- This is the increase in supply current for each input at 3.4V .
- For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.
- This parameter is valid for any V_{CC} between 0V and 2.1V with a transition time of up to 10msec . For $V_{CC} = 2.1\text{V}$ to $V_{CC} = 5\text{V} \pm 10\%$, a transition time of up to $100\mu\text{sec}$ is permitted.

AC CHARACTERISTICS

$\text{GND} = 0\text{V}$, $t_R = t_F = 2.5\text{ns}$, $C_L = 50\text{pF}$, $R_L = 500\Omega$

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T _{amb} = +25°C V _{CC} = +5.0V			T _{amb} = -40 to +85°C V _{CC} = +5.0V ±0.5V		
			Min	Typ	Max	Min	Max	
t _{MAX}	Maximum clock frequency	1	125	200		125		MHz
t _{PLH} t _{PHL}	Propagation delay CP to Qn	1	2.1 2.2	4.3 4.4	5.9 6.1	2.1 2.2	6.8 6.7	ns
t _{PHL}	Propagation delay MR to Qn	2	2.0	4.1	6.3	2.0	7.1	ns
t _{PZH} t _{PZL}	Output enable time to High and Low level	4 5	1.0 2.2	3.0 4.1	4.5 5.6	1.0 2.2	5.3 6.3	ns
t _{PHZ} t _{PLZ}	Output disable time from High and Low level	4 5	2.7 2.8	4.8 5.0	6.2 6.4	2.7 2.8	6.9 6.9	ns

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AC SETUP REQUIREMENTS

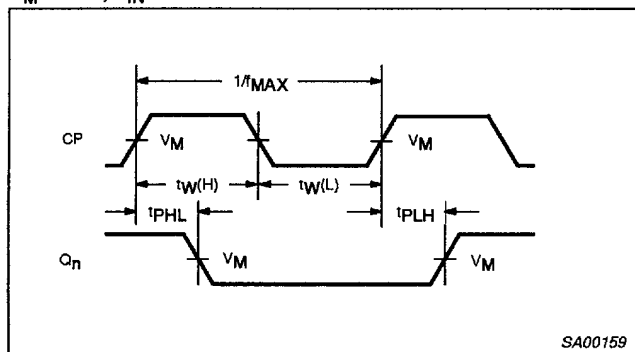
GND = 0V, $t_R = t_F = 2.5\text{ns}$, $C_L = 50\text{pF}$, $R_L = 500\Omega$

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			$T_{\text{amb}} = +25^\circ\text{C}$ $V_{\text{CC}} = +5.0\text{V}$		$T_{\text{amb}} = -40 \text{ to } +85^\circ\text{C}$ $V_{\text{CC}} = +5.0\text{V} \pm 0.5\text{V}$	
			Min	Typ	Min	
$t_s(\text{H})$ $t_s(\text{L})$	Setup time, High or Low Dn to CP	3	2.1 2.1	0.5 0.2	2.1 2.1	ns
$t_h(\text{H})$ $t_h(\text{L})$	Hold time, High or Low Dn to CP	3	1.3 1.3	0.0 -0.3	1.3 1.3	ns
$t_w(\text{H})$ $t_w(\text{L})$	CP pulse width High or Low	1	2.9 3.8	1.9 2.8	2.9 3.8	ns
$t_s(\text{H})$ $t_s(\text{L})$	Setup time, High or Low CE to CP	3	2.0 3.3	-0.5 1.5	2.0 3.3	ns
$t_h(\text{H})$ $t_h(\text{L})$	Hold time, High or Low CE to CP	3	1.0 2.0	-1.4 0.7	1.0 2.0	ns
$t_w(\text{L})$	MR pulse width, Low	2	5.5	4.0	5.5	ns
t_{rec}	Recovery time MR to CP	2	2.5	0.6	2.5	ns

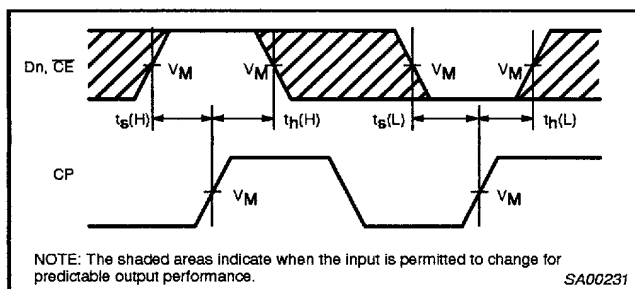
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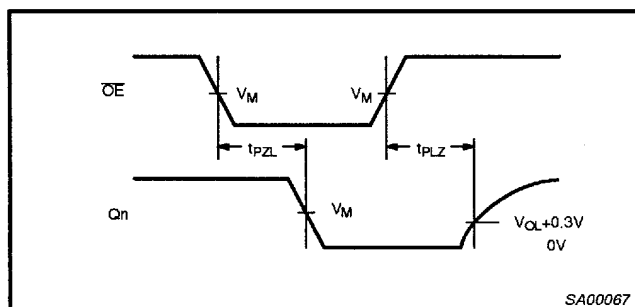
AC WAVEFORMS

 $V_M = 1.5V$, $V_{IN} = GND$ to $3.0V$ 

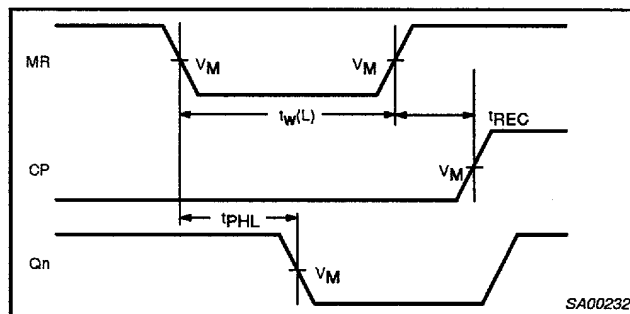
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



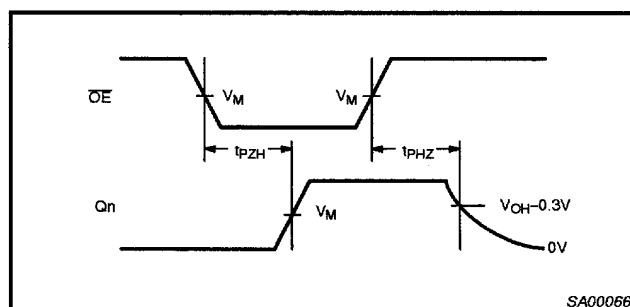
Waveform 3. Data Setup and Hold Times



Waveform 5. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level



Waveform 2. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time

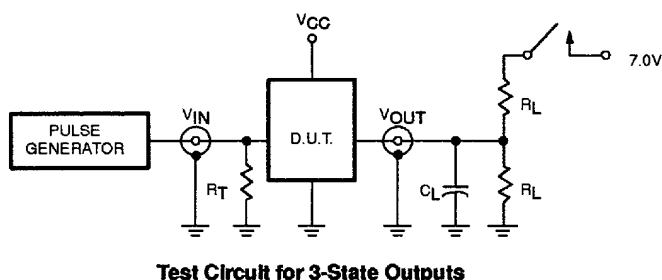


Waveform 4. 3-State Output Enable Time to High Level and Output Disable Time from High Level

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TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs

SWITCH POSITION

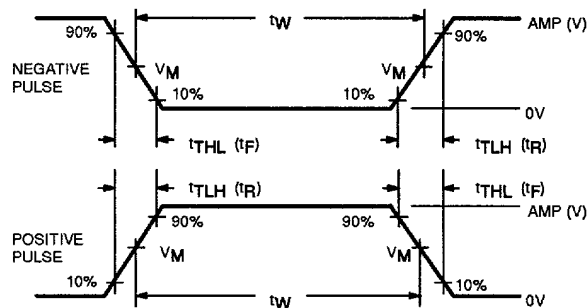
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



$$V_M = 1.5V$$

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT	3.0V	1MHz	500ns	2.5ns	2.5ns

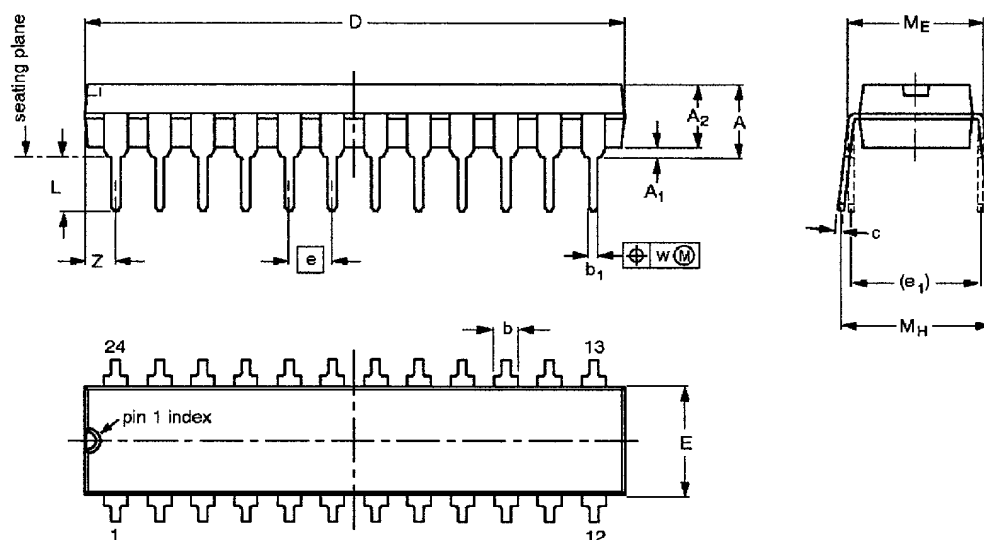
SA00012

9-bit D-type flip-flop with reset and enable (3-State)

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DIP24: plastic dual in-line package; 24 leads (300 mil)

SOT222-1

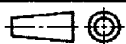


DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A max.	A ₁ min.	A ₂ max.	b	b ₁	c	D ⁽¹⁾	E ⁽¹⁾	e	e ₁	L	M _E	M _H	w	Z ⁽¹⁾ max.
mm	4.70	0.38	3.94	1.63 1.14	0.56 0.43	0.36 0.25	31.9 31.5	6.73 6.48	2.54	7.62	3.51 3.05	8.13 7.62	10.03 7.62	0.25	2.05
inches	0.185	0.015	0.155	0.064 0.045	0.022 0.017	0.014 0.010	1.256 1.240	0.265 0.255	0.100	0.300	0.138 0.120	0.32 0.30	0.395 0.300	0.01	0.081

Note

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT222-1		MS-001AF				95-03-11

74ABT823

SOT137-1



UNIT	A _{max.}	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.050	0.42 0.39	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

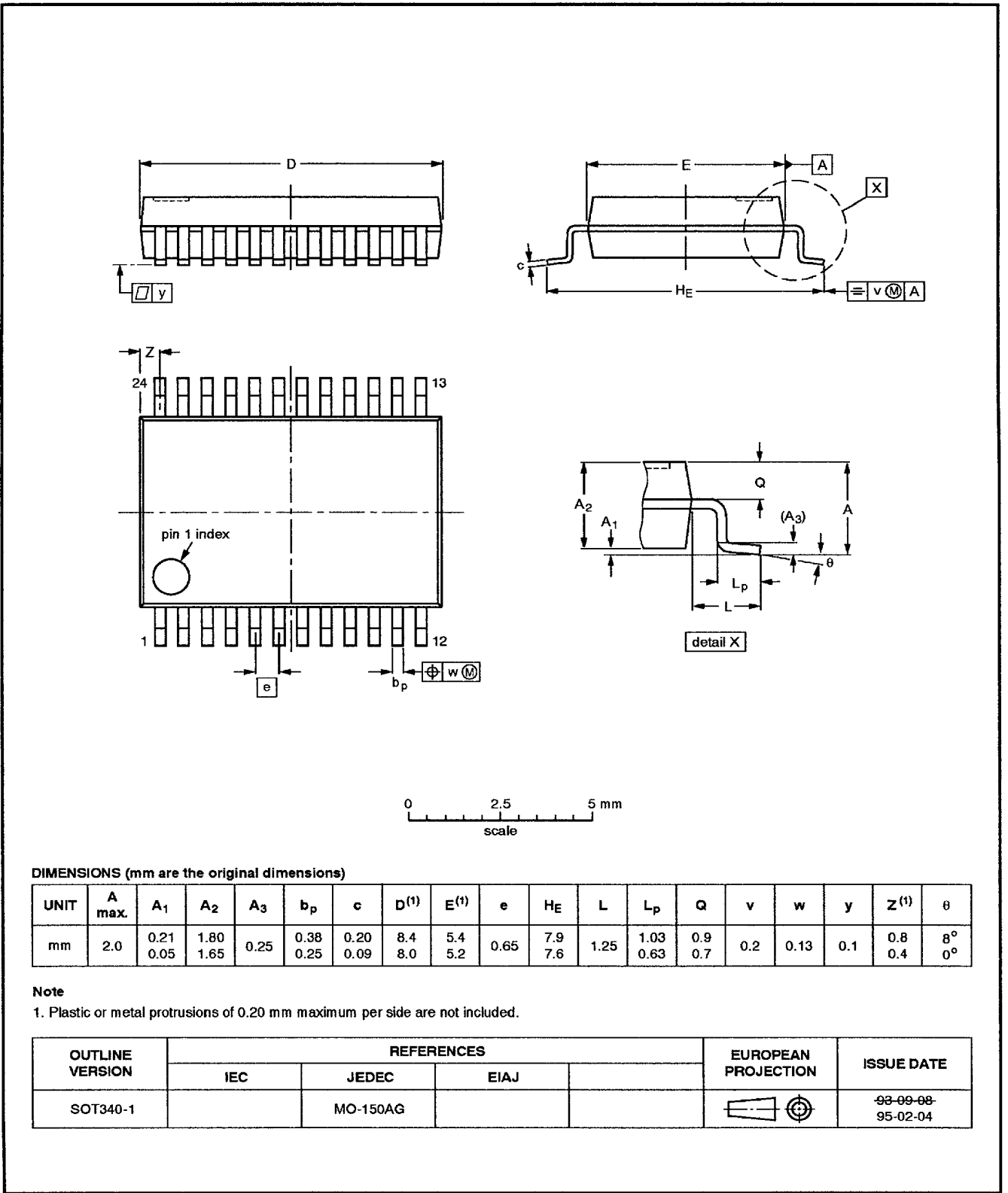
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT137-1	075E05	MS-013AD				92-11-17 95-01-24

9-bit D-type flip-flop with reset and enable
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SSOP24: plastic shrink small outline package; 24 leads; body width 5.3 mm

SOT340-1

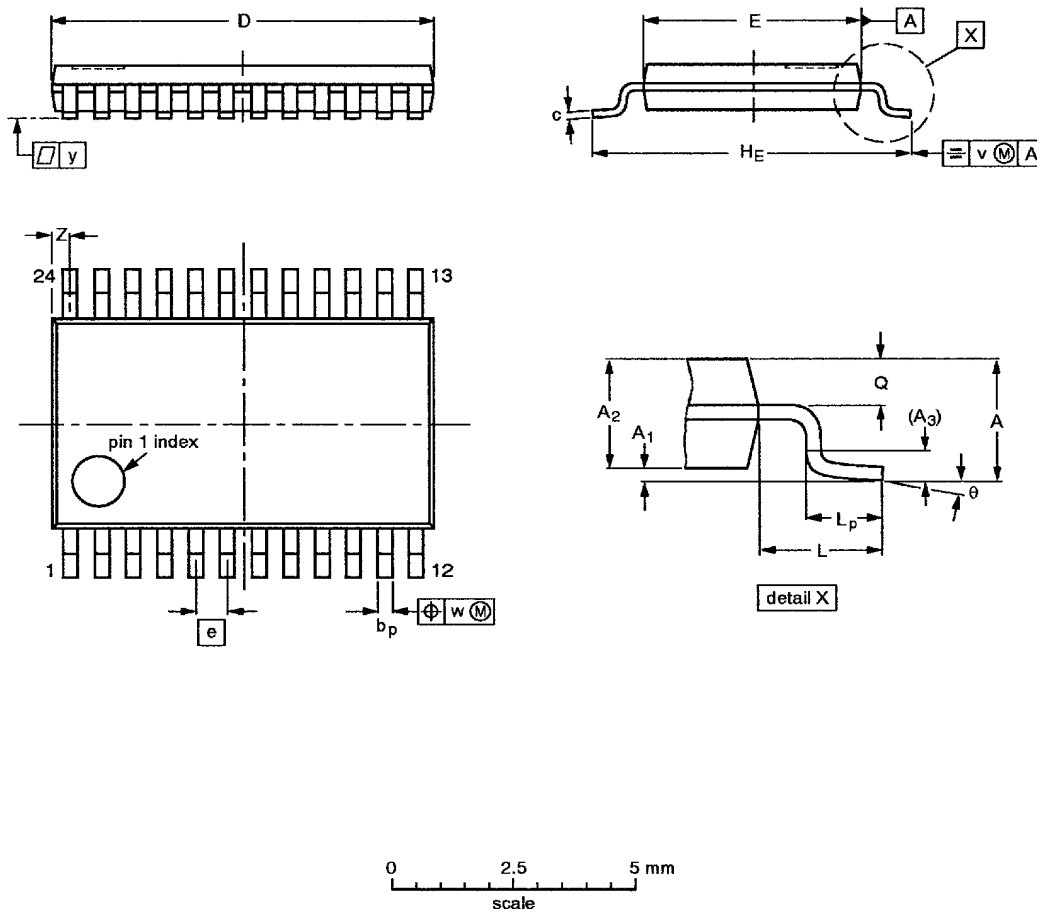


9-bit D-type flip-flop with reset and enable (3-State)

74ABT823

TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm

SOT355-1

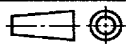


DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	z ⁽¹⁾	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	7.9 7.7	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT355-1		MO-153AD				93-06-16 95-02-04