Austria Mikro Systeme International AG

AS8401
Multipurpose control ASIC for OMNIFET

Data Sheet

Key Features

- Multipurpose control ASIC for OMNIFET (SGS Thompson intelligent power FET family)
- Contains one channel on-chip
- Applicable in low or high side switch circuits
- Supply voltage range 10V – 60V
- Up to +/- 3V potential difference between system's digital ground and power ground possible.
- Current controlled interface
- Provides load circuit surveillance and fault back signal
- Typical rise time shorter then 2.4us
- Typical fall time shorter then 3.8us
- 8 pin SOIC Package

General Description

The ASIC's purpose is to drive one OMNIFET n-channel power FET device. (OMNIFET is a trademark of SGS-THOMSON). The OMNIFET's integrated protection circuits (current limitation, over temperature protection, ...) are supplied via the OMNIFET's gate input. Thus in the OMNIFET's on-state, a DC gate current of 0.5mA is required. In a failure case (e.g. excessive temperature) an internal resistor of about 100Ω is connected between the OMNIFET's gate and source. This state is used to detect errors by the controlling ASIC.

The control ASIC's standard application is in the use as a high side or low side switch (selectable) in a 24V-supply system, where the functionality is guaranteed up to a maximum driver voltage of 55V.

In the load dump case (VTR = 60V, Pulse duration about 5ms, 5 pulses) the ASIC remains functioning (function state A) with modified parameters (rise times and fall times).
The ASIC contains one driver circuit (OMNIFET driver) and realises the following functions:

- Current controlled on switch / off switch with defined rise, fall and delay times (programmable externally at the control input), that is usable as a high side or low side switch.
- Automatic mode change between low side and high side use. This allows processing both, relatively low driver voltages (up to 25V, low side switch) and high driver voltages (up to 60V, high side switch) by detecting the present driver voltage related to OMNIFET's source potential.
- Error detection for the OMNIFET and generation of an error status signal.
- Gate to source voltage limitation for the OMNIFET to a maximum of 13V (OMNIFET protection).
- Floating ground interface between the controlling processor (control and status signal) and the driven OMNIFET; provided by separation of digital and power ground. The OMNIFET's source potential is the ASIC's ground.
- Power reduction in the off-state (Supply current falling to less than 80µA after switching the ASIC off).

The driver can be used as low or high side switch.
The control and the fault back signal are realised with current sources in order to guarantee the separation of digital ground (of the processor) and power ground (at the load circuit). This is a safety function for a broken ASIC ground line and it fulfils EMC demands.

In applications as a high side driver the OMNIFET's source is connected to the ASIC ground, which switches together with the load circuit. Changes in the ASIC's ground potential of up to 58V, and rise and fall speeds of up to 58V/µs are permitted.

Functional Description

Block diagram

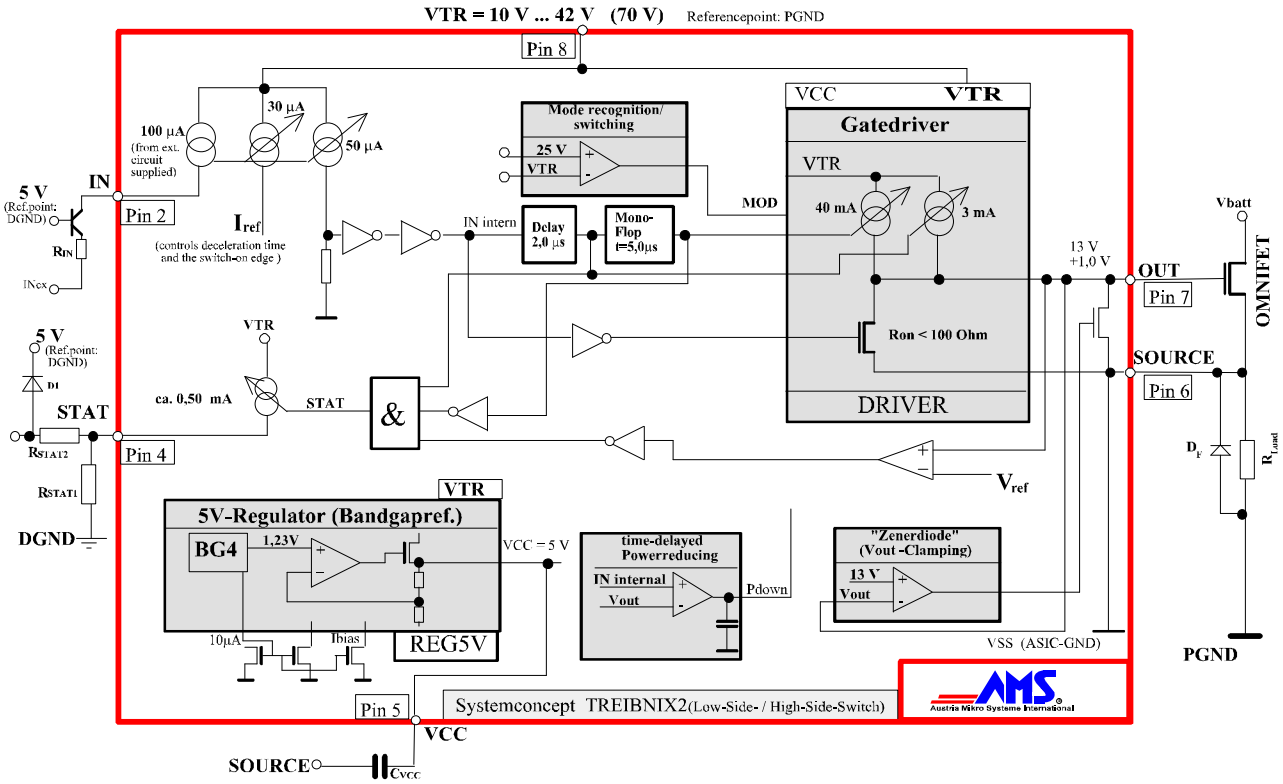

Figure 1: Block diagram of the AS8401

Description

From the functional view the chip can be divided into the following units:

A driving circuit, which implements a current-controlled switching of the OMNIFET with current pulses of approximately +30 mA, and makes the following further functions available:

- Detection of the operating condition of the OMNIFET and generation of an error status signal (Output of a current of approximately 0.5 mA in the event of an error)
- Defined delay of the switching-on-impulse of approximately 2.0µs and implementation of a delay of the switch-off-impulse of smaller than 0.5µs
- Defined (current-controlled) rise/fall times of approximately. 2.0µs/1,0µs
- Disconnection of the switching-on-impulse after approximately 5,0µs and connecting a current source of approximately 3 mA whilst the OMNIFET is switched on for the supply of the OMNIFET's protective circuits and error recognition
- Current sinking at the OMNIFET drive pin of up to 30 mA during the off state ensures a safe off status.

1. Automatic mode recognition / mode switching, which is controlled by detection of the driver voltage VTR related to the source potential:
   - Operating as a low side switch (mode1), the driver voltage is approximately 10V and the point of switching is approximately 25V.
   - When the AS8401 operates as a high side switch, during the transition of the OMNIFET to conduction, provided that the ASIC's supply voltage, VTR, remains constant, the ASIC's output current should be maintained.

2. A bandgap stabilised 5V voltage regulator, which generates the supply voltage for the digital control section and all the voltage references

3. A floating ground interface to the controlling processor (pin IN), comprised of a reference current supply and a general current supply, which implements the following functions:
   - Generation of a logic voltage signal from the ground-free input current at the pin IN
   - In on-state there are further derived currents for the production of the delay and rise/fall times of the driver from the input current at the pin IN
   - After the OMNIFET has been switched off and an additional time delay, the control ASIC enters power down mode. During power down the current consumption is 80µA or less. The time delay is necessary to ensure fast comparator operation in order to complete the power down sequence.

4. A time-delayed power down circuit for the control of the generation of supply current (see point 4)

5. Voltage delimitation which limits the voltage between gate and source of the OMNIFET to 13V ±1,0V (Protection of the OMNIFET).

The ASIC controls the OMNIFET between gate and source (in particular also when it is used in high-side-switch applications). The operating condition in which the source potential is more positive than the gate potential, not permitted for the OMNIFET, is avoided. The use of the source potential of the OMNIFET as ASIC ground for the ground free coupling between ASIC and the processor causes fast variable ASIC ground potential during the switching operation particularly when the AS8401 is used in high side switch applications.

The size of the switching-on pulses and switching-off pulses and thus the rise and fall times with given gate-source capacities of the OMNIFET can be programmed by an external resistance R_{IN}, which determines the input current at the pin IN, within certain limits. The switching time varies approximately in inverse proportion to the current I_{IN} at the pin IN. Thereby it is possible to adapt the AS8401 to the particular requirements of the OMNIFET (taking into account gate source capacitance and required delay/transition times) within certain limits (this adjustment range is not constituent of these Device Specification). This adaptability is limited by the possible range of the current at the input pin IN.

Definition of the logic signals

Symbol	Logic meaning	Level meaning		
IN	Control input for the driver, the input is current controlled, i.e.:			
	a) According to to a current from 0,1mA to DGND externally produced	I_{IN}= -0,1 mA	➲	a) appropriate driver output goes high (according to $V_{OUT} = V_{TR}$)
	b) According to no current (< 5 mA)	I_{IN} = 0	➲	b) appropriate driver output goes low (according to $V_{OUT} = V_{SOURCE}$)
STAT	Accumulated error status signal for the controlled OMNIFET, the output is current controlled, i.e.:			Error at the OMNIFET during the on-status (signal is valid after termination of the switch-on procedure)
	a) fault condition according to a current from 0,35 mA to 0.5 mA from the ASIC to DGND	I_{STAT} = -0,5mA	➲	a) an error of the OMNIFET during the on-status,
	b) normally operation according to no current	I_{STAT} = 0	➲	b) normal operation or off-status of the OMNIFET

Electrical Characteristics

Absolute Maximum Ratings (Non Operating)

SYMBOL	PARAMETER	MIN	MAX	NOTE
VTR - VPGND	DC Supply Voltage	-0.5 V	55 V	
VDL	Load Dump Voltage		60V	DIN 40839 vol. 2: 5 pulse, 500ms with Ri = 2 Ohm
I_{INmax}	Maximum Input Current	-30 mA	30 mA	$V_{IN} < V_{Inmin}$ respectively $V_{IN} >$ VTR
V_{INA}	Digital input level	VPGND - 0.3V	55V	
T_{strg}	Storage Temperature	-55 ^{o}C	150 ^{o}C	
T_{sold}	Soldering Temperature		260 ^{o}C	1)
t_{sold}	Soldering Time		10 sec	Reflow and Wave
H	Humidity	5 %	85 %	
ESD	Electrostatic Discharge	1000 V		HBM: R = 1.5 kΩ, C = 100 pF

Note:

1) 360 ^{o}C and 3s for manual soldering

Recommended Operating Conditions

The following values are valid for a temperature range from –40 to 105°C and a supply voltage range VTR from 10V to 42V. If the supply voltage VTR rises above 42V and stays below 60V (load dump case) the circuit stay fully functional with different parameters. In every case it is guaranteed, that the switch-off-delay is 600ns shorter than the switch-on-delay.

SYMBOL	PARAMETER	MIN	TYP	MAX	NOTE
Static parameters					
Driver circuit					
VTR	Driver voltage	10V		42V	1)
VCC	Chip internal 5V power supply	4.7V	5.0V	5.7V	External using not allowed
I_{VTRoff}	Leakage current to power ground (PGND) in the off state			80µA	VTR = 10V, Low side switch application, off state, I_{IN} = 0A, T = 27°C
			80µA	100µA	VTR = 34V, High side switch application, off state, I_{IN} = 0A, T = 27°C
				150µA	VTR = 42V, High side switch application, off state, I_{IN} = 0A, T = 105°C
I_{VTRon}	Current consumption in on state			3mA	VTR = 10V, on state, I_{IN} = 100µA
I_{OUToff}	Peak switch current of the driver in the switch-off phase	20mA		50mA	2)
I_{OUTon}	Peak switch current of the driver in the switch on-phase	-60mA		-30mA	3)
I_{OUTN}	Output current of the “normal-condition“ in the on-state	0.3mA		-30mA	4)
I_{OUTF}	Output current of the “fault condition“ in the on-state	2mA		4mA	
$V_{sat\ normal}$	Saturation voltage of the “normal-condition“ in the on-state			0.5V	
$V_{sat\ fault}$	Saturation voltage of the “fault-condition“ in the on-state			2V	
$V_{OUT/Source}$	Output voltage limitation between OUT and SOURCE	12V		14V	5)
Control input IN					
I_{INon}	Input current of the control signal for the on-state		-100µA		6)
I_{INoff}	Input current of the control signal for the off-state	-5µA		0	
Status output STAT					
$I_{STATonf}$	Output current of status pin of the error case (fault condition) for the on-state	-1.2mA		-0.5mA	
$I_{STATonn}$	Output current of status pin of the normal condition for the on-state	-50µA		5µA	

Recommended Operating Conditions (continued)

SYMBOL	PARAMETER	MIN	TYP	MAX	NOTE
Dynamic parameters					
T_{RISE}	Rise time			2.4µs	
T_{FALL}	Fall time			3.8µs	
T_{PDon}	Switch on delay	0.75µs		3.9µs	
T_{PDoff}	Switch off delay			4.0µs	
T_{SP}	Duration of the switch-on current pulse	4.0µs	5.0µs	7.0µs	

Note:

1) The maximum driver voltage VTR at full function it is VTR = 42V. At VTR = 60V in the load dump case all defined functions are staying valid (function state A). In this state it is possible that some times some parameters are different from the specified value, but in every time the switch off delay is shorter then the switch on delay.
2) Valid for an input current I_{IN} = 0A. This possibility of the output OUT is valid the off state.
3) Valid for an input current I_{IN} = 100µA. This possibility of the output OUT is valid the on state.
4) This is the input current of the OMNIFET in the on-state
5) This is a chip internal dynamical limitation of the output voltage.
6) Correspondent with the output current of the control circuit. The capacity on the pin IN has to be low ($C_{PIN\ extern}$ < 1 pF). The tolerance of this current controls the switch timing.

Pin-out Information

Pin Description

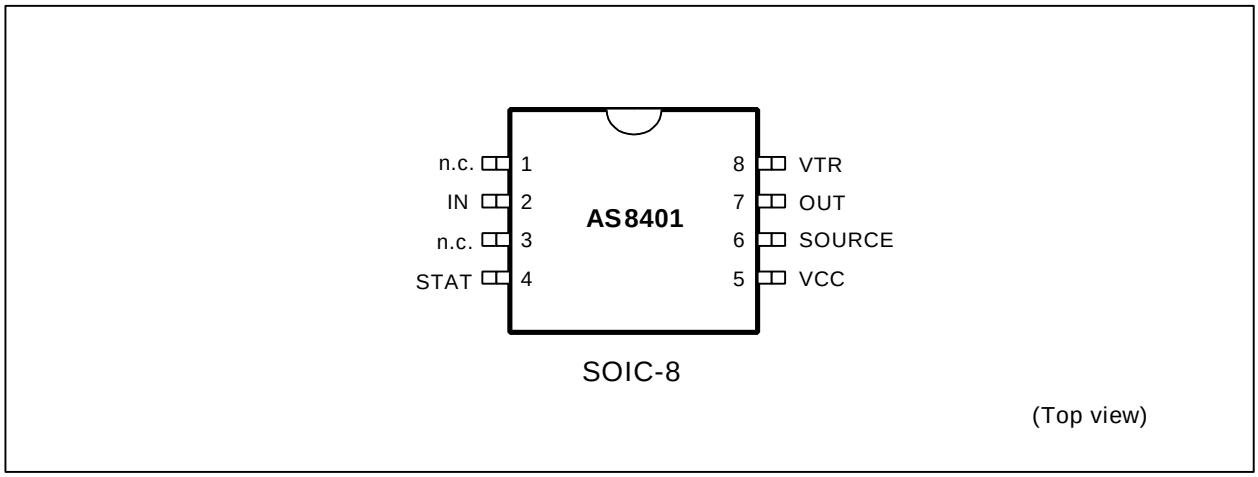

Figure 2: Pin-out AS8401

Pin list

Pin No.	Pin Name	Type	Description
1	n.c.		Not connected
2	IN	Input	Control input of the driver
3	n.c.		Not connected
4	STAT	Output	Output for state signal (error state)
5	VCC	Output	Internal supply for logic (5V)
6	SOURCE	Ground	Source of the OMNIFET and ground of the ASIC
7	OUT	Output	Driver output (gate of the OMNIFET)
8	VTR	Supply	Supply of the Driver

Application Schematic

High side switch

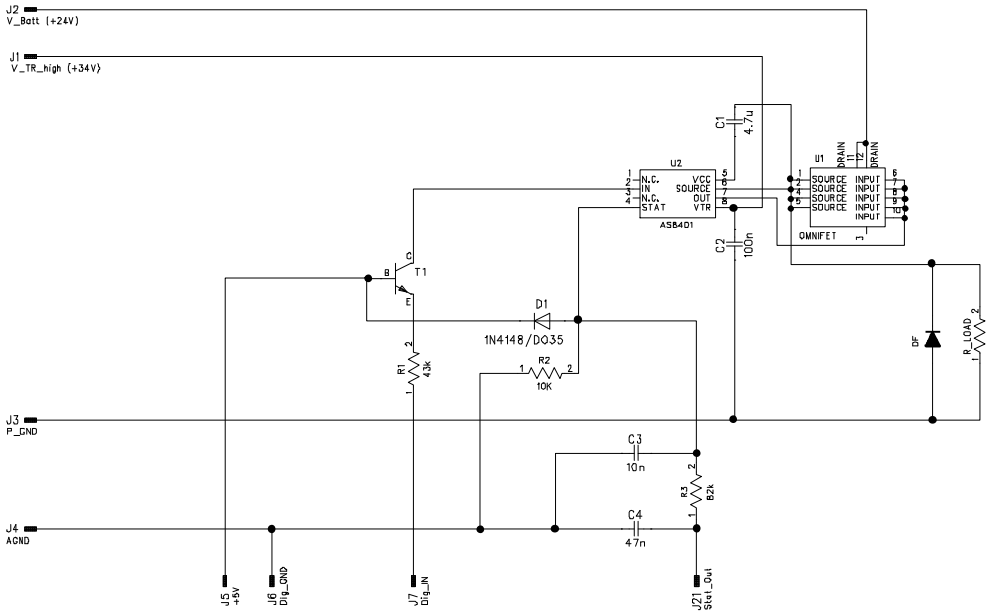

Figure 3: AS8401/OmniFet as high-side switch

Low side switch

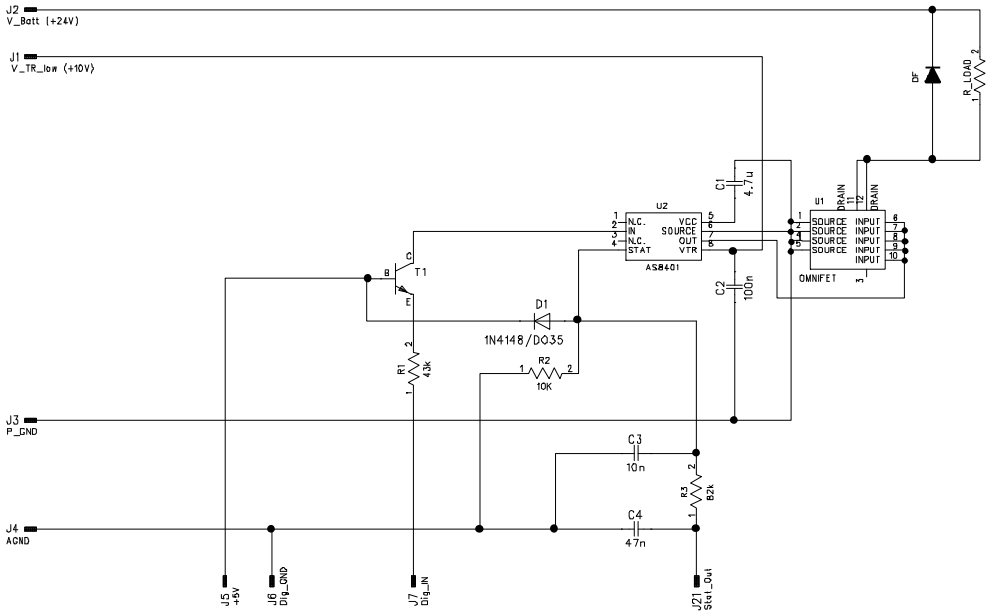

Figure 4: AS8401/OmniFet as low-side switch

Grounding concept

In Figure 3 and 4 two possible application circuits for the AS8401/OmniFet were shown. For a better understanding of this two application circuits in Figure 5 a Grounding/Supply-concept for this two circuits is shown.

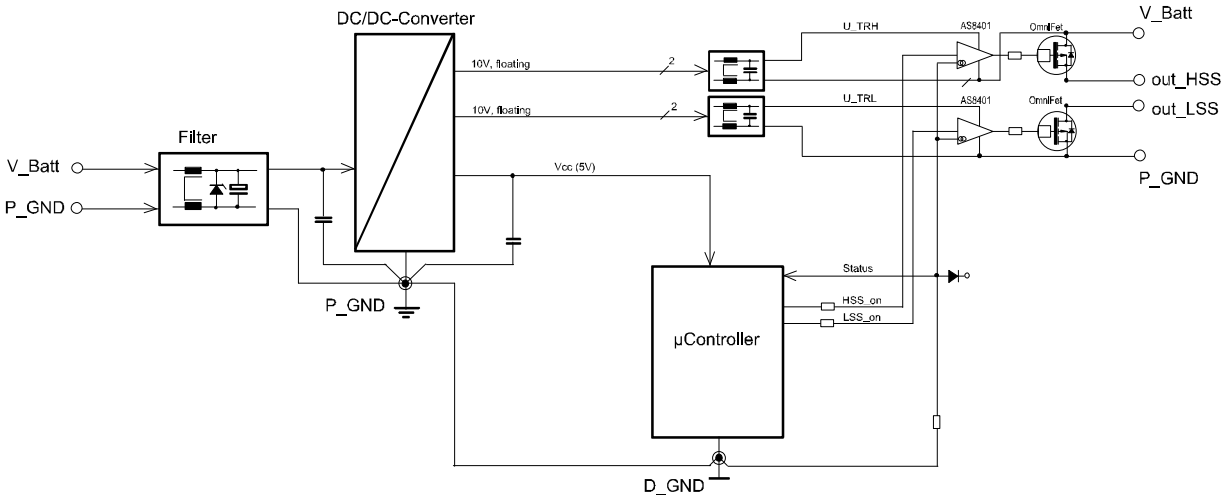

Figure 5: AS8401/OmniFet application circuits grounding/supply-concept

Package Information

Package : **SOIC 8** small outline

SOIC 8	
Marking	
AS8401	Chip number
YY	Year of Production
WW	Week of Production
XXX	Assembly-ID

SOIC 8 small outline			
(Dimensions in mm)			
	min.	nom.	max.
A	1,6	1,6	1,7
A1	0,1	0,15	0,3
A2	1,40	1,5	1,6
B	0,4	0,4	0,5
C	0,19	0,2	0,3
D	4,8	4,9	5
E	3,8	3,9	3,99
e	1,27 BSC		
H	5,8	5,99	6,2
h	0,25	0,33	0,41
L	0,41	0,64	0,9
α	0°	5°	8°

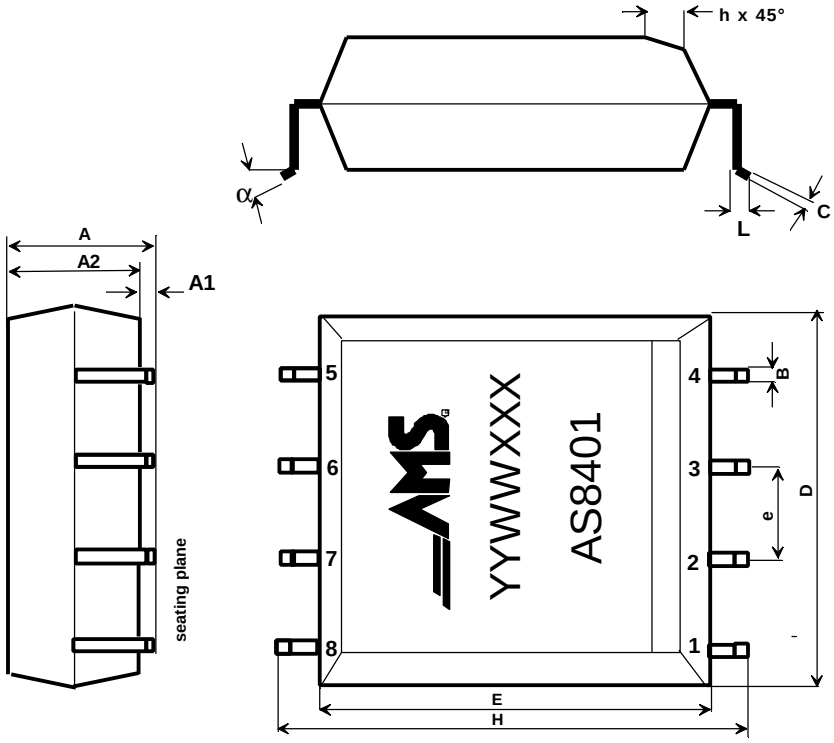

Figure 6: Physical package dimensions