# HM5116100 Series —

**16,777,216-word × 1-bit Dynamic Random Access Memory**

The Hitachi HM5116100 is a CMOS dynamic RAM organized 16,777,216 words × 1 bit. It employs the most advanced CMOS technology for high performance and low power. The HM5116100 offers Fast Page Mode as a high speed access mode.

## Features

- Single 5 V (±10%)
- High speed
  - Access time
    60 ns/ 70 ns/ 80 ns (max)
- Low power dissipation
  - Active mode
    440 mW/385 mW/358 mW (max)
  - Standby mode 11′mW (max)
- Fast page mode capability
- Long refresh period
  - 4096 refresh cycles : 64 ms
- 3 variations of refresh
  - $\overline{\text{RAS}}$-only refresh
  - $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh
  - Hidden refresh
- Test function
  - 16-bit parallel test mode

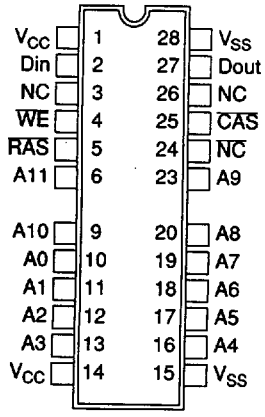
## Ordering Information

| Type No. | Access time | Package |
|---|---|---|
| HM5116100J-6 | 60 ns | 400-mil 24/28-pin plastic SOJ (CP–24DA) |
| HM5116100J-7 | 70 ns | |
| HM5116100J-8 | 80 ns | |
| HM5116100Z-6 | 60 ns | 475-mil 24-pin plastic ZIP (ZP-24A) |
| HM5116100Z-7 | 70 ns | |
| HM5116100Z-8 | 80 ns | |
| HM5116100TT-6 | 60 ns | 24/28-pin plastic TSOP II (TTP-24D) |
| HM5116100TT-7 | 70 ns | |
| HM5116100TT-8 | 80 ns | |
| HM5116100RR-6 | 60 ns | |
| HM5116100RR-7 | 70 ns | |
| HM5116100RR-8 | 80 ns | |

Note: This specification is fully compatible with the 16 Mbit DRAM specifications from TEXAS INSTRUMENTS.

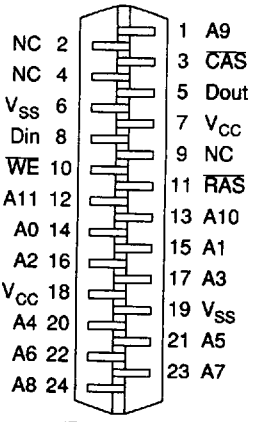
## Pin Arrangement

**HM5116100J Series**



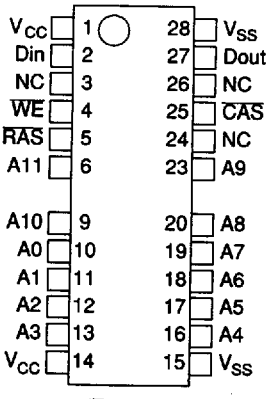

(Top view)

**HM5116100Z Series**



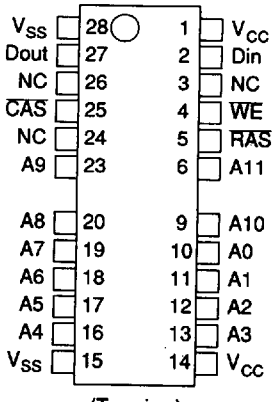

(Bottom view)

**HM5116100TT Series**




(Top view)

**HM5116100RR Series**



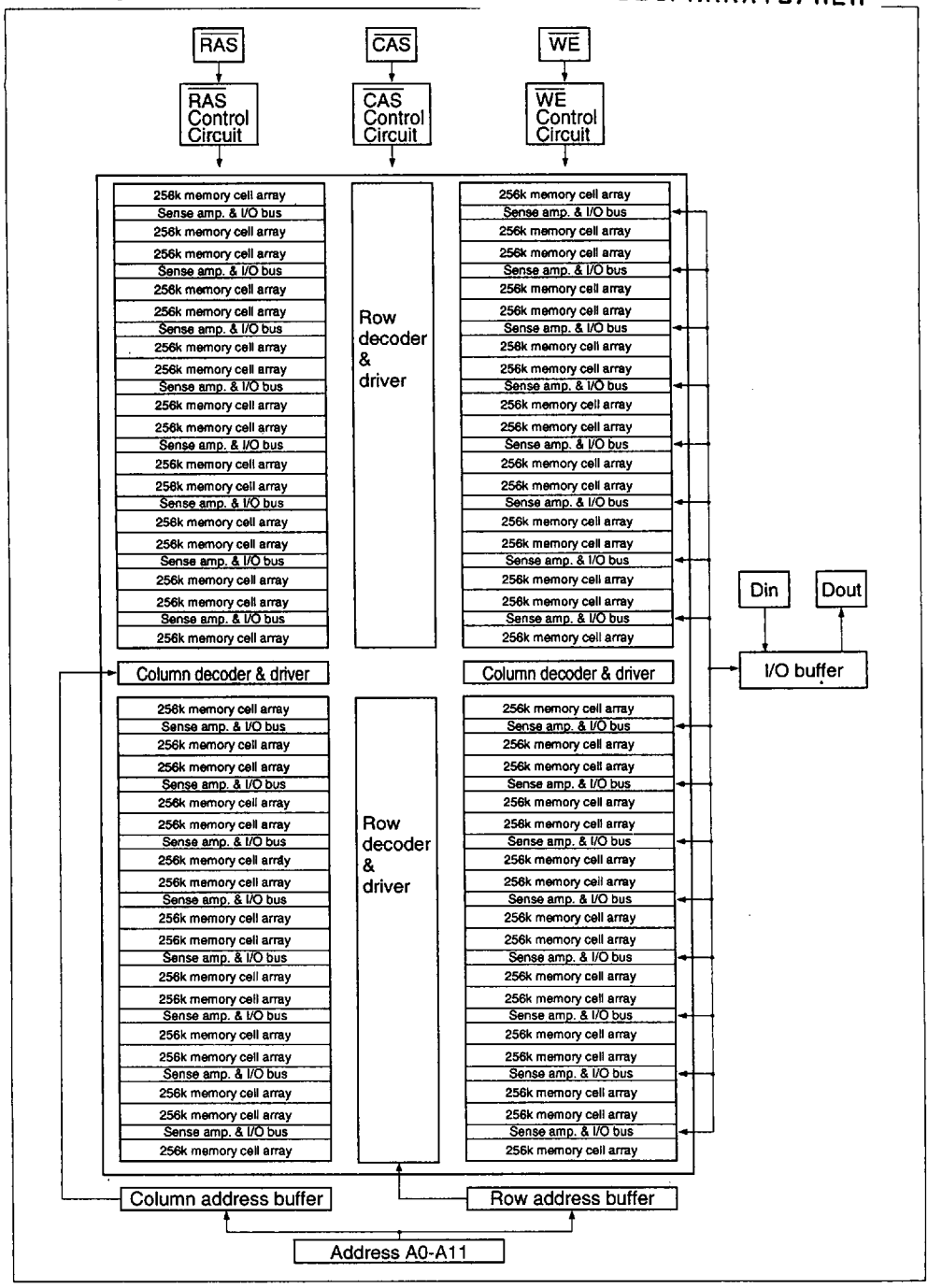

(Top view)

## Pin Description

| Pin Name | Function |
|---|---|
| A0 to A11 | Address input |
| A0 to A11 | Refresh address input |
| Din | Data input |
| Dout | Data output |
| $\overline{RAS}$ | Row address strobe |
| $\overline{CAS}$ | Column address strobe |
| $\overline{WE}$ | Read/write enable |
| $V_{CC}$ | Power supply (+5 V) |
| $V_{SS}$ | Ground |
| NC | No connection |

## Block Diagram

HITACHI/ LOGIC/ARRAYS/MEM



## Absolute Maximum Ratings

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Voltage on any pin relative to $V_{SS}$ | $V_T$ | −1.0 to +7.0 | V |
| Supply voltage relative to $V_{SS}$ | $V_{CC}$ | −1.0 to +7.0 | V |
| Short circuit output current | Iout | 50 | mA |
| Power dissipation | $P_T$ | 1.0 | W |
| Operating temperature | Topr | 0 to +70 | °C |
| Storage temperature | Tstg | −55 to +125 | °C |

## Recommended DC Operating Conditions (Ta = 0 to +70°C)

| Parameter | Symbol | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| Supply voltage | $V_{CC}$ | 4.5 | 5.0 | 5.5 | V | 1 |
| Input high voltage | $V_{IH}$ | 2.4 | — | 6.5 | V | 1 |
| Input low voltage | $V_{IL}$ | −1.0 | — | 0.8 | V | 1 |

Note : 1. All voltage referenced to $V_{SS}$

## DC Characteristics (Ta = 0 to +70°C, $V_{CC}$ = 5 V ± 10%, $V_{SS}$ = 0 V)

| | | HM5116100 -6 | | HM5116100 -7 | | HM5116100 -8 | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Parameter | Symbol | Min | Max | Min | Max | Min | Max | Unit | Test condition | Notes |
| Operating current | $I_{CC1}$ | — | 80 | — | 70 | — | 65 | mA | $t_{RC}$ = min | 1, 2 |
| Standby current | $I_{CC2}$ | — | 2 | — | 2 | — | 2 | mA | TTL interface<br>$\overline{RAS}$, $\overline{CAS}$ = $V_{IH}$<br>Dout = High-Z | |
| | | — | 1 | — | 1 | — | 1 | mA | CMOS interface<br>$\overline{RAS}$, $\overline{CAS}$ ≥ $V_{CC}$ −0.2V<br>Dout = High-Z | |
| $\overline{RAS}$-only refresh current | $I_{CC3}$ | — | 80 | — | 70 | — | 65 | mA | $t_{RC}$ = min | 2 |
| Standby current | $I_{CC5}$ | — | 5 | — | 5 | — | 5 | mA | $\overline{RAS}$ = $V_{IH}$<br>$\overline{CAS}$ = $V_{IL}$<br>Dout = enable | 1 |

## DC Characteristics (Ta = 0 to +70°C, $V_{CC}$ = 5 V ± 10%, $V_{SS}$ = 0 V)(cont)

| Parameter | Symbol | HM5116100 -6 Min | HM5116100 -6 Max | HM5116100 -7 Min | HM5116100 -7 Max | HM5116100 -8 Min | HM5116100 -8 Max | Unit | Test condition | Notes |
|---|---|---|---|---|---|---|---|---|---|---|
| $\overline{CAS}$-before-$\overline{RAS}$ refresh current | $I_{CC6}$ | — | 80 | — | 70 | — | 65 | mA | $t_{RC}$ = min | |
| Fast page mode current | $I_{CC7}$ | — | 80 | — | 70 | — | 65 | mA | $t_{PC}$ = min | 1,3 |
| Input leakage current | $I_{LI}$ | −10 | 10 | −10 | 10 | −10 | 10 | µA | 0 V ≤ Vin ≤ 7 V | |
| Output leakage current | $I_{LO}$ | −10 | 10 | −10 | 10 | −10 | 10 | µA | 0 V ≤ Vout ≤ 7 V<br>Dout = disable | |
| Output high voltage | $V_{OH}$ | 2.4 | $V_{CC}$ | 2.4 | $V_{CC}$ | 2.4 | $V_{CC}$ | V | High Iout = −5 mA | |
| Output low voltage | $V_{OL}$ | 0 | 0.4 | 0 | 0.4 | 0 | 0.4 | V | Low Iout = 4.2 mA | |

Notes : 1. $I_{CC}$ depends on output load condition when the device is selected. $I_{CC}$ max is specified at the output open condition.
2. Address can be changed once or less while $\overline{RAS}$ = $V_{IL}$.
3. Address can be changed once or less while $\overline{CAS}$ = $V_{IH}$.

## Capacitance (Ta = 25°C, $V_{CC}$ = 5 V ± 10%)

| Parameter | Symbol | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|
| Input capacitance (Address, Data-in) | $C_{I1}$ | — | 5 | pF | 1 |
| Input capacitance (Clocks) | $C_{I2}$ | — | 7 | pF | 1 |
| Output capacitance (Data-out) | $C_O$ | — | 7 | pF | 1,2 |

Notes : 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = $V_{IH}$ to disable Dout.

## AC Characteristics (Ta = 0 to +70°C, $V_{CC}$ = 5 V ± 10%, $V_{SS}$ = 0 V) 1), 2), 16)

**Test Conditions**

Input rise and fall times: 5 ns
Input timing reference levels: 0.8 V, 2.4 V
Output load: 2 TTL gate + $C_L$ (100 pF)
(Including scope and jig)

**Read, write, read-modify-write and refresh cycles** (Common parameters)

| | | HM5116100 -6 | | HM5116100 -7 | | HM5116100 -8 | | | |
|---|---|---|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | **Unit** | **Notes** |
| Random read or write cycle time | $t_{RC}$ | 110 | — | 130 | — | 150 | — | ns | |
| $\overline{RAS}$ precharge time | $t_{RP}$ | 40 | — | 50 | — | 60 | — | ns | |
| $\overline{CAS}$ precharge time | $t_{CP}$ | 10 | — | 10 | — | 10 | — | ns | |
| $\overline{RAS}$ pulse width | $t_{RAS}$ | 60 | 10000 | 70 | 10000 | 80 | 10000 | ns | |
| $\overline{CAS}$ pulse width | $t_{CAS}$ | 15 | 10000 | 18 | 10000 | 20 | 10000 | ns | |
| Row address setup time | $t_{ASR}$ | 0 | — | 0 | — | 0 | — | ns | |
| Row address hold time | $t_{RAH}$ | 10 | — | 10 | — | 10 | — | ns | |
| Column address setup time | $t_{ASC}$ | 0 | — | 0 | — | 0 | — | ns | |
| Column address hold time | $t_{CAH}$ | 15 | — | 15 | — | 15 | — | ns | |
| $\overline{RAS}$ to $\overline{CAS}$ delay time | $t_{RCD}$ | 20 | 45 | 20 | 52 | 20 | 60 | ns | 3 |
| $\overline{RAS}$ to column address delay time | $t_{RAD}$ | 15 | 30 | 15 | 35 | 15 | 40 | ns | 4 |
| $\overline{RAS}$ hold time | $t_{RSH}$ | 15 | — | 18 | — | 20 | — | ns | |
| $\overline{CAS}$ hold time | $t_{CSH}$ | 60 | — | 70 | — | 80 | — | ns | |
| $\overline{CAS}$ to $\overline{RAS}$ precharge time | $t_{CRP}$ | 5 | — | 5 | — | 5 | — | ns | |
| Transition time (rise and fall) | $t_T$ | 3 | 30 | 3 | 30 | 3 | 30 | ns | 5 |

## Read cycle



| Parameter | Symbol | HM5116100 -6 Min | HM5116100 -6 Max | HM5116100 -7 Min | HM5116100 -7 Max | HM5116100 -8 Min | HM5116100 -8 Max | Unit | Notes |
|---|---|---|---|---|---|---|---|---|---|
| Access time from $\overline{RAS}$ | $t_{RAC}$ | — | 60 | — | 70 | — | 80 | ns | 6, 7, 17 |
| Access time from $\overline{CAS}$ | $t_{CAC}$ | — | 15 | — | 18 | — | 20 | ns | 7, 8, 15, 17 |
| Access time from address | $t_{AA}$ | — | 30 | — | 35 | — | 40 | ns | 7, 9, 15, 17 |
| Read command setup time | $t_{RCS}$ | 0 | — | 0 | — | 0 | — | ns | |
| Read command hold time to $\overline{CAS}$ | $t_{RCH}$ | 0 | — | 0 | — | 0 | — | ns | 10 |
| Read command hold time to $\overline{RAS}$ | $t_{RRH}$ | 5 | — | 5 | — | 5 | — | ns | 10 |
| Column address to $\overline{RAS}$ lead time | $t_{RAL}$ | 30 | — | 35 | — | 40 | — | ns | |
| Column address to $\overline{CAS}$ lead time | $t_{CAL}$ | 30 | — | 35 | — | 40 | — | ns | |
| $\overline{CAS}$ to output in low-Z | $t_{CLZ}$ | 0 | — | 0 | — | 0 | — | ns | |
| Output data hold time | $t_{OH}$ | 3 | — | 3 | — | 3 | — | ns | |
| Output buffer turn-off time | $t_{OFF}$ | — | 15 | — | 18 | — | 20 | ns | 11 |

## Write cycle

| Parameter | Symbol | HM5116100 -6 Min | HM5116100 -6 Max | HM5116100 -7 Min | HM5116100 -7 Max | HM5116100 -8 Min | HM5116100 -8 Max | Unit | Notes |
|---|---|---|---|---|---|---|---|---|---|
| Write command setup time | $t_{WCS}$ | 0 | — | 0 | — | 0 | — | ns | 12 |
| Write command hold time | $t_{WCH}$ | 15 | — | 15 | — | 15 | — | ns | |
| Write command pulse width | $t_{WP}$ | 15 | — | 15 | — | 15 | — | ns | |
| Write command to $\overline{RAS}$ lead time | $t_{RWL}$ | 15 | — | 18 | — | 20 | — | ns | |
| Write command to $\overline{CAS}$ lead time | $t_{CWL}$ | 15 | — | 18 | — | 20 | — | ns | |
| Data-in setup time | $t_{DS}$ | 0 | — | 0 | — | 0 | — | ns | 13 |
| Data-in hold time | $t_{DH}$ | 15 | — | 15 | — | 15 | — | ns | 13 |

### Read-modify-write cycle

| Parameter | Symbol | HM5116100-6 Min | HM5116100-6 Max | HM5116100-7 Min | HM5116100-7 Max | HM5116100-8 Min | HM5116100-8 Max | Unit | Notes |
|---|---|---|---|---|---|---|---|---|---|
| Read-modify-write cycle time | $t_{RWC}$ | 130 | — | 153 | — | 175 | — | ns | |
| $\overline{RAS}$ to $\overline{WE}$ delay time | $t_{RWD}$ | 60 | — | 70 | — | 80 | — | ns | 12 |
| $\overline{CAS}$ to $\overline{WE}$ delay time | $t_{CWD}$ | 15 | — | 18 | — | 20 | — | ns | 12 |
| Column address to $\overline{WE}$ delay time | $t_{AWD}$ | 30 | — | 35 | — | 40 | — | ns | 12 |

### Refrtesh cycle

| Parameter | Symbol | HM5116100-6 Min | HM5116100-6 Max | HM5116100-7 Min | HM5116100-7 Max | HM5116100-8 Min | HM5116100-8 Max | Unit | Notes |
|---|---|---|---|---|---|---|---|---|---|
| $\overline{CAS}$ setup time (CBR refresh cycle) | $t_{CSR}$ | 10 | — | 10 | — | 10 | — | ns | |
| $\overline{CAS}$ hold time (CBR refresh cycle) | $t_{CHR}$ | 20 | — | 20 | — | 20 | — | ns | |
| $\overline{WE}$ setup time (CBR refresh cycle) | $t_{WRP}$ | 10 | — | 10 | — | 10 | — | ns | |
| $\overline{WE}$ hold time (CBR refresh cycle) | $t_{WRH}$ | 10 | — | 10 | — | 10 | — | ns | |
| $\overline{RAS}$ precharge to $\overline{CAS}$ hold time | $t_{RPC}$ | 0 | — | 0 | — | 0 | — | ns | |

### Fast page mode cycle

| Parameter | Symbol | HM5116100-6 Min | HM5116100-6 Max | HM5116100-7 Min | HM5116100-7 Max | HM5116100-8 Min | HM5116100-8 Max | Unit | Notes |
|---|---|---|---|---|---|---|---|---|---|
| Fast page mode cycle time | $t_{PC}$ | 40 | — | 45 | — | 50 | — | ns | |
| Fast page mode $\overline{RAS}$ pulse width | $t_{RASP}$ | — | 100000 | — | 100000 | — | 100000 | ns | 14 |
| Access time from $\overline{CAS}$ precharge | $t_{CPA}$ | — | 35 | — | 40 | — | 45 | ns | 7, 15, 17 |
| $\overline{RAS}$ hold time from $\overline{CAS}$ precharge | $t_{CPRH}$ | 35 | — | 40 | — | 45 | — | ns | |

### Fast page mode read-modify-write cycle

| Parameter | Symbol | HM5116100 -6 Min | HM5116100 -6 Max | HM5116100 -7 Min | HM5116100 -7 Max | HM5116100 -8 Min | HM5116100 -8 Max | Unit | Notes |
|---|---|---|---|---|---|---|---|---|---|
| Fast page mode read-modify-write cycle time | $t_{PRWC}$ | 60 | — | 68 | — | 75 | — | ns | |
| $\overline{WE}$ delay time from $\overline{CAS}$ precharge | $t_{CPW}$ | 35 | — | 40 | — | 45 | — | ns | 12 |

### Test mode cycle *16

| Parameter | Symbol | HM5116100 -6 Min | HM5116100 -6 Max | HM5116100 -7 Min | HM5116100 -7 Max | HM5116100 -8 Min | HM5116100 -8 Max | Unit | Notes |
|---|---|---|---|---|---|---|---|---|---|
| Test mode $\overline{WE}$ setup time | $t_{WTS}$ | 10 | — | 10 | — | 10 | — | ns | |
| Test mode $\overline{WE}$ hold time | $t_{WTH}$ | 10 | — | 10 | — | 10 | — | ns | |

### Counter test cycle

| Parameter | Symbol | HM5116100 -6 Min | HM5116100 -6 Max | HM5116100 -7 Min | HM5116100 -7 Max | HM5116100 -8 Min | HM5116100 -8 Max | Unit | Notes |
|---|---|---|---|---|---|---|---|---|---|
| $\overline{CAS}$ precharge time in counter test cycle | $t_{CPT}$ | 40 | — | 40 | — | 40 | — | ns | |

### Refresh

| Parameter | Symbol | Max | Unit | Notes |
|---|---|---|---|---|
| Refresh period | $t_{REF}$ | 64 | ms | 4096 cycles |

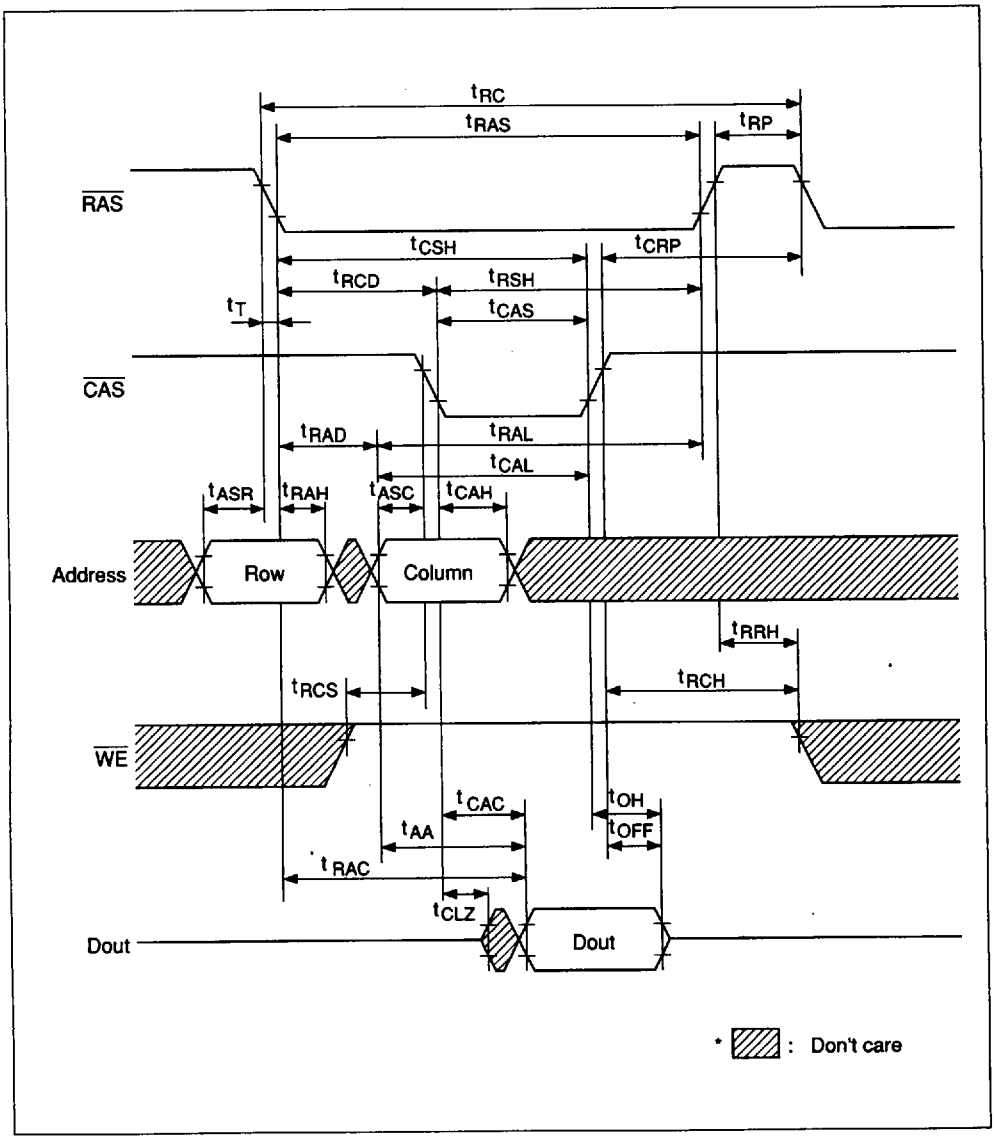
Notes:
1. AC measurements assume $t_T$ = 5 ns.
2. An initial pause of 200 µs is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{RAS}$-only refresh or $\overline{CAS}$-before-$\overline{RAS}$ refresh). If the internal refresh counter is used, a minimum of eight $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles are required.
3. Operation with the $t_{RCD}$(max) limit insures that $t_{RAC}$(max) can be met, $t_{RCD}$(max) is specified as a reference point only; if $t_{RCD}$ is greater than the specified $t_{RCD}$(max) limit, then access time is controlled exclusively by $t_{CAC}$.
4. Operation with the $t_{RAD}$(max) limit insures that $t_{RAC}$(max) can be met, $t_{RAD}$(max) is specified as a reference point only; if $t_{RAD}$ is greater than the specified $t_{RAD}$(max) limit, then access time is controlled exclusively by $t_{AA}$.
5. $V_{IH}$(min) and $V_{IL}$(max) are reference levels for measuring timing of input signals. Also, transition times are measured between $V_{IH}$(min) and $V_{IL}$(max).

6. Assume that $t_{RCD} < t_{RCD}(max)$ and $t_{RAD} < t_{RAD}(max)$. If $t_{RCD}$ or $t_{RAD}$ is greater than the maximum recommended value shown in this table, $t_{RAC}$ exceeds the value shown.
7. Measured with a load circuit equivalent to 2TTL loads and 100 pF.
8. Assume that $t_{RCD} \geq t_{RCD}(max)$ and $t_{RAD} \leq t_{RAD}(max)$.
9. Assume that $t_{RCD} \leq t_{RCD}(max)$ and $t_{RAD} \geq t_{RAD}(max)$.
10. Either $t_{RCH}$ or $t_{RRH}$ must be satisfied for a read cycles.
11. $t_{OFF}(max)$ defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
12. $t_{WCS}$, $t_{RWD}$, $t_{CWD}$, $t_{AWD}$ and $t_{CPW}$ are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}(min)$, the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}(min)$, $t_{CWD} \geq t_{CWD}(min)$ and $t_{AWD} \geq t_{AWD}(min)$, or $t_{CWD} \geq t_{CWD}(min)$, $t_{AWD} \geq t_{AWD}(min)$ and $t_{CPW} \geq t_{CPW}(min)$, the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
13. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.
14. $t_{RASP}$ defines $\overline{RAS}$ pulse width in fast page mode cycles.
15. Access time is determined by the longer of $t_{AA}$ or $t_{CAC}$ or $t_{CPA}$.
16. The 16M DRAM offers a 16-bits time saving parallel test mode. Address CA0, CA1, CA10, and CA11 for the 16M × 1 are don't care during test mode. Test mode is set by performing a $\overline{WE}$-and-$\overline{CAS}$-before-$\overline{RAS}$ (WCBR) cycle. In 16-bits parallel test mode, data is written into 16 bits in parallel at Din and read out from Dout.
    If 16 bits are equal (all 1s or 0s), data output pin is a high state during test mode read cycle, then the device has passed. If they are not equal, data output pin is a low state, then the device has failed.
    Refresh during test mode operation can be performed by normal read cycles or by WCBR refresh cycles.
    To get out of test mode and enter a normal operation mode, perform either a regular $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle or $\overline{RAS}$-only refresh cycle.
17. In a test mode read cycle, the value of $t_{RAC}$, $t_{AA}$, $t_{CAC}$ and $t_{CPA}$ is delayed by 2 ns to 5 ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.

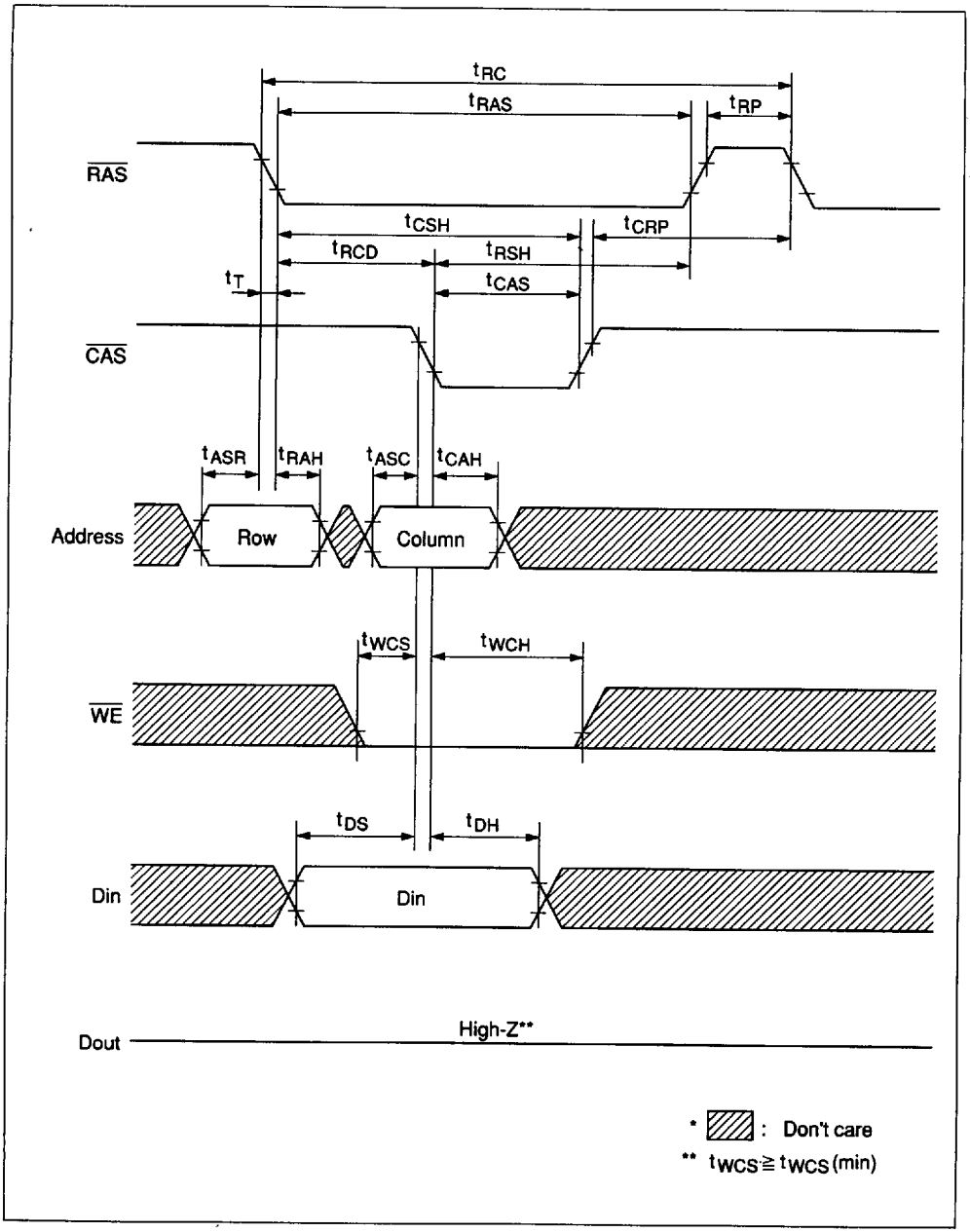
## Timing Waveforms



### Read Cycle

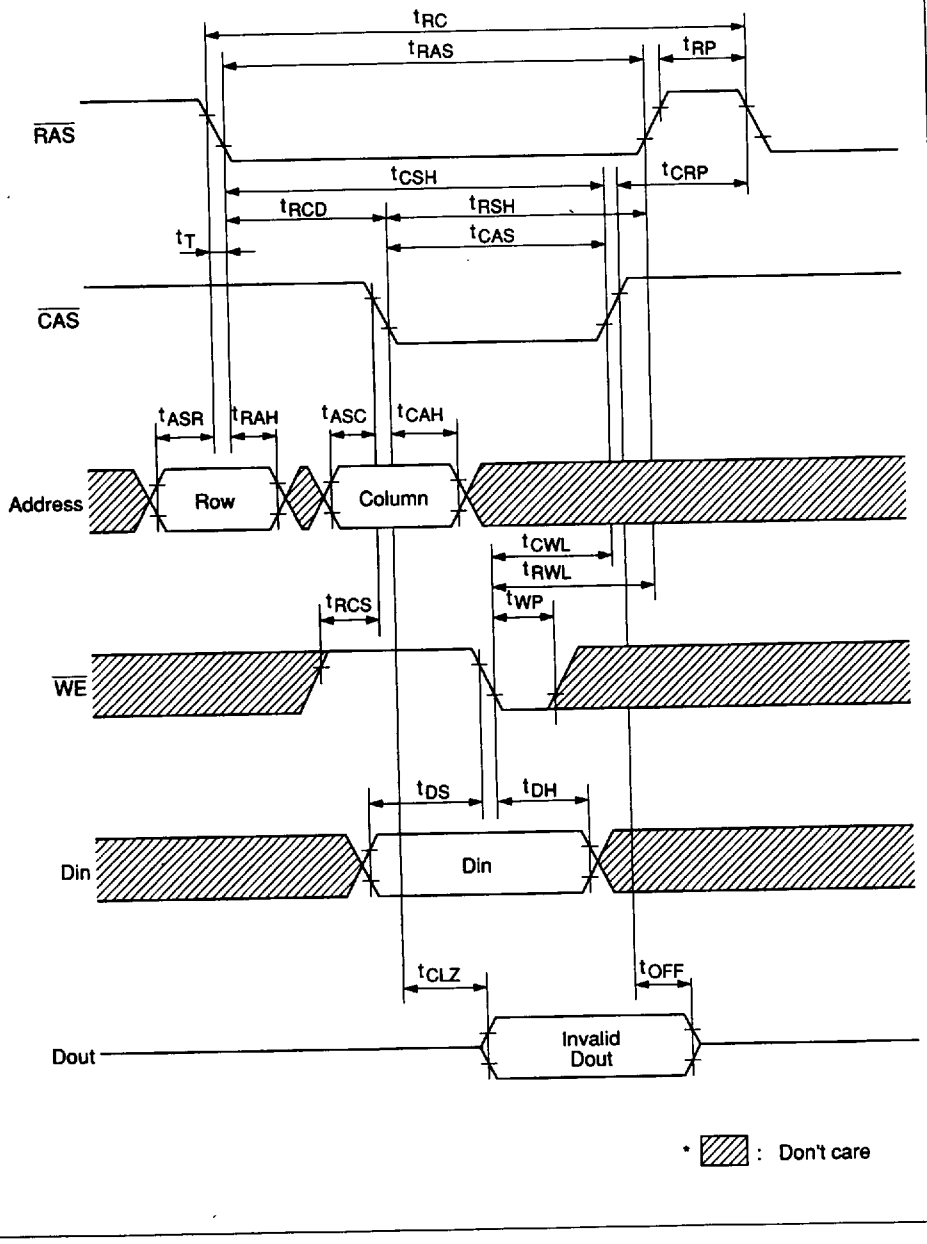


**Early Write Cycle**

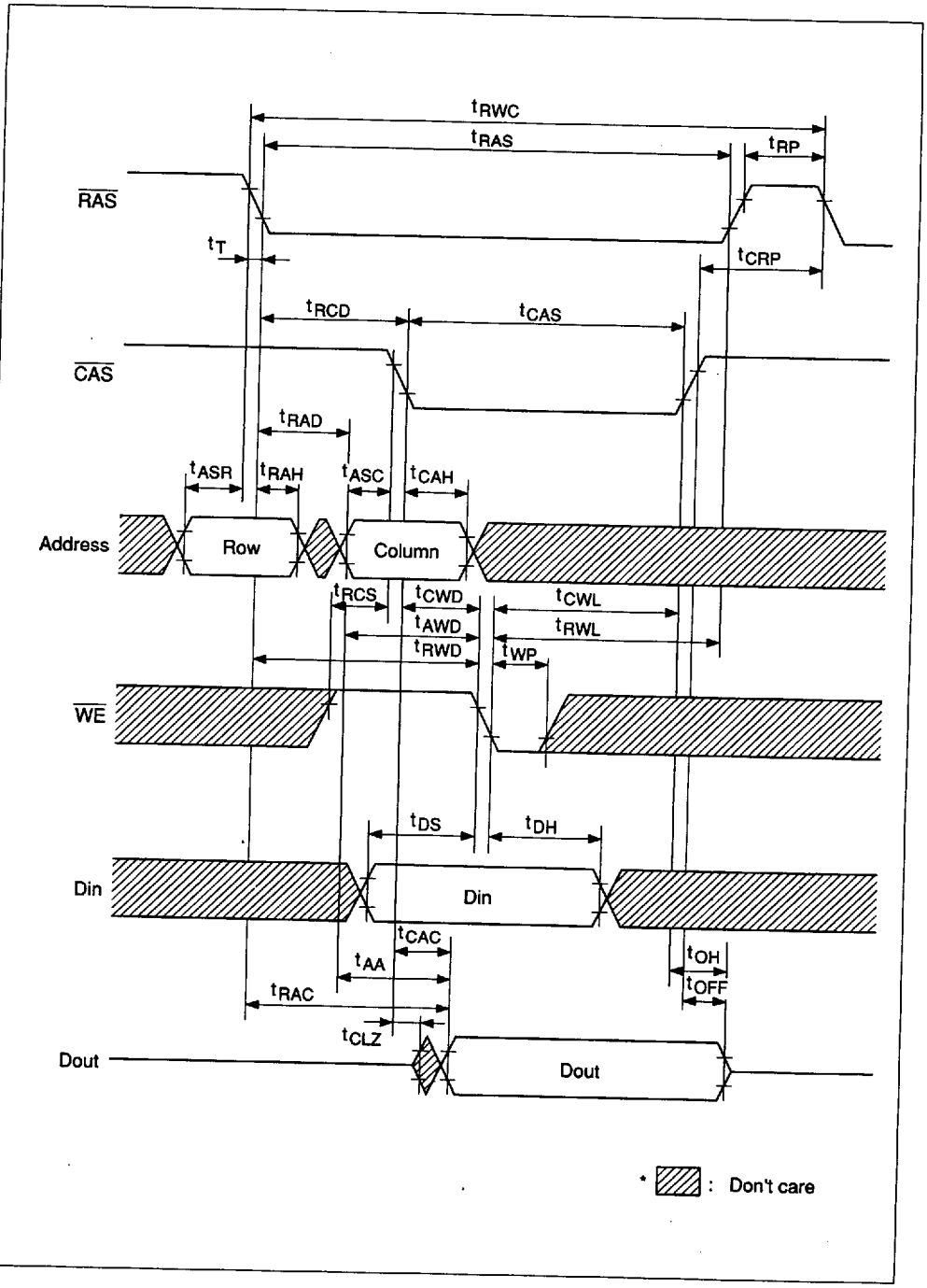


**Delayed Write Cycle**



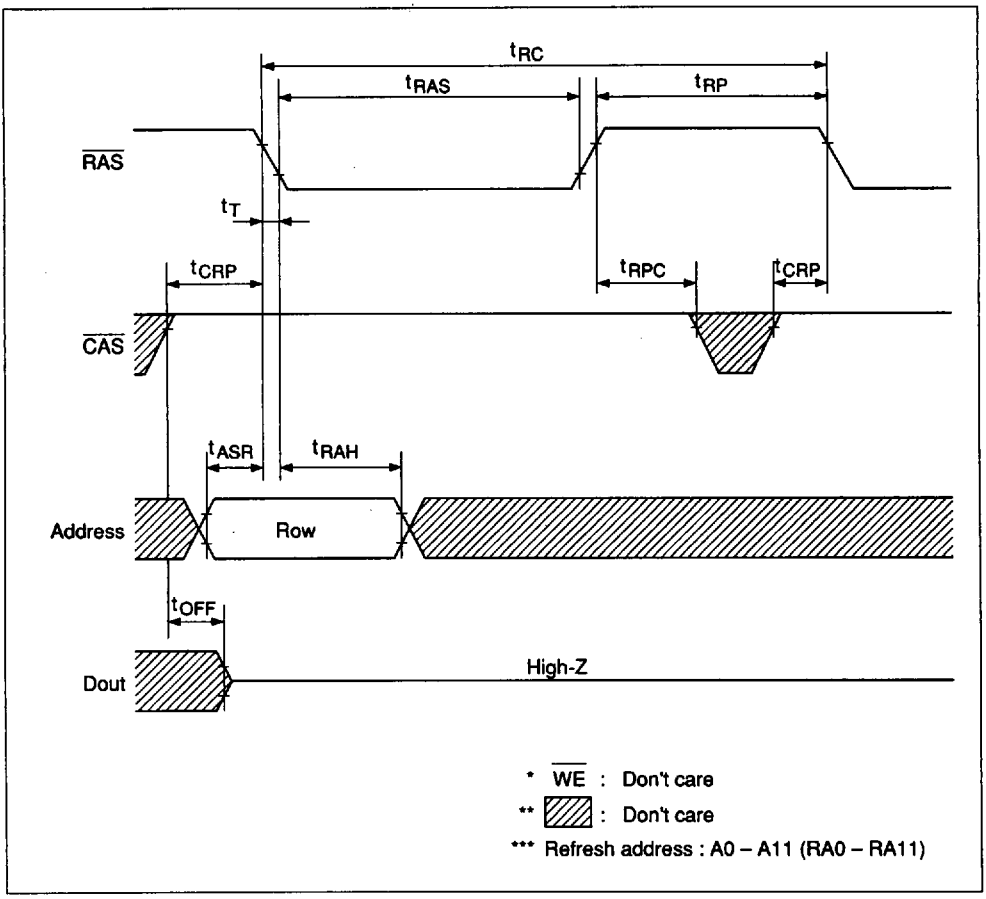


## Read–Modify–Write Cycle

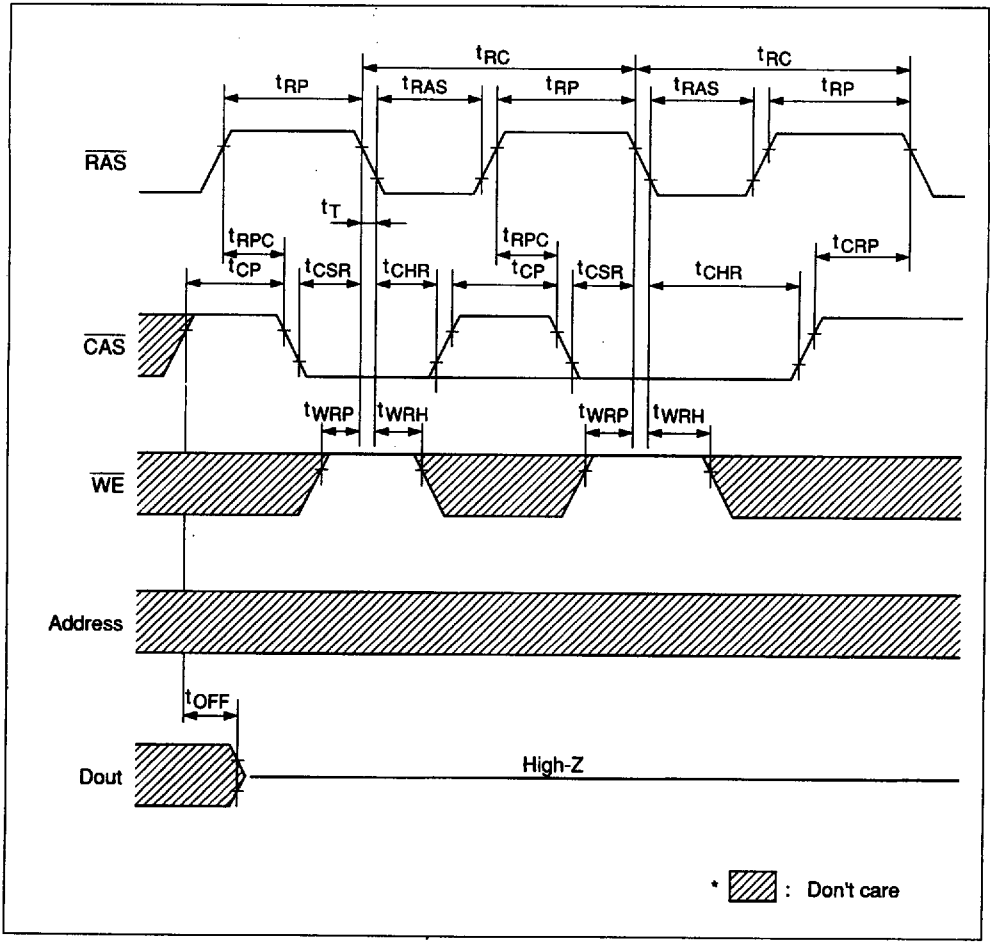


## $\overline{RAS}$-Only Refresh Cycle



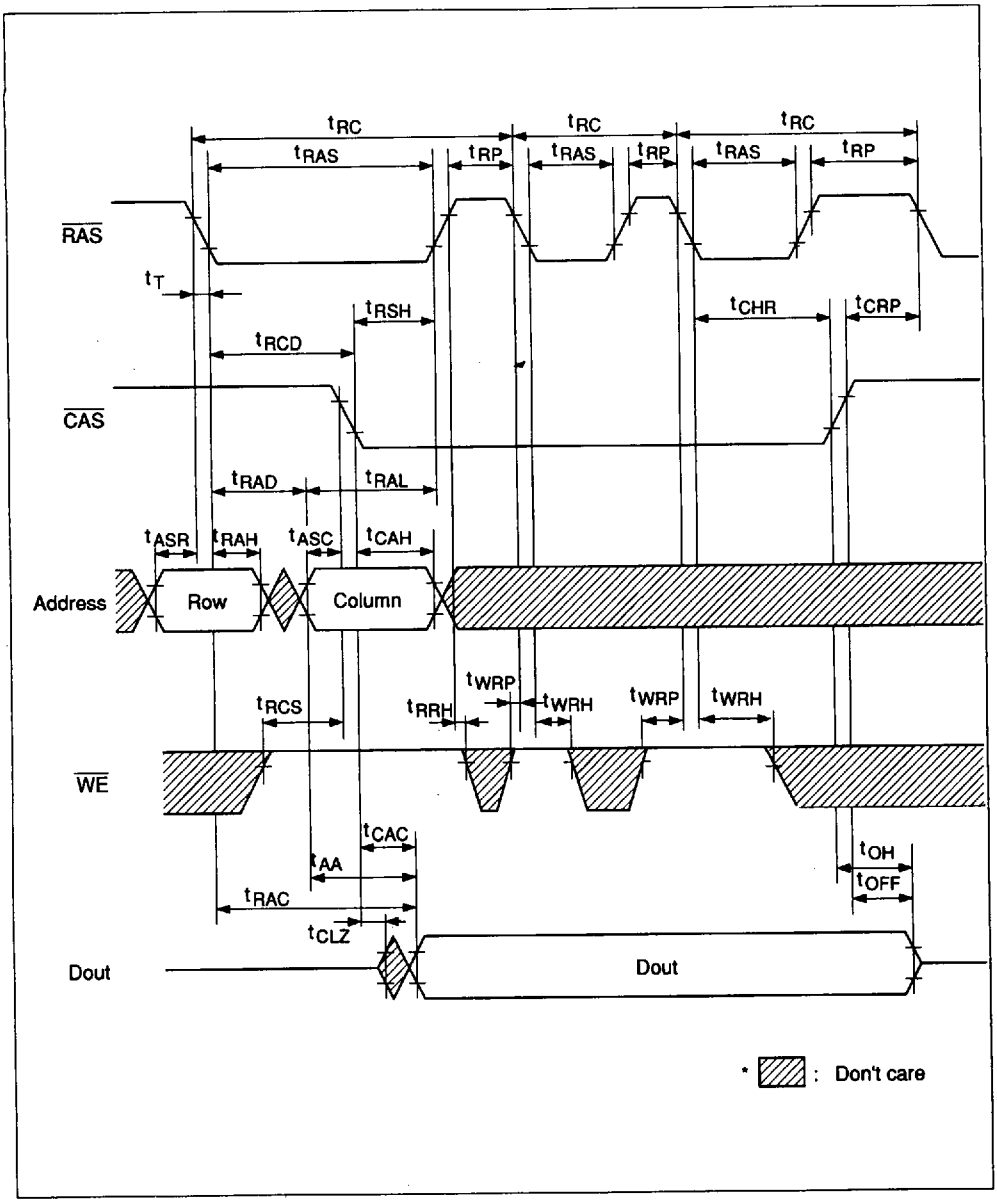


## $\overline{CAS}$–Before–$\overline{RAS}$ Refresh Cycle

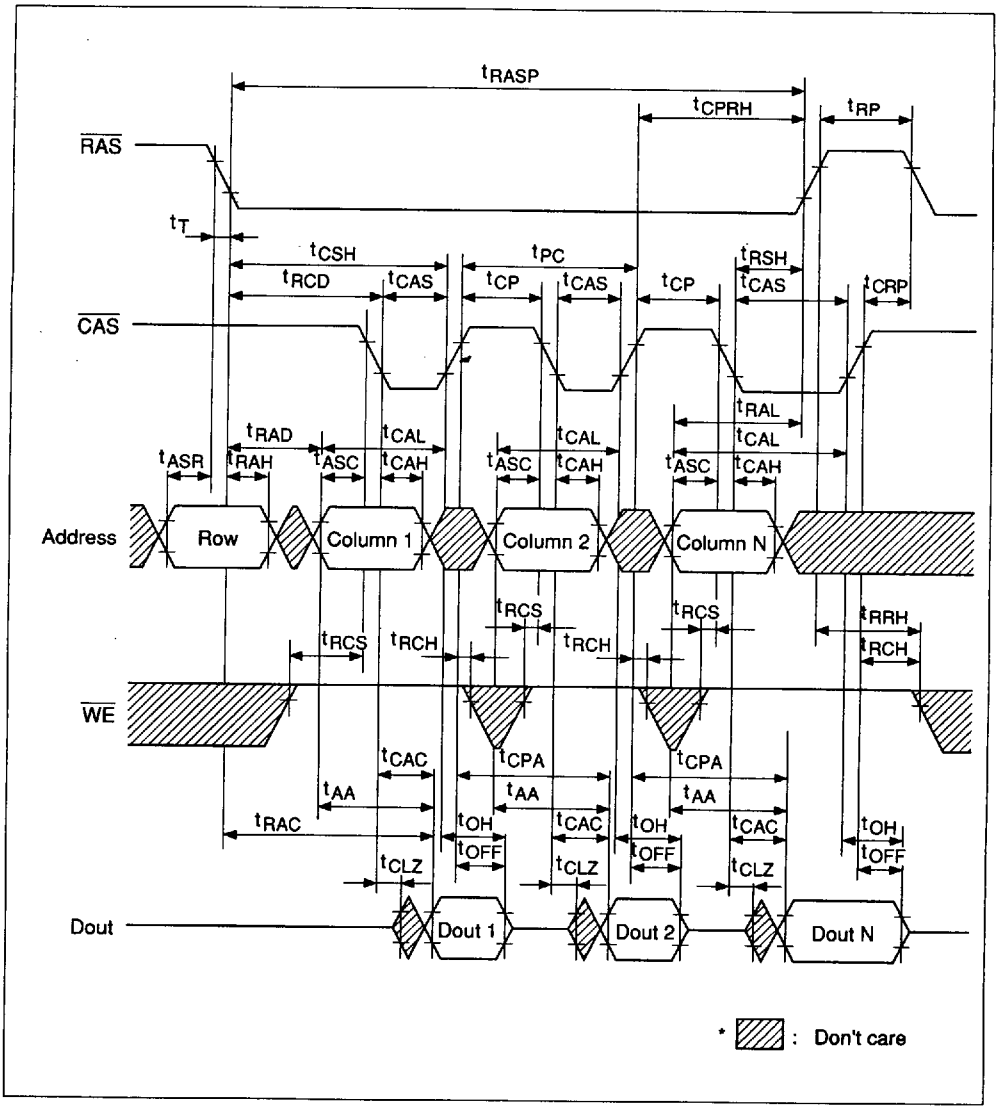


## Hidden Refresh Cycle

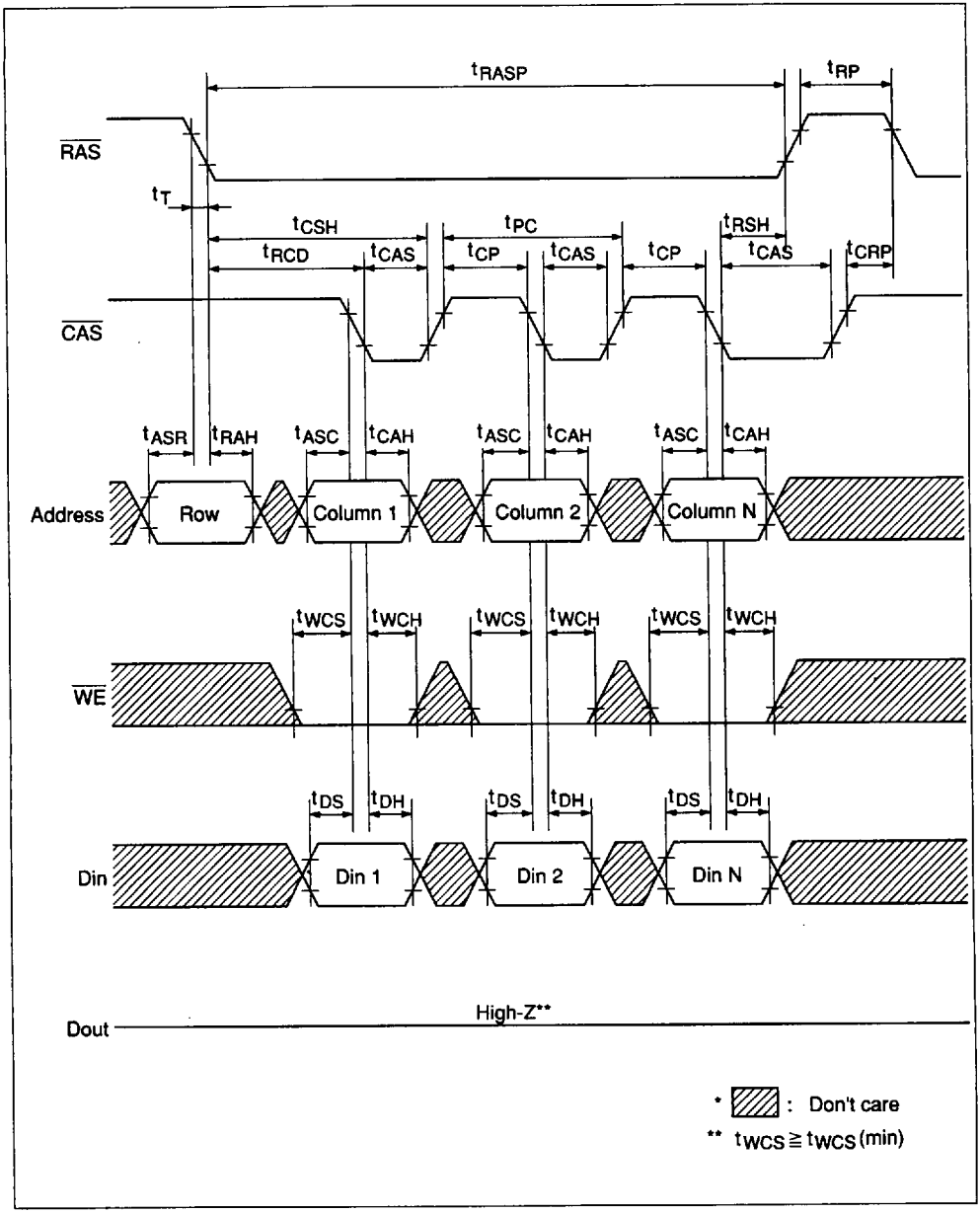




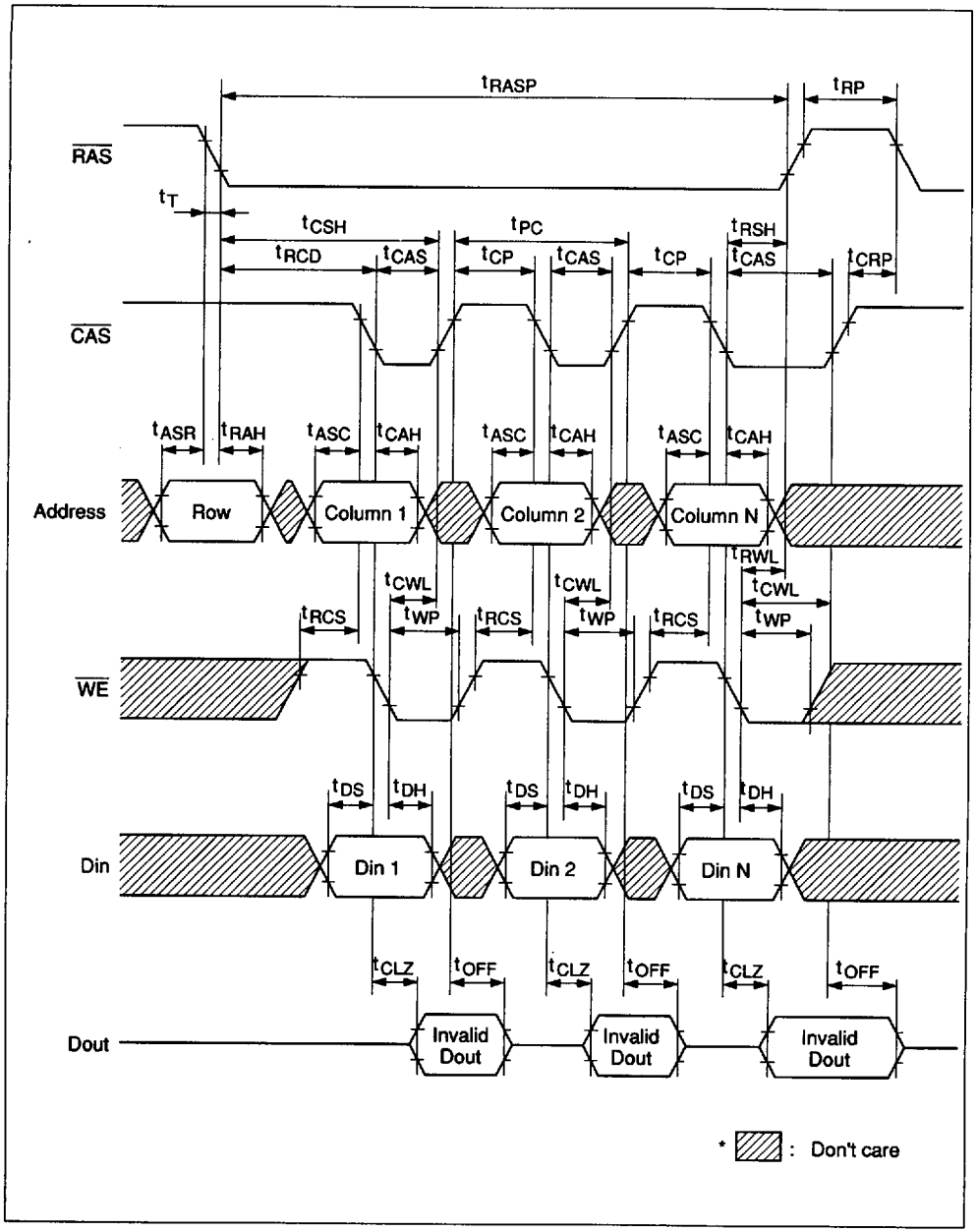
**Fast Page Mode Read Cycle**



**Fast Page Mode Early Write Cycle**

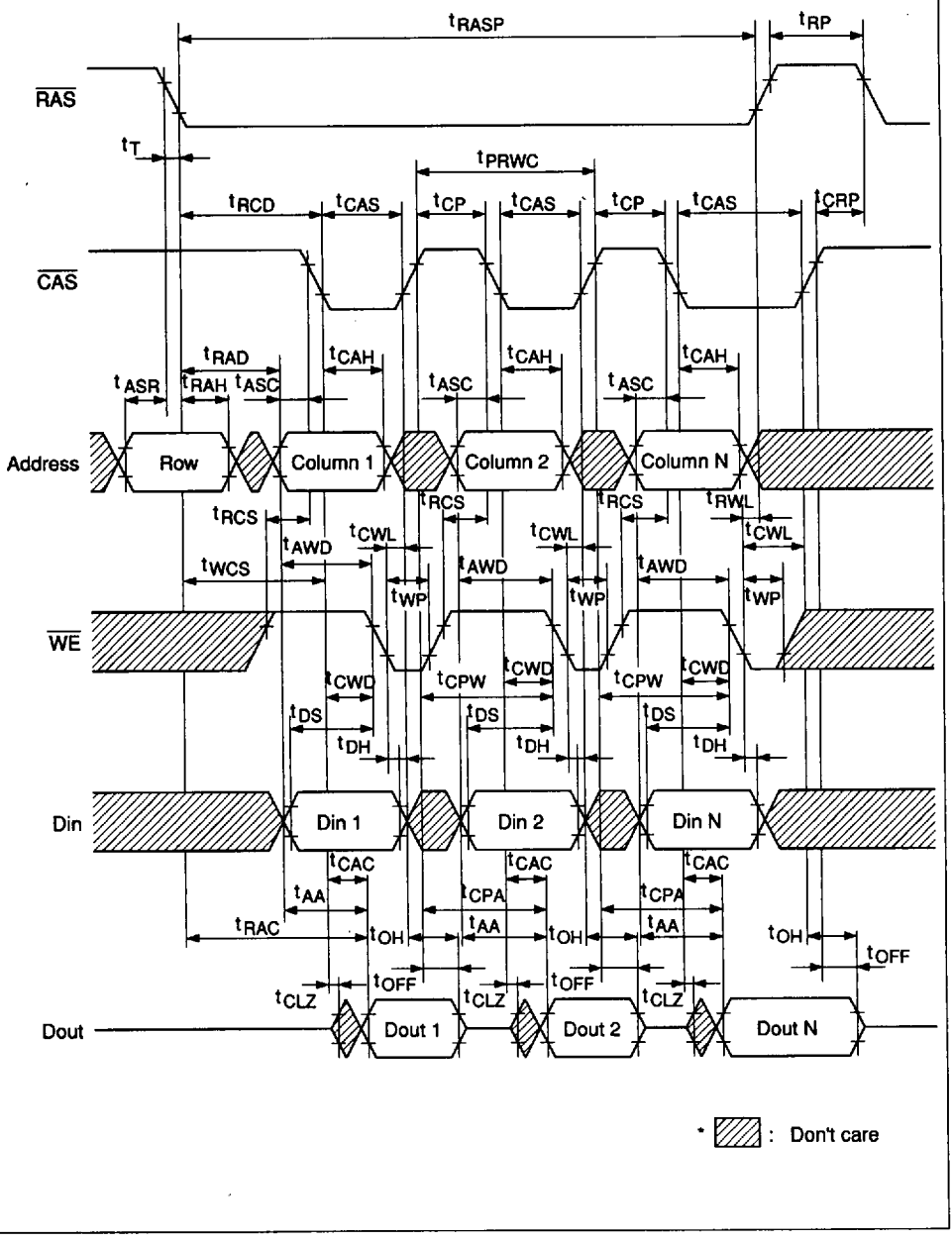


**Fast Page Mode Delayed Write Cycle**

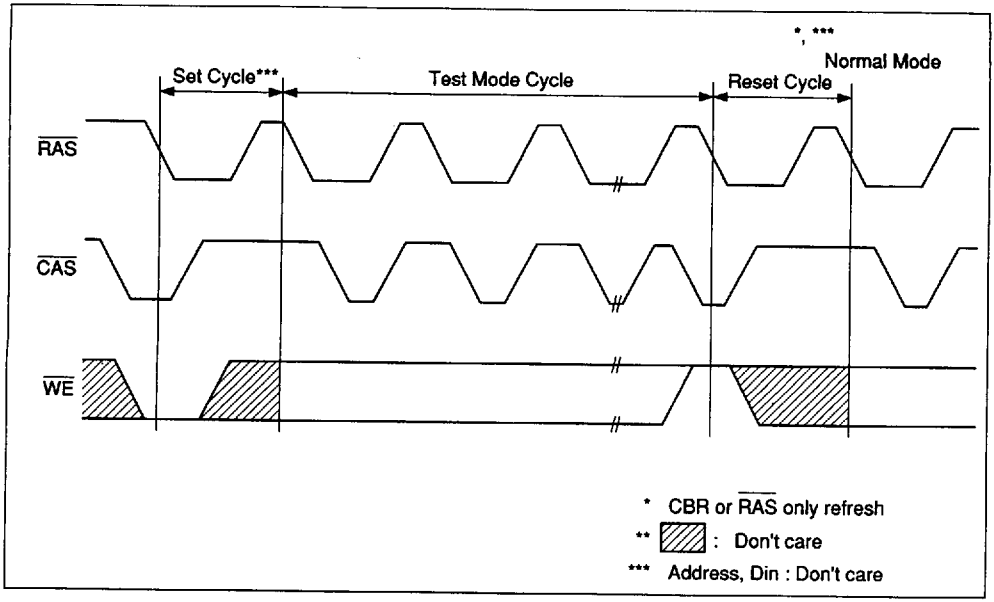


**Fast Page Mode Read–Modify–Write Cycle**

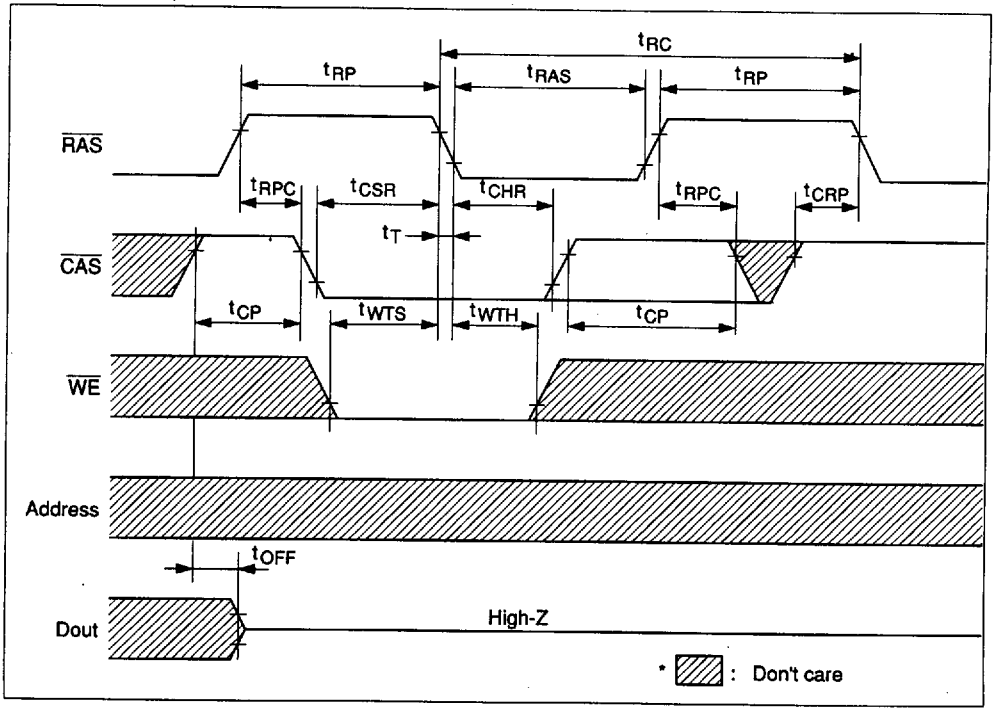




**Test Mode Cycle** *16



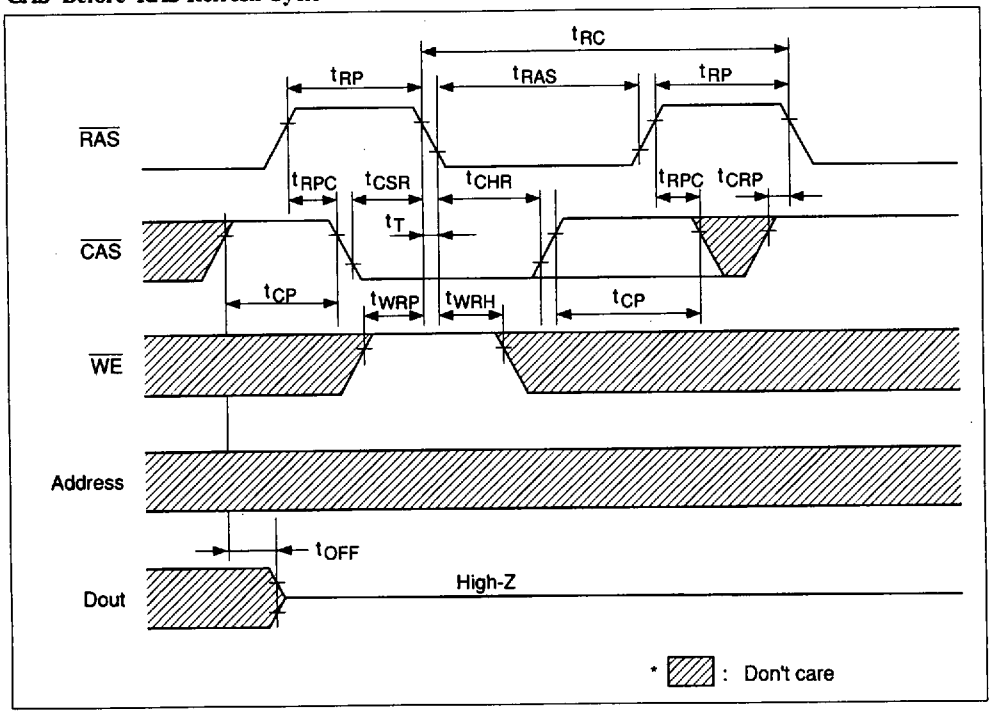

**Test Mode Set Cycle**



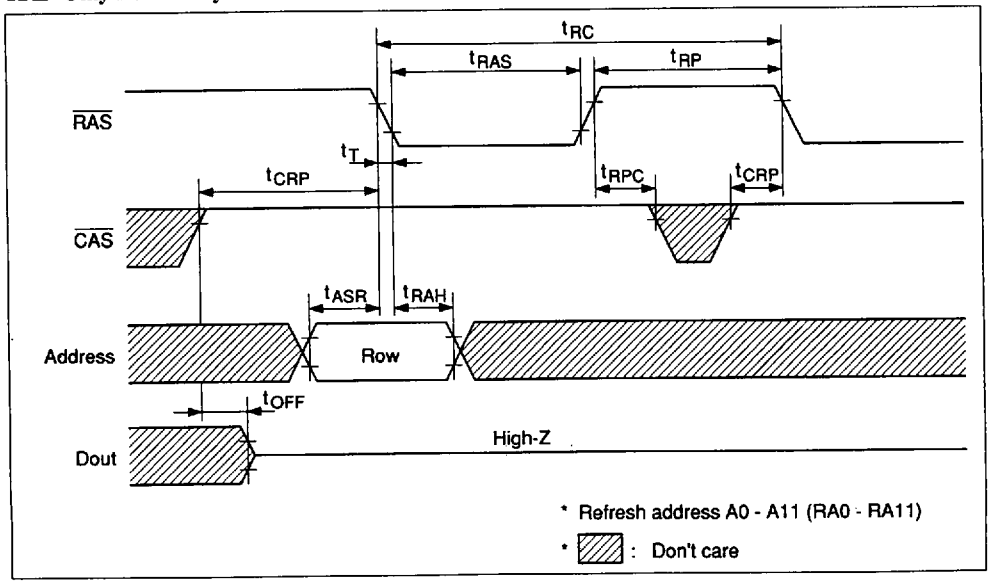
## Test Mode Reset Cycle

HITACHI/ LOGIC/ARRAYS/MEM

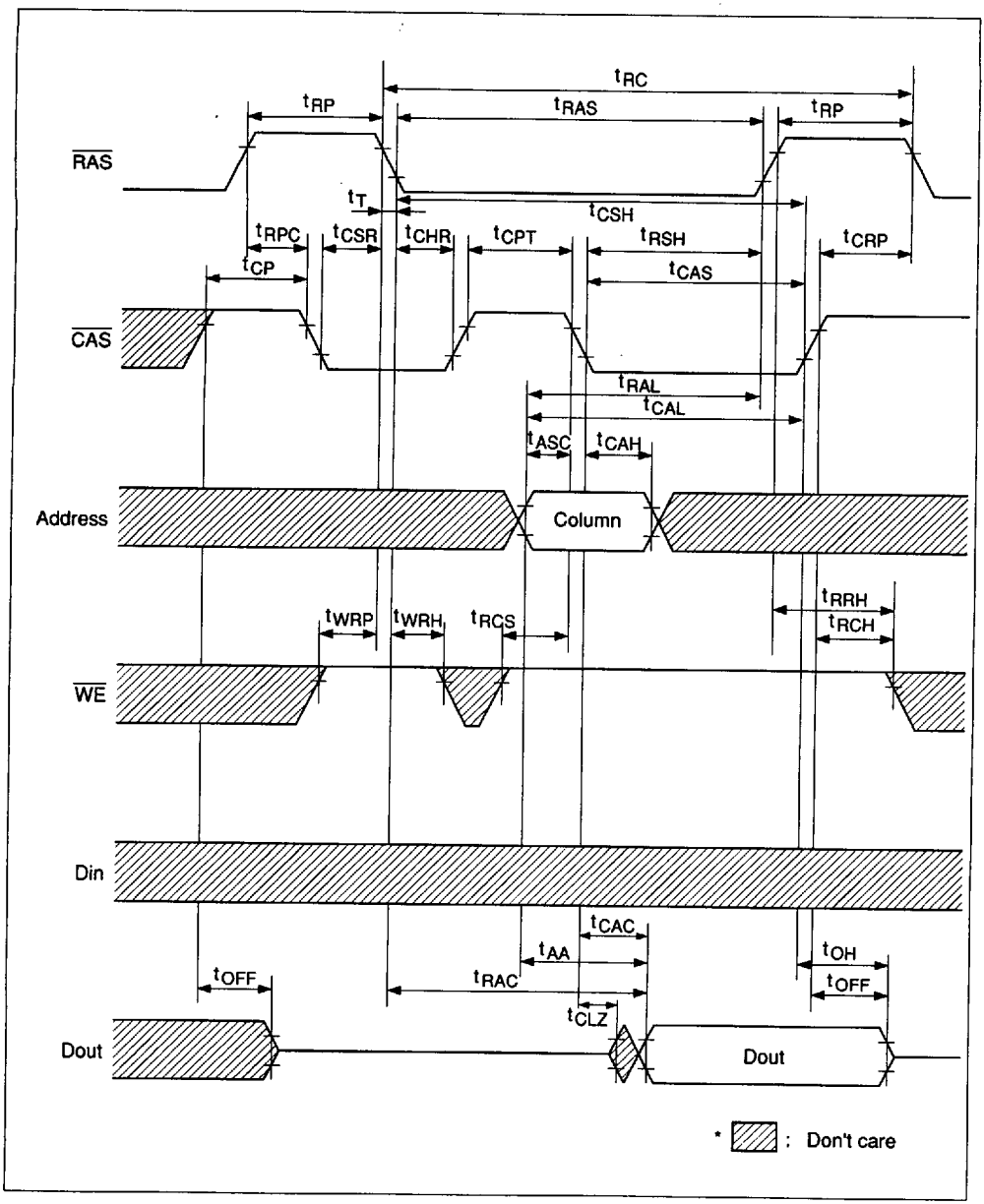
### $\overline{CAS}$–Before–$\overline{RAS}$ Refresh Cycle




### $\overline{RAS}$–Only Refresh Cycle



**$\overline{CAS}$–Before–$\overline{RAS}$ Refresh Counter Check Cycle (Read)**



**$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Counter Check Cycle (Write)**