

### Typical Applications

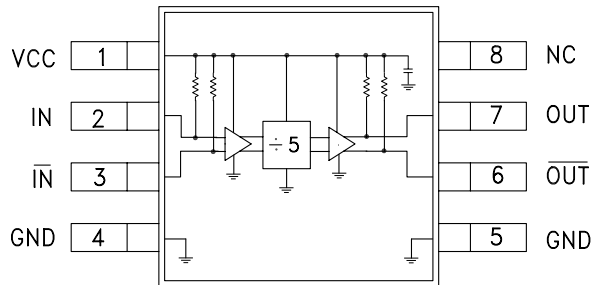
Prescaler for DC to C Band PLL Applications:

- UNII, Pt. - Pt. & VSAT Radios
- 802.11a & HiperLAN WLAN
- Fiber Optic
- Cellular / 3G Infrastructure

### Features

- SSB Phase Noise: -153 dBc/Hz @ 100KHz
- Wide Bandwidth
- Output Power: -1 dBm
- Single DC Supply: +5V @ 80 mA
- MS8G SMT Package

### Functional Diagram



### General Description

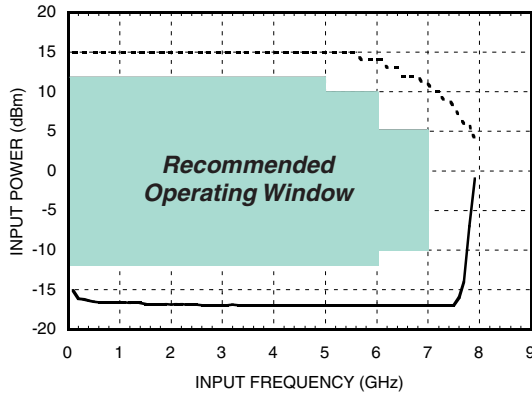
The HMC438MS8G is a low noise Divide-by-5 Static Divider utilizing InGaP GaAs HBT technology in a low cost 8 lead surface mount plastic package. This device operates from DC (with a square wave input) to 7.0 GHz input frequency from a single +5.0V DC supply. The low additive SSB phase noise of -153 dBc/Hz at 100 kHz offset helps the user maintain good system noise performance.

### Electrical Specifications, $T_A = +25^\circ C$ , 50 Ohm System, $V_{cc} = 5V$

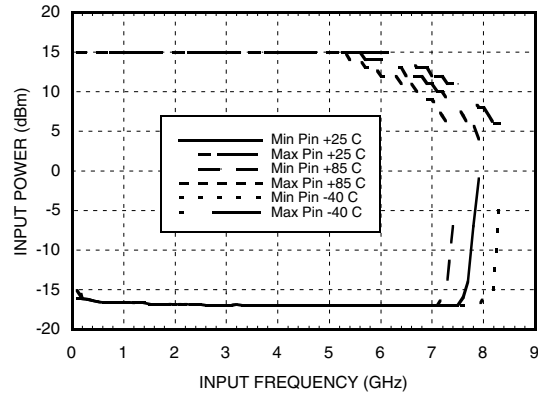
| Parameter                        | Conditions                            | Min. | Typ. | Max. | Units  |
|----------------------------------|---------------------------------------|------|------|------|--------|
| Maximum Input Frequency          |                                       | 7.0  | 7.5  |      | GHz    |
| Minimum Input Frequency          | Sine Wave Input [1]                   |      | 0.1  |      | GHz    |
| Input Power Range                | $F_{in} = 1$ to 5 GHz                 | -12  | -15  | +12  | dBm    |
|                                  | $F_{in} = 5$ to 6 GHz                 | -12  | -15  | +10  | dBm    |
|                                  | $F_{in} = 6$ to 7 GHz                 | -10  | -15  | +5   | dBm    |
| Output Power                     |                                       | -4   | -1   |      | dBm    |
| Reverse Leakage                  | Both RF Outputs Terminated            |      | -50  |      | dBm    |
| SSB Phase Noise (100 kHz offset) | $P_{in} = 0$ dBm, $F_{in} = 6$ GHz    |      | -153 |      | dBc/Hz |
| Output Transition Time           | $P_{in} = 0$ dBm, $F_{out} = 882$ MHz |      | 100  |      | ps     |
| Supply Current ( $I_{cc}$ )      |                                       |      | 80   |      | mA     |

1. Divider will operate down to DC for square-wave input signal.

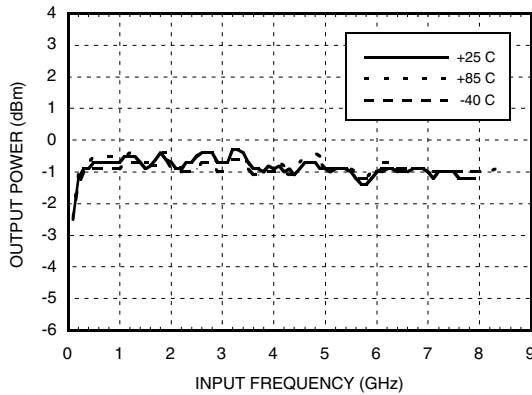
**Input Sensitivity Window, T= 25 °C**



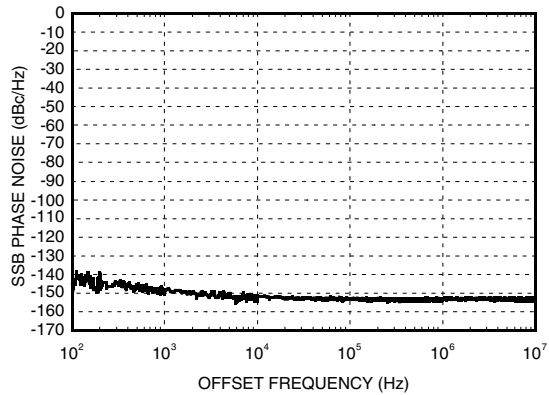
**Input Sensitivity Window vs. Temperature**



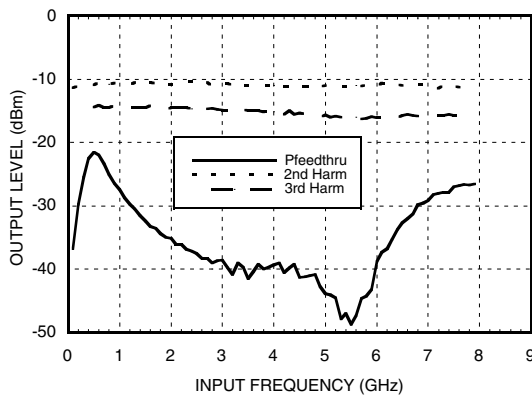
**Output Power vs. Temperature**



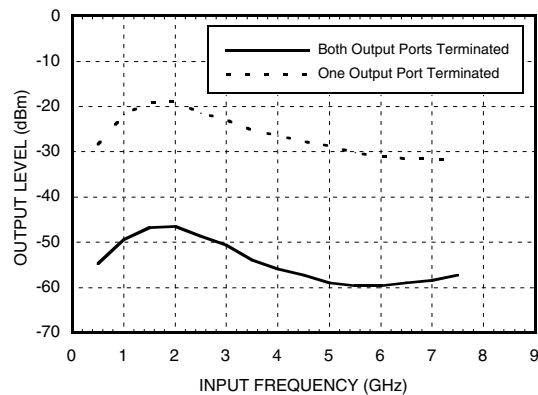
**SSB Phase Noise Performance,  
Pin= 0 dBm, Fin= 6GHz, T= 25 °C**



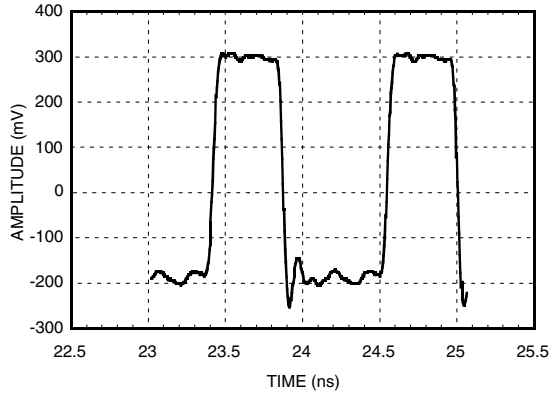
**Output Harmonic Content, Pin= 0 dBm, T= 25 °C**



**Reverse Leakage, Pin= 0 dBm, T= 25 °C**



**Output Voltage Waveform,**  
*Pin= 0 dBm, Fout= 882 MHz, T= 25 °C*



### Absolute Maximum Ratings

|  |                |
|--|----------------|
| RF Input (Vcc= +5V)  | +13 dBm        |
| Vcc  | +5.5V          |
| Maximum Channel Temperature  | 135 °C         |
| Continuous P <sub>diss</sub> (T=85 °C)<br>(derate 11.3mW/°C above 92 °C) | 485mW          |
| Storage Temperature  | -65 to +150 °C |
| Operating Temperature  | -40 to +85 °C  |

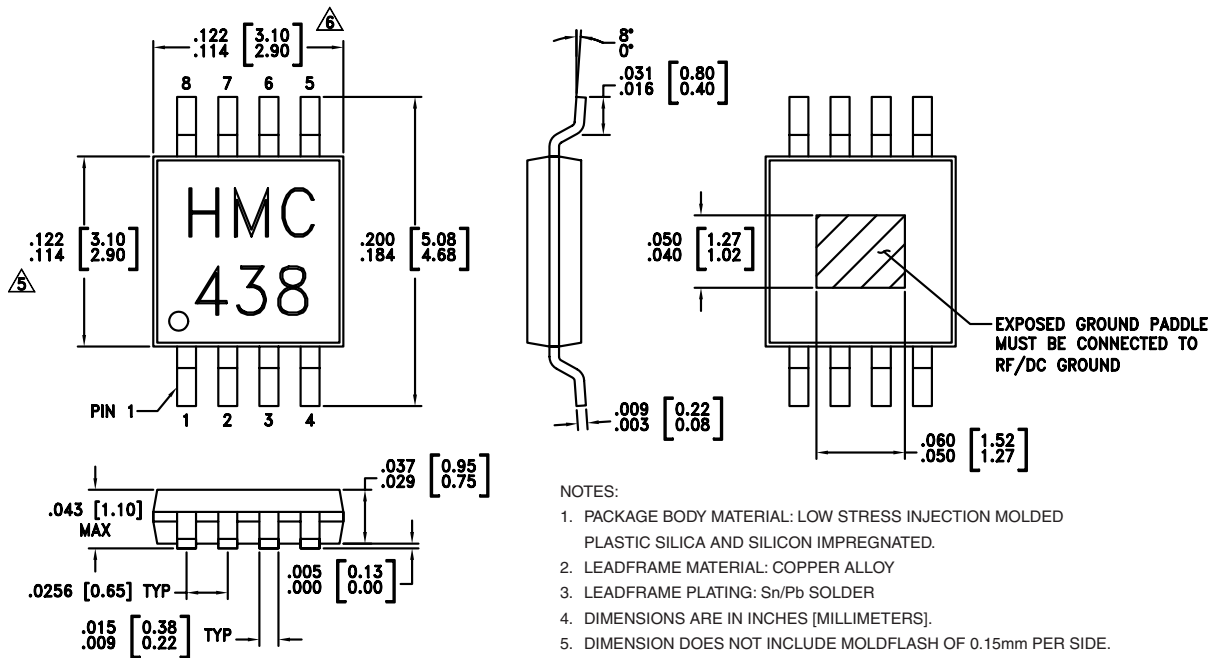
DC blocking capacitors are required at RF input and RF output ports. Choose value for lowest frequency of operation.

### Typical Supply Current vs. Vcc

| Vcc (V) | Icc (mA) |
|---------|----------|
| 4.75    | 75       |
| 5.0     | 80       |
| 5.25    | 87       |

Note: Divider will operate over full voltage range shown above

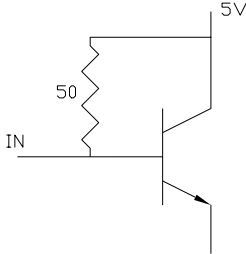
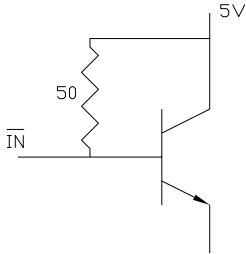

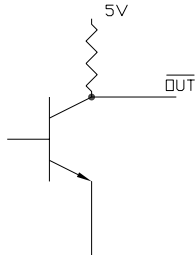
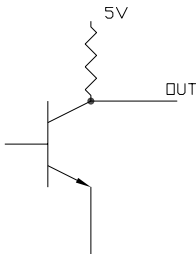
### Outline Drawing



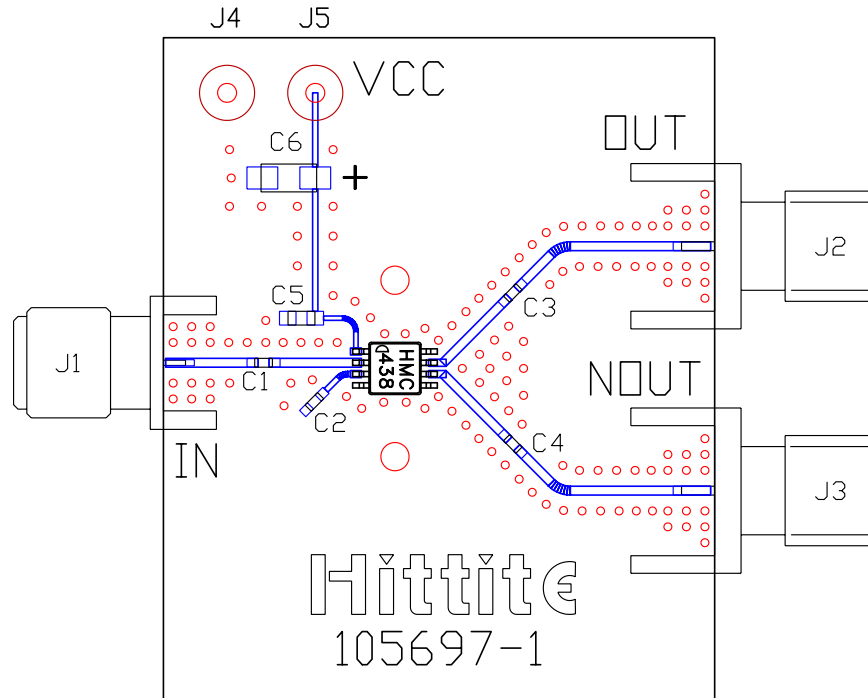
NOTES:

1. PACKAGE BODY MATERIAL: LOW STRESS INJECTION MOLDED PLASTIC SILICA AND SILICON IMPREGNATED.
2. LEADFRAME MATERIAL: COPPER ALLOY
3. LEADFRAME PLATING: Sn/Pb SOLDER
4. DIMENSIONS ARE IN INCHES [MILLIMETERS].
5. DIMENSION DOES NOT INCLUDE MOLDFLASH OF 0.15mm PER SIDE.
6. DIMENSION DOES NOT INCLUDE MOLDFLASH OF 0.25mm PER SIDE.
7. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.

### Pin Description

| Pin Number | Function                | Description   | Interface Schematic   |
|------------|-------------------------|---|---|
| 1          | Vcc                     | Supply voltage 5V ± 0.25V.  |   |
| 2          | IN                      | RF input must be DC blocked.  |    |
| 3          | $\overline{\text{IN}}$  | RF input 180° out of phase with pin 2 for differential operation. AC ground for single ended operation. |   |
| 4, 5       | GND                     | All ground leads and ground paddle must be soldered to PCB RF/DC ground.                                |  |
| 6          | $\overline{\text{OUT}}$ | Divided output 180° out of phase with pin 7.  |  |
| 7          | OUT                     | Divided Output.   |  |
| 8          | N/C                     | No Connection   |   |

### Evaluation PCB



### List of Materials

| Item                                  | Description                    |
|---------------------------------------|--------------------------------|
| J1 - J3                               | PC Mount SMA RF Connector      |
| J4, J5                                | DC Pin                         |
| C1 - C4                               | 100 pF Capacitor, 0402 Pkg.    |
| C5                                    | 10,000 pF Capacitor, 0603 Pkg. |
| C6                                    | 4.7 µF Tantalum Capacitor      |
| U1                                    | HMC438MS8G Divide-by-5         |
| PCB*                                  | 105697 Eval Board              |
| * Circuit Board Material: Rogers 4350 |                                |

The circuit board used in the final application should use RF circuit design techniques. Signal lines should have 50 ohm impedance while the package ground leads and backside ground slug should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request. This evaluation board is designed for single ended input testing. J2 and J3 provide differential output signals.

### Application Circuit

