# Low-Voltage, Low $R_{ON}$, Single SPDT Analog Switch.

## DESCRIPTION

The PA2011 is a low on-resistance, single-pole double- throw monolithic CMOS analog switch. It is designed for low voltage applications with guaranteed operation at 2 V.

The PA2011 is ideal for portable and battery powered equipment, requiring high performance and efficient use of board space. In additional to the low on-resistance (1.8 Ω at 2.7 V), charge injection is less than 10 pC over the entire analog range.

The switch conducts equally well in both directions when on, and blocks up to the power supply level when off.

Break-before-make is guaranteed.

## FEATURES

- Low Voltage Operation (1.8 V to 3.3 V)
- Low On-Resistance - $r_{ON}$: 1.8 Ω at 2.7 V
- Low Charge Injection
- Low Voltage Logic Compatible
- SC-89 Package (1.6 x 1.6 mm)

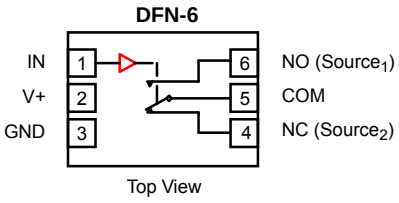
## BENEFITS

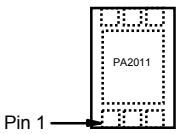
- Reduced Power Consumption
- Simple Logic Interface
- High Accuracy
- Reduce Board Space
- Guaranteed 2 V Operation

## APPLICATIONS

- Cellular Phones
- Communication Systems
- Portable Test Equipment
- Battery Operated Systems
- Sample and Hold Circuits
- ADC and DAC Applications

## FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION




Device Marking: PA2011
xx Date Code

**TRUTH TABLE**

| Logic | NC | NO |
|---|---|---|
| 0 | ON | OFF |
| 1 | OFF | ON |

**ORDERING INFORMATION**

| Temp Range | Package | Part Number |
|---|---|---|
| - 40 to 85 °C | SC-89<br>Tape and Reel | PA2011- T7 |
| | SC-89<br>Lead (Pb)-free with<br>Tape and Reel | PA2011-LF<br>PA2011-LF-T7 |

## ABSOLUTE MAXIMUM RATINGS $T_A$ = 25 °C, unless otherwise noted

| Parameter | | Symbol | Limit | Unit |
|---|---|---|---|---|
| Reference V+ to GND | | | - 0.3 to + 3.3 | V |
| IN, COM, NC, NO[1] | | | - 0.3 to (V+ + 0.3 V) | |
| Continuous Current (NO, NC, COM pins) | | | ± 150 | mA |
| Peak Current (Pulsed at 1 ms, 10 % duty cycle) | | | ± 300 | |
| Storage Temperature | D Suffix | | - 65 to 150 | °C |
| Power Dissipation (Packages)[2] | SC-89[3] | | 172 | mW |

Notes:
1. Signals on NC, NO, or COM or IN exceeding V+ will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
2. All leads welded or soldered to PC Board.
3. Derate 2.15 mW/°C above 70°C.

## SPECIFICATIONS (V+ = 2.0 V)

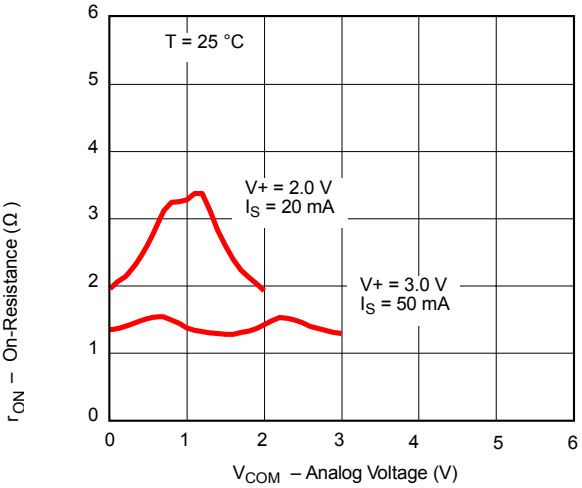
| Parameter | Symbol | Test Conditions Otherwise Unless Specified V+ = 2.0 V, $V_{IN}$ = 0.4 V or 1.6 V[5] | Temp[1] | Limits - 40 to 85 °C Min[2] | Typ[3] | Max[2] | Unit |
|---|---|---|---|---|---|---|---|
| **Analog Switch** | | | | | | | |
| Analog Signal Range[4] | $V_{NO}$, $V_{NC}$, $V_{COM}$ | | Full | 0 | | V+ | V |
| On-Resistance | $r_{ON}$ | V+ = 2.0 V, $V_{COM}$ = 0.2 V/0.9 V<br>$I_{NO}$, $I_{NC}$ = 20 mA | Room<br>Full | | 3.5 | 5.5<br>5.5 | Ω |
| Switch Off Leakage Current[5] | $I_{NO(off)}$<br>$I_{NC(off)}$ | V+ = 2.2 V,<br>$V_{NO}$, $V_{NC}$= 0.5 V/1.5 V, $V_{COM}$ = 1.5 V/0.5 V | Room<br>Full | - 1<br>- 10 | | 1<br>10 | nA |
| | $I_{COM(off)}$ | | Room<br>Full | - 1<br>- 10 | | 1<br>10 | |
| Channel-On Leakage Current[6] | $I_{COM(on)}$ | V+ = 2.2 V, $V_{NO}$, $V_{NC}$ = $V_{COM}$ = 0.5 V/1.5 V | Room | - 1<br>- 10 | | 1<br>10 | |
| **Digital Control** | | | | | | | |
| Input High Voltage | $V_{INH}$ | | Full | 1.5 | | | V |
| Input Low Voltage | $V_{INL}$ | | Full | | | 0.4 | |
| Input Capacitance | $C_{in}$ | | Full | | 4 | | pF |
| Input Current | $I_{INL}$ or $I_{INH}$ | $V_{IN}$ = 0 or V+ | Full | 1 | | 1 | µA |
| **Dynamic Characteristics** | | | | | | | |
| Turn-On Time | $t_{ON}$ | $V_{NO}$ or $V_{NC}$ = 1.5 V, $R_L$ = 300 Ω, $C_L$ = 35 pF | Room<br>Full | | 25 | 36<br>40 | ns |
| Turn-Off Time | $t_{OFF}$ | | Room<br>Full | | 10 | 15<br>16 | |
| Break-Before-Make Time | $t_{BBM}$ | | Room | 9 | 15 | | |
| Charge Injection[4] | $Q_{INJ}$ | $C_L$ = 1 nF, $V_{GEN}$ = 0 V, $R_{GEN}$ = 0 Ω | Room | | 7 | | pC |
| Off-Isolation[4] | OIRR | $R_L$ = 50 Ω, $C_L$ = 5 pF, f = 1 MHz | Room | | - 113 | | dB |
| Crosstalk[4] | $X_{TALK}$ | | Room | | - 112 | | |
| $N_O$, $N_C$ Off Capacitance[4] | $C_{NO(off)}$<br>$C_{NC(off)}$ | $V_{IN}$ = 0 or V+, f = 1 MHz | Room | | 26 | | pF |
| Channel-On Capacitance[4] | $C_{ON}$ | | Room | | 85 | | |
| **Power Supply** | | | | | | | |
| Positive Supply Range | V+ | $V_{IN}$ = 0 or V+ | | 1.8 | | 3.3 | V |
| Negative Supply Current | I+ | | | | 0.01 | 1.0 | µA |

## SPECIFICATIONS (V+ = 3 V)

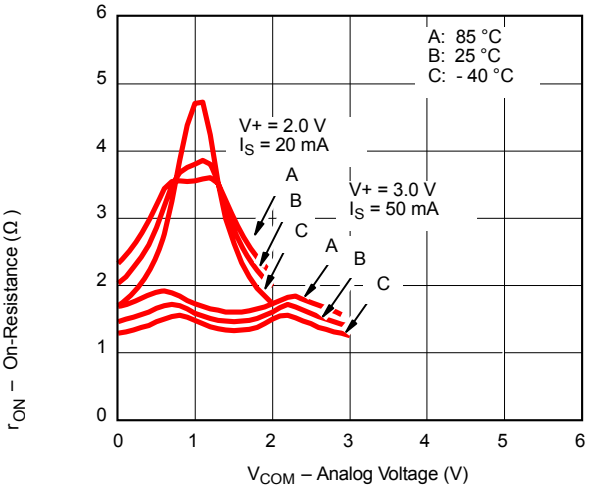
| Parameter | Symbol | Test Conditions Otherwise Unless Specified V+ = 3 V, ±10 %, $V_{IN}$ = 0.4 V or 2.0 V[5] | Temp[1] | Limits –40 to 85 °C Min[2] | Typ[3] | Max[2] | Unit |
|---|---|---|---|---|---|---|---|
| **Analog Switch** | | | | | | | |
| Analog Signal Range[4] | $V_{NO}$, $V_{NC}$, $V_{COM}$ | | Full | 0 | | V+ | V |
| On-Resistance | $r_{ON}$ | V+ = 2.7 V, $V_{COM}$ = 0.9 V/1.5 V $I_{NO}$, $I_{NC}$= 50 mA | Room<br>Full | | 1.8 | 2.7<br>2.9 | Ω |
| $r_{ON}$ Match | $\Delta r_{ON}$ | | Room | | | 0.2 | |
| $r_{ON}$ Flatness | $r_{ON}$ Flatness | | Room | | 0.2 | 0.5 | |
| Switch Off Leakage Current | $I_{NO(off)}$<br>$I_{NC(off)}$ | V+ = 3.3 V, $V_{NO}$, $V_{NC}$= 1 V/3 V, $V_{COM}$ = 3 V/1 V | Room<br>Full | - 1<br>- 10 | | 1<br>10 | nA |
| | $I_{COM(off)}$ | | Room<br>Full | - 1<br>- 10 | | 1<br>10 | |
| Channel-On Leakage Current[6] | $I_{COM(on)}$ | V+ = 3.3 V, $V_{NO}$, $V_{NC}$ = $V_{COM}$ = 1 V/3 V | Room | - 1<br>- 10 | | 1<br>10 | |
| **Digital Control** | | | | | | | |
| Input High Voltage | $V_{INH}$ | | Full | 1.6 | | | V |
| Input Low Voltage | $V_{INL}$ | | Full | | | 0.4 | |
| Input Capacitance | $C_{in}$ | | Full | | 4 | | pF |
| Input Current | $I_{INL}$ or $I_{INH}$ | $V_{IN}$ = 0 or V+ | Full | 1 | | 1 | µA |
| **Dynamic Characteristics** | | | | | | | |
| Turn-On Time | $t_{ON}$ | $V_{NO}$ or $V_{NC}$ = 2.0 V, $R_L$ = 300 Ω, $C_L$ = 35 pF | Room<br>Full | | 16 | 24<br>27 | ns |
| Turn-Off Time | $t_{OFF}$ | | Room<br>Full | | 7 | 9<br>16 | |
| Break-Before-Make Time | $t_{BBM}$ | | Room | 7 | 9 | | |
| Charge Injection[4] | $Q_{INJ}$ | $C_L$ = 1 nF, $V_{GEN}$ = 0 V, $R_{GEN}$ = 0 Ω | Room | | 2 | | pC |
| Off-Isolation[4] | OIRR | $R_L$ = 50 Ω, $C_L$ = 5 pF, f = 1 MHz | Room | | - 107 | | dB |
| Crosstalk[4] | $X_{TALK}$ | | Room | | - 107 | | |
| $N_O$, $N_C$ Off Capacitance[4] | $C_{NO(off)}$<br>$C_{NC(off)}$ | $V_{IN}$ = 0 or V+, f = 1 MHz | Room | | 26 | | pF |
| Channel-On Capacitance[4] | $C_{ON}$ | | Room | | 84 | | |
| **Power Supply** | | | | | | | |
| Power Supply Range | V+ | | | 1.8 | | 3.3 | V |
| Power Supply Current | I+ | $V_{IN}$ = 0 or V+ | | | 0.01 | 1.0 | µA |
| Power Consumption | $P_C$ | | | | | 3.3 | µW |

Notes:
1. Room = 25 °C, Full = as determined by the operating suffix.
2. Typical values are for design aid only, not guaranteed nor subject to production testing.
3. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
4. Guarantee by design, nor subjected to production test.
5. $V_{IN}$ = input voltage to perform proper function.
6. Guaranteed by 3.3V leakage testing, not production tested.

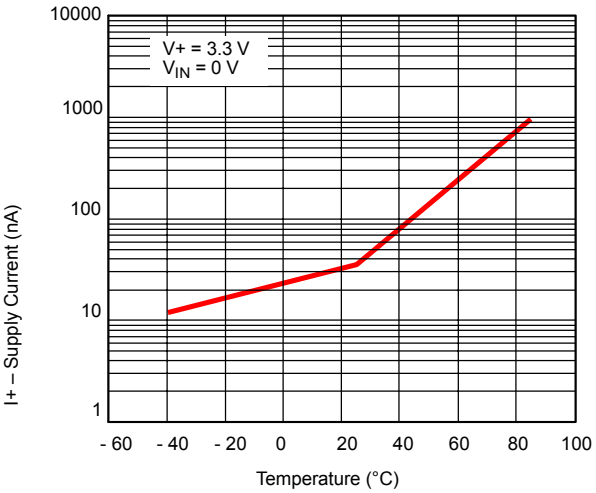
## TYPICAL CHARACTERISTICS $T_A$ = 25 °C, unless otherwise noted



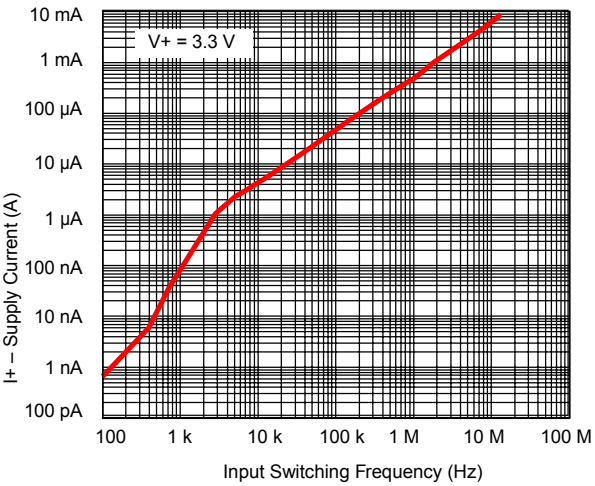

**$r_{ON}$ vs. $V_{COM}$ and Supply Voltage**



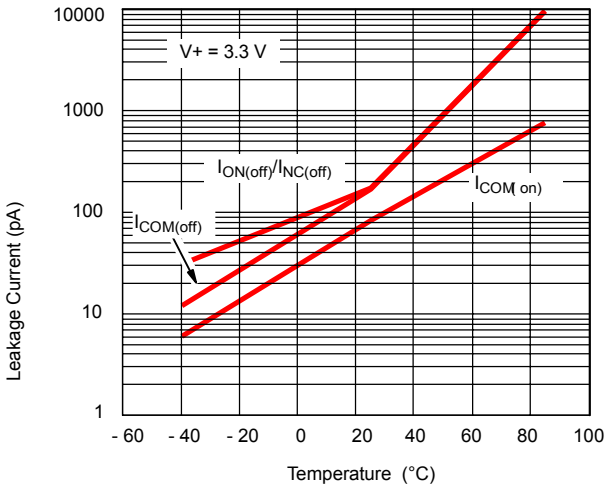

**$r_{ON}$ vs. Analog Voltage and Temperature**



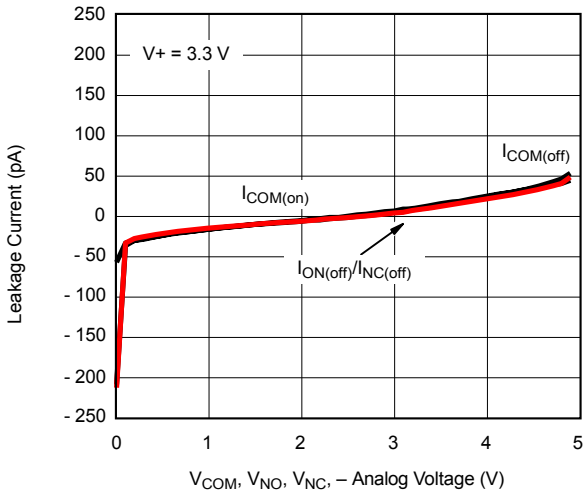

**Supply Current vs. Temperature**




**Supply Current vs. Input Switching Frequency**

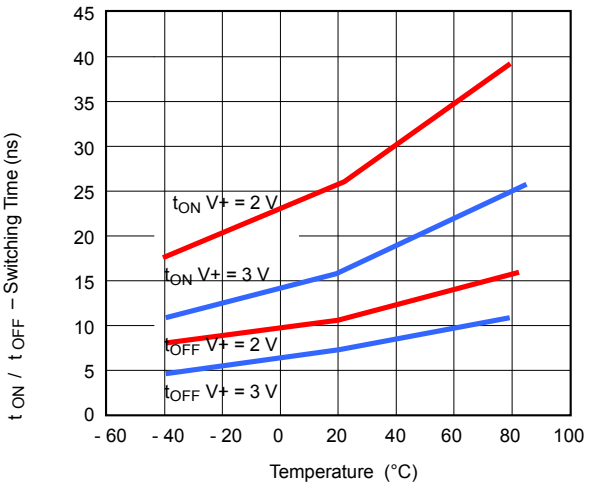



**Leakage Current vs. Temperature**

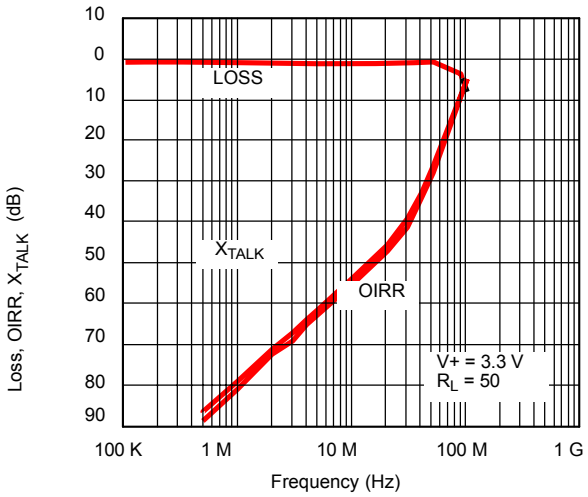



**Leakage vs. Analog Voltage**

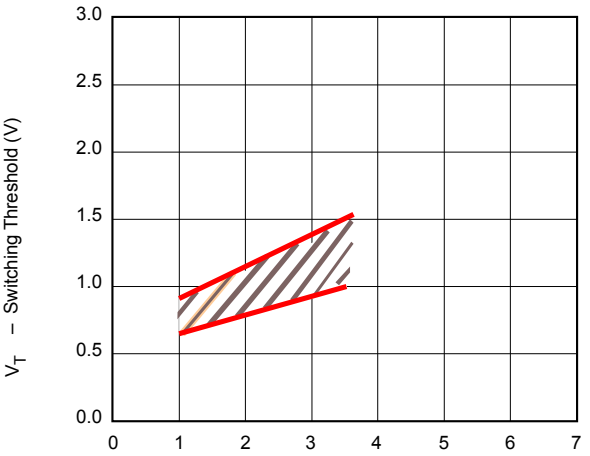
## TYPICAL CHARACTERISTICS $T_A$ = 25 °C, unless otherwise noted



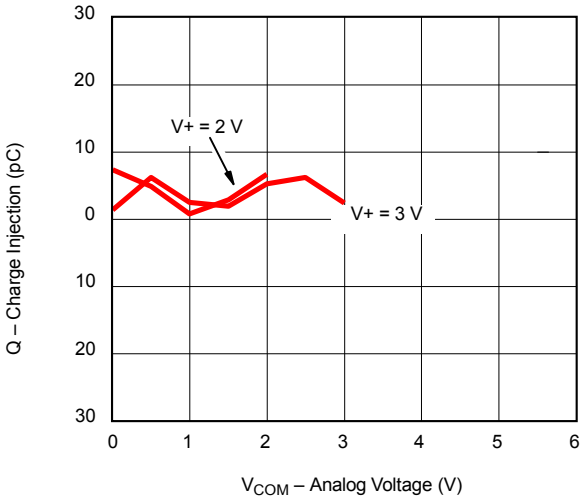

**Switching Time vs. Temperature and Supply Voltage**




**Insertion Loss, Off-Isolation, Crosstalk vs.Frequency**

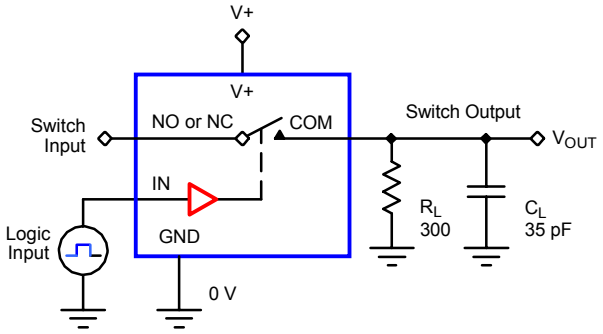



**Switching Threshold vs. Supply Voltage**



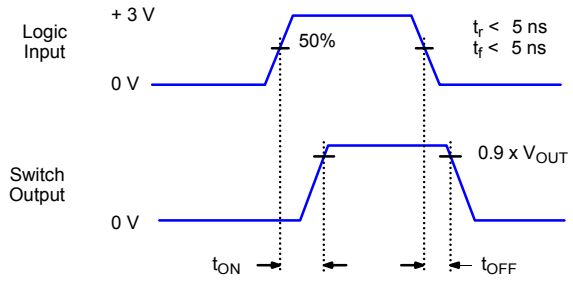

**Charge Injection vs. Analog Voltage**

## TEST CIRCUITS



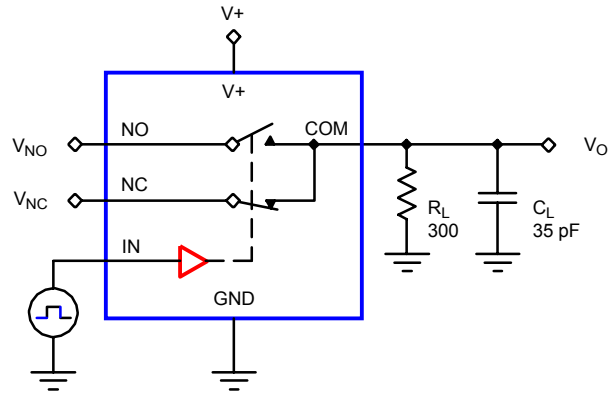

$C_L$ (includes fixture and stray capacitance)

$$V_{OUT} = V_{COM}\left(\frac{R_L}{R_L + R_{ON}}\right)$$




Logic "1" = Switch On
Logic input waveforms inverted for switches that have the opposite logic sense.

**Figure 1. Switching Time**




$C_L$ (includes fixture and stray capacitance)

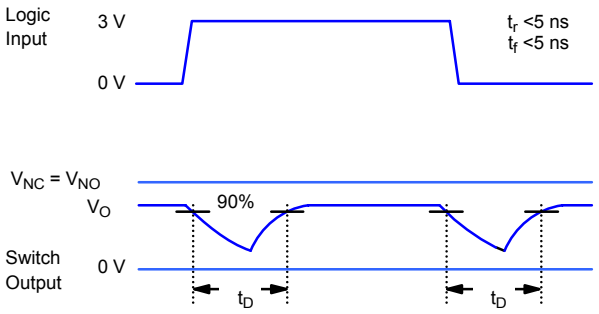
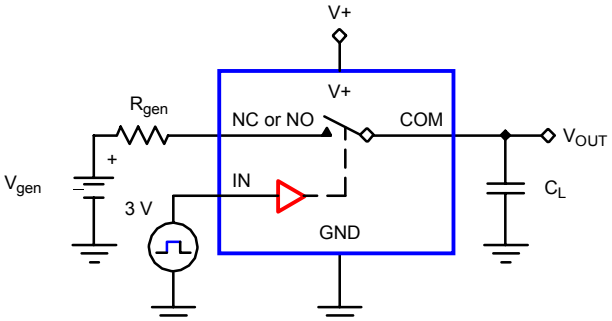
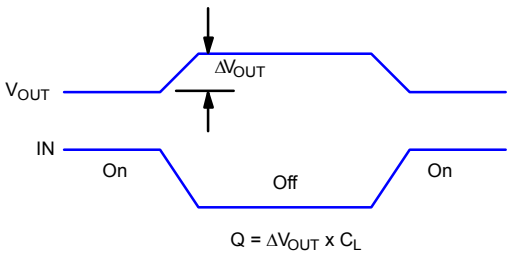



**Figure 2. Break-Before-Make Interval**




$Q = \Delta V_{OUT} \times C_L$

**Figure 3. Charge Injection**

IN depends on switch configuration: input polarity determined by sense of switch.

## TEST CIRCUITS

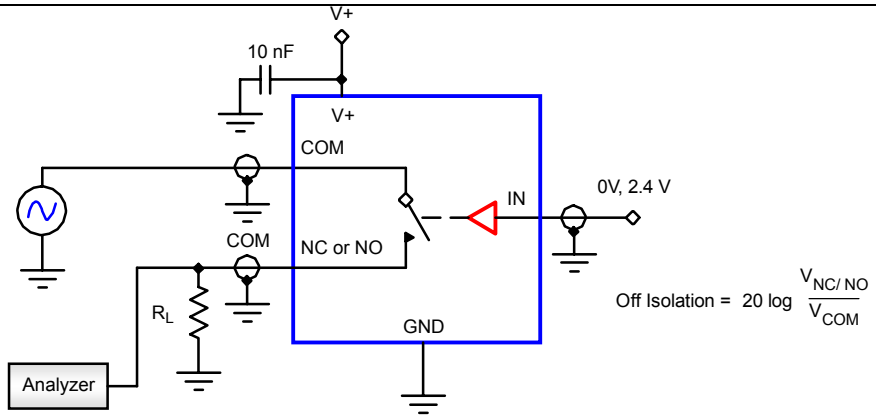



**Figure 4. Off-Isolation**

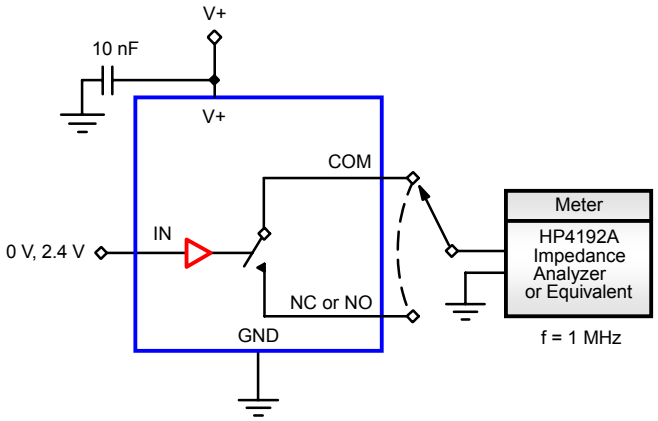



**Figure 5. Channel Off/On Capacitance**

## TYPICAL APPLICATIONS