Telmos
TELMOS INC.

TMD54HCT373/TMD74HCT373
3 STATE OCTAL LATCHES
TMD54HCT374/TMD74HCT374
3 STATE OCTAL D-FLIP-FLOPS

Features

- TTL INPUT COMPATIBLE
- 15 NS PROPOGATION DELAY TYP.
- 1 μA MAX. INPUT CURRENT
- DRIVES 30 LS-TTL LOADS
- FULL PARALLEL LOAD ACCESS
- 3 STATE BUS-DRIVING OUTPUTS
- CLOCK/ENABLE INPUT HAS HYSTERESIS TO IMPROVE NOISE REJECTION
- MEETS OR EXCEEDS JEDEC STANDARD NUMBER 7

Description

The 373 and 374 series octal latches and flip-flops use a 3 micron silicon gate P-well CMOS process. They are the ideal CMOS replacement for low power schottky with the ability to drive 30 LS-TTL loads in addition to possessing high noise immunity and low power consumption. These devices are ideally suited for interfacing with bus lines in a bus organized system. These 8 bit registers feature three-state outputs designed specifically for driving high capacitive or relatively low impedance loads. When driving a bus no interface or pull-up resistors are required.

When the LATCH ENABLE input of the 373HCT series is high, the Q outputs will follow the D inputs. When the LATCH ENABLE goes low, data at the D inputs will be retained at the outputs until LATCH ENABLE returns high again. When a high logic level is applied to the OUTPUT CONTROL input, all outputs go to a high impedance state.

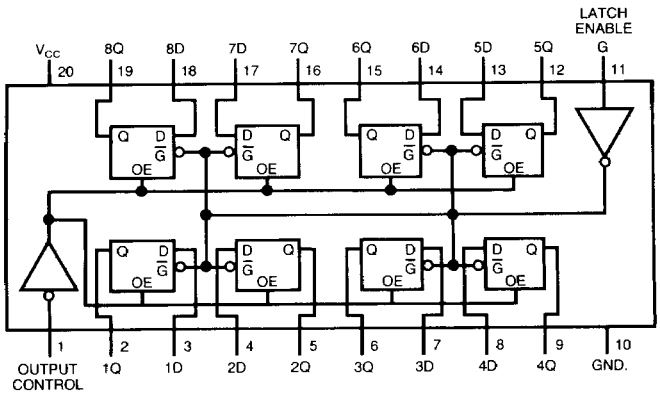
The 374HCT series are positive edge triggered flip-flops. Data at the D inputs, meeting the setup and hold time requirements, is transferred to the Q outputs on positive going transitions of the clock (CK) input. Application of a high level to the OUTPUT CONTROL (OC) input causes all outputs to go to a high impedance state.

Schmitt-trigger buffered inputs at the enable/clock lines simplify system design as AC and DC noise rejection is improved by typically 300 millivolts due to input hysteresis.

This 54HCT/74HCT family is pinout, function and speed compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal clamps to V_{CC} and ground.

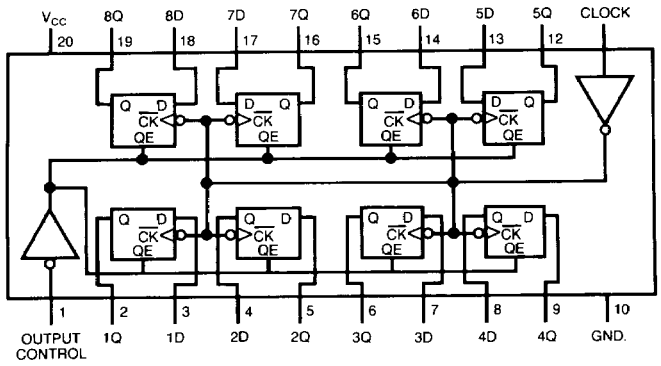
All unused inputs must be connected to an appropriate logic voltage level (either V_{CC} or GND).

Connection Diagram



TMD54HCT373
TMD74HCT373

Connection Diagram



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Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 +7.0V
DC Input Voltage (V_{IN})	− .5 to V_{CC} + .5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} + 0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±50 mA
DC Output Current, per pin (I_{OUT})	±50 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±100 mA
Latch up current	±100 mA
Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temperature Range (T_A)			
74HCT	−40	+85	°C
54HCT	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics

V_{CC} = 5V ±10% (unless otherwise specified)

Symbol	Parameter	Conditions	T_A = 25°C	74HCT T_A −40 to 85°C	54HCT T_A = −55 to 125°	Units
			Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\|$ = 20 μA	V_{CC}	V_{CC}−0.1	V_{CC}−0.1	V_{CC}−0.1	V
		$\|I_{OUT}\|$ = 6.0 mA, V_{CC} = 4.5V	4.3V	4.0	3.9	3.8	V
		$\|I_{OUT}\|$ = 15 mA, V_{CC} = 4.5V	4.0	3.7	3.5	3.3	V
V_{OL}	Maximum Low Level Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\|$ = 20 μA	0	0.1	0.1	0.1	V
		$\|I_{OUT}\|$ = 12 mA,	0.2	0.4	0.4	0.4	V
		$\|I_{OUT}\|$ = 24 mA,	0.3	0.5	0.5	—	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum 3-STATE Output Leakage Current	V_{OUT} = V_{CC} or GND Enable = V_{IH} or VIL		±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation Temperature derating-plastic package: − 12mW/°C from 65°C to 85°C; cerdip package: −12mW/°C from 100°C to 125°C.

AC Electrical Characteristics TMD54HCT373/TMD74HCT373

V_{CC} = 4.5V. $t_r = t_f$ = 6ns (unless otherwise specified) (see note 4)

Symbol	Parameter	Conditions	T_A = 25°C	74HCT T_A = −40 to 85°C	54HCT T_A = −55 to 125°C		Units
			Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay Data to Output	C_L = 50pF C_L = 150pF	13 19	20 26	25 33	28 37	ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Latch Enable to Output	C_L = 50pF C_L = 150pF	15 20	25 33	30 40	33 44	ns ns
t_{PZH}, t_{PZL}	Maximum Enable Propagation Delay Control to Output	C_L = 50pF C_L = 150pF R_L = 1 kΩ	14 19	24 32	29 39	33 44	ns ns
t_{PHZ}, t_{PLZ}	Maximum Disable Propagation Delay Control to Output	C_L = 50 pF R_L = 1 kΩ	23	30	34	37	ns
t_W	Minimum Clock Pulse Width			15	19	23	ns
t_S	Minimum Setup Time Data to Clock			0			ns
t_H	Minimum Hold Time Clock to Data			10	13	15	ns
C_{IN}	Maximum Input Capacitance		5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance		10	20	20	20	pF

AC Electrical Characteristics TMD54HCT374/TMD74HCT374

V_{CC} = 4.5V. $t_r = t_f$ = 6ns (unless otherwise specified) (see note 4)

Symbol	Parameter	Conditions	T_A = 25°C	74HCT T_A = −40 to 85°C	54HCT T_A = −55 to 125°C		Units
			Typ	Guaranteed Limits			
f_{MAX}	Maximum Clock Frequency			35	30	25	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock to Output	C_L = 50pF C_L = 150pF	15 20	26 35	31 41	34 45	ns ns
t_{PZH}, t_{PZL}	Maximum Enable Propagation Delay Control to Output	C_L = 50pF C_L = 150pF R_L = 1 kΩ	14 19	24 32	29 39	33 44	ns ns
t_{PHZ}, t_{PLZ}	Maximum Disable Propagation Delay Control to Output	C_L = 50 pF R_L = 1 kΩ	23	30	34	37	ns
t_W	Minimum Clock Pulse Width			14	17	20	ns
t_S	Minimum Setup Time Data to Clock			20	24	28	ns
t_H	Minimum Hold Time Clock to Data			0			ns
C_{IN}	Maximum Input Capacitance		5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance		10	20	20	20	pF

Note 4 Refer to JEDEC standard No. 7 for AC switching waveforms and test circuits.

Truth Tables '373

Output Control	Enable G	Data	373 Output	573 Output
L	H	H	H	L
L	H	L	L	H
L	L	X	Q_0	Q_0
H	X	X	Z	Z

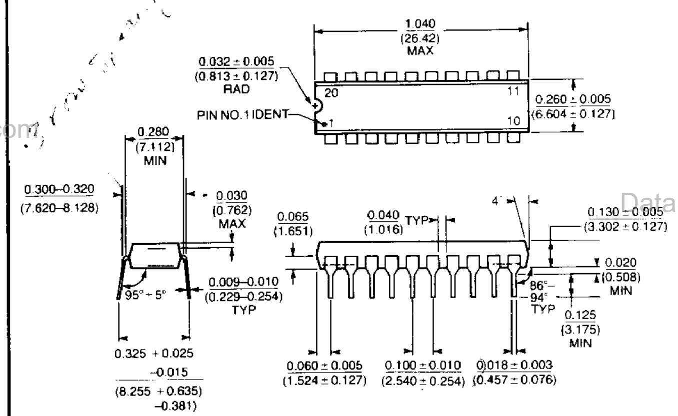
H = high level, L = low level
Q_0 = level of output before steady-state input conditions were established.
Z = high impedance

'374

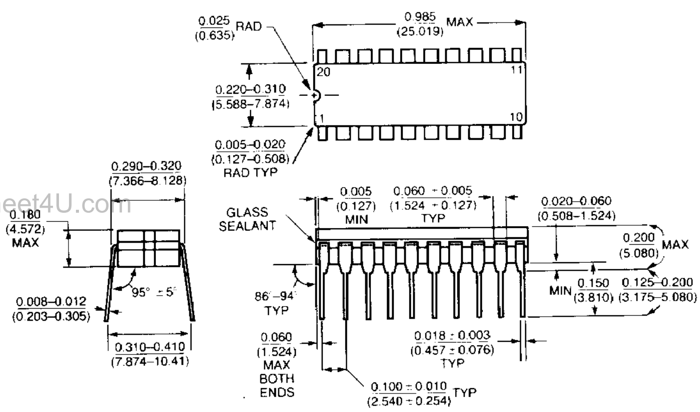
Output Control	Clock	Data	(374) Output	(534) Output
L	↑	H	H	L
L	↑	L	L	H
L	L	X	Q_0	Q_0
H	X	X	Z	Z

H = High Level, L = Low Level
X = Don't Care
↑ = Transition from low-to-high
Q_0 = The level of the output before steady state input conditions were established.

List Elem. 17



20-Pin Plastic



20-Pin Cerdip

All dimensions in inches (millimeters)

Ordering Information

RANGE	PART NUMBER	TYPE	PACKAGE
INDUSTRIAL TEMP. RANGE	TMD74HCT373	OCTAL LATCH	20 PIN PLASTIC
	TMD74HCT374	FLIP-FLOP	20 PIN PLASTIC
MILITARY TEMP. RANGE	TMD54HCT373	OCTAL LATCH	20 PIN CERDIP
	TMD54HCT374	FLIP-FLOP	20 PIN CERDIP

Cerdip order BE suffix } per TELMOS 5/22/84

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