STAF Device
SONET/SDH Transceiver and Framer
622/155.5 Mbit/s
TXC-02623
DATA SHEET
Preliminary

FEATURES

- Byte-parallel multiplexing, demultiplexing, framing, and clock synthesis PLL in one device
- Choice of STS-12/STM-4 or STS-3/STM-1 transmission rates
- Configurable master or slave reference clock generation by PLL, or bypass for external clock
- Two versions of device to accommodate either of two reference clock input frequencies for the master clock: 51.84 MHz for the "A" version device or 38.88 MHz for the "B" version device
- External RC loop filter
- Pass-through mode and three loopback modes for enhanced field diagnostics
- Frame-synchronous and byte-aligned demultiplexer output, according to SONET/SDH framing standards
- Search, detect, and recovery of framing on out-of-frame (OOF) input
- Standard TTL and differential or single-ended ECL I/O (except TXCK is single-ended only)
- Tri-state TTL output for factory circuit-board testability
- 68-pin surface-mount ceramic quad flat package with integral CuW heat spreader
- Dual power supply operation (+5V and –5.2V)
- Low power dissipation (1.9W nominal)

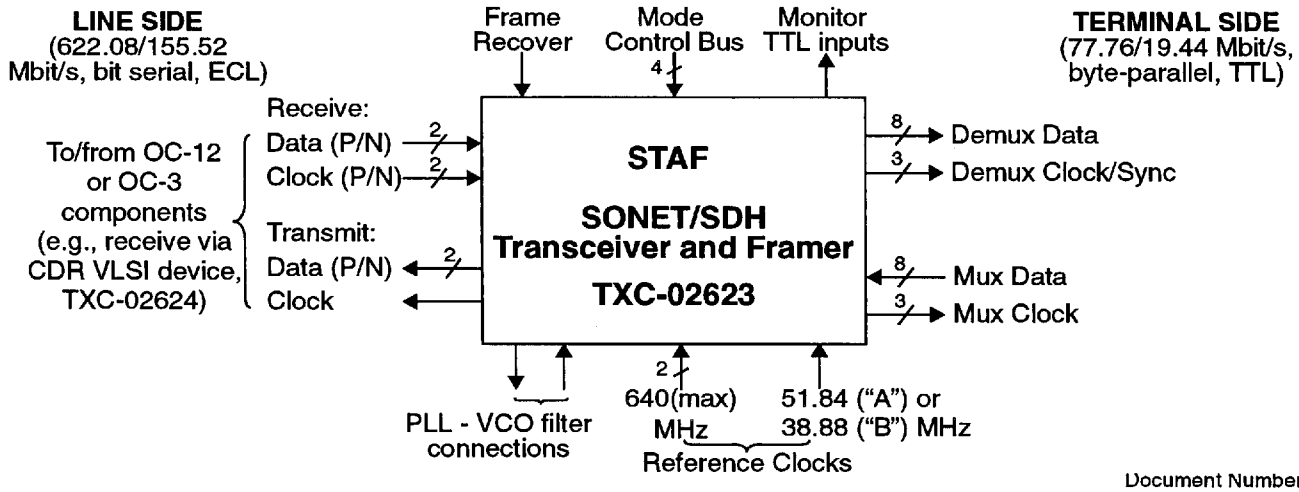
DESCRIPTION

The STAF VLSI device is a SONET/SDH transceiver and framer. It combines multiplexing, demultiplexing, SONET/SDH framing, clock synthesis PLL, and loopback functions in a single monolithic integrated circuit. Implementation with the STAF device requires only a simple external RC loop filter and standard TTL and ECL power supplies. For optimal performance, the STAF device is packaged in a 68-pin multilayer ceramic (MLC) surface-mount package with an integral heat spreader. The STAF device provides physical interfaces for STS-12/STM-4 (622.08 Mbit/s) or STS-3/STM-1 (155.52 Mbit/s) SONET/SDH systems.

The STAF device meets ANSI, Bellcore, and ITU requirements for a SONET/SDH device. The phase-locked loop (PLL) provides 77.76 MHz or 19.44 MHz output for the multiplexer and 77.76 MHz or 19.44 MHz and 51.84 MHz for the demultiplexer. In Master mode, the PLL uses a reference clock input at 51.84 MHz (for the "A" version) or 38.88 MHz (for the "B" version).

APPLICATIONS

- Transmission system transport cards
- Switch and cross-connect line cards
- Repeaters
- ATM physical layer interfaces
- Test equipment
- Add/drop multiplexers



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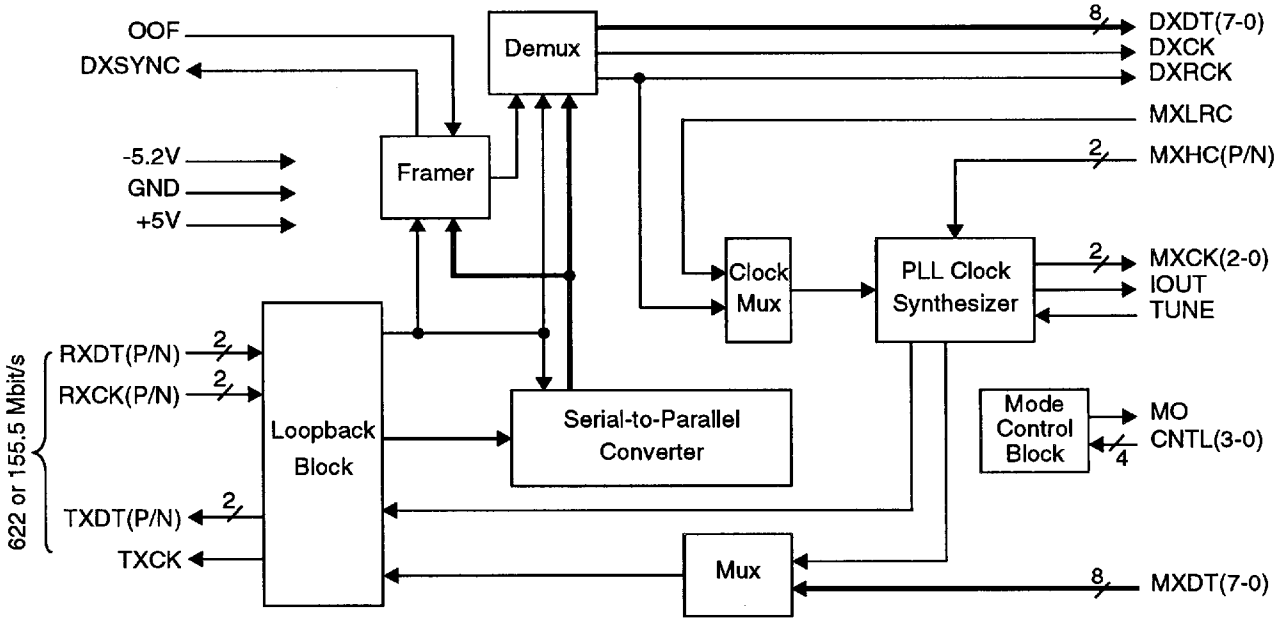
BLOCK DIAGRAM



Notes:
1. Thick lines represent byte-parallel data paths.
2. TUNE and IOUT are typically joined and connected to V_{EE} via 600Ω in series with 0.68µF.

Figure 1. STAF TXC-02623 Block Diagram

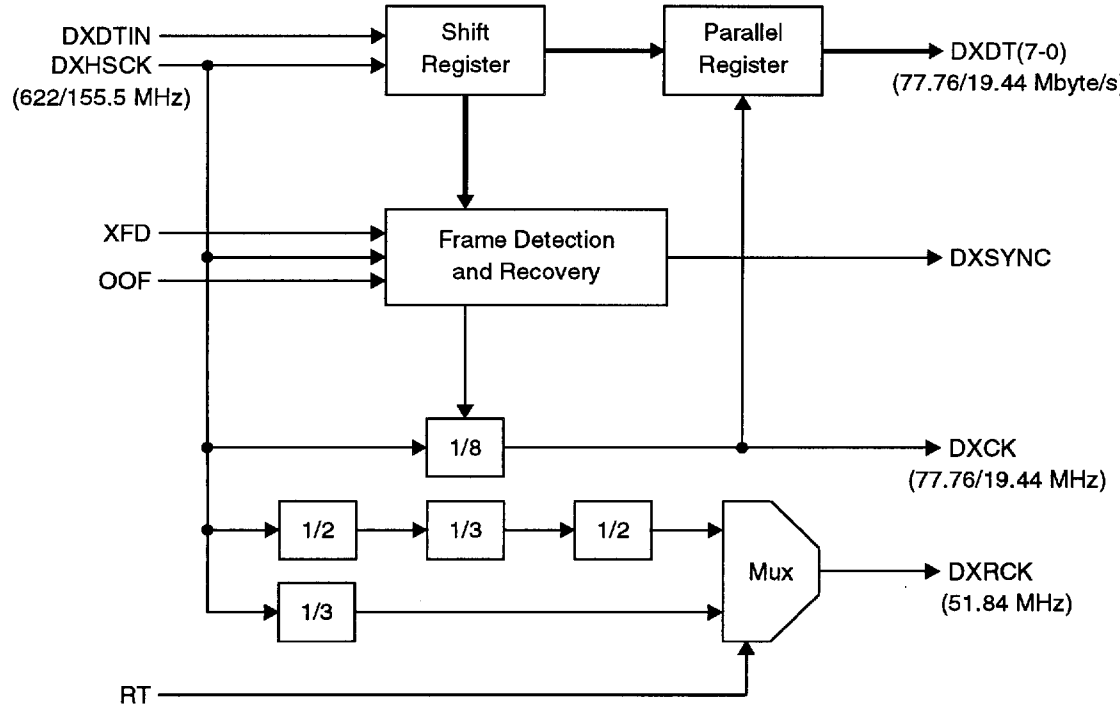
BLOCK DIAGRAM DESCRIPTION

The block diagram in Figure 1 shows the demultiplexer (with serial-to-parallel converter), framer, PLL clock synthesizer, multiplexer, mode control and loopback blocks of the STAF device, which are described below. Additional information is provided in the Pin Descriptions, Timing Characteristics and Operation sections. These blocks work together to integrate the conversion of serial and parallel SONET/SDH data with bit alignment and clock synthesis in a single device.

DEMULTIPLEXER

The receive side functions are shown in more detail in Figure 2, which includes signals internal to the device. The demultiplexer block converts incoming serial data on DXDTIN. Byte-parallel output data is presented on DXDT(7-0) shortly after the falling edge of the output demultiplexer clock, DXCK (see Figure 5).

The demultiplexer block also includes clock divider circuitry for the line-rate clock DXHSCK, which is used by the demultiplexer to provide a divide-by-8 output on DXCK. The STAF device also provides a divide-by-3 or divide-by-12 output, DXRCK (51.84 MHz), under the control of pins CNTL(3-0), as described in Figure 8.



Note: Thick lines represent byte-parallel data paths.

Figure 2. Receive Side Functions

FRAMER

The demultiplexer block operates in conjunction with a framer block that contains the frame detection and recovery circuit. Regardless of the state of the OOF input signal, this framer block takes DXSYNC high for one period of DXCK whenever it detects a pattern of three A1 bytes followed by three A2 bytes (see Figure 6).

Frame recovery is initiated by the rising edge of the OOF input signal. The recovery process involves a search for a bit rotation that satisfies the three-A1–three-A2 byte pattern specified for SONET/SDH. Once the pattern is found, DXSYNC goes high and the bit rotation is synchronized to the correct byte boundaries. No further byte boundary adjustments are made, regardless of A1-A2 indication, unless they have been preceded by an OOF rising edge.

PLL CLOCK SYNTHESIZER

The phase-locked loop (PLL) utilizes a monolithic voltage-controlled oscillator (VCO), with a typical tuning constant of 50 to 100 MHz per volt on the TUNE input, to generate a synthesized clock. This configuration provides jitter performance superior to other technologies. In a typical SONET/SDH application, the TUNE input of the VCO is connected to the charge pump output IOUT of the PLL, with a serial R-C link to V_{EE} (600 ohms in series with 0.68 microfarads).

MULTIPLEXER

Byte-parallel input data on MXDT(7-0) is continuously strobed into the multiplexer on the rising edge of the triplicated multiplexer clock output, MXCK(2-0), as shown in Figure 4. Any of these three MXCK pins may be used as a reference point for relative timing. MXCK nominally runs at one-eighth of the serial rate on the line side.

Either the on-chip synthesized line-rate clock or an external high-speed multiplexer clock, MXHC(P/N), serializes the input data bytes. In the normal mode of operation, the serial data is then buffered as ECL-compatible differential outputs on TXDT(P/N). A single-ended ECL output is provided for the transmit clock, TXCK.

MODE CONTROL

The signals on pins CNTL(3-0) are used to control the clock rate, clock modes, loopback modes, testing of TTL input pins, tri-state setting of TTL output pins, disabling of frame recovery, and device reset. In one of the two clock modes, the internal PLL high-speed clock may be disabled, allowing an external clock source to be used on the MXHCP and MXHCN pins. The other clock mode selects the reference clock source used by the PLL. It should be noted that device reset does not initiate frame search, which is activated only by a rising edge on input pin OOF. The sixteen control states are described in the Operation section (Figure 8).

LOOPBACK

The STAF device provides three separate loopback modes under control of the CNTL(3-0) pins: equipment, split and facility loopbacks (see Figure 8 and the Loopback subsection below).

PIN DIAGRAM

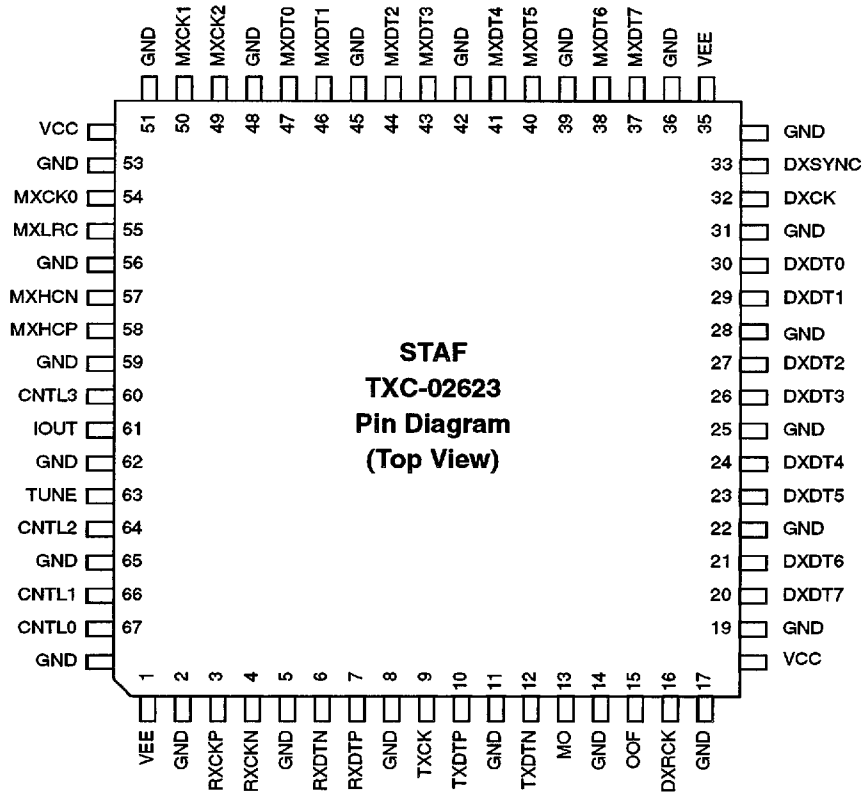


Figure 3. STAF TXC-02623 Pin Diagram

PIN DESCRIPTIONS

POWER SUPPLY AND GROUND

Symbol	Pin No.	I/O/P *	Type	Name/Function
VCC	18, 52	P		V_{CC}: +5 volt supply, +5.0V ± 0.5V. Nominal high level for TTL signals.
VEE	1, 35	P		V_{EE}: -5.2 volt supply, -5.2V ± 0.3V.
GND	2, 5, 8, 11, 14, 17, 19, 22, 25, 28, 31, 34, 36, 39, 42, 45, 48, 51, 53, 56, 59, 62, 65, 68	P		**Ground:** Zero volts reference. Nominal low level for TTL signals.

*Note: I=Input; O=Output; P=Power

LINE SIDE INTERFACE

Symbol	Pin No.	I/O/P	Type *	Name/Function
RXDTP	7	I	ECL	**Receive Data Input-Positive:** Receive bit-serial data input, positive lead of differential input. First bit of received byte is the MSB. See Note 1.
RXDTN	6	I	ECL	**Receive Data Input-Negative:** Receive bit-serial data input, negative lead of differential input. See Note 1.
RXCKP	3	I	ECL	**Receive Clock Input-Positive:** Receive bit-serial clock input, positive lead of differential input. Used by PLL for its slave mode timing. RXDTP and RXDTN are clocked in on the rising edge of RXCKP. See Note 1 and Figure 4.
RXCKN	4	I	ECL	**Receive Clock Input-Negative:** Receive bit-serial clock input, negative lead of differential input. See Note 1.
OOF	15	I	TTL	**Out of Frame:** A rising edge of OOF initiates frame recovery on the receive line side, to re-synchronize DXSYNC.
TXDTP	10	O	ECL	**Transmit Data Output-Positive:** Transmit bit-serial data output, positive lead of differential output. First bit of transmitted byte is the MSB. See Note 1.
TXDTN	12	O	ECL	**Transmit Data Output-Negative:** Transmit bit-serial data output, negative lead of differential output. See Note 1.
TXCK	9	O	ECL	**Transmit Clock Output:** Transmit bit-serial clock output, single-ended output. TXDTP and TXDTN change after the falling edge of this clock. See Figure 5.

*Note: See Input/Output Parameters section below for digital Type definitions.

Note 1: For single-ended ECL applications, the positive pin should be used for the signal lead and the negative pin should be connected via a 50Ω termination resistor to V_{TT} = -2.0V.

TERMINAL SIDE INTERFACE

Symbol	Pin No.	I/O/P	Type	Name/Function
DXDT(7-0)	20, 21, 23, 24, 26, 27, 29, 30	O (tri-state)	TTL	**Demultiplexer Data Output (7-0):** Receive byte-parallel data output, bits 7 to 0. Bit 7 is the MSB. The high level is logic 1.
DXCK	32	O (tri-state)	TTL	**Demultiplexer Clock Output:** Receive byte-rate clock output, 77.76 MHz or 19.44 MHz. DXDT(7-0) change after the falling edge of DXCK. See Figure 5.
DXSYNC	33	O (tri-state)	TTL	**Demultiplexer Synchronization Output:** A high pulse, approximately eight receive line clock cycles in duration, that immediately follows the third A2 byte in the receive data output (see Figure 6).
DXRCK	16	O (tri-state)	TTL	**Demultiplexer Reference Clock Output:** 51.84 MHz clock, derived by dividing line rate by 12 or 3, with 50 pF backplane driving capacity.

Symbol	Pin No.	I/O/P	Type	Name/Function
MXDT(7-0)	37, 38, 40, 41, 43, 44, 46, 47	I	TTL	**Multiplexer Data Input (7-0):** Transmit byte-parallel data input, bits 7-0. Bit 7 is the MSB. The high level is logic 1.
MXCK(2-0)	49, 50, 54	O (tri-state)	TTL	**Multiplexer Clock Output (2-0):** Three identical byte-rate clock outputs. Rising edges are used to clock in MXDT(7-0). Nominal frequency is 77.76 MHz in STS-12/ STM-4 mode or 19.44 MHz in STS-3/STM-1 mode. See Figure 4.

REFERENCE CLOCKS, PLL/VCO LINK, CONTROLS AND TEST OUTPUT

Symbol	Pin No.	I/O/P	Type	Name/Function
MXHCP	58	I	ECL	**Multiplexer High-Speed Reference Clock Input-Positive:** High-speed clock input, 640 MHz maximum, positive lead of differential input. Used for Bypass mode timing instead of PLL-generated clock (Normal mode).
MXHCN	57	I	ECL	**Multiplexer High-Speed Reference Clock Input-Negative:** High-speed clock input, 640 MHz maximum, negative lead of differential input.
MXLRC	55	I	TTL	**Multiplexer Low-Speed Reference Clock Input:** Reference clock input, frequency 51.84 MHz for the "A" version device or 38.88 MHz for the "B" version device. This reference clock is used by the PLL for its Master mode timing.
IOUT	61	O	Analog	**Charge Pump Output:** PLL output. Normally connected to TUNE input of VCO and to VEE via 600 ohms and 0.68 µF in series.
TUNE	63	I	Analog	**VCO Tuning Control Input:** VCO frequency control input. Normally connected to IOUT output of PLL and to VEE via 600 ohms and 0.68 µF in series.
CNTL(3-0)	60, 64, 66, 67	I	TTL	**Control Inputs (3-0):** 16-state control input for clock rate, clock mode, loopback mode, tri-state pins, frame recovery, device reset and NAND-tree test of all other TTL inputs. See Figure 8 for details of operation.
MO	13	O	TTL	**Monitor Output:** Test output pin. Shows result of NAND-gating all TTL input pins except CNTL(3-0), when activated by setting CNTL(3-0) to 2H.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min *	Max *	Unit
+5V power supply voltage	V_{CC}	0.0	+7.0	V
-5.2V power supply voltage	V_{EE}	-7.0	0.0	V
DC input voltage, TTL inputs	V_{IT}	-0.5	V_{CC}+0.5	V
DC input current, TTL inputs	I_{IT}	-1	1	mA
DC input voltage, ECL inputs	V_{IE}	V_{EE}-0.5	+0.5	V
DC input current, ECL inputs	I_{IE}	-1	1	mA
DC output voltage, TTL inputs	V_{OT}	-0.5	V_{CC}+0.5	V
DC output current, TTL inputs	I_{OT}	-	20	mA
DC output voltage, ECL inputs	V_{OE}	V_{EE}-0.5	+0.5	V
DC output current, ECL inputs	I_{OE}	-	40	mA
Continuous power dissipation	P_C		TBD	W
Ambient operating temperature	T_A	0	70	°C
Operating junction temperature	T_J	-55	+150	°C
Storage temperature	T_S	-65	+175	°C
ESD limit, digital I/O		TBD		V
ESD limit, analog I/O		TBD		V

*Note: Operating conditions outside the min-max ranges specified may cause permanent device failure. Exposure to conditions near the min or max limits for extended periods may impair device reliability.

THERMAL CHARACTERISTICS

Parameter	Min	Typ	Max	Unit	Test Conditions
Thermal resistance - junction to ambient		TBD	TBD	°C/W	TBD
Thermal resistance - junction to case		TBD	4	°C/W	TBD

POWER REQUIREMENTS

Parameter	Min	Nom	Max	Unit	Test Conditions
V_{CC}	4.5	5.0	5.5	V	TBD
V_{EE}	-5.5	-5.2	-4.9	V	TBD
I_{CC}		40	55	mA	TBD
I_{EE}		320	420	mA	TBD
P_{CC}		200	303	mW	TBD
P_{EE}		1664	2310	mW	TBD
P_{TOTAL}		1.9	2.6	W	TBD

INPUT/OUTPUT PARAMETERS

Input/Output Parameters For ECL (see Note 1)

Parameter	Symbol	Min	Nom	Max	Unit	Test Conditions
Internal ECL reference	V_{REF}		0,26*V_{EE}		mV	See Note 2.
Common mode voltage	V_{COM}	-1500		-1100	mV	See Note 3.
Differential mode voltage	V_{DIFF}	200		1200	mV	See Note 3.
Input HIGH voltage	V_{IH}	-1100		-400	mV	See Note 4.
Input LOW voltage	V_{IL}	V_{EE}		-1500	mV	
Output HIGH voltage	V_{OH}	-1000		-500	mV	See Note 5.
Output LOW voltage	V_{OL}	V_{TT} -100		-1600	mV	See Note 5.
Input HIGH current	I_{IH}			30	µA	at V_{IH} max.
Input LOW current	I_{IL}	-30			µA	at V_{IL} min.
Output HIGH current	I_{OH}	20	23	30	mA	See Note 6.
Output LOW current	I_{OL}	-2	5	8	mA	See Note 6.
Input capacitance	C_{IN}		3		pF	
Output capacitance	C_{OUT}		3		pF	
ESD breakdown	V_{ESD}	500			V	See Note 7.

Input/Output Parameters For TTL (see Note 1)

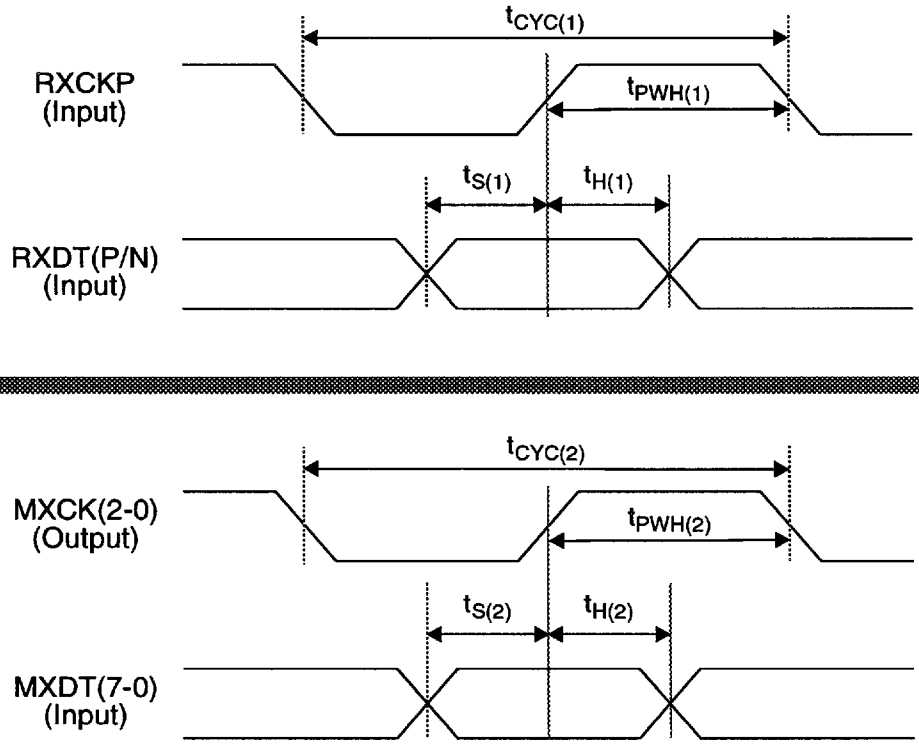
Parameter	Symbol	Min	Nom	Max	Unit	Test Conditions
Input HIGH voltage	V_{IH}	2.0		V_{CC}	V	
Input LOW voltage	V_{IL}	0		0.8	V	
Output HIGH voltage	V_{OH}	2.4	0	V_{CC}	V	I_{OH} = 3mA
Output LOW voltage	V_{OL}	0		0.4	V	I_{OL} = -1mA
Input HIGH current	I_{IH}			100	µA	at V_{IH} max
Input LOW current	I_{IL}	-100			µA	at V_{IL} min
Tri-state current	I_{OZ}	-100		100	µA	
Input capacitance	C_{IN}		8		pF	
Output capacitance	C_{OUT}		10		pF	
ESD breakdown	V_{ESD}	1000			V	See Note 7.

Notes:
1. Applies over specified power supply voltage operating ranges and 0 to 70°C ambient operating temperature range.
2. Single-ended inputs.
3. Differential inputs.
4. V_{REF} =-1300 mV.
5. R_{LOAD} = 50 ohms connected to V_{TT} = -2.0V.
6. Not tested. Consistent with V_{OH} and V_{OL} tests.
7. Design objective.

TIMING CHARACTERISTICS

The input and output signal timing of the STAF device is described in Figures 4 through 7. Values given for timing parameters correspond to operation at the 622 Mbit/s line rate.

Figure 4. Line and Terminal Side Input Timing

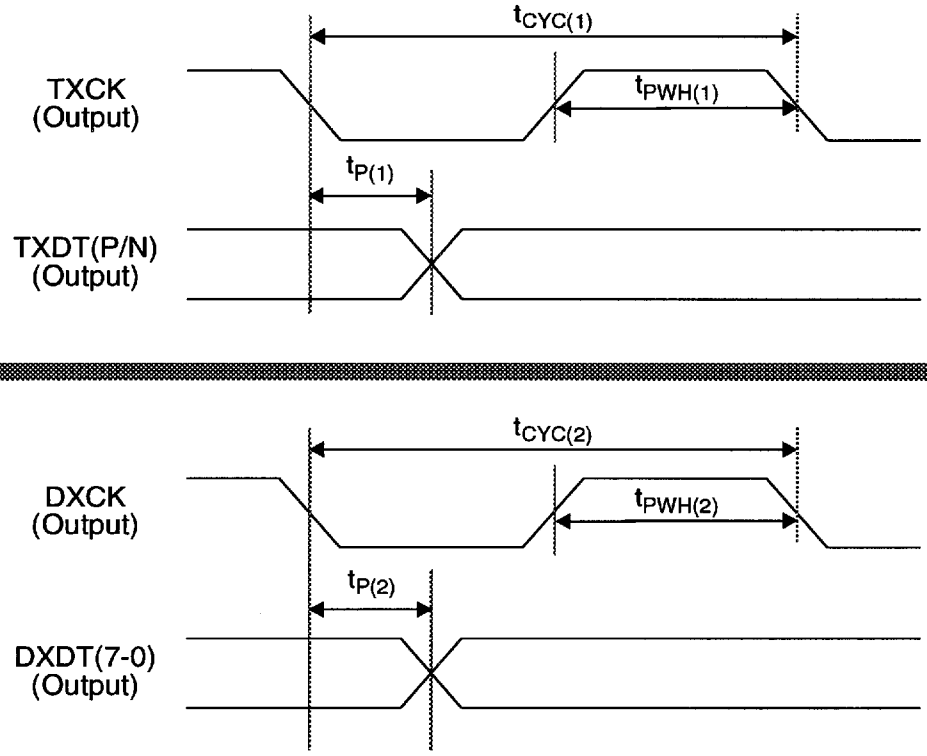


Parameter	Symbol	Min	Nominal	Max	Unit
RXCK clock period	$t_{CYC(1)}$	1.6	--	--	ns
RXCK clock duty cycle, $t_{PWH(1)}/t_{CYC(1)}$		30	50	70	%
RXDT setup time to RXCKP↑	$t_{S(1)}$	400	--	--	ps
RXDT hold time after RXCKP↑	$t_{H(1)}$	200	--	--	ps
MXCK clock period	$t_{CYC(2)}$	12.8	--	--	ns
MXCK clock duty cycle, $t_{PWH(2)}/t_{CYC(2)}$		45	50	55	%
MXDT(7-0) setup time to MXCK↑	$t_{S(2)}$	2500	--	--	ps
MXDT(7-0) hold time after MXCK↑	$t_{H(2)}$	500	--	--	ps
High-speed rise/fall time* (more than 79 MHz)		--	--	320	ps
Low-speed rise/fall time* (less than 79 MHz)		--	--	2.56	ns

Notes:

* 20% to 80% of min V_{OH} and max V_{OL} levels

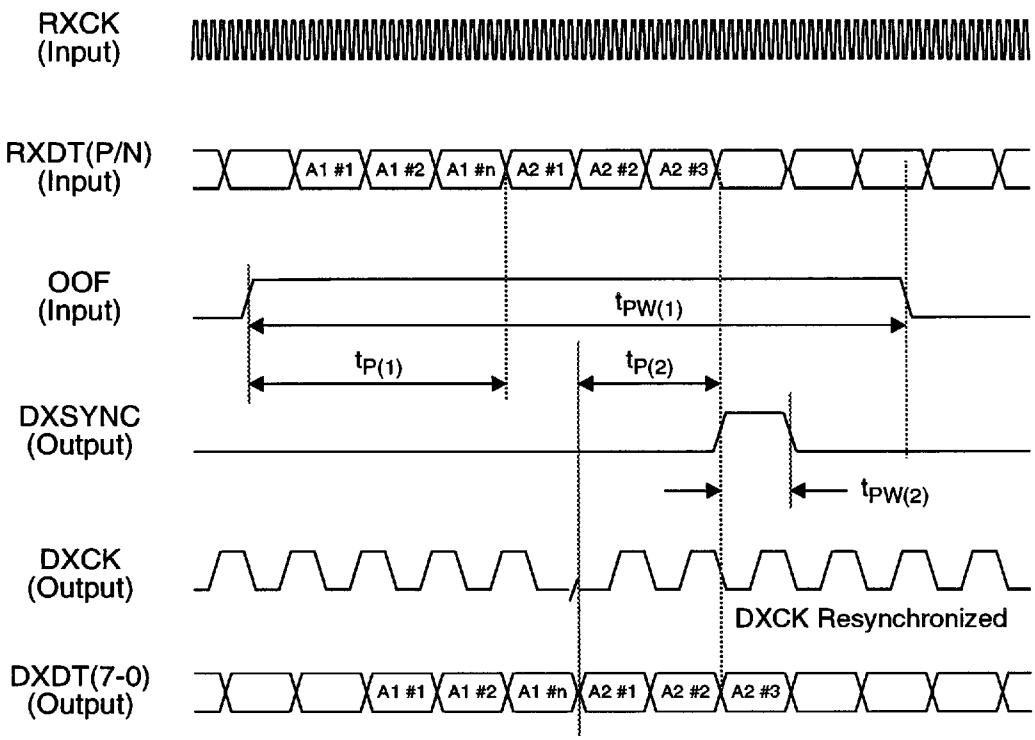
Figure 5. Line and Terminal Side Output Timing



Parameter	Symbol	Min	Nominal	Max	Unit
TXCK clock period	$t_{CYC(1)}$	1.6	--	--	ns
TXCK clock duty cycle, $t_{PWH(1)}/t_{CYC(1)}$		45	50	55	%
TXCK falling edge to TXDT	$t_{P(1)}$	--	--	500	ps
DXCK clock period	$t_{CYC(2)}$	12.8	--	--	ns
DXCK clock duty cycle, $t_{PWH(2)}/t_{CYC(2)}$		45	50	55	%
RXCK clock period	$t_{C(RXCK)}$	1.6	--	--	ns
DXCK falling edge to valid parallel data output	$t_{P(2)}$	$t_{C(RXCK)}$	$t_{C(RXCK)}$+0.5	$t_{C(RXCK)}$+1.5	ns
High-speed rise/fall time* (more than 79 MHz)		--	--	320	ps
Low-speed rise/fall time* (less than 79 MHz)		--	--	2.56	ns

Notes:
* 20% to 80% min V_{OH} and max V_{OL} levels

Figure 6. Demultiplexer Timing



Parameter	Symbol	Min	Nominal	Max	Unit
RXCK clock period		1.6	--	--	ns
RXCK clock duty cycle		30	50	70	%
OOF pulse width	$t_{PW(1)}$	12.86	--	--	ns
OOF rising edge before A1 changes to A2	$t_{P(1)}$	51.44	--	--	ns
DXSYNC rising edge from parallel data output change from A1 to A2	$t_{P(2)}$	--	25.72	--	ns
DXSYNC pulse width	$t_{PW(2)}$	12.86	--	--	ns
High-speed rise/fall time* (more than 79 MHz)		--	--	320	ps
Low-speed rise/fall time* (less than 79 MHz)		--	--	2.56	ns

Notes:

* 20% to 80% of min V_{OH} and max V_{OL} levels

Figure 7. Multiplexer and Miscellaneous Timing

Parameter	Min	Nominal	Max	Unit
DXRCK clock period		19.29	--	ns
DXRCK clock duty cycle	45	50	55	%
MXLRC clock period ("A" version, 51.84 MHz)	18.87	19.29	19.61	ns
MXLRC clock period ("B" version, 38.88 MHz)	25.16	25.72	26.15	ns
MXLRC clock duty cycle	30	50	70	%
MXHC clock period	1.6	--	--	ns
MXHC clock duty cycle	30	50	70	%
CNTL(2-0) setup time to CNTL(3) transition	5500	--	--	ps
CNTL(2-0) hold time after CNTL(3) transition	2000	--	--	ps
High-speed rise/fall time* (more than 79 MHz)	--	--	320	ps
Low-speed rise/fall time* (less than 79 MHz)	--	--	2.56	ns

Notes:

* 20% to 80% of min V_{OH} and max V_{OL} levels

OPERATION

MODE CONTROL

Four mode control input leads, CNTL(3-0), are provided. When CNTL3=1, the eight values of CNTL(2-0) control the selection of one of eight combinations of clock rate (one of two) and clock modes (two, each one of two). When CNTL3=0, the same eight values instead temporarily enable either a loopback mode (one of three) or another special state (one of five). The functions of the sixteen states of CNTL(3-0) are described in Figure 8.

The three clock rate and mode selections are as follows:

1. Rate Selection: The STAF device may be operated with a serial line rate of either 622.08 Mbit/s for STS-12/STM-4 (selected by CNTL1=1) or 155.52 Mbit/s for STS-3/STM-1 (selected by CNTL1=0). This selection is applied to both the transmit and receive sides of the device.
2. Master/Slave Reference Clock Input Selection: The PLL synthesizer may be operated with either of two clocks as its reference input. In Master mode (selected by CNTL0=1), the reference is the reference clock applied to the MXLRC input pin (51.84 MHz for the "A" version or 38.88 MHz for the "B" version). In Slave mode (selected by CNTL0=0) the reference is an internal image of the receiver-derived 51.84 MHz clock that appears at the DXRCK output pin. DXRCK is a divided-down version of the receive line-rate clock applied to the differential input pins RXCKP and RXCKN.
3. Normal/Bypass Line-Rate Clock Source Selection for Multiplexer: The multiplexer on the transmit side of the device may be operated with either of two line-rate clocks. In Normal mode (selected by CNTL2=1), the internal PLL's VCO is used as the clock source. In Bypass mode (CNTL2=0), the external line-rate clock applied to the differential input pins MXHCP and MXHCN is used as the clock source.

The modes established by the sixteen available states of the control leads (0H to FH, where CNTL3 is the MSB and high is logic 1) are defined in Figure 8. At power-up, or during initialization, the STAF device should first be reset by setting CNTL(3-0) briefly to 0000 or 0H. After reset, with CNTL3 still at 0, the control inputs CNTL(2-0) should be set to the values required for selection of the desired clock rate and modes, as described above. This will place the device temporarily in one of the eight special states, 0H to 7H, described in Figure 8. CNTL3 should then be switched from 0 to 1 to activate the clock rate and modes selection, terminate the special state, and commence normal device operation. The selected clock rate and modes will then be retained until another one of the eight alternatives is selected. Note that any change in the CNTL(2-0) settings while CNTL3 remains at 1 will cause an immediate corresponding change in the clock rate and/or modes selected.

If it is desired to set the device into one of the eight temporary states, 0H-7H, in which CNTL3=0, then CNTL3 should first be switched from 1 to 0. This will latch the current state of the clock rate and modes selection until CNTL3 is returned to 1. When CNTL3 becomes 0 the device will enter the temporary state in Figure 8 defined by the CNTL(2-0) values last selected for clock rate and modes while CNTL3 was 1. If a different state is desired, the values of CNTL(2-0) should be changed accordingly to effect an immediate change. Any desired sequence of such temporary states may be selected in turn by changing CNTL(2-0) while holding CNTL3 at 0. When it is desired to return to normal operation, then CNTL(2-0) should be reset to the values for clock rate and modes selection that they had before CNTL3 was switched from 1 to 0. This will place the device into the corresponding temporary state once again. CNTL3 should then be changed from 0 to 1 to restore normal operation without changing the clock rate and modes selection from their previous states.

Figure 8. Mode Control by CNTL(3-0) Input Pins

CNTL (3-0)	Modes of Operation
0H	Reset all internal counters, dividers, loopbacks and the phase-frequency detector to known initial states (without initiating frame search). *Note: This feature is intended for device initialization after power-up and for use in factory device screening at relatively slow test clock rates.*
1H	Tri-state all TTL outputs except DXRCK (pin 16) and MO (pin 13). *Used for factory board testing.*
2H	NAND-tree test all TTL inputs, except CNTL(3-0). MO (pin 13) goes low if all of these inputs are high. *Used for factory testing of V_{IH} and V_{IL} parameters and for board testing.*
3H	Tri-state DXRCK TTL output (pin 16). Disables 51.84 MHz output driver if not required in the application. Does not affect operation in Slave mode.
4H	Frame recovery disable. Disables the framer from resynchronizing the demux timing to the SONET A1/A2 boundary. This does not disable DXSYNC (pin 33), which goes high when an A1A1A1/A2A2A2 boundary sequence is received.
5H	Equipment loopback. Loops back the line-rate serial data and clock from the output of the multiplexer to the input of the demultiplexer. The output of the multiplexer also appears as transmit output data and clock on TXDTP (pin 10), TXDTN (pin 12) and TXCK (pin 9). See Note 1.
6H	Facility loopback. Loops back the line-rate serial data and clock of the receiver input at RXDTP (pin 7), RXDTN (pin 6), RXCKP (pin 3) and RXCKN (pin 4) to the output pins of the transmitter at outputs TXDTP (pin 10), TXDTN (pin 12) and TXCK (pin 9). The input of the receiver is also passed on to the data and clock outputs of the demultiplexer.
7H	Split loopback. Loops back the line-rate serial data and clock from the output of the multiplexer to the input of the demultiplexer. Also loops back the line-rate serial data and clock of the receiver from pins RXDTP (pin 7), RXDTN (pin 6), RXCKP (pin 3) and RXCKN (pin 4) to the output pins of the transmitter at TXDTP (pin 10), TXDTN (pin 12) and TXCK (pin 9). See Note 1.
8H	STS-3 rate, Slave mode, Bypass mode. See Notes 2 and 5.
9H	STS-3 rate, Master mode, Bypass mode. See Notes 2 and 4.
AH	STS-12 rate, Slave mode, Bypass mode. See Notes 2 and 5.
BH	STS-12 rate, Master mode, Bypass mode. See Notes 2 and 4.
CH	STS-3 rate, Slave mode, Normal mode. See Notes 3 and 5.
DH	STS-3 rate, Master mode, Normal mode. See Notes 3 and 4.
EH	STS-12 rare, Slave mode, Normal mode. See Notes 3 and 5.
FH	STS-12 rate, Master mode, Normal mode. See Notes 3 and 4.

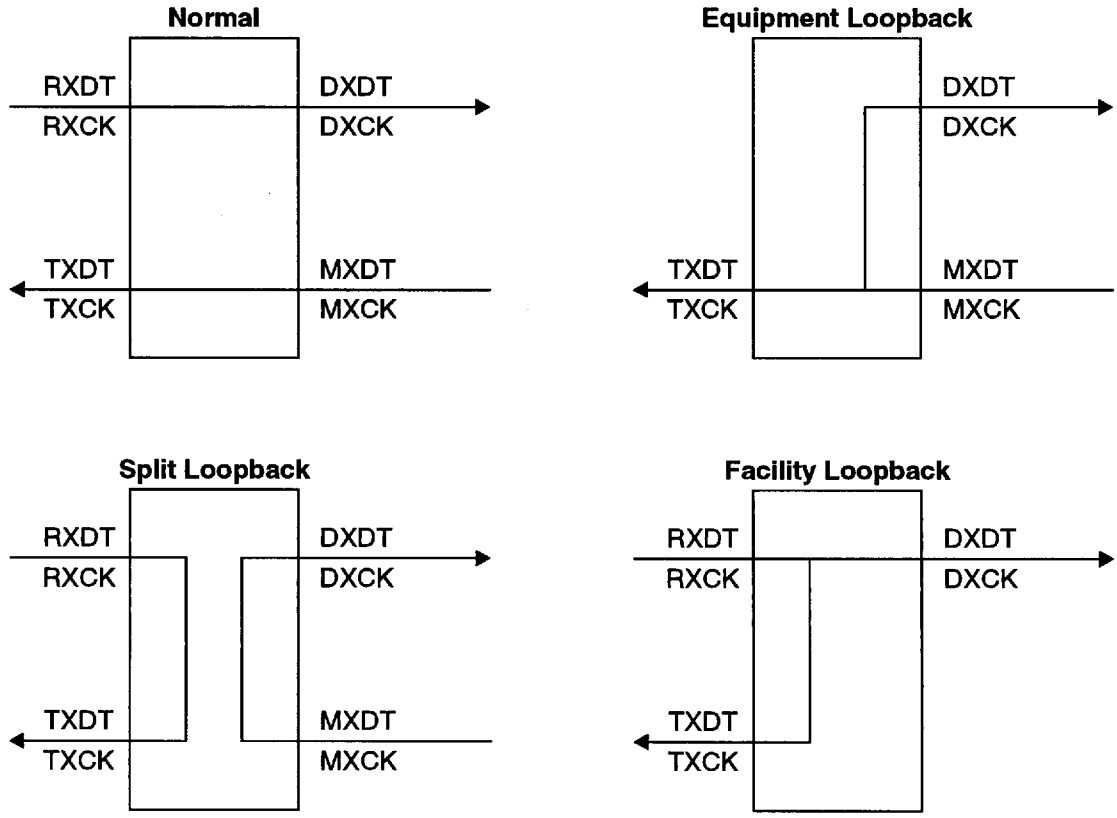
Notes:

1. When the device is configured in Slave mode, activation of either Equipment Loopback or Split Loopback will cause unpredictable synthesizer output frequencies to occur, because the synthesizer uses an image of its own output (TXCK-to-RXCK-to DXRCK) as its reference input. This problem may be avoided by connecting an external reference clock to the MXLRC input at pin 55 (51.84 MHz for the "A" version of the device and 38.88 MHz for the "B" version) and setting the mode to Master before activating Equipment Loopback or Split Loopback.
2. Bypass mode indicates the use of the external high-speed clock (MXHCP, MXHCN at pins 58 and 57) in lieu of the internal transmit PLL output for MXHSRCK.
3. Normal mode indicates use of the internal transmit PLL.
4. Master mode derives PLL timing from the reference oscillator input, MXLRC, which is 51.84 MHz for the "A" version device and 38.88 MHz for the "B" version device.
5. Slave mode derives PLL timing from the demultiplexer clock input, RXCK.

LOOPBACK

The STAF device features three loopback modes in addition to its normal mode of operation (pass-through, no loopback): these are equipment loopback, split loopback, and facility loopback. Loopback modes are controlled by pins CNTL(3-0). Note that the loopback mode does not affect the latched selection of clock modes and rates, and that the RXCK input is directly connected to the TXCK output in most loopback modes, as shown in Figure 9.

Figure 9. Data and Clock Paths in Normal Operation and Three Loopback Modes



SONET/SDH CONSIDERATIONS

Jitter Tolerance

This measurement does not apply to the STAF device, since data is transmitted from the input parallel bus relative to a STAF-generated clock output, MXCK(2-0). The user must meet setup and hold time requirements in order to ensure that data tracking is maintained.

Jitter Transfer

The jitter transfer characteristics of the STAF device are shown in Figure 10.

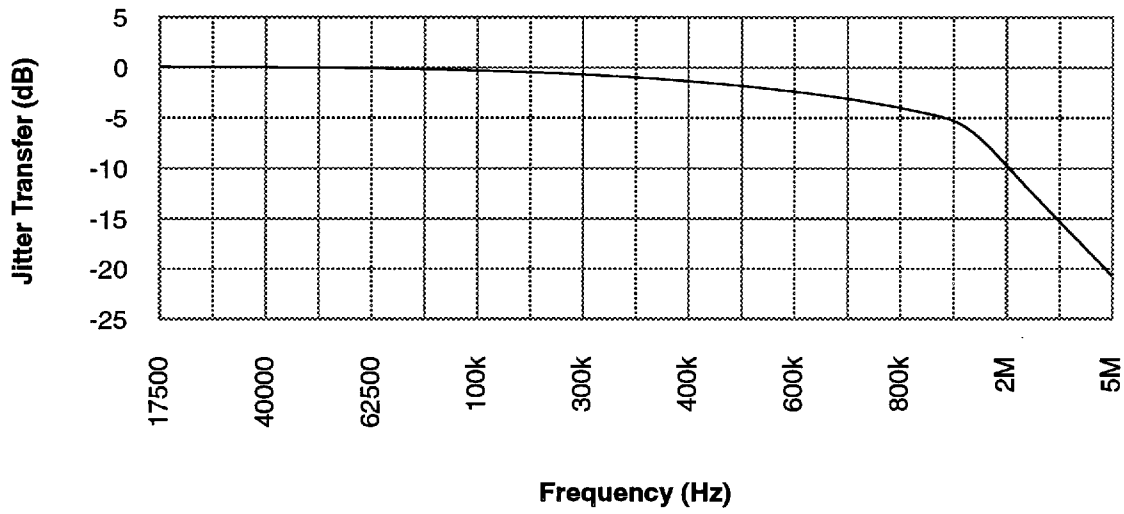


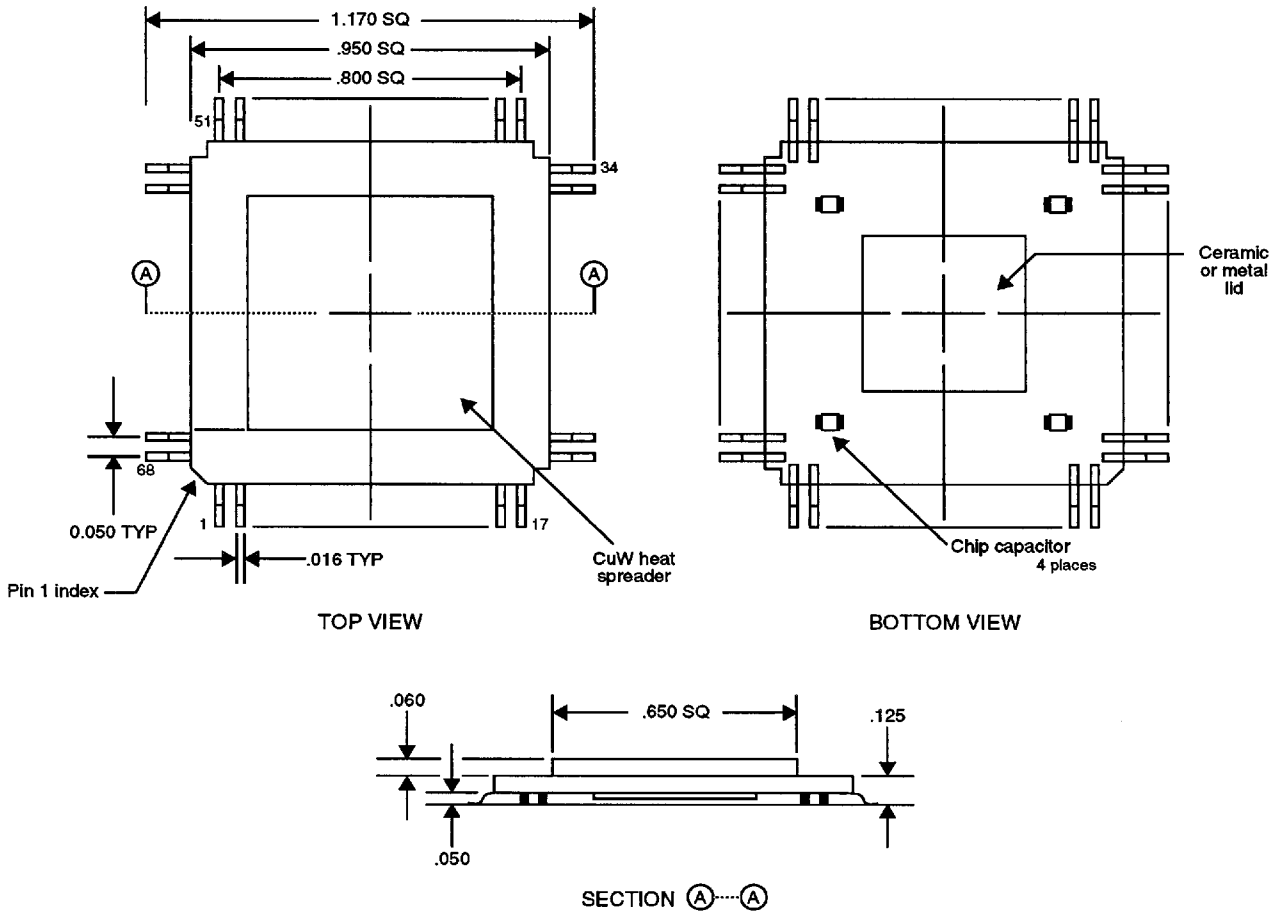
Figure 10. STAF Device Jitter Transfer

Jitter Generation

By exploiting material characteristics, fully differential SCFL logic, and on-chip reactive elements, the STAF device typically has a jitter generation of 0.008 UI RMS (where 1 UI is 1/system frequency), using the recommended loop filter component values of 600 Ω and 0.68 µF in series for connecting the joined TUNE and IOUT pins to V_{EE}.

PACKAGE INFORMATION

The STAF device is packaged in a 68-pin ceramic quad flat package (CQFP) with four external chip capacitors mounted on its underside and a heat spreader on its top, suitable for surface mounting, as shown in Figure 11.



Notes:

1. All dimensions are in inches.
2. All dimension values are nominal unless otherwise indicated.

Figure 11. STAF TXC-02623 68-pin Ceramic Quad Flat Package

ORDERING INFORMATION

"A" Version Part Number:	TXC-02623-ACCQ	68-pin ceramic quad flat package
"B" Version Part Number:	TXC-02623-BCCQ	68-pin ceramic quad flat package

RELATED PRODUCTS

TXC-02624, CDR VLSI device (SONET/SDH Clock and Data Recovery). Receives 622 Mbit/s SONET/SDH bit-serial NRZ data, extracts the high-speed clock, and presents the separated serial data and clock at its differential ECL outputs.