Version 1.2 2007

PEX 8533

Flexible & Versatile PCI Express™ Switch

Features

- **PEX 8533 General Features**
  - 32-lane PCI Express switch
    - Integrated SerDes
  - Up to six configurable ports
  - 35mm x 35mm, 680 pin PBGA package
  - Pin Compatible with PEX 8532
  - Typical Power: 3.3 Watts

- **PEX 8533 Key Features**
  - **Standards Compliant**
    - PCI Express Base Specification, r1.1
    - PCI SHPC Specification, r1.0
  - **High Performance**
    - Cut-through with **120ns** packet latency
    - Max Payload Size of **1024 Bytes**
    - Non-blocking switch fabric
    - Full line rate on all ports
  - **Flexible Configuration**
    - Six highly flexible and configurable ports (x1, x2, x4, x8, or x16)
    - Configurable with strapping pins, EEPROM, I^2C or Host software
    - Lane and polarity reversal
  - **PCI Express Power Management**
    - Link power management states: L0, L0s, L1, L2/L3 Ready, and L3
    - Device states: D0 and D3hot
  - **Quality of Service (QoS)**
    - Eight Traffic Classes per port
    - Round robin and weighted RR port arbitration
  - **Reliability, Availability, Serviceability**
    - 3 Standard Hot-Plug Controllers
    - Upstream port as hot-plug client
    - Transaction Layer end-to-end CRC
    - Poison bit
    - INTA & FATAL ERROR signal support
    - Advanced Error Reporting in addition to PCIe baseline error reporting
    - Port Status bits and GPO available
    - Per port performance monitoring
      - Average packet size, number of packets, CRC errors
    - JTAG boundary scan

Multi-Purpose, Feature Rich PCI Express ExpressLane™ Switch

The *ExpressLane™* PEX 8533 device offers PCI Express switching capability conforming to the latest revision of the PCIe Base specification. This device enables users to add scalable high bandwidth, non-blocking interconnects to a wide variety of applications including servers, storage systems, communications platforms, blade servers, and embedded-control products. The PEX 8533 is well suited for **fan-out**, **aggregation**, **peer-to-peer, backplane,** and **switch fabric applications**.

Highly Flexible Port Configurations

The *ExpressLane™* PEX 8533 offers highly configurable ports. There are a maximum of 6 ports that can be configured to any legal width from x1 to x16, in any combination to support your specific bandwidth needs. The ports can be **symmetric** (each port having the same lane width) or **asymmetric** (ports having different lane widths). Any of the ports can be designated as the upstream port, which can be changed dynamically.

High Performance

The *ExpressLane™* PEX 8533 architecture supports packet **cut-through with a latency of 115ns (x8 to x8).** This, combined with large packet memory **(256 to 1024 byte maximum payload size)** and **non-blocking internal switch architecture**, provide **full line rate** on its ports for performance hungry applications such as storage servers or storage switch fabrics.

End-to-End Packet Integrity

The *ExpressLane™* PEX 8533 provides **optional end-to-end CRC** protection (ECRC) and **Poison bit** support to enable designs that require **guaranteed error-free packets**.

Configuration Flexibility

The *ExpressLane™* PEX 8533 provides several ways to configure its operations. The device can be configured through strapping pins, **I^2C** interface, CPU configuration cycles, or an optional serial EEPROM. This allows for easy debug during the development phase, performance monitoring during the operation phase, and driver or software upgrade.

Interoperability

The *ExpressLane™* PEX 8533 is designed to be fully compliant with the PCI-SIG specification. Additionally, it supports auto-negotiation, lane reversal, and polarity reversal. The PEX 8533 also undergoes thorough Interoperability testing in PLX's **Interoperability Lab**.

Low Power with Granular SerDes Control

The *ExpressLane™* PEX 8533 provides **low power** capability that is fully compliant with the PCI Express power management specification. In addition, the SerDes physical links can be turned off when unused for even lower power.

Flexible Port Width Configuration

The lane width of each port can be individually configured through **auto-negotiation**, hardware strapping, host software configuration, I^2C interface, or through an optional EEPROM.

The PEX 8533 supports a large number of port configurations. For example, if you are using the PEX 8533 in a fan-out application, you may configure the upstream port as a x8 and the downstream as one x8 port & four x4 ports; two x8 & two x4 ports; or other combinations, as long as you don't run out of lanes (32) or ports (6). For a **dual-graphics application**, you may configure the device as one x16 upstream and two x8 downstream ports (see Figure 1). The device can also support x2 & x1 ports by auto-negotiating its x4 ports to the width of the actual end-device it is interfacing with.

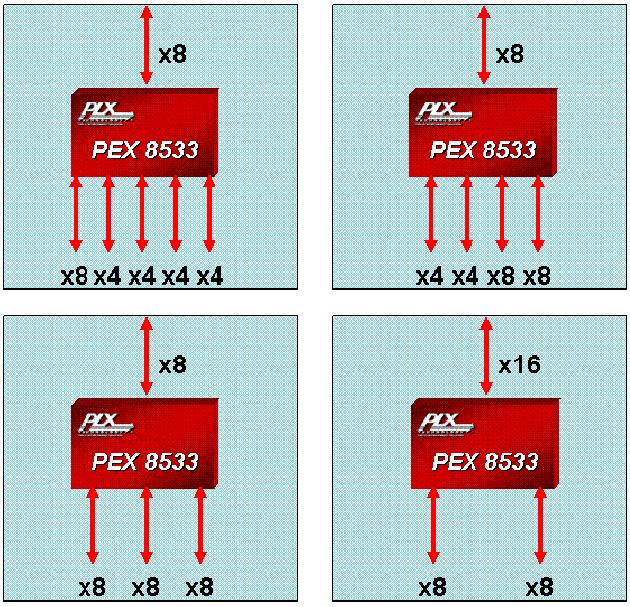


Figure 1. Port Flexibility

Low Packet Latency

The PEX 8533 supports packet cut-through with a latency of 115ns between symmetric x8 ingress and egress ports. The low latency enables many applications to achieve high throughput and performance. In addition to low latency, the device supports a packet payload size of up to 1024 bytes, enabling the user to achieve even higher throughput.

Hot Plug for High Availability

Hot plug capability allows users to replace hardware modules and perform maintenance without powering down the system. The ExpressLane PEX 8533 hot plug capabilities and **Advanced Error Reporting** features make them suitable for **high availability (HA) applications**. Three of the six ports include a **Standard Hot Plug Controller**. If the PEX 8533 is used in an application where one or more of its downstream ports connect to PCI Express slots, the ports with the Hot Plug Controller feature can be used for these slots. The device will automatically manage the hot-plug event of its hot-plug capable ports/slots. Furthermore, the hot-plug capable ports can be used as a **hot-plug client or master,** allowing it to be **used on hot-pluggable carrier modules, backplanes, and fabric modules**.

Fully Compliant Power Management

For applications that require power management, the PEX 8533 device supports both link (L0, L0s, L1, L2/L3 Ready, and L3) and device (D0 and D3hot) power management states, in compliance with the PCI Express power management specification.

SerDes Power and Signal Management

The ExpressLane PEX 8533 supports **software control of the SerDes outputs** to allow optimization of power and signal strength in a system. The PLX SerDes implementation supports four levels of power – off, low, typical and high. The SerDes block also supports **loop-back modes** and **advanced reporting of error conditions**, which enables efficient debug and management of the entire system.

Applications

Suitable for **host-centric** as well as **peer-to-peer** traffic patterns, the PEX 8533 can be configured for a wide variety of form factors and applications.

Host Centric Fan-out

The ExpressLane PEX 8533 device, with its versatile symmetric or asymmetric lane configuration capability, allows for user specific tuning to a variety of host-centric applications.

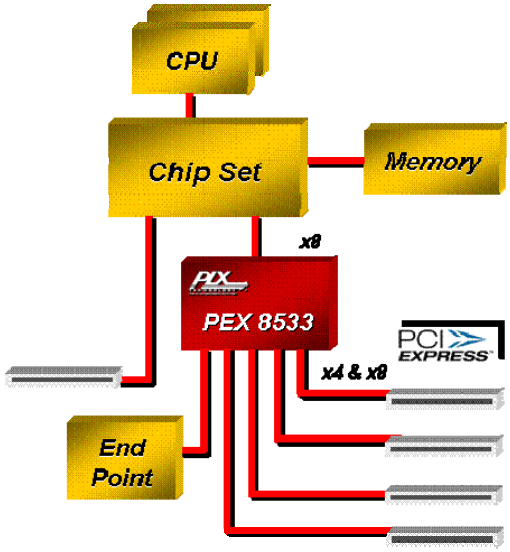


Figure 2. Fan-in/out Usage

Figure 2 shows a typical **server-based** design, where the Root Complex provides a PCI Express link that needs to be expanded into a larger number of smaller ports for a variety of I/O functions, each with different bandwidth requirements.

In this example, the ExpressLane PEX 8533 would typically have an 8-lane upstream port, and as many as 5 downstream ports. The downstream ports can be of differing widths if required.

Peer-to-Peer & Backplane Usage

The PEX 8533 is also suitable for peer-to-peer applications such as switch fabrics and backplanes. Figure 3 represents a backplane where the device provides peer-to-peer data exchange for a large number of line cards where the CPU/Host plays the management role.

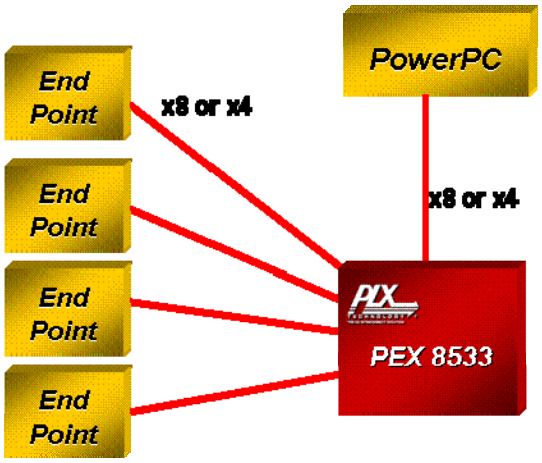


Figure 3. Peer-to-Peer/Backplane Usage

Graphics Fan-out Switch

High resolution 3D graphics applications can take full advantage of the PEX 8533 three port configuration. Applications such as **dual graphics, high resolution scientific use, and image processing** can benefit from the performance of the PEX 8533 switch. Figure 4 illustrates use of the device in a dual graphics application while supporting PCI port expansion through another PLX PCIe switch. The upstream x16 port links to the Root Complex and the two downstream ports connect to the Graphics modules. The peer-to-peer support of the PEX 8533 allows the two GPU modules to communicate with each other for maximum performance. Figure 4 also illustrates use of PCIe bridges to connect to PCI and PCI-X busses.

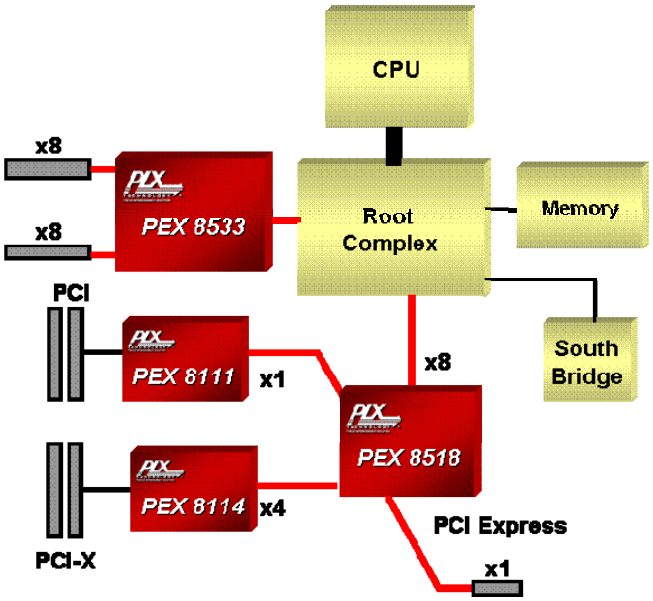


Figure 4. Dual Graphics

Redundant Switch Fabric

The PEX 8533 can be used in redundant switch fabrics for high availability applications. In the example shown in Figure 5, the PEX 8533 is used in conjunction with the PEX 8518 switch that offers **non-transparent bridging (NTB)**. The PEX 8533 provides high performance non-blocking switching while the PEX 8518s keep the two fabrics and hosts isolated.

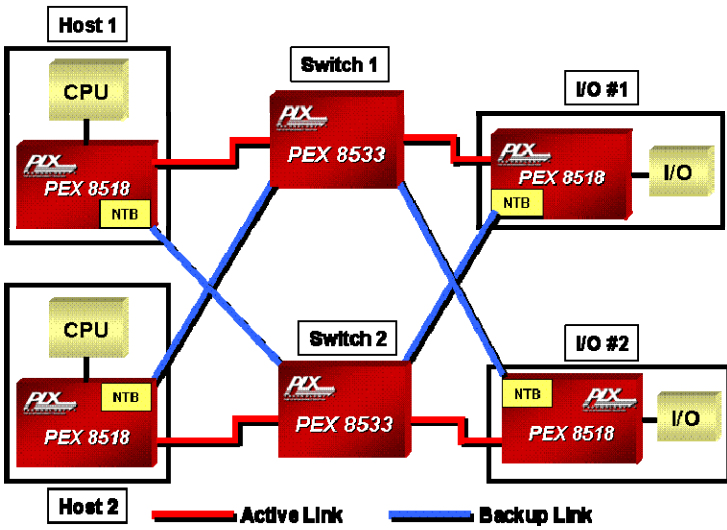


Figure 5. Blade Server

The number of ports and port widths can be configured as needed. This example assumes a x8 link to each CPU blade and a x8 link to each I/O blade.

Development Tools

PLX is offering hardware and software tools (PEX 8533 RDK) to enable rapid customer design activity. These tools are bundled in a Rapid Development Kit (RDK). The RDK consists of hardware, hardware documentation and a Software Development Kit (SDK).

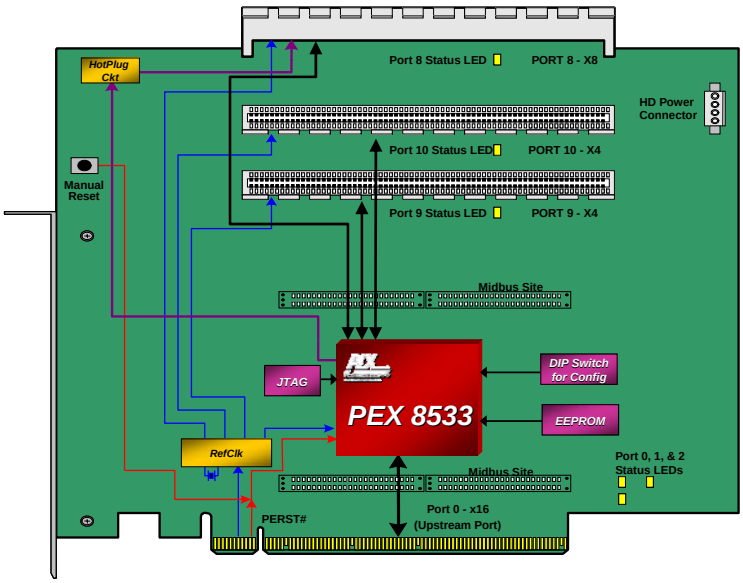


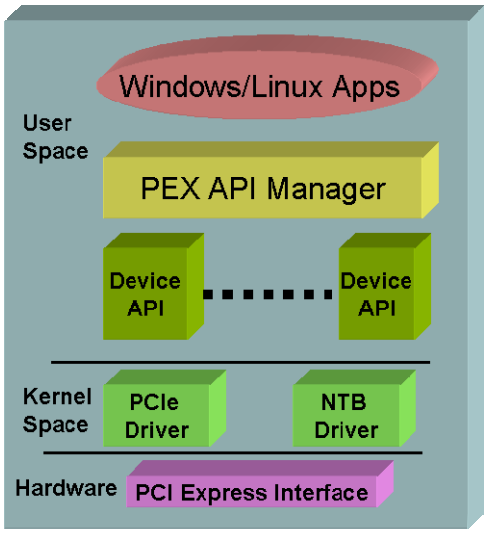
Figure 6. PEX 8533 RDK

The PEX 8533 RDK offers a x16 upstream port, one x8 downstream port, and two x4 downstream ports. The PEX 8533 RDK board can be installed on a motherboard, used as a riser card, or configured as a bench-top board. The PEX 8533 RDK can be used to test and validate customer software. Additionally, it can be used as an evaluation vehicle for PEX 8533 features and benefits. The PEX 8533 RDK provides everything that a user needs to get their hardware and software development started.

SDK

The SDK tool set includes:

- GUI to use and configure the switch
- Linux and Windows drivers
- C/C++ Source code, Objects, libraries
- User's Guides, Application examples, Tutorials



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Product Ordering Information

Part Number	Description
PEX8533-AA25BI	32-Lane PCI Express Switch
PEX8533-AA25BI G	32-Lane PCI Express Switch, Pb-free
PEX 8533-AA RDK	PEX 8533 Rapid Development Kit w/ x16 Connector

Please visit the PLX Web site at http://www.plxtech.com or contact PLX sales at 408-774-9060 for sampling.