SINO WEALTH

SH86270

Highly-integrated Digital Music SOC

Preliminary
Ver 0.91
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CONTENT

1. FEATURES

- Single-cycle 8051 CPU core:
  - Internal adjustable operation frequency (1/6/12/15/27/33.75MHz) for energy saving.
  - 12K-byte program SRAM, 256-byte internal data SRAM and 128-byte SFR.
  - 7K-byte external data SRAM.
- Fully compatible with full-speed USB2.0 specification:
  - Support one device address.
  - Support 3 endpoints: one control endpoint, one bulk-in endpoint and one bulk-out endpoint.
- Built-in NAND flash controller:
  - Flexible engine for SLC and MLC NAND flash (including NAND Flash memories by Samsung, Toshiba, Hynix, ST, Micron and other types.)
- Built-in MMC/SD card engine.
- Built-in LCD module interface:
  - Support 8080 compatible LCD interface byte parallel mode and serial mode.
  - Support bit antitone.
  - Support HT1621 (32x4) interface.
- Built-in MPEG audio decoder:
  - Support 8/11.025/12/16/22.05/24/32/44.1/48kHz sampling frequencies for MPEG bit stream.
  - Support 32/40/48/56/64/80/96/112/128/160/192/224/256/320kbps bit rate for MPEG1.
  - Support 8/16/24/32/40/48/56/64/80/96/112/128/144/160kbps bit rates for MPEG2.
  - Support 8/16/24/32/40/48/56/64/80/96/112/128/144/160kbps bit rates for MPEG2.5.
  - Support single channel, dual channel and stereo format.
  - EQ effects support Natural/Pop/Rock/Classic/Jazz/ String/HP-Enhance/Reggae/Extra-Bass sound effects.
- On-chip CODEC:
  - 16-bit sigma-delta stereo DAC for audio play.
  - 8-bit ADC for voice record and battery voltage detection.
  - FM-in for external FM module.
  - Stereo headphone amplifier. Headphone driver output with short-circuit protected.
- Built-in one 16-bit timer.
- 12MHz external clock input with on-chip PLL.
- Low power 1.8V core operation voltage and 3.3V I/O operation voltage.
- Built-in DC/DC
- Support two power management mode: IDLE mode and STOP mode.
- Power consumption below 45mW (While decoding 128kbps @44.1kHz MPEG audio bit stream).
- Four reset sources:
  - Power-on reset (POR).
  - Lower voltage reset (LVR).
  - Watchdog reset (WDR).
  - External pin reset (EPR).
- Available in LQFP64 (10mm x 10mm) package, QFP100 (14mm x 20mm) package and COB.

2. GENERAL DESCRIPTION

The SH86270 is a single-cycle 8051 CPU core embedded device with a powerful flash card/memory controller and MPEG audio decoder. It includes a single-cycle 8051 CPU core, USB2.0 full-speed SIE and PHY functional block, one ADC and one DAC, a MPEG audio decoder and relevant interfaces in LQFP64 package.

SH86270 is really suitable for any data storage related products, i.e. Full-speed USB2.0 Flash Disk, portable MPEG audio player, card reader/writer, etc.

3. PAD & PIN ASSIGNMENT

3.1. Main Chip Pin Assignment (LQFP64)

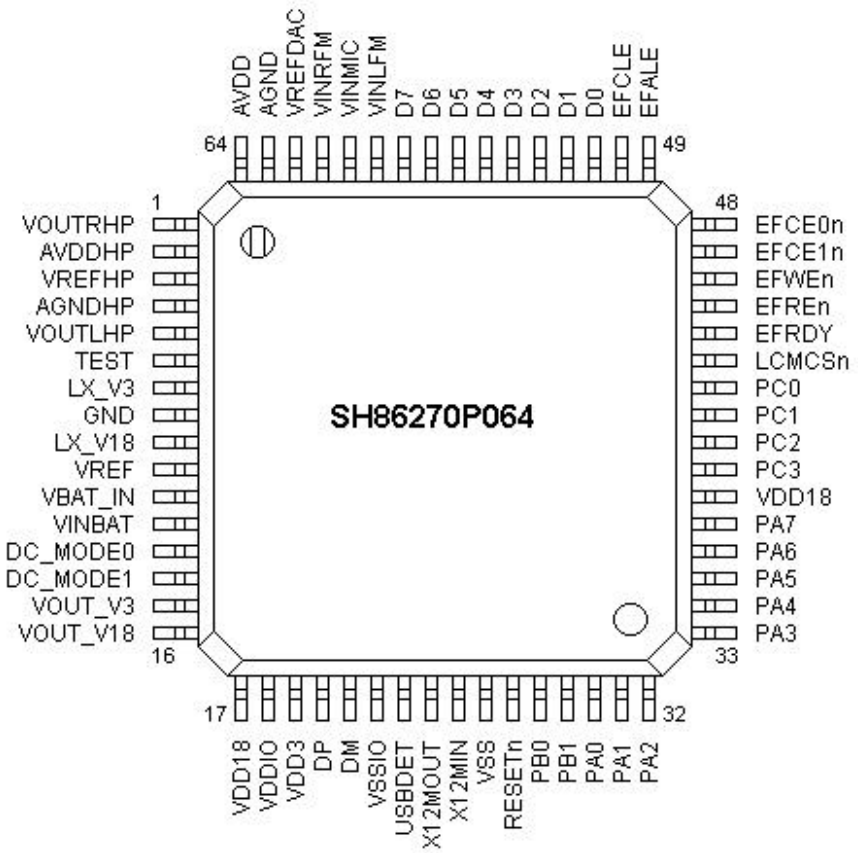

Figure 1. Main Chip Pin Assignment (LQFP64)

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	VOUTRHP	17	VDD18	33	PA3	49	EFALE
2	AVDDHP	18	VDDIO	34	PA4	50	EFCLE
3	VREFHP	19	VDD3	35	PA5	51	D0
4	AGNDHP	20	DP	36	PA6	52	D1
5	VOUTLHP	21	DM	37	PA7	53	D2
6	TEST	22	VSSIO	38	VDD18	54	D3
7	LX_V3	23	USBDET	39	PC3	55	D4
8	GND	24	X12MOUT	40	PC2	56	D5
9	LX_V18	25	X12MIN	41	PC1	57	D6
10	VREF	26	VSS	42	PC0	58	D7
11	VBAT_IN	27	RESETn	43	LCMCSn	59	VINLFM
12	VINBAT	28	PB0	44	EFRDY	60	VINMIC
13	DC_MODE0	29	PB1	45	EFREn	61	VINRFM
14	DC_MODE1	30	PA0	46	EFWEn	62	VREFDAC
15	VOUT_V3	31	PA1	47	EFCE1n	63	AGND
16	VOUT_V18	32	PA2	48	EFCE0n	64	AVDD

Table 1. Main Chip with Built-in DC/DC Pin Assignment (LQFP64)

3.2. PAD & PIN Description

Category	PAD No.	PAD Name	Type	State	I_{dr}/I_{Si}	Description	Pin No. EV	Pin No. MC
DAC	1	VOUTRHP	O	-	-	Headphone output right	5	1
DAC	2	AVDDHP	P	-	-	Headphone supply voltage	6	2
DAC	3	VREFHP	O	-	-	Headphone reference voltage	7	3
DAC	4	AGNDHP	P	-	-	Headphone ground	8	4
DAC	5	VOUTLHP	O	-	-	Headphone output left	9	5
System	6	TEST	I	PL	-	Test mode	10	6
GPIO	7	PB2	I/O	CP	1mA	General purpose I/O pin	11	-
System	8	VSS	P	-	-	Digital ground of ROM	12	GND
DC/DC	9 10	LX_V3	O	-	-	Pin for switching 3V power	13	7
DC/DC	11 12 13	GND	P	-	-	DC/DC digital ground	14	8
DC/DC	14 15	LX_V18	O	-	-	Pin for switching 1.8V power	15	9
DC/DC	16	VREF	I	-	-	Reference voltage input	16	10
DC/DC	17	VBAT_IN	P	-	-	1xAA, 1xAAA battery voltage input	17	11
ADC	18	VINBAT	I	-	-	Battery voltage input	18	12
DC/DC	19	DC_MODE0	I	-	-	DC/DC Mode Select 0	19	13
DC/DC	20	DC_MODE1	I	-	-	DC/DC Mode Select 1	20	14
DC/DC	21	TMODE0	I	-	-	DC/DC test pad	21	-
DC/DC	22	TMODE1	I	-	-	DC/DC test pad	22	-
DC/DC	23 24	VOUT_V3	O	-	-	3V Voltage Output	23	15
DC/DC	25 26	VOUT_V18	O	-	-	1.8V Voltage Output	29	16
System	27 28	VDD18	P	-	-	1.8V supply voltage for core circuit	30	17
DC/DC	29	TPIN4	I/O	-	-	DC/DC test pad	31	-
DC/DC	30	TPIN2	I/O	-	-	DC/DC test pad	32	-
DC/DC	31	TPIN3	I/O	-	-	DC/DC test pad	33	-
DC/DC	32	TPIN1	I/O	-	-	DC/DC test pad	34	-
System	33	VDDIO	P	-	-	3V supply voltage for peripheral circuit	35	18
System	34	VDD3	P	-	-	3V supply voltage for core circuit	36	19
USB	35	DP	I/O	-	-	USB data in data positive pin terminal	37	20
USB	36	DM	I/O	-	-	USB data in data negative pin terminal	38	21
System	37 38	VSSIO	P	-	-	Digital ground of 3V peripheral circuit	39	22
USB	39	VDDUSBPU	O	-	-	USB pull-up supply voltage on DP	40	-
GPIO	40	PB3	I/O	CP	1mA	General purpose I/O pin	41	-
USB	41	USBDET	I	-	-	USB power detection	42	23
System	42	X12MOUT	O	-	-	12MHz crystal output.	43	24
System	43	X12MIN	I	-	-	12MHz crystal or TTL compatible clock input.	44	25
System	44 45	VSS	P	-	-	Digital ground of core circuit	45	26

Table 2. PAD & PIN Description

Category	PAD No.	PAD Name	Type	State	I_{dr}/I_{Si}	Description	Pin No.	
							EV	MC
System	46	DISWDT	I	-	-	Used to dis able watchdog	46	GND
System	47	RESETn	I	PH	-	System reset	47	27
GPIO	48	PB0	I/O	CO	1mA	General purpose I/O pin	48	28
GPIO	49	PB1	I/O	CO	1mA	General purpose I/O pin	49	29
GPIO	50	PA0	I/O	CP	1mA	General purpose I/O pin	50	30
GPIO	51	PA1	I/O	CP	1mA	General purpose I/O pin	51	31
GPIO	52	PA2	I/O	CP	1mA	General purpose I/O pin	52	32
GPIO	53	PA3	I/O	CP	1mA	General purpose I/O pin	57	33
GPIO	54	PA4	I/O	CP	1mA	General purpose I/O pin	58	34
GPIO	55	PA5	I/O	CP	1mA	General purpose I/O pin	59	35
GPIO	56	PA6	I/O	CP	1mA	General purpose I/O pin	60	36
GPIO	57	PA7	I/O	CP	1mA	General purpose I/O pin	61	37
ICE	58	DOCD_CLK	O	-	1mA	ICE interface clock line.	62	-
ICE	59	DOCD_DATO	O	-	1mA	ICE interface data output line.	63	-
ICE	60	DOCD_DATI	I	-	1mA	ICE interface data input line.	64	GND
System	61 62	VDD18	P	-	-	1.8V supply voltage for core circuit	65	38
MSI	63	MSCLK	O	-	2mA	MMC/SD clock line	66	39
GPIO		PC3	I/O	CP		General purpose I/O pin		
MSI	64	MSWP	I	PH	1mA	MMC/SD card write protection input	67	40
GPIO		PC2	I/O	CP		General purpose I/O pin		
MSI	65	MSCDn	I	PH	1mA	MMC/SD card detection input	68	41
GPIO		PC1	I/O	CP		General purpose I/O pin		
MSI	66	MSCMD	I/O	PH	2mA	MMC/SD command line	69	42
GPIO		PC0	I/O	CP		General purpose I/O pin		
System	67	VSS	P	-	-	Digital ground of MADE	70	GND
System	68	OPTION	I	-	-	System option	71	GND
LCMI	69	LCMCSn	O	-	1mA	LCD chip selection	72	43
EFI	70	EFRDY	I	-	1mA	NAND flash ready/busy detection	73	44
EFI	71	EFREn	O	-	2mA	NAND flash read enable	74	45
LCMI		LCMREn	O	-		LCD read enable		
EFI	72	EFWEn	O	-	2mA	NAND flash write enable	75	46
LCMI		LCMWEn	O	-		LCD write enable		
EFI	73	EFCE1n	O	-	1mA	NAND flash chip enable	76	47
EFI	74	EFCE0n	O	-	1mA	NAND embedded flash chip enable	80	48
EFI	75	EFALE	O	-	1mA	NAND flash address latch enable	81	49
LCMI		LCMA0	O	-		LCD data/command selection		
EFI	76	EFCLE	O	-	1mA	NAND flash command latch enable	82	50
EFI	77	EFD0	I/O	-	1mA	EFI data line	83	51
LCMI		LCMD0	I/O	-		LCMI data line		
EFI	78	EFD1	I/O	-	1mA	EFI data line	84	52
LCMI		LCMD1	I/O	-		LCMI data line		
EFI	79	EFD2	I/O	-	1mA	EFI data line	85	53
LCMI		LCMD2	I/O	-		LCMI data line		
EFI	80	EFD3	I/O	-	1mA	EFI data line	86	54
LCMI		LCMD3	I/O	-		LCMI data line		

Table 3. PAD & PIN Description (Continue)

Category	PAD No.	PAD Name	Type	State	I_{dr}/I_{Si}	Description	Pin No.	
							EV	MC
EFI	81	EFD4	I/O	-	2mA	EFI data line	87	55
LCMI		LCMD4	I/O	-		LCMI data line		
MSI		MSD0	I/O	PH		MSI data line		
EFI	82	EFD5	I/O	-	2mA	EFI data line	88	56
LCMI		LCMD5	I/O	-		LCMI data line		
MSI		MSD1	I/O	PH		MSI data line		
EFI	83	EFD6	I/O	-	2mA	EFI data line	89	57
LCMI		LCMD6	I/O	-		LCMI data line		
MSI		MSD2	I/O	PH		MSI data line		
EFI	84	EFD7	I/O	-	2mA	EFI data line	90	58
LCMI		LCMD7	I/O	-		LCMI data line		
MSI		MSD3	I/O	PH		MSI data line		
DAC	85	VINLFM	I	-	-	FM input left	91	59
System	86	VSS	P	-	-	Digital ground	92	GND
	87							
ADC	88	VINMIC	I	-	-	Microphone input	93	60
DAC	89	VINRFM	I	-	-	FM input right	94	61
DAC	90	VREFDAC	I	-	-	DAC reference voltage	95	62
	91							
ADC	92	AGNDADC	P	-	-	ADC ground	96	63
DAC	93	AGNDDAC	P	-	-	DAC ground	97	
ADC	94	AVDDADC	P	-	-	ADC supply voltage	98	64
DAC	95	AVDDDAC	P	-	-	DAC supply voltage	99	

Table 4. PAD & PIN Description (Continue)

Note: 1. Type: P? Power, I? Input, O? Output, I/O? Input/Output
2. State: PL? Pull-low, PH? Pull-high, CP? Configurable Pull-low/Pull-high, CO? Configurable Open-drain.
3. EV indicates the EV chip and its package is QFP100. MC indicates the main chip with built-in DC/DC and its package is LQFP64.

4. ELECTRICAL SPECIFICATIONS

4.1. DC Characteristics

(V_{DD33} = 3.0V, V_{DD18} = 1.8V, GND = 0V, T_A = 25℃, F_{OSC} = 12MHz, unless otherwise specified.)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
3.3V Operating Voltage	V_{DD33}	2.8	3.3	3.6	V	
3.3V Operating Current	I_{DD33}	-	TBD	-	mA	
1.8V Operating Voltage	V_{DD18}	1.6	1.8	2.0	V	
1.8V Operating Current	I_{DD18}	-	TBD	-	mA	
Power Consumption	P	-	45	TBD	mW	@128kbps MP3+LCM+EF
High-level Output Voltage	V_{OH}	$0.7V_{DD33}$	-	V_{DD33}	V	@V_{DD}=3.0V, I_{OH}=-2mA
Low-level Output Voltage	V_{OL}	0	-	$0.3V_{DD33}$	V	@V_{DD}=3.0V, I_{OL}=2mA
High-level Input Voltage	V_{IH}	$0.7V_{DD33}$	-	V_{DD33}	V	
Low-level Input Voltage	V_{IL}	0	-	$0.3V_{DD33}$	V	
Voltage Detection Range	V_{DR}	0.8	-	1.8	V	
Voltage Detection Resolution	V_{DRRES}	-	-	±0.03	V	
3.3V Power On Reset Level	V_{POR33}	2.2	2.4	2.6	V	
1.8V Low Voltage Reset Level	V_{LVR18}	1.2	1.3	1.4	V	
1.8V Power On Reset Level	V_{POR18}	0.8	1.0	1.2	V	
Pull-high Resistor	R_H		75k		kΩ	
Pull-low Resistor	R_L		75k		kΩ	

Table 5. DC Characteristics

4.2. AC Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Voltage detector setup time	t_{PDS}		100	TBD	us	
Voltage detector response time	t_{PDR}		20	TBD	us	
Power-On-Reset time	$t_{RST(POR)}$		40		ms	
Low-Voltage-Reset time	$t_{RST(LVR)}$		50		us	
Low-Voltage-Reset debounce time	t_{LVRDEB}	50			us	
External pin reset period	$t_{RST(EPR)}$			1	ms	
External pin reset debounce time	t_{EPRDEB}	150	200		us	

Table 6. AC Characteristics

5. PACKAGE OUTLINE

5.1. LQFP64 Outline (for Main Chip Package)

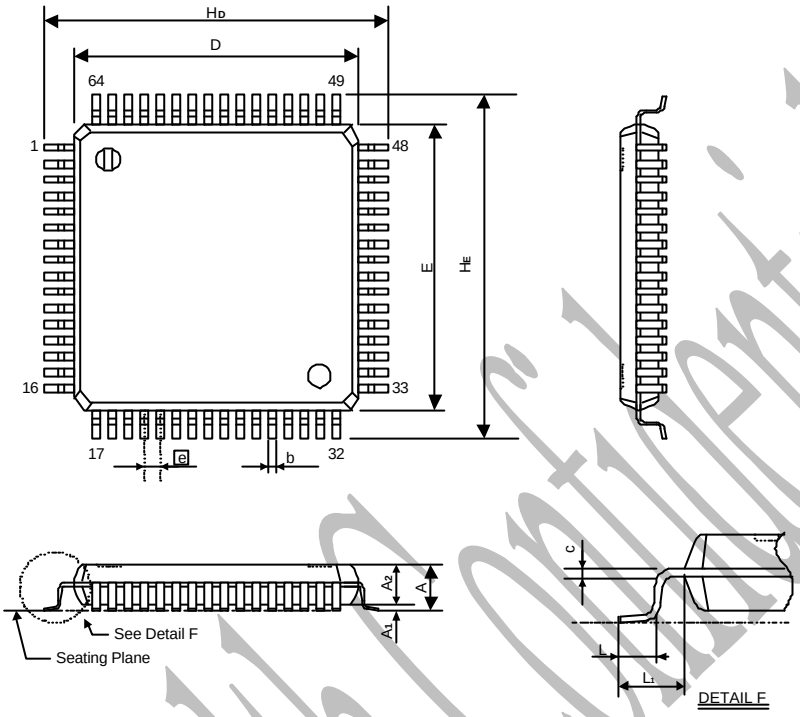

Figure 2. LQFP64 Outline

Symbol	Dimensions in inch	Dimensions in mm
A	0.063 (MAX)	1.60 (MAX)
A_1	0.002 (MIN.), 0.006(MAX.)	0.05 (MIN), 0.15 (MAX)
A_2	0.055 ± 0.002	1.40 ± 0.05
b	0.009 ± 0.002	0.22 ± 0.05
c	0.004 (MIN), 0.008 (MAX)	0.09 (MIN), 0.20 (MAX)
D	0.394 BASIC	10.00 BASIC
E	0.394 BASIC	10.00 BASIC
e	0.020 BASIC	0.50 BASIC
H_D	0.472 BASIC	12.00 BASIC
H_E	0.472 BASIC	12.00 BASIC
L	0.024 ± 0.006	0.60 ± 0.15
L_1	0.039 REF	1.00 REF

Table 7. LQFP64 Outline Dimensions