

NEC

User's Manual

IE-703037-MC-EM1

In-circuit Emulator Option Board

Target device
V850/SB1™

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- Availability of related technical literature
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INTRODUCTION

Target Readers This manual is intended for users who design and develop application systems using the V850/SB1™.

Purpose The purpose of this manual is to describe the proper operation of the IE-703037-MC-EM1 and its basic specifications.

Organization This manual is divided into the following parts.

- Overview
- Names and functions of components
- Cautions

How to Read This Manual It is assumed that the reader of this manual has general knowledge in the fields of electrical engineering, logic circuits, and microcontrollers. The IE-703037-MC-EM1 is used connected to the IE-703002-MC in-circuit emulator. This manual explains the basic setup procedure and switch settings of the IE-703002-MC when it is connected to the IE-703037-MC-EM1. For the names and functions of parts, and the connection of elements, refer to the IE-703002-MC User's Manual.

To learn about the basic specifications and operation methods
→ Read this manual in the order of the **CONTENTS**.

To learn the operation methods and command functions, etc., of the IE-703002-MC and IE-703037-MC-EM1
→ Read the user's manual of the debugger (sold separately) that is used.

Conventions

Note: Footnote for item marked with **Note** in the text

Caution: Information requiring special attention

Remark: Supplementary information

Numeral representation: Binary ... xxxx or xxxxB
Decimal ... xxxx
Hexadecimal ... xxxxH

Prefix indicating an exponent of 2 (address space, memory capacity):

K (kilo): $2^{10} = 1024$
M (mega): $2^{20} = 1024^2$

Terminology The meanings of terms used in this manual are listed below.

Target device	The device that is targeted for emulation.
Target system	The system (user-built system) that is targeted for debugging. This includes the target program and user-configured hardware.

Related Documents

When using this manual, refer to the following manual.

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

○ Documents related to development tools (User's Manual)

Document Name		Document Number
IE-703002-MC (In-circuit emulator)		U11595E
IE-703037-MC-EM1 (In-circuit emulator option board)		This manual
CA850 (C Compiler package)	Operation UNIX™ based	U12839E
	Operation Windows™ based	U12827E
	C language	U12840E
	Assembly Language	U10543E
	Project manager Windows-based	U11991E
ID850 (Integrated debugger)	Operation Windows-based	U13716E
RX850 (Real-time OS)	Basics	U13430E
	Technical	U13431E
	Installation	U13410E
RX850 Pro (Real-time OS)	Basics	U13773E
	Technical	U13772E
	Installation	U13774E
RD850 (Task debugger) ^{Note}		U11158E
RD850 (Ver.3.0) (Task debugger)		U13737E
AZ850 (System performance analyzer) Operation		U11181E

Note For ID850 (Ver. 1.31 only)

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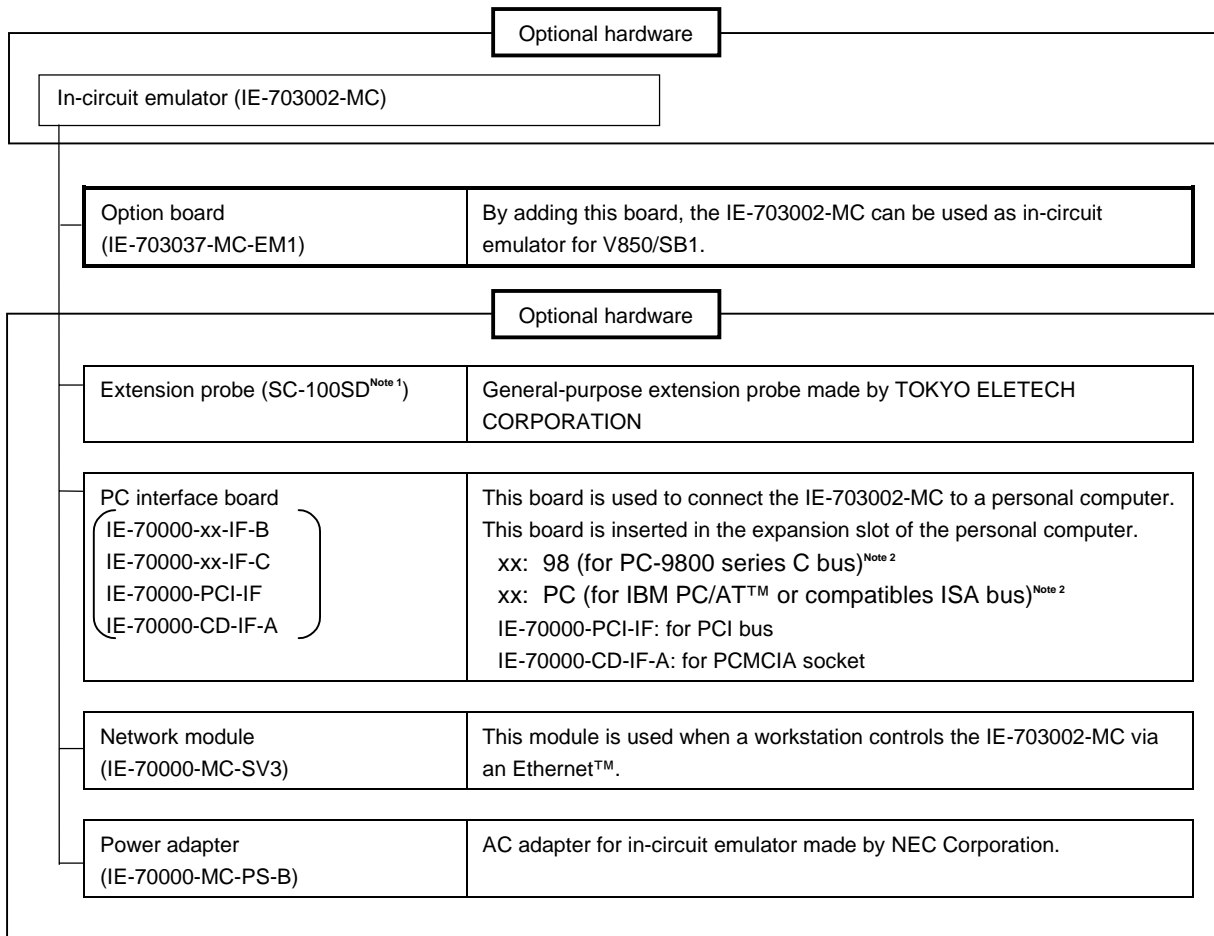
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CHAPTER 1 OVERVIEW

The IE-703037-MC-EM1 is an option board for the IE-703002-MC in-circuit emulator. By connecting the IE-703037-MC-EM1 and IE-703002-MC, hardware and software can be debugged efficiently in system development using the V850/SB1.

In this manual, the basic setup procedure and switch settings of the IE-703002-MC when using the IE-703037-MC-EM1 are described. For the names and functions of the parts of the IE-703002-MC, and for the connection of elements, refer to the **IE-703002-MC User's Manual**.

1.1 Hardware Configuration



- Notes**
- For further information, contact to Daimaru Kogyo Co., Ltd.
Tokyo Electronics Department (TEL +81-3-3820-7112)
Osaka Electronics Department (TEL +81-6-6244-6672)
 - Cannot be used for PC98-NX series

1.2 Features (When Connected to IE-703002-MC)

- Maximum operating frequency: 20 MHz (at 3.3 to 5.0-V operation)
- Extremely lightweight and compact
- Higher equivalence with target device can be achieved by omitting buffer between signal cables.
- The following pins can be masked.
RESET, NMI, WAIT, HLDRQ
- Two methods of connection to target system:
 - Pod tip direct connection (For information on the pod, refer to the **IE-703002-MC User's Manual**)
 - Attach an extension probe (sold separately) to the pod tip for connection
- The dimensions of the IE-703037-MC-EM1 are as follows.

Parameter		Value
Power consumption (Max. value at 3.3-V supply voltage)		0.35 W (at 20-MHz operation frequency) ^{Note}
External dimensions (Refer to APPENDIX PACKAGE DRAWINGS)	Height	15 mm
	Length	194 mm
	Width	96 mm
Weight		160 g

Note 10.35 W when IE-703002-MC connected to IE-703037-MC-EM1

1.3 Function Specifications (When Connected to IE-703002-MC)

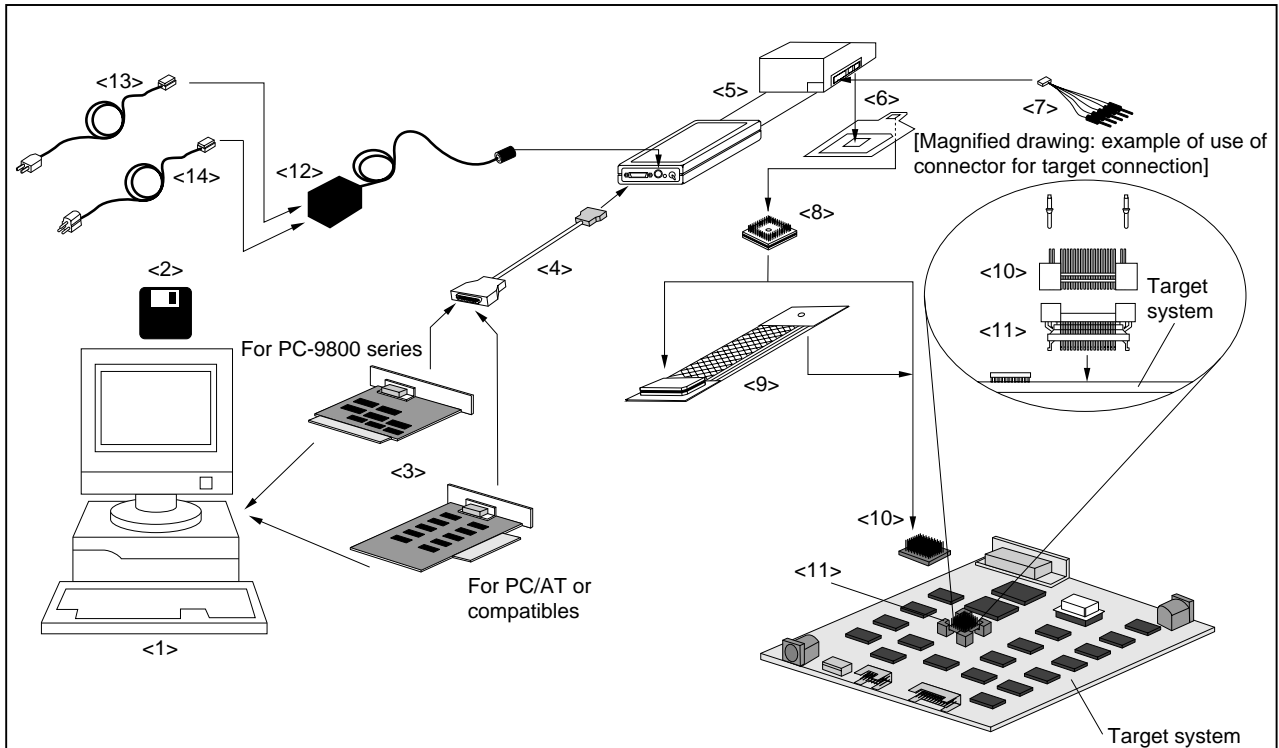
Parameter		Specification	
Emulation memory capacity	Internal ROM	256 Kbytes	
	External memory	In ROM-less mode	2 Mbytes
		When using iROM	1 Mbyte
Execution/pass detection coverage memory capacity	Internal ROM	256 Kbytes	
	External memory	In ROM-less mode	2 Mbytes
		When using iROM	1 Mbyte
Memory access detection coverage memory capacity (external memory)		1 Mbyte	
Coverage memory capacity for branching entry number counting	Internal ROM	256 Kbytes	
	External memory	In ROM-less mode	2 Mbytes
		When using iROM	1 Mbyte

Caution Some of the functions may not be supported, depending on the debugger used.

1.4 System Configuration

The system configuration when connecting the IE-703002-MC to the IE-703037-MC-EM1 and a personal computer (PC-9800 series or PC/AT™ (or compatibles)) is shown below.

Figure 1-1. System Configuration



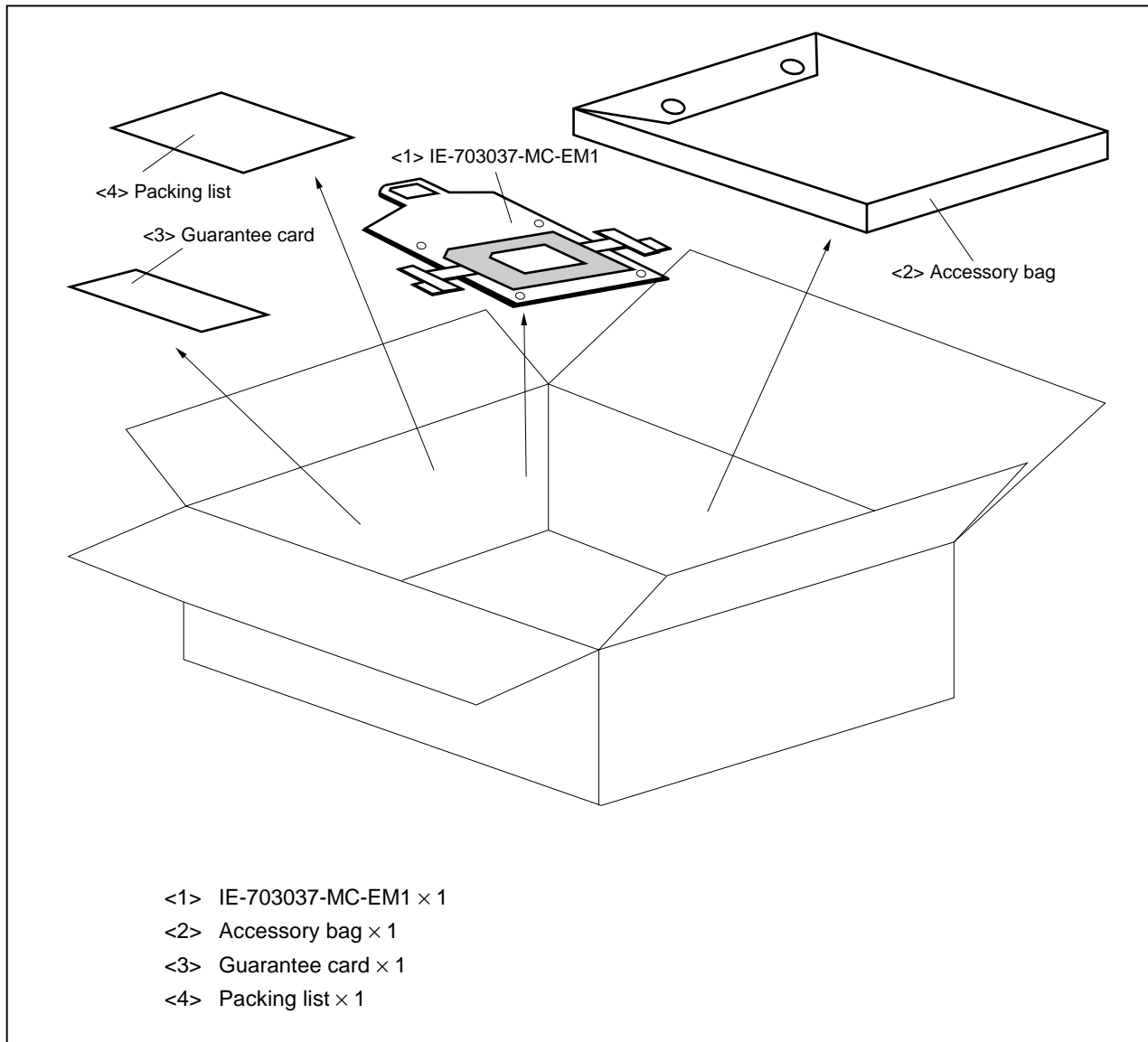
Remark

- <1> Personal computer (PC-9800 series or PC/AT or compatibles)
- <2> Debugger (sold separately)
- <3> PC interface board
(IE-70000-98-IF-B/IE-70000-98-IF-C, IE-70000-PC-IF-B/IE-70000-PC-IF-C: sold separately)
- <4> PC interface cable (included with IE-703002-MC)
- <5> In-circuit emulator (IE-703002-MC: sold separately)
- <6> In-circuit emulator option board (IE-703037-MC-EM1)
- <7> External logic probe (included with IE-703002-MC)
- <8> Socket for target connection (YQSOCKET100SDN: included with IE-703002-MC)
- <9> Extension probe (SC-100SD: sold separately)
- <10> Connector for emulator connection (YQPACK100SD: included in IE-703002-MC)
- <11> Connector for target connection (NQPACK100SD: included)
- <12> Power adapter (IE-70000-MC-PS-B : sold separately)
- <13> AC100-V power cable (sold separately: included with IE-70000-MC-PS-B)
- <14> AC220-V power cable (sold separately: included with IE-70000-MC-PS-B)

1.5 Contents in Carton

The carton of the IE-703037-MC-EM1 contains a main unit, guarantee card, packing list, and accessory bag. Make sure that the accessory bag contains this manual and the connector accessories. If there are missing or damaged items, please contact an NEC sales representative or an NEC distributor.

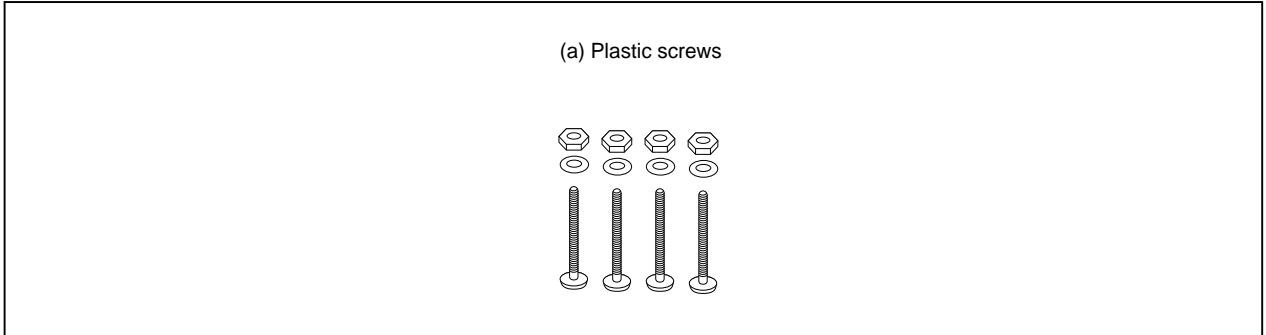
Figure 1-2. Contents in Carton



Check that the accessory bag contains this manual, an accessory list, and the following accessories.

- (a) Plastic screws × 4
(including nuts and washer × 4 sets)

Figure 1-3. Accessories



1.6 Connection between IE-703002-MC and IE-703037-MC-EM1

The procedure for connecting the IE-703002-MC and IE-703037-MC-EM1 is described below.

Caution Connect carefully so as not to break or bend connector pins.

- <1> Remove the pod cover (upper and lower) of the IE-703002-MC.
- <2> Set the PGA socket lever of the IE-703037-MC-EM1 to the OPEN position as shown in Figure 1-4 (b).
- <3> Connect the IE-703037-MC-EM1 to the PGA socket at the back of the IE-703002-MC pod (refer to Figure 1-4 (c)). When connecting, position the IE-703002-MC and IE-703037-MC-EM1 so that they are horizontal.
- <4> Set the PGA socket lever of the IE-703037-MC-EM1 to the CLOSE position as shown in Figure 1-4 (b).
- <5> Set the IE-703002-MC pod jumpers (JP1 to JP4).
 - Open JP1 (Remove the jumper contact and attach the removed jumper contact to one of the jumper pins to avoid losing it.)
 - Retain the factory settings of JP2 (pins 1 and 2 shorted, and pins 5 and 6 shorted).
 - Short pins 1 and 2 of JP3.
 - Retain the factory settings of JP4 (pins 2 and 3 shorted).
- <6> Fix the IE-703037-MC-EM1 between the IE-703002-MC pod covers (upper and lower) with the plastic screws (supplied with the IE-703002-MC).
- <7> Fix the IE-703002-MC pod cover (upper) end with nylon rivets.

Remark For the JP1 setting, refer to **2.3 Illegal Access Detection ROM Setting**. For JP3 and JP4, refer to **2.4 CPU Operation Voltage Range Switch Setting**.

Figure 1-4. Connection between IE-703002-MC and IE-703037-MC-EM1 (1/2)

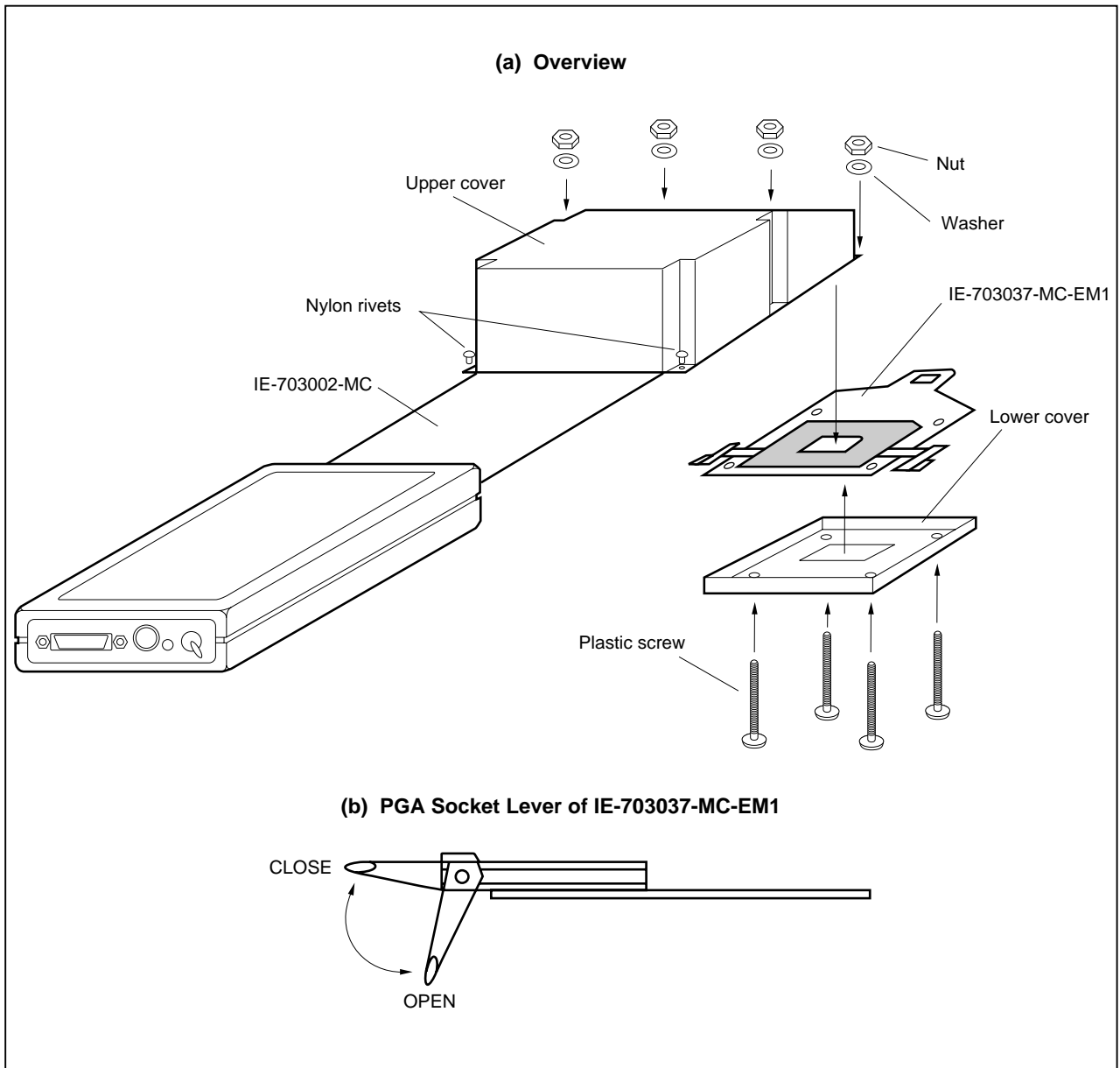
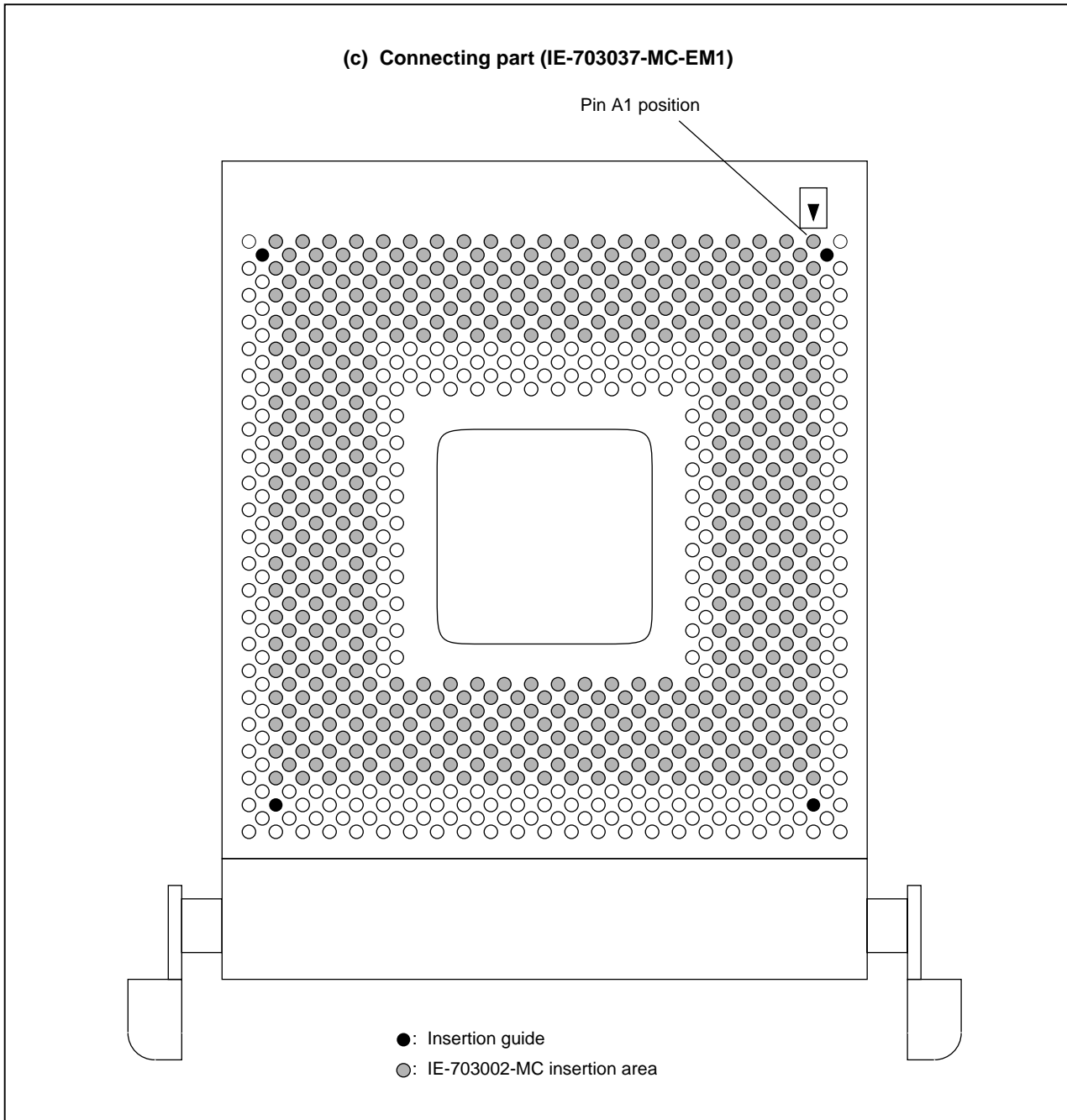


Figure 1-4. Connection between IE-703002-MC and IE-703037-MC-EM1 (2/2)

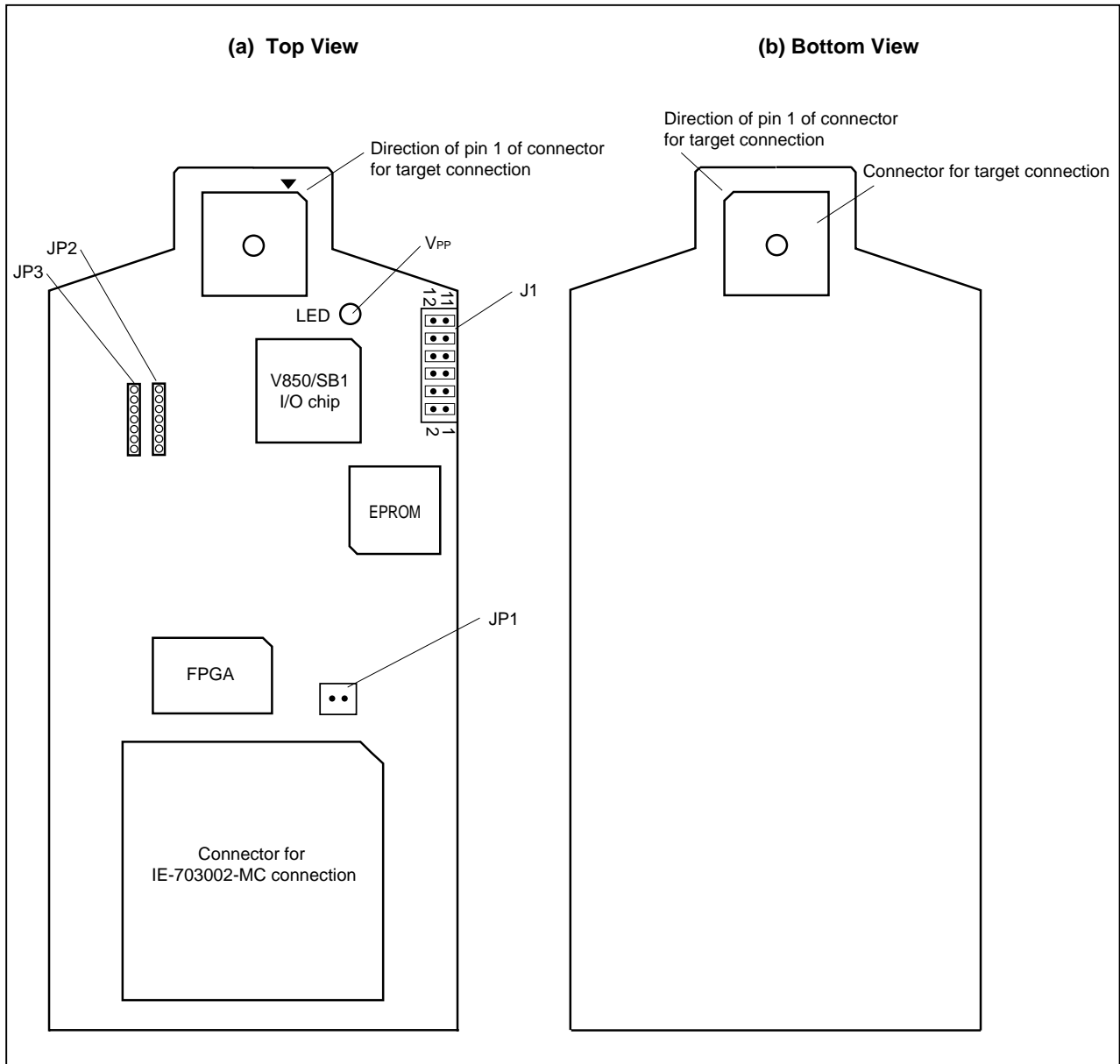


CHAPTER 2 NAMES AND FUNCTIONS OF COMPONENTS

This chapter describes the names, functions, and switch settings of components in the IE-703037-MC-EM1. For the details of the pod, jumper, and switch positions, etc., refer to the **IE-703002-MC User's Manual**.

2.1 Component Names and Functions of IE-703037-MC-EM1

Figure 2-1. IE-703037-MC-EM1



(1) JP1

This is the jumper switch for product check. Leave open.

(2) JP2

This is the switch jumper of the main system clock supply source. (For details, refer to **2.2 Clock Settings**)

(3) JP3

This is a pin board for supplying the subsystem clock. (For details, refer to **2.2 Clock Settings**)

(4) LED

LED for V_{PP}

ON: Voltage is applied to V_{PP}

OFF: Voltage is not applied to V_{PP}

(5) Connector for IE-703002-MC connection

This is a connector for connecting with the IE-703002-MC.

(6) Connector for target connection

This is a connector for connecting with the target system or the extension probe.

2.2 Clock Settings

This section describes the clock settings.

For JP1 and JP2 position in the IE-703037-MC-EM1, refer to Figure 2-1.

For the jumper switch position in the IE-703002-MC, refer to the **IE-703002-MC User's Manual**.

2.2.1 Main system clock setting

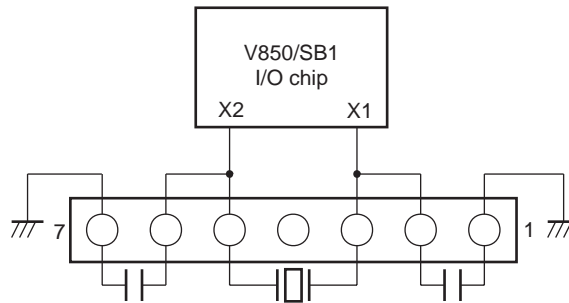
Table 2-1. Main System Clock Setting

Emulator Use Environment	Clock Supply Method	IE-703037-MC-EM1 Setting	IE-703002-MC Setting		
		JP2	SW1	SW2	JP2
When using emulator as standalone unit	Internal clock ^{Note 1}	Oscillator mounted (a 20-MHz oscillator is mounted when shipped) ^{Note 2}	ON	ON	

Notes 1. A target clock is not supported.

2. To use a main system clock frequency other than 20 MHz, remove the oscillator on JP2 and mount any oscillator.

The specifications of JP2 are as follows.

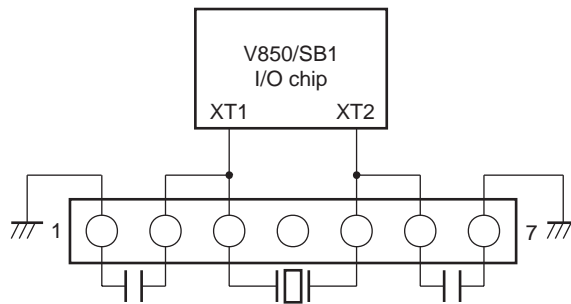


2.2.2 Subsystem clock setting

Table 2-2. Subsystem Clock Setting

Emulator Use Environment	Clock Supply Method	IE-703037-MC-EM1 Setting
		JP3
When using emulator as standalone unit	Internal clock ^{Note 1}	Oscillator mounted (a 32.768-kHz oscillator is mounted when shipped) ^{Note 2}

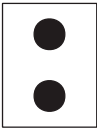
- Notes**
1. A target clock is not supported. Internal clock does not support the clock input by oscillator.
 2. To use a subsystem clock frequency other than 32.768 kHz, remove the oscillator on JP3 and mount any oscillator.
The specifications of JP3 are as follows.



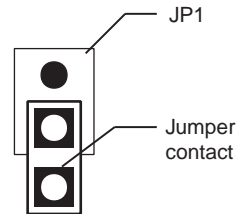
2.3 Illegal Access Detection ROM Setting

If using the IE-703002-MC for an in-circuit emulator for the V850/SB1 by connecting the IE-703037-MC-EM1, set JP1 of the IE-703002-MC as follows.

Table 2-3. JP1 Setting in IE-703002-MC

JP1		Description
Open ^{Note}		Illegal Access Detection ROM (mounted on IE-703037-MC-EM1) for V850/SB1 is used.

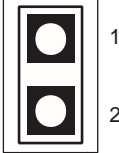

Note When JP1 is set open, keep the removed jumper contact attached to one pin as shown in the drawing on the right.



2.4 CPU Operation Voltage Range Switching Setting

If using the IE-703002-MC for an in-circuit emulator for the V850/SB1 by connecting the IE-703037-MC-EM1, set JP3 and JP4 of the IE-703002-MC as follows.

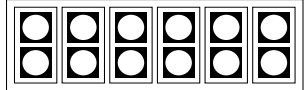
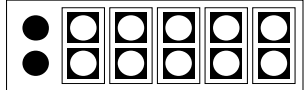
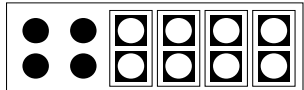
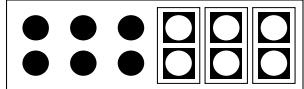
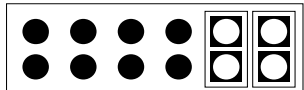
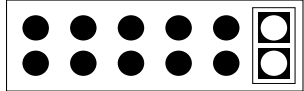
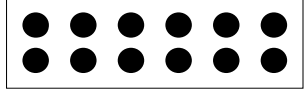
Table 2-4. JP3 and JP4 Setting in IE-703002-MC

JP3, JP4	
JP3	 <p>1 2</p> <p>(Short)</p>
JP4	 <p>1 2 3</p>


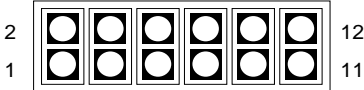
2.5 Separate Bus Function Setting

To use the separate bus function, J1 of the IE-703037-MC-EM1 must be set. Table 2-5 shows the correspondence between the MAM register and J1 settings.

Table 2-5. MAM Register and J1 Setting Correspondence

MAM2	MAM1	MAM0	Operation of P34 to P36, P100 to P107, P110 to P113		J1 Setting
0	0	0	P34 to P36	Port mode	
			P100 to P107	Port mode	
			P110 to P113	Port mode	
0	1	0	P34 to P36	Port mode	
			P100 to P107	Port mode	
			P110 to P113	A1 to A4	
0	1	1	P34 to P36	Port mode	
			P100 to P103	A5 to A8	
			P104 to P107	Port mode	
			P110 to P113	A1 to A4	
1	0	0	P34 to P36	Port mode	
			P100 to P107	A5 to A12	
			P110 to P113	A1 to A4	
1	0	1	P34	A13	
			P35, P36	Port mode	
			P100 to P107	A5 to A12	
			P110 to P113	A1 to A4	
1	1	0	P34, P35	A13, A14	
			P36	Port mode	
			P100 to P107	A5 to A12	
			P110 to P113	A1 to A4	
1	1	1	P34 to P36	A13 to A15	
			P100 to P107	A5 to A12	
			P110 to P113	A1 to A4	

CHAPTER 3 FACTORY SETTINGS

Item	Description	Remark
JP1		Jumper switch for product check
JP2	Oscillator mounted	20-MHz clock supplied for main system clock.
JP3	Oscillator mounted	32.768-kHz clock supplied for subsystem clock.
J1		Set to port mode (P34 to P36, P100 to P107, P110 to P113)

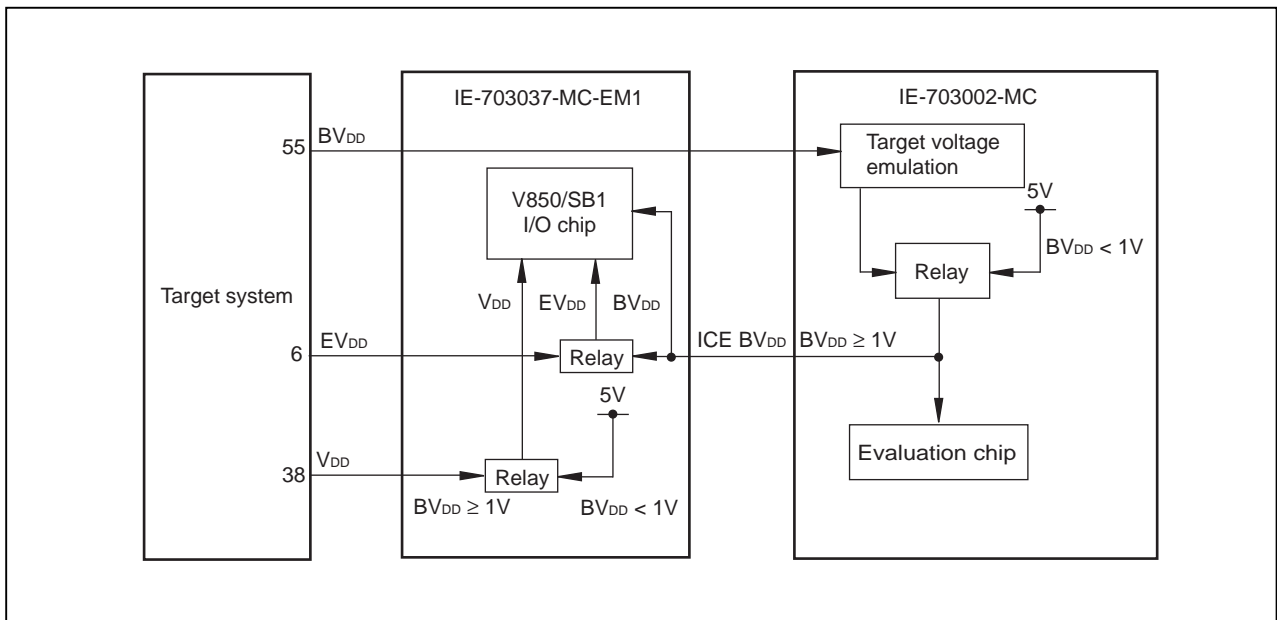
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CHAPTER 4 CAUTIONS

4.1 V_{DD} , BV_{DD} , and EV_{DD} of Target System

- (1) BV_{DD} in the target system is not connected to BV_{DD} in the evaluation chip in the IE-703002-MC.
The IE-703002-MC uses BV_{DD} of the target system for the following purposes:
 - Power ON/OFF detection of target system
 - BV_{DD} emulation of target system
- (2) When the BV_{DD} voltage of the target system is 1 V or higher, the evaluation chip in the emulator operates using the supply of V_{DD} and EV_{DD} from the target system. The power consumption is equivalent to that of the V850/SB1.
- (3) When the BV_{DD} voltage of the target system is lower than 1 V, the emulator recognizes the target system power is off and operates at $V_{DD} = BV_{DD} = EV_{DD} = 5.0$ V.

Figure 4-1. Schematic Diagram of Power Supply Acquisition

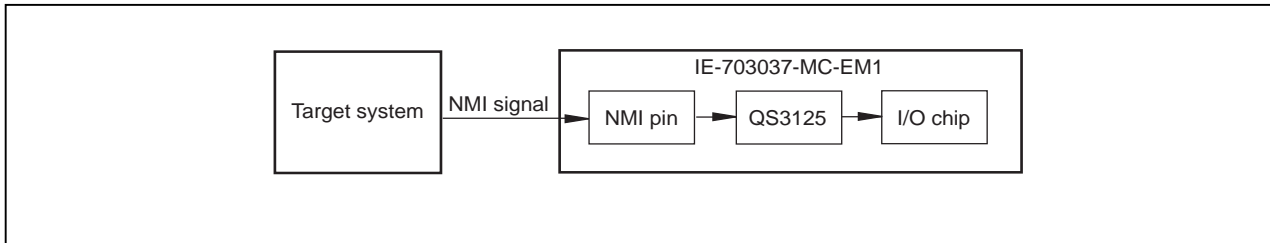


4.2 NMI Signal

The input signal (NMI signal) from the target system is delayed ($t_{pD} = 0.25$ ns (TYP.)) because it passes through QS3125 (Q switch) before it is input to the I/O chip of the emulator.

In addition, the DC characteristics change. The input voltage becomes $V_{IH} = 2.0$ V (MIN.), and $V_{IL} = 0.8$ V (MAX.). The input current becomes $I_{IN} = \pm 0.5$ μ A (MAX.).

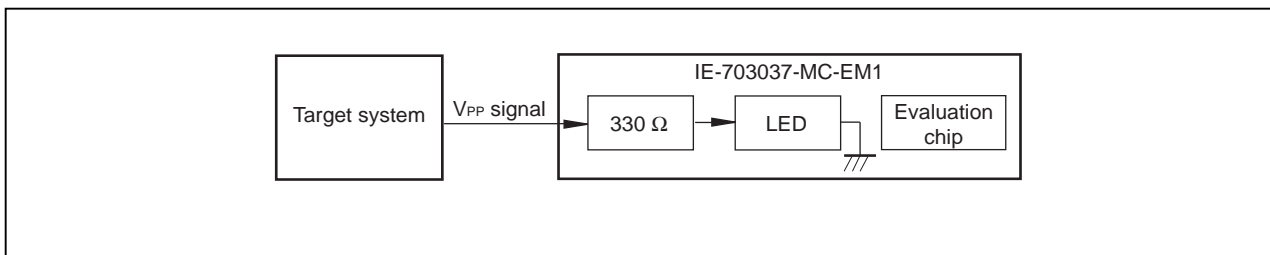
Figure 4-2. NMI Signal Flow Path



4.3 V_{PP} Signal

The V_{PP} signal from the target system is connected to LED via a 330- Ω resistor in the emulator. It is not connected to the evaluation chip in the emulator.

Figure 4-3. V_{PP} Signal Flow Path



4.4 MAM Register

Debugging of the MAM register cannot be performed in the emulator. If debugging the MAM register with software, proceed with care.

In the target device, ports can be used as address buses by setting values to the MAM register (address: FFFFF068H), which is mapped in the internal peripheral I/O area, using software (separate bus function). In the emulator, however, switching to the separate bus through a MAM register setting by software is impossible.

To use the separate bus function, set the J1 jumper in advance. (Refer to **2.5 Separate Bus Function Setting**)

4.5 NMI Signal Mask Function

When using the P00/NMI pin in the port mode, do not mask the NMI signal.

4.6 Bus Interface Pin

The operation of the pin for the bus interface differs between the emulator and the target device as follows.

Table 4-1. Bus Interface Pin Operation List (1/2)
(a) During break

Pin Name	Internal Memory							External Memory				
	Memory Used by Emulator			Internal ROM	Internal RAM		Internal Peripheral I/O		Emulation RAM		Target System	
	F	R	W	R	R	W	R	W	R	W	R	W
A16 to A21	Hold the last accessed address							Active		Active		
AD0 to AD15	Hi-Z							Active		Active		
ASTB	H							Active		Active		
$\overline{R/W}$	H							Active		Active		
\overline{DSTB}	H							H		Active		
\overline{LBEN}	H							Active		Active		
\overline{UBEN}	H							Active		Active		
\overline{WAIT}	Invalid							Maskable		Maskable		
\overline{HLDRQ}	Maskable							Maskable		Maskable		
\overline{HLDAK}	H or L							H or L		H or L		
\overline{WRL}	H							H		H	Note	
\overline{WRH}	H							H		H	Note	
\overline{RD}	H							H		Note	H	

Note Active

- Remarks**
- F: Fetch

R: Read

W: Write
 - H: High-level output

L: Low-level output

Hi-Z: High-impedance

**Table 4-1. Bus Interface Pin Operation List (2/2)
(b) During run**

Pin Name	Internal Memory							External Memory					
	Internal ROM		Internal RAM			Internal Peripheral I/O		Emulation RAM			Target System		
	F	R	F	R	W	R	W	F	R	W	F	R	W
A16 to A21	Hold the last accessed address							Active			Active		
AD0 to AD15	Hi-Z							Active			Active		
ASTB	H							Active			Active		
$\overline{R/W}$	H							Active			Active		
\overline{DSTB}	H							H			Active		
\overline{LBEN}	H							Active			Active		
\overline{UBEN}	H							Active			Active		
\overline{WAIT}	Invalid							Maskable			Maskable		
\overline{HLDRQ}	Maskable							Maskable			Maskable		
\overline{HLDAK}	H or L							H or L			H or L		
\overline{WRL}	H							H			H		Note
\overline{WRH}	H							H			H		Note
\overline{RD}	H							H			Note		H

Note Active

- Remarks**
- F: Fetch

R: Read

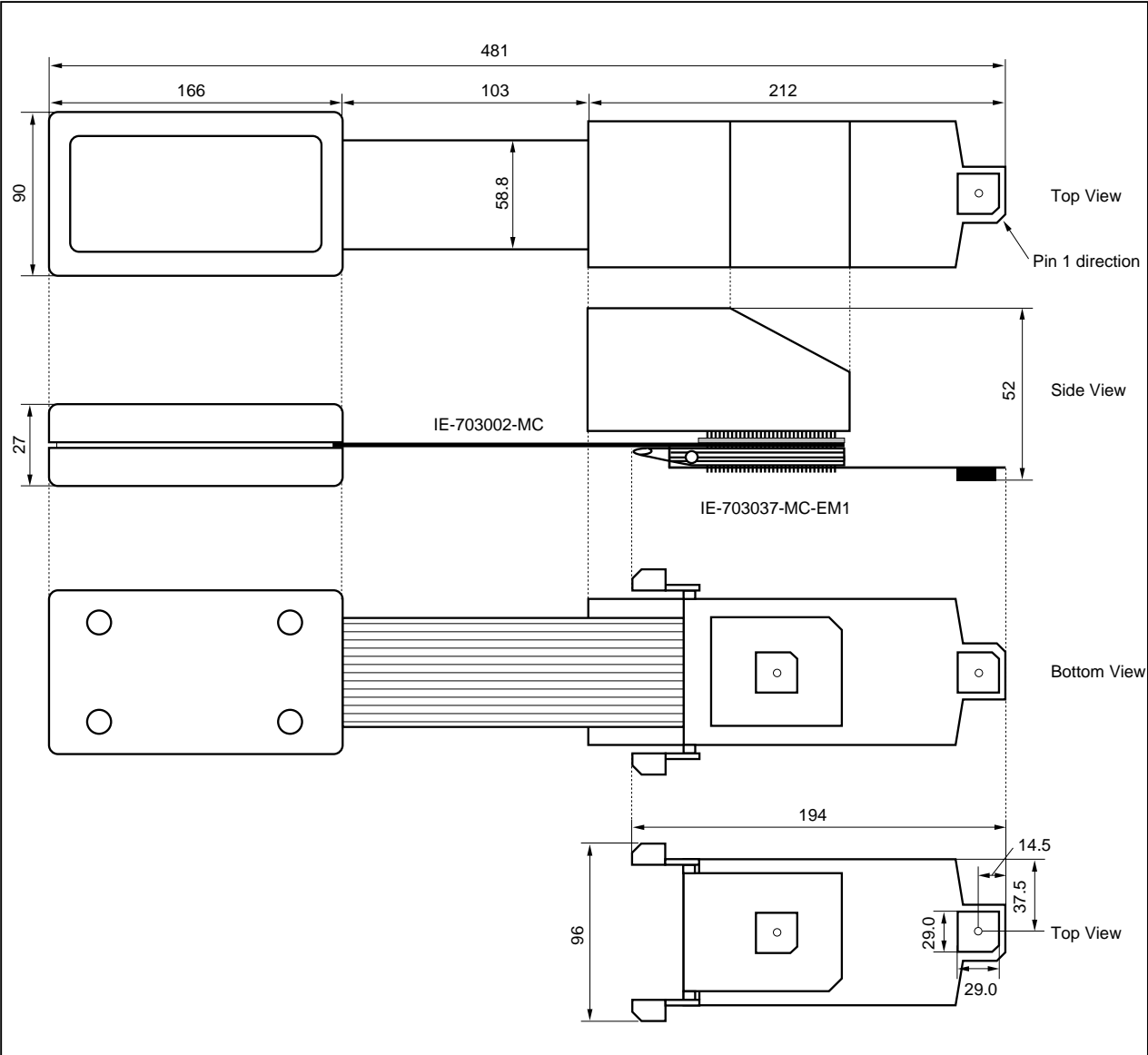
W: Write
 - H: High-level output

L: Low-level output

Hi-Z: High-impedance

APPENDIX PACKAGE DRAWINGS

IE-703002-MC + IE-703037-MC-EM1 (Unit: mm)



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