AK130/131

TCM Integrated Transceiver

Features

- Completely integrated baseband transceiver for 2-wire twisted pair applications
- 2B+1D+1M channels of PCM-BUS framed data, using time compression multiplexing
- Data rate: 160kbps (2B+1D+1M)
- Loop coverage: 1 km (AK130) / 2 km (AK131)
- Pin compatible between AK130 and AK131
- Low amplitude pulse-shaped Alternate Mark Inversion (AMI) coding for reduced spectral radiation
- Differential receiver architecture for highly reliable data recovery
- Bit error rate less than 10^{-7}
- PCM and Microprocessor ports that are pin selectable for single or combined port operation
- Operates on a single +5 V power supply and draws only 75 mW active power (typ)
- Package: 24 pin SOP

Block Diagram

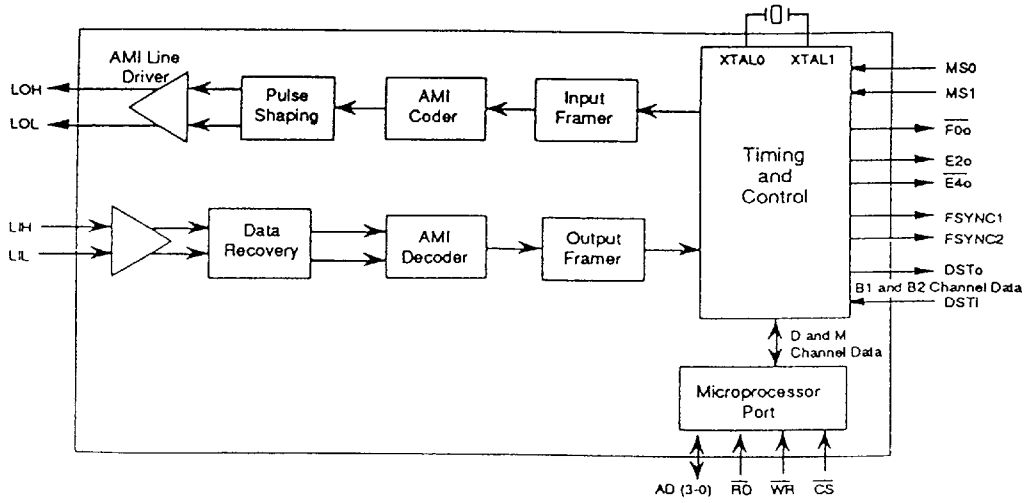


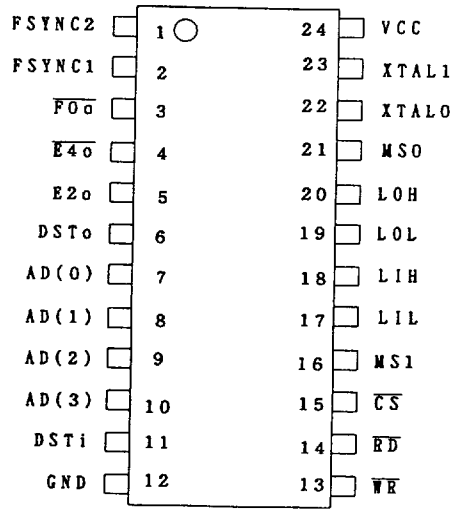
Fig-1 Block Diagram

General Description

The AK130/131 is a fully integrated transceiver for high-speed data transmission over unshielded twisted-pair subscriber loops. The device transmits at 160 kbps (line rate 512 kbps) over a single twisted pair wire, using a Time Compression Multiplex (TCM) transmission scheme.

The AK130/131 provides transparent, burst mode transmission of 2B+1D+1M channels in subscriber loop applications, typically KTS or PBX systems. It operates up to 1 km (AK130) / 2 km (AK131) on 0.5 mm (24 AWG) LOCAP station cable. The AK130/131 is designed for use in Slave-only, Terminal Equipment (TE) and is suited for use with most industry standard codecs. It uses a 2048 kbps synchronous serial PCM-BUS.

Pin assignment



Ordering information

AK130-VS	24 pin SOP
AK131-VS	24 pin SOP

Pin / Function

Pin #	Symbol	I/O	Function
1	FSYNC2	O	With F1-type sync (MS0=1), these pins go low to indicate that the associated B channel is active on the PCM-BUS. With FS-type sync (MS0=0), a 244 ns-wide positive pulse is output on these pins, 488 ns before start of the associated B channel. With HFS-type sync (MS0=E2o), a 244 ns-wide positive pulse is output on these pins, 244 ns before start of the associated B channel.
2	FSYNC1	O	
3	$\overline{F0o}$	O	An 8 kHz, 244-ns wide active low pulse output, indicating the start of the device's active channel times.
4	$\overline{E4o}$	O	A 4.096MHz output clock derived from the crystal oscillator.
5	E2o	O	A 2.048MHz output clock derived from the crystal oscillator.
6	DSTo	O	A 2.048 Mbps serial PCM-BUS output. In single port mode, this bus contains the B, D, and M channel data received from the line input. In the combined port mode only the B channel data is carried on the PCM-BUS.
7 8 9 10	AD(0) AD(1) AD(2) AD(3)	I/O I/O I/O I/O	Bidirectional microprocessor data bus. These lines are inactive in the single port mode. In the combined port mode they carry D and M channel data.
11	DSTi	I	Input line for the 2.048 Mbps serial PCM-BUS. In single port mode, this bus contains the B, D, and M channel data to be transmitted on the line. In the combined port mode only the B channel data is carried on the PCM-BUS.
12	GND	-	Ground.
13	$\overline{WR}$	I	Active low input to enable microprocessor port write.
14	$\overline{RD}$	I	Active low input to enable microprocessor port read.
15	$\overline{CS}$	I	Active low chip select signal to enable microprocessor port.
16	MS1	I	A high on this pin selects the single port mode. In single port mode, D, M, and B channel data are carried on the PCM-BUS. A low in this pin selects the combined port mode. In this mode D and M channel data are carried by the microprocessor port, and B channel data is carried by the PCM port.
17 18	LIL LIH	I I	Differential Receive Inputs. These inputs are insensitive to the polarity of the receive signal.
19 20	LOL LOH	O O	Differential Driver Outputs. Idle level at these outputs is VCC/2. A positive mark results in a voltage of VCC/2 + 1.25 V at LOH and VCC/2 - 1.25 V at LOL.
21	MS0	I	Frame Sync Select Signal. When MS0=1, AK130/131 produces F1-type frame sync signals on FSYNC1 and FSYNC2. When MS0=0, AK130/131 produces FS-type frame sync signals. When MS0 is connected to the E2o pin, AK130/131 produces HFS-type frame sync signals.

Pin #	Symbol	I/O	Function
22	XTAL0	I	Crystal oscillator or external clock input (8.192 MHz). If an external TTL clock is used, it must be coupled through a 0.1μF capacitor. An external CMOS clock may be connected directly.
23	XTAL1	O	Crystal oscillator output. This pin is not connected if an external clock is used.
24	VCC	-	+5 VDC power supply input.

Absolute Maximum Ratings

Parameter	Symbol	min	max	units
Supply Voltage	V_{CC}	-0.3	7.0	V
Voltage on any I/O pin	$V_{I/O}$	GND - 0.3	V_{CC} + 0.3	V
Current on any I/O pin	$I_{I/O}$	-50	50	mA
Package power dissipation	P_D		600	mW
Storage Temperature	T_{st}	-65	150	℃

Warning: Exceeding absolute maximum ratings may cause permanent damage.
Normal operation is not guaranteed at these extremes.

Operating Conditions

Voltages are with respect to ground (GND) unless otherwise stated.
Typical figures are at 25 ℃ and are for design aid only, not guaranteed and not subject to production testing.

Parameter	Symbol	min	typ	max	unit	Condition
Supply Voltage	V_{CC}	4.75	5	5.25	V	
Operating Temperature	T_{OP}	0		70	℃	

■ DC Electrical Characteristics – Clocked operation over recommended temperature and power supply ranges.

Parameter	Symbol	min	typ	max	unit	Condition
Supply current(Transmitting a space)	I_{CC}	-	-	11.5	mA	15pF load
Supply current(Transmitting a mark)	I_{CC}	-	-	15	mA	15pF load
Input high voltage	V_{IH}	2.0	-	-	V	Note-2
Input low voltage	V_{IL}	-	-	0.8	V	Note-2
Output high voltage	V_{OH}	2.4	-	-	V	I_{OH}=40μA
Output low voltage	V_{OL}	-	-	0.4	V	I_{OL}=1.6mA
Output high voltage	V_{OH}	4.6	-	-	V	I_{OH}=10μA
Output low voltage	V_{OL}	-	-	0.4	V	I_{OL}=10μA
Output high current	I_{OH}	-	-	40	μA	V_{OH}=2.4V
Output low current	I_{OL}	-	-	1.6	mA	V_{OL}=0.4V
Input leakage current (Note-1)	I_{LL}	-	±1	±10	μA	Note-3

Note-1: And output buffer leakage, when tristated.
Note-2: Digital input
Note-3: Input between VCC and GND

■ AC Electrical Characteristics – Clock timing (Note-1); Crystal or Digital Clock Input

Parameter	Symbol	min	typ	max	unit	Condition
Operating frequency	f_C	-	8.192	-	MHz	
Frequency tolerance	T_C	-	-	±1000	ppm	
Clock duty cycle		40	50	60	%	

Note-1: TTL clock signals on XTAL0 must be coupled through a 0.1 μF capacitor.

■ Analog Characteristics

Parameter	Symbol	min	typ	max	unit	Condition
Transmit differential amplitude	V_{AO}	2.2	2.5	2.8	Vp	RL=800Ω
Transmit common mode offset	XCMR	0	-	±75	mV	Note-1
Transmit pulse output rise/fall time	T_{DRF}	-	-	400	ns	
Receive differential input amplitude	V_{AI}	0.35	-	1.5	V	

Note-1: Relative to VCC/2

■ AC Electrical Characteristics: PCM-BUS Timing (See Fig-2)

Timing figures are over recommended temperature and power supply voltages.

Parameter	Symbol	min	typ	max	unit	Condition
F0o output pulse width	tFLFH	-	244	-	ns	15pF Load
E4o to F0o delay	tEHFE	-20		20	ns	15pF Load
E4o output clock period	t4L4L	-	244	-	ns	15pF Load
E4o pulse width high or low	t4E4E	-	122	-	ns	15pF Load
E2o output clock period	t2H2H	-	488	-	ns	15pF Load
E2o pulse width high or low	t2E2E	-	244	-	ns	15pF Load
FSYNC, F0o, E4o, E2o transition time	tRF	-	-	11	ns	15pF Load
FS pulse to E2o clock transition	tSHEL	50	-	-	ns	15pF Load
E2o fall to FS pulse fall	tELSL	100	-	-	ns	15pF Load
FS mode pulse width	tSHSL	-	244	-	ns	15pF Load
HFS pulse to E2o clock transition	tHHEH	50	-	-	ns	15pF Load
E2o rise to HFS pulse fall	tEHHL	100	-	-	ns	15pF Load
HFS mode pulse width	tHHHL	-	244	-	ns	15pF Load
$\overline{F1o}$ pulse to E2o clock transition	t1LEH	50	-	-	ns	15pF Load
E2o fall to $\overline{F1o}$ pulse rise	tEL1H	100	-	-	ns	15pF Load
$\overline{F1o}$ mode pulse width	t1L1H	-	3906	-	ns	15pF Load
Serial input setup time	tDVEL	30	-	-	ns	
Serial input hold time	tELDX	50	-	-	ns	
Serial output delay	tEEDV	-	-	125	ns	15pF Load

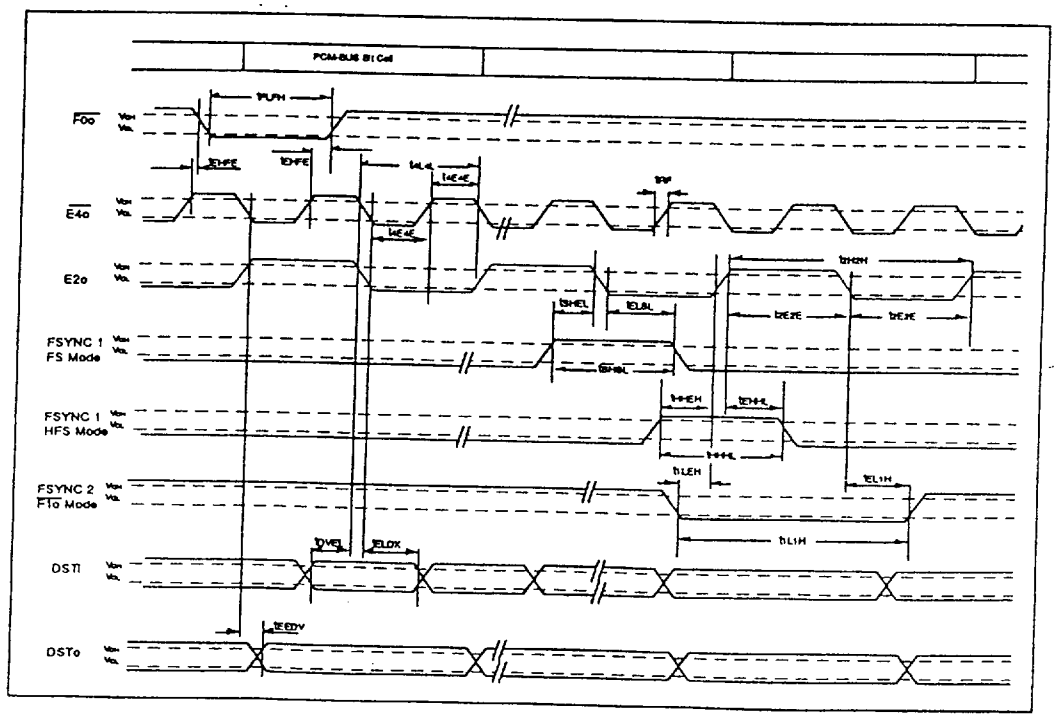


Fig-2 PCM-BUS Timing

■ AC Electrical Characteristics: Microprocessor Port Timing (See Fig-3 and Fig-4)

Timing figures are over recommended temperature and power supply voltages.

Parameter	Symbol	Min	Max	Unit	Condition
Data hold after Read or Chip Select	Trhdx	0	-	ns	15pF Load
Data float after Read or Chip Select	Trhdz	-	90	ns	15pF Load
Read or Chip Select to valid data	Trldv	-	90	ns	15pF Load
Data setup before Write or Chip Select	Tdvwh	40	-	ns	15pF Load
Data hold after Write or Chip Select	Twhdx	15	-	ns	15pF Load
Minimum pulse width $\overline{CS}$ and $\overline{WR}$	Twlwh	80	-	ns	15pF Load

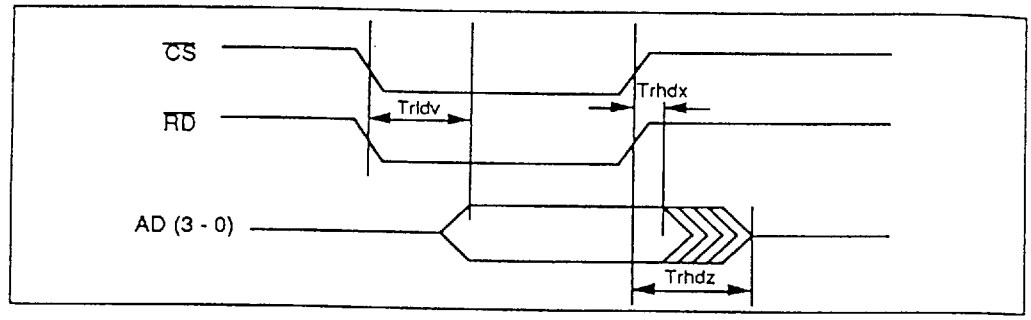


Fig-3 Microprocessor Port Read Cycle Timing

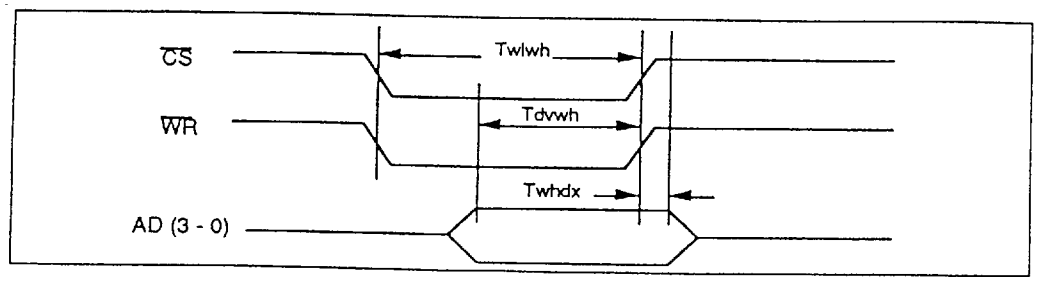


Fig-4 Microprocessor Port Write Cycle Timing

Functional Description

The AK130/131 is a high-speed 2-wire TCM transceiver for PBX and KTS systems. It provides 160 kbps for transparent transmission of 2B+D+M channels. It is clocked to produce self-contained AMI pulses at a line rate of 512 kbps. Designed for Terminal Equipment (TE) (Slave only), the AK130/131 allows effective full-duplex transmission of high-speed digital data over existing twisted-pair installations. The AK130/131 can operate over most customer premises wiring, ranging from 19 to 26 AWG. In typical systems (24 AWG), the AK130 is effective in subscriber loops of up to 1 km, and the AK131 is effective in subscriber loops of up to 2 km.

The transmission incorporates an 800 Ω fully differential line driver that, when coupled through two 200 Ω series termination resistors and a 2:1 step-down transformer, produces a peak line signal of 625 mV on a 100 Ω line from a single +5 V power supply. It uses AMI line coding for minimum spectral radiation and reduce RFI.

The receiver uses a fully differential architecture to reduce the effect of impulsive noise. The adaptive data slicers and peak detectors (AK130), or the adaptive equalizer (AK131), ensure optimum signal-to-noise ratio regardless of received signal strength. These design allow data recovery with a Bit Error Rate of less than 10^{-7} over the specific operating conditions.

The system interface includes a simple PCM port and a microprocessor port. The PCM port is compatible with a variety of codecs and data codecs, including the MT896x, MT8950, TP305x and TP306x. The PCM port is also compatible with the MT8994B and MT8995B integrated digital telephone chips, and remains active even if no data is received from the line. The microprocessor port is compatible with both multiplexed and non-multiplexed microprocessor buses.

Fig-1 is a simplified block diagram of the AK130/131. The signal received from the twisted-pair line is applied to the AK130/131 at LIH and LIL. This differential signal is processed, through the adaptive data slicer and peak detectors (AK130), or the adaptive equalizer (AK131), and then routed to the data recovery section. The recovered data signal is passed to the AMI decoder. Decoded data is then processed through the output framer to the PCM-BUS or microprocessor port registers.

■ Internal Timing

The AK130/131 incorporates an on-chip 8.192 MHz crystal oscillator which generates all internal clocks. It also produces two output clocks E4o (4.096 MHz) and E2o (2.048 MHz). These clocks can be used directly as input clocks for peripheral devices such as codecs or integrated digital telephone chips.

■ Line Code

The AK130/131 transmits data encoded in self-contained AMI pulses at an effective line rate of 512 kbps. A mark is defined as a voltage differential between LOH and LOL, rather than a specific ground-referenced voltage. LOH and LOL are both held at VCC/2 for a space. See Fig-5.

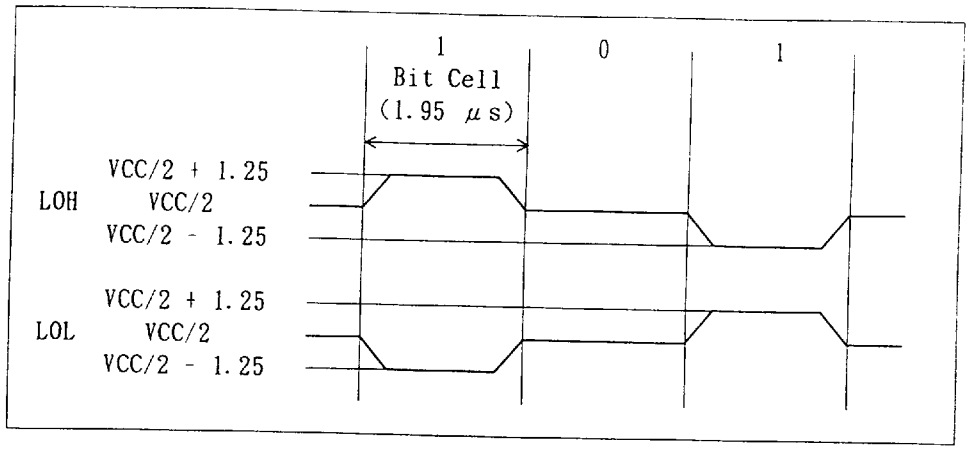


Fig-5 Self-Contained Rectangular AMI Bits

■ TCM Frame Format

The AK130/131 transmits and receives high speed digital data over twisted-pair loops using the 23-bit frame format shown in Fig-6. The 20 data bits are framed by the Start Bit (SB) on one end and two Space Bits (SP) on the other end. The 8 kHz line provides 160 kbps for transparent transmission of two 64 kbps B channels, one 16 kbps D channel and one 16 kbps control and maintenance channel (M channel). Both the D and M channel data are available either on the PCM-BUS or through the microprocessor port. B channel data is available only on the PCM-BUS.

■ Operating Modes

The AK130/131 operates in both single and combined port modes. Mode of operation is set by the MS1 level. When MS1 is set to 1, the AK130/131 operates in the single port mode and the microprocessor port is inactive. When MS1 is set to 0, the AK130/131 operates in the combined port mode with both the PCM-BUS and the microprocessor port active.

■ PCM-BUS

One system interface to the AK130/131 is the flexible PCM-BUS. The PCM-BUS is a synchronous time-division multiplexed serial bus with data streams operating at 2048 kbps. The serial streams are divided into 125 μ sec frames made up of 32 8-bit channels. Synchronization is achieved with an 8 kHz frame pulse (F0o) which identifies the framing boundaries as shown in Fig-7. Data is clocked into the device on the falling edge of the E4o clock, halfway into the bit cell. Data is clocked out on the falling edge of the E4o clock at the start of the bit cell.

The AK130/131 uses only four of the 32 channels available in each PCM-BUS frame. In single port mode, the D channel occupies time slot 0; the M channel occupies time slot 1; and the B1 and B2 channels occupy time slot 2 and 3, respectively, as shown in Fig-8. In combined port mode, time slots 0 and 1 are not used; the B1 and B2 channels occupy time slots 2 and 3.

FSYNC1 and FSYNC2 can be set to $\overline{F1}$-, FS- or HFS-type sync pulses by the MS0 pin.

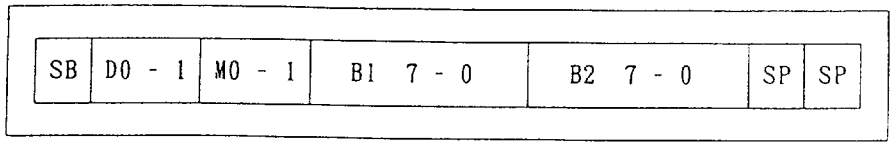


Fig-6 TCM Frame Format

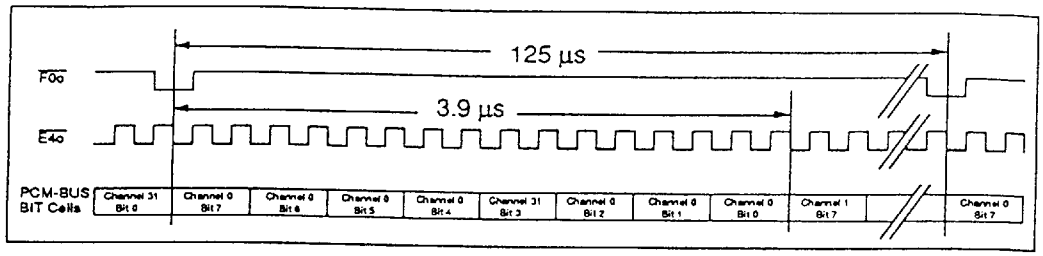


Fig-7 PCM-BUS Stream Format Diagram

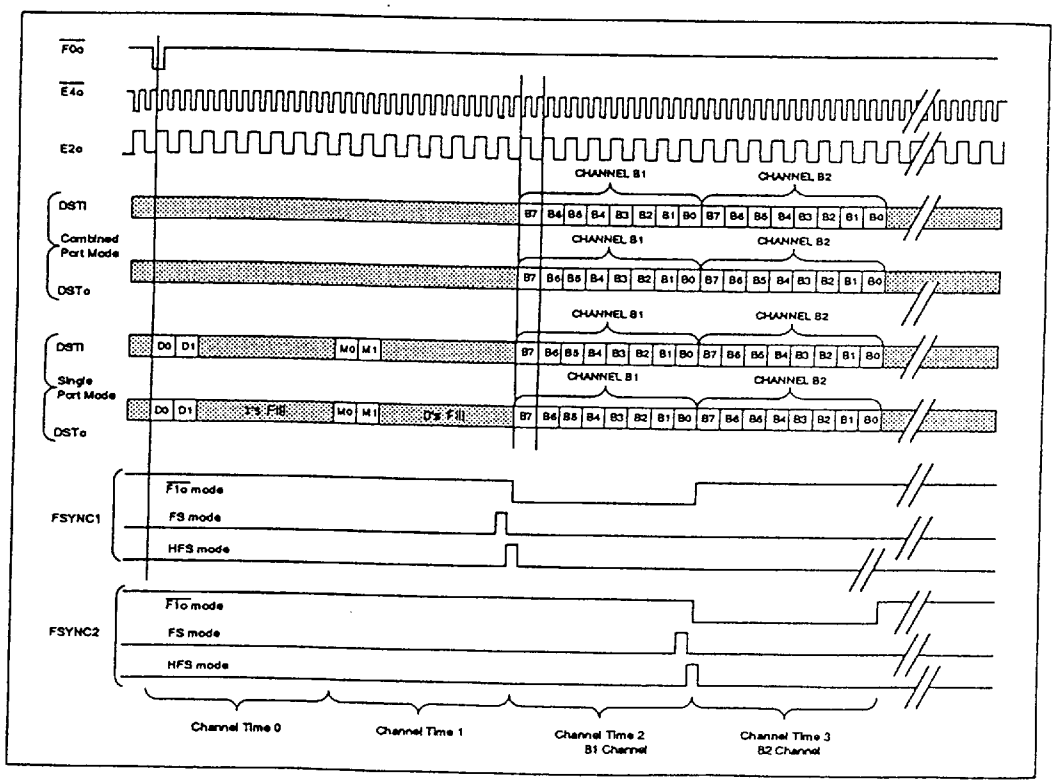


Fig-8 PCM-BUS Allocation

■ Microprocessor Port Operation

The microprocessor port is active only in combined port operation. This mode is selected by setting the MS1 pin low. In this mode the two bits from the D channel and the two bits from the M channel are accessed in a common 4-bits nibble. The bandwidth of the two channels can be combined to form an uncommitted 32 kbps channel, or divided into sub-rate channels to meet specific applications. The bit order in the microprocessor port is as follows:

AD(3)	AD(2)	AD(1)	AD(0)
D1	D0	M1	M0

Since only one register is accessible for reading or writing, no address or ALE signal is required. Data is accessed with either a normal bus read or write operation, or a port read or write operation during the 115 μs period following the F0o pulse as shown in Fig-9. The AK130/131 microprocessor port includes an active low Chip Select ($\overline{CS}$) to allow an external microprocessor to interface with other peripherals.

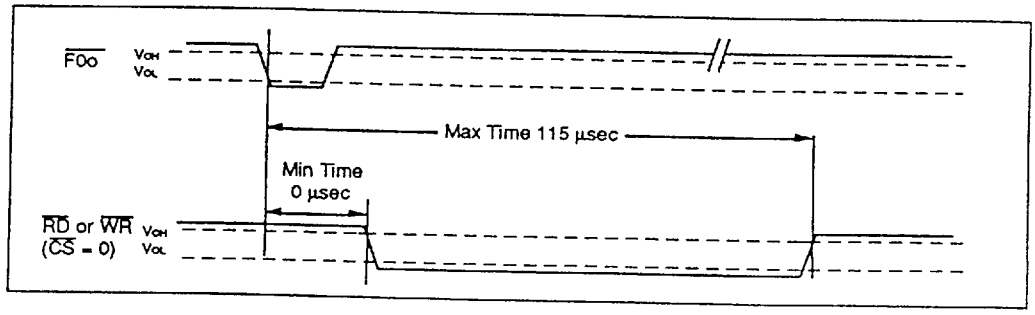


Fig-9 Microprocessor Port Read/Write Access

Applications

Fig-10 through Fig-12 illustrate typical applications for Voice Terminal, Data and Voice Terminals, and Digital Telephone Set, respectively.

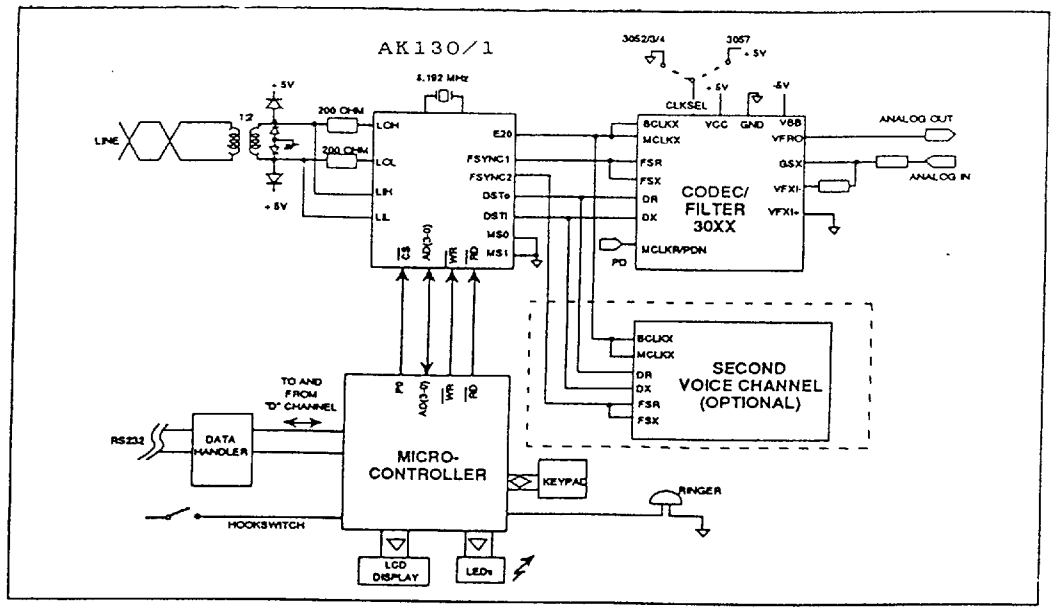


Fig-10 Typical Application - Single or Dual Voice Terminal

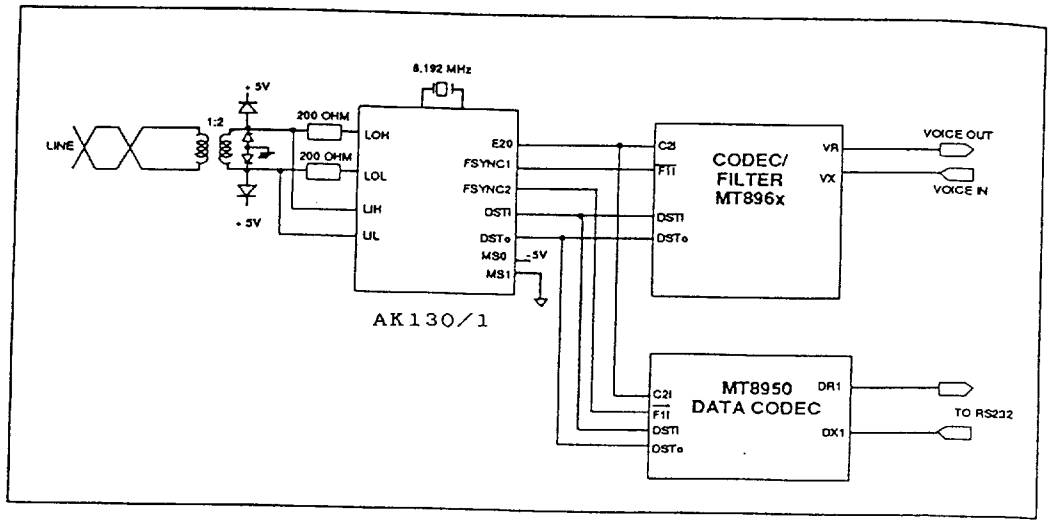


Fig-11 Typical Application - Data and Voice Terminal

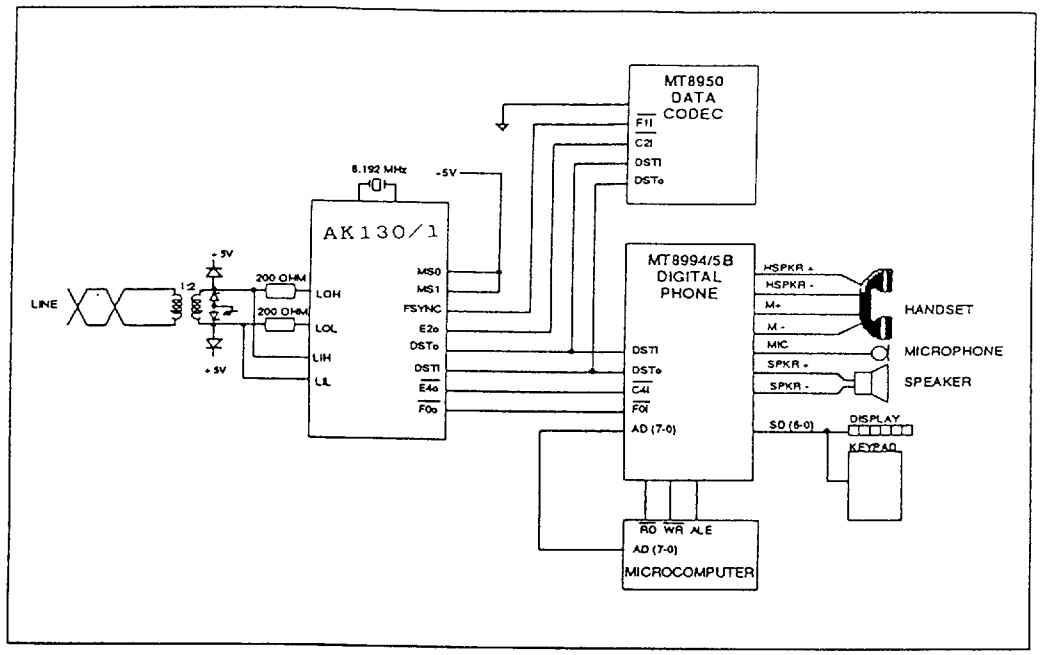


Fig-12 Typical Application – Voice and Data Digital Telephone Set

Packaging Information

Outline Dimensions

24 pin SOP