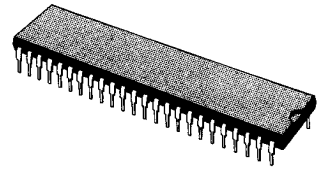
DIGITAL ECHO CANCELLER

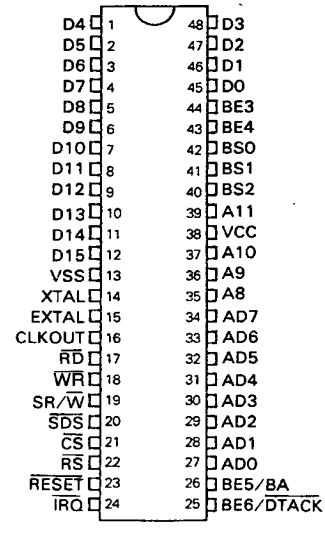
- SIMPLIFIED INTERFACE CIRCUITRY FOR FLEXIBLE ADAPTION TO A WIDE RANGE OF V.32 CONFIGURATIONS
- DOVETAILED HARDWARE AND FIRMWARE CONNECTION WITH TS68950/1/2 MODEM ANALOG FRONT-END CHIP SET
- KEY COMPONENT IN THE ADVANCED TS7532 V.32 MODEM
- 16 msec OF ECHO PATH IMPULSE RESPONSE IN THE NEAR END AND IN THE FAR-END CANCELLERS
- 1.14 SEC OF CHANNEL DELAY (two satellite hops) IN FAR-END ECHO CANCELLER.
- 10Hz OF FREQUENCY OFFSET IN FAR-END ECHO PATH
- MEETS OR EXCEEDS THE REQUIREMENTS OF CCITT RECOMMENDATION V.32



P
DIP–48
(Plastic Package)

(Ordering Information at the end of the datasheet)

PIN CONNECTIONS



M88TS75320–01

DESCRIPTION

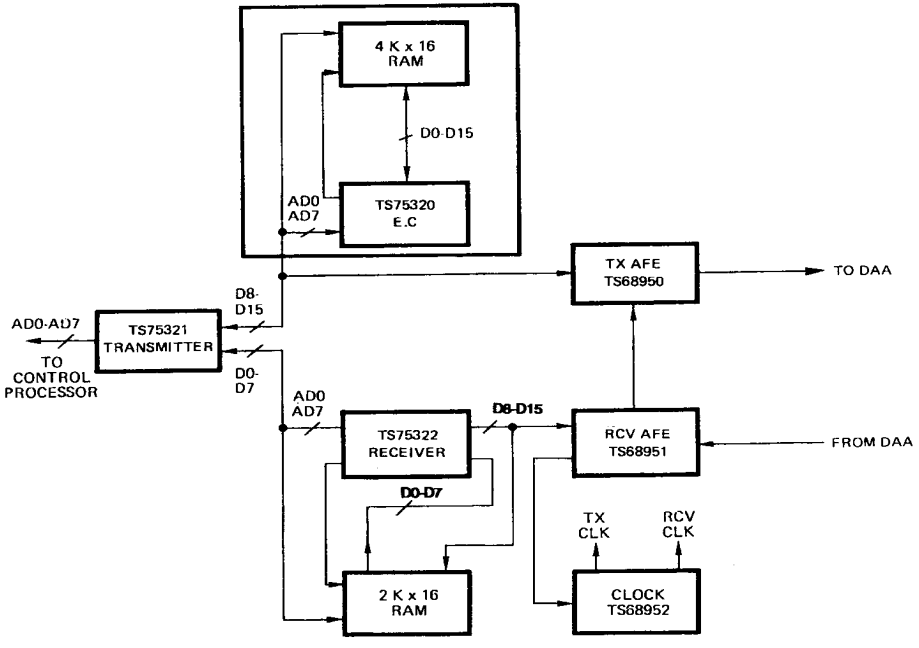
The TS75320 is a high performance voiceband data modem echo canceller implemented on a single chip using advanced digital signal processing technology. Using sophisticated adaptive algorithms, the TS75320 realizes the high precision cancellation of near-end and far-end echoes, even in the presence of frequency offset in the far end echo.

The residual cancellation levels and convergence rates of the TS75320 meet or exceed the demanding requirements of high performance V.32 modems.

The TS75320 is ideally suited for high performance low-cost integrated V.32 solutions.

BLOCK DIAGRAM

Figure 1 : Shows a Configuration for a V.32 Modem utilizing the TS75320 with the TS68950/51/52 MAFE Chip Set.



M88TS75320-02

PIN DESCRIPTION

LOCAL INTERFACE

Pin Name	Pin N°	Type	Function	Description
D (0:15)	45-48 1-11	I/O	Data Bus	D(0:15) Data Bus
A (8:11)	35.37.39	O	Address Bus	High Order Addresses for Local Interface
$\overline{RD}$	17	O	Read	Transfer Data Read
$\overline{WR}$	18	O	Write	Transfer Data Write
CLKOUT	16	O	Clock Output	The frequency of CLKOUT is one half the frequency of the input clock or crystal.

SYSTEM INTERFACE

Pin Name	Pin N°	Type	Function	Description
AD (0:7)	27-34	I/O	System Data Bus or Local Address Bus	The data exchanges between the processor and a master via a mailbox is the function of this bus. It is also used to generate the addresses of an external RAM.
$\overline{CS}$	21	I	Chip Select	Used by a Master to Gain Access to the Mailbox and System Bus
$\overline{RS}$	22	I	Register Select	Used by a Master to Gain Access to the Mailbox and System Bus
$\overline{SDS}$	20	I	System Data Strobe	Synchronizes the Transfer on the System Bus
SR/$\overline{W}$	19	I	System Read/Write	Indicates the Current System Bus Cycle State
$\overline{DTACK}$	25	O	Data Transfer Acknowledge	Indicates that the processor has recognized it is being accessed.
BA	26	O	Bus Available	Indicates Availability of System Bus to Master
$\overline{IRQ}$	24	O	Interrupt Request	Handshake signal sent to the master gain access to the mailbox.

OTHER PINS

Pin Name	Pin N°	Type	Function	Description
EXTAL	15	I	Clock	Crystal Input Pin for Internal Oscillator or Input Pin for External Oscillator
XTAL	14	I	Clock	Together with EXTAL it is used for the external 25 MHz crystal.
VCC	38	I	Power Supply	
VSS	13	I	Ground	
$\overline{RESET}$	23	I	Reset	

FUNCTIONAL DESCRIPTION

PERFORMANCE SUMMARY

The TS75320 performance figures below are obtained with analog front-end D/A converters with integral linearity of 12 bits or better, such as the TS68950.

- Near-end echo cancellation : > 55 dB

  With a near-end echo level of - 10 dBm at the receiver input, in the absence of a far-end signal and of a far-end echo, the residual echo level is below - 65 dBm.
- Combined near–end and far–end echo cancellers :

  For a typical receive level of –20 dBm and far-end echo smaller than –28 dBm the received signal to residual echo ratio is better than 24 dB even in the presence of up to 10 Hz of frequency offset in the far-end echo.
- The signal to residual echo ratio is better than 21 dB even for receive levels as small as –40 dBm, provided that the far-end echo is 8 dB below the received far-end signal.
- The far-end echo channel delay can be as large as 1.14 s.
- Convergence Time : meets or exceeds CCITT V.32 handshake requirements.

ECHO CANCELLER OPERATION

The principal task of the echo canceller is the determination by means of adaptive algorithms, of the coefficients of digital filters and phasing processors that will generate a modem receiver input free of near-end or far-end echoes. The signals processed by the echo canceller are the cancellation error at the receiver input and the V.32 date sequence being transmitted. These signals will normally be available in the appropriate format in a digitally realized modem.

The echo canceller hardware and firmware have been designed for ease of interface with a general purpose DSP or microprocessor and require minimal interaction with the modem. In this section we describe the hardware and software interfaces to the TS75320.

HARDWARE INTERFACE

The TS75320 echo canceller is configured as an essentially self-contained digital peripheral interfaced to a host microcontroller or to a host digital signal processor through an 8-bit system bus. The bus interface dovetails with the control bus of the TS68930 digital signal processor. Straightforward interconnection to other processors or to peripheral circuits is realized by wirtue of an asynchronous mailbox that is readily controlled by means of a flexible handshake protocol.

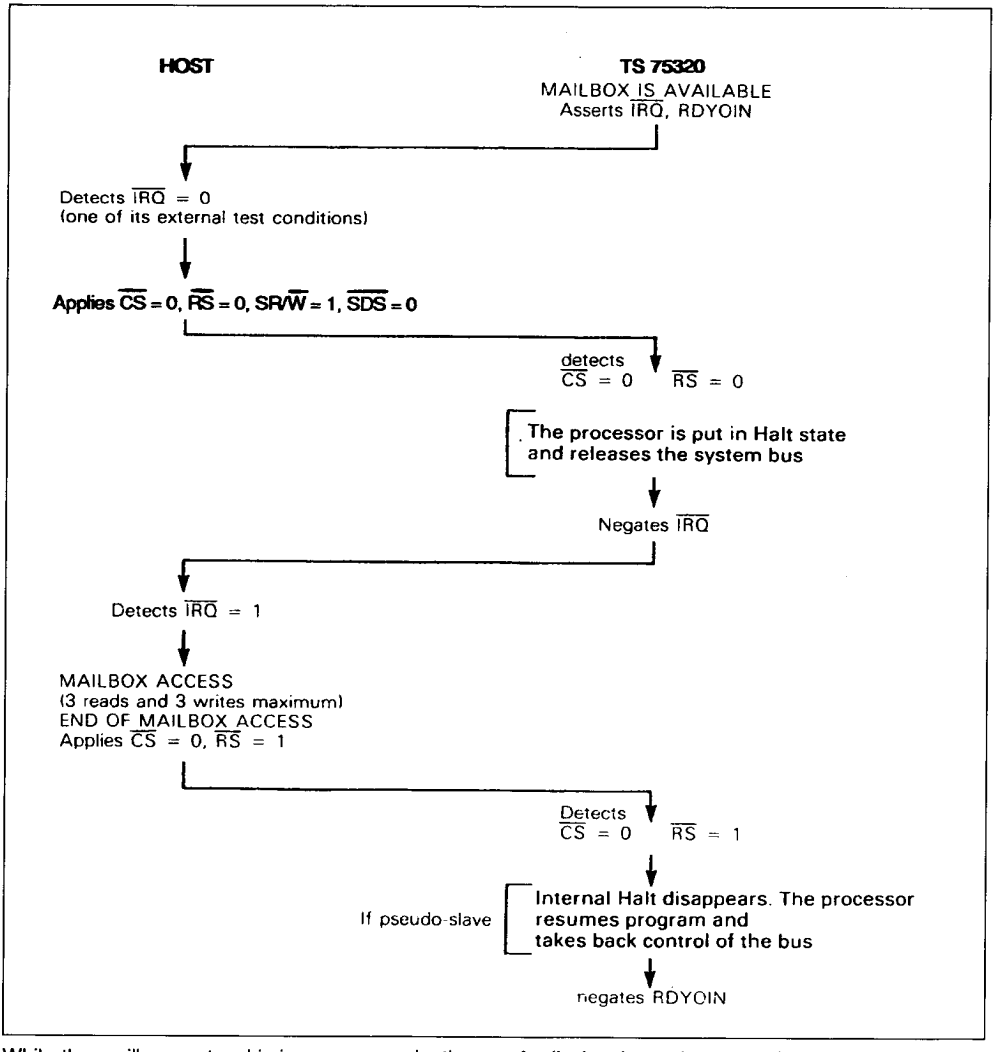
The system bus is also used for addressing the echo canceller external RAM, during which time it is not available to the host controller. Data transfer to the echo canceller's RAM is effected through the 16-bit data bus.

The timing of all communications with the host is determined by the echo canceller.

Data for transmission to the host is loaded into the TS75320 three-byte wide ROUT shift register. The communication process is effected by means of the mailbox transfer protocol. Data for transmission from the host is stored in the TS75320 RIN register, which is also three bytes wide.

The operation of the mailbox transfer protocol is described schematically in the flow chart in Figure 2.

Figure 2 : Mailbox Handshake Protocol.



While the mailbox protocol is in progress only, the host may deselect the TS75320 ($\overline{CS} = 1$) to use the system bus to communicate with other peripherals.

At all other times, the system bus is under the control of the TS75320 and it is therefore essential that the connection of the bus to the host be tri-state at those times.

FIRMWARE INTERFACE

The echo canceller firmware is designed in the first instance for V.32 modem applications, and therefore operates at a Baud rate of 2400 symbols per second. The sampling rate is 7200 per second, i.e. three samples per Baud interval.

In the period of one Baud interval, the echo canceller generates three echo estimates, one for each of the three receiver samples, and it requires the input of the three corresponding echo cancellation errors. The echo estimates and the cancellation errors are both 16 bit quantities. The echo canceller requires also the input of the complex-valued V.32 format current symbol from the transmitter, this is the reference signal for the computation of the echo estimates. By virtue of the V.32 constellation requirements, three bits are sufficient for the representation of the real and imaginary parts, respectively. Hence, the transfer of this signal is effected with a single byte (the four MSBs for the real part, the four LSBs for the imaginary part).

Three mailbox exchanges are required per Baud interval to transfer the data. Once an echo estimate has been computed, it is stored in the TS75320 ROUT register (3-byte wide). The LSB and MSB are stored in the first and second bytes, respectively.

The TS75320 then initiates a mailbox transfer during which the host reads the echo estimate (LSBs followed by MSBs) and stores the two bytes for the transmitted symbol. The mailbox transfer operation is identical for the second and third echo estimates and for the cancellation errors except that there is no need for the transmitted symbol to be transferred more than once per baud interval.

Particular care must be taken, however, to ensure that the modem does not hold the echo canceller during the mailbox transfer for more than the time required for the data transfer. Otherwise problems relating to cycle duration may arise.

INITIALIZATION

The echo canceller is initialized by first asserting the reset signal (RESET = 0) for at least 640 ns. The TS75320 will then automatically clear its internal status and filter coefficients. It will then wait for a mailbox transfer consisting of the following three hexadecimal bytes : AA AA 00. This will indicate the beginning of echo canceller configuration.

The first mailbox transfer after the configuration bytes must contain the far-end echo round trip delay expressed in number of Baud periods. This number must be smaller than 3000 (1.25 seconds). The echo canceller will interpret the first two bytes in its RIN register as the round trip delay, LSBs followed by MSBs, right justified. If the third byte is 0, the far-end echo canceller is disabled. If it is 1, the far-end canceller is enabled.

The near-end echo canceller convergence is enabled by the following 3 bytes in the RIN register of the TS75320 : AA AA 01. If the far-end echo canceller is enabled it will start adapting automatically once the near-end echo canceller has converged.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}*	Supply Voltage	– 0.3 to 7.0	V
V_{in}*	Input Voltage	– 0.3 to 7.0	V
T_A	Operating Temperature Range	0 to 70	°C
T_{stg}	Storage Temperature Range	– 55 to 150	°C

* With respect to V_{SS}.

Stresses above those hereby listed may cause permanent damage to the device. The ratings are stress ones only and functional operation of the device at these or any conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. Standard MOS circuits handling procedure should be used to avoid possible damage to the device.

DC ELECTRICAL OPERATING - CHARACTERISTICS

V_{CC} = 5.0 V ± 5 %, V_{SS} = 0, T_{amb} = 0 to + 70 °C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IL}	Input Low Voltage	– 0.3	–	0.8	V
V_{IH}	Input High Voltage	2.4	–	V_{CC}	V
I_{in}	Input Leakage Current Except EXTAL	– 10	–	10	µA
I_i	Input EXTAL Current	– 50	–	50	µA
V_{OH}	Output High Voltage (I_{load} = – 300 µA)	2.7	–	–	V
V_{OL}	Output Low Voltage (I_{load} = 3.2 mA)	–	–	0.5	V
P_D	Power Dissipation	–	1.5	–	W
C_{in}	Input Capacitance	–	10	–	pF
I_{TSI}	Three State (off state) Input Current	– 20	–	20	µA

AC ELECTRICAL SPECIFICATIONS - CLOCK AND CONTROL PINS TIMING

(VCC = 5.0V ± 5%, Tamb = 0° to +70°C ; see figure 3)

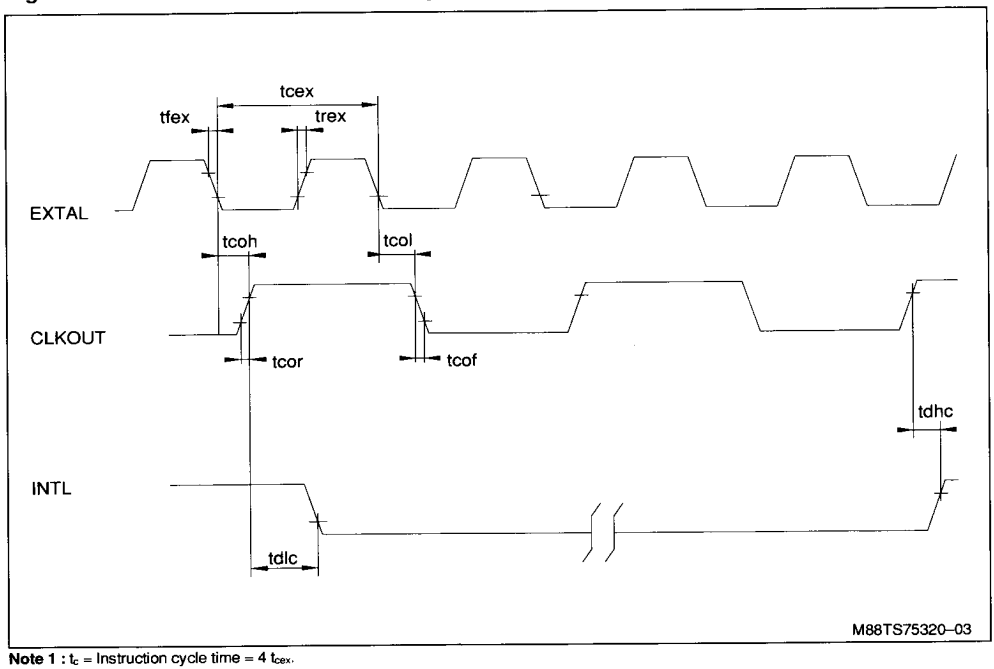
Output load = 50 pF + DC characteristics load

Reference levels : V_{IL} : 0.45 V V_{IH} : 2.4 V

V_{OL} : 0.45 V V_{OH} : 2.4 V tr, tf ≤ 5 ns for input signals

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{cex}	External Clock Cycle Time	40		160	ns
t_{fex}	External Clock Fall Time			5	ns
t_{rex}	External Clock Rise Time			5	ns
t_{coh}	EXTAL to CLKOUT High Delay		25		ns
t_{col}	EXTAL to CLKOUT Low Delay		25		ns
t_{rco}	CLKOUT Rise Time			10	ns
t_{fco}	CLKOUT Fall Time			10	ns
t_{dsl}	CLKOUT to $\overline{DS}$, $\overline{RD}$, $\overline{WR}$ Low		5		ns
t_{dsh}	CLKOUT to $\overline{DS}$, $\overline{RD}$, $\overline{WR}$ High		5		ns
t_{sc}	Control Inputs Set-up Time (BS0... BS2, BE3... BE6, $\overline{Reset}$, $\overline{Halt}$)	20			ns
t_{hc}	Control Inputs Hold Time (BS0... BS2, BE3... BE6, $\overline{Reset}$, $\overline{Halt}$)	10			ns
t_{dlc}	CLKOUT to Control Output Low ($\overline{IRQ}$, BA)			50	ns
t_{dhc}	CLKOUT to Control Output High (BA, $\overline{IRQ}$)			50	ns

Figure 3 : Clock and Control Pins Timing.

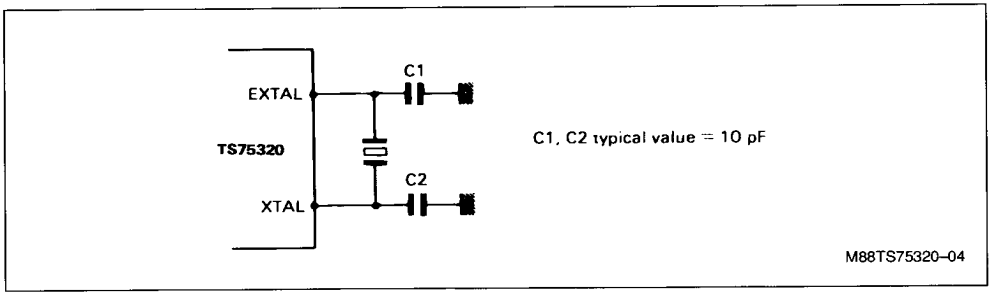


Note 1 : t_c = Instruction cycle time = 4 t_{cex}.

INTERNAL CLOCK OPTION

A crystal oscillator can be connected across XTAL and EXTAL. The frequency of CLKOUT : tc/2 is half the crystal fundamental frequency.

Figure 4.

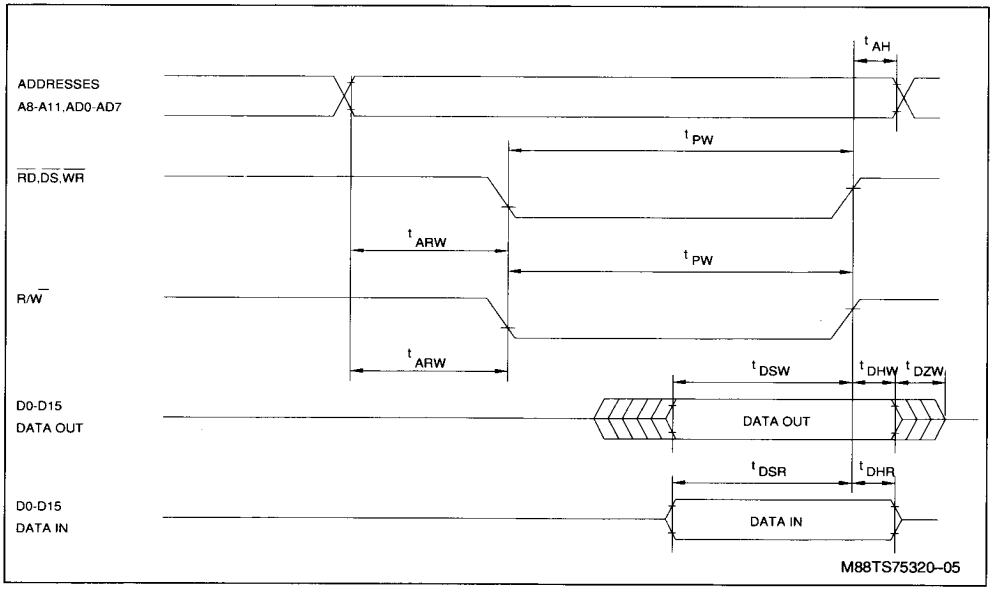


ELECTRICAL CHARACTERISTICS - LOCAL BUS TIMING

(V_{CC} = 5.0 V ± 5 %, T_{amb} = 0 °C to + 70 °C ; see figure 5)

Symbol	Parameter	Min.	Max.	Unit
t_{PW}	$\overline{RD}$, $\overline{WR}$, $\overline{SDS}$, Pulse Width	1/5 tc – 15	1/2 tc	ns
t_{AH}	Address Hold Time	10	–	ns
t_{DSW}	Data Set-up Time, Write Cycle	25	–	ns
t_{DHW}	Data Hold Time, Write Cycle	10	–	ns
t_{DZW}	$\overline{SDS}$ High to Data High Impedance, Write Cycle	–	40	ns
t_{DSR}	Data Set-up Time, Read Cycle	20	–	ns
t_{DHR}	Data Hold Time, Read Cycle	5	–	ns
t_{ARW}	Address Valid to $\overline{WR}$, $\overline{SDS}$, $\overline{RD}$ Low	1/2 tc – 40	–	ns

Figure 5 : Local Bus Timing Diagram.



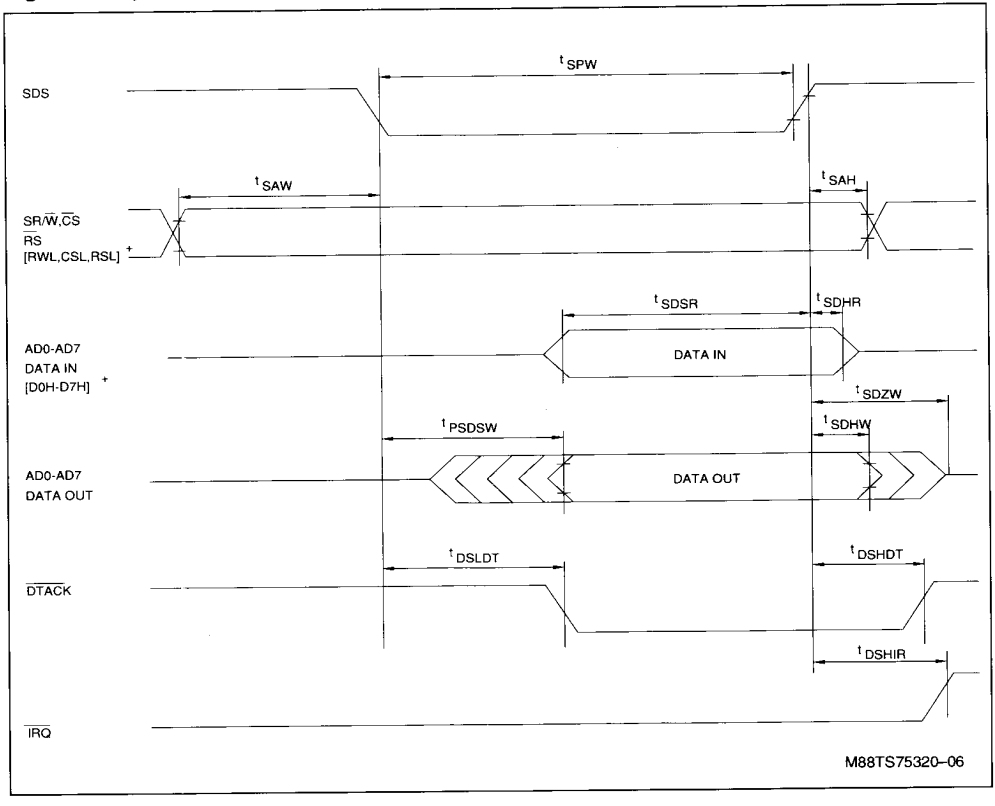
AC ELECTRICAL SPECIFICATIONS. SYSTEM BUS TIMING

(V_{CC} = 5.0 V ± 5 %, T_{amb} = 0 °C to + 70 °C ; see figure 6)

Symbol	Parameter	Min.	Max.	Unit
t_{SPW}	$\overline{SDS}$ Pulse Width	60	–	ns
t_{SAW}	SR/$\overline{W}$, $\overline{CS}$, $\overline{RS}$ Set-up Time	20	–	ns
t_{SAH}	SR/$\overline{W}$, $\overline{CS}$, $\overline{RS}$ Hold after $\overline{SDS}$ High	5	–	ns
t_{SDSR}	Data Set-up Time, Read Cycle	20	–	ns
t_{SDHR}	Data Hold Time, Read Cycle	5	–	ns
t_{SDSW}	Data Set-up Time, Write Cycle	–	35	ns
t_{SDHW}	Data Hold Time, Write Cycle	10	50	ns
t_{DSLDT}	$\overline{SDS}$ Low to $\overline{DTACK}$ Low	–	50	ns
t_{DSHDT}	$\overline{SDS}$ High to $\overline{DTACK}$ High *	–	50	ns
t_{DSHIR}	$\overline{SDS}$ High to $\overline{IRQ}$ High	–	50	ns
t_{SDZW}	$\overline{SDS}$ High to Data High Impedance, Write Cycle	–	40	ns

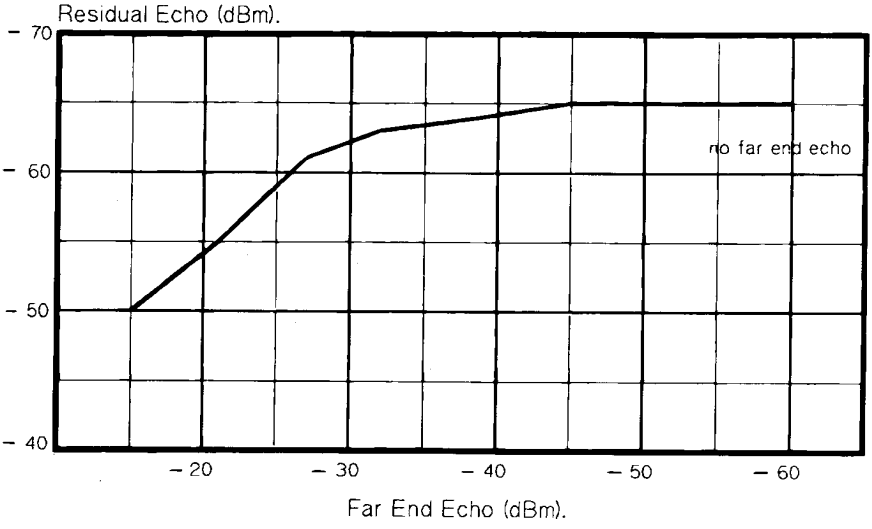
* $\overline{DTACK}$ is an open drain output test load include R_L = 890Ω at V_{CC}.

Figure 6 : System Bus Timing Diagram.



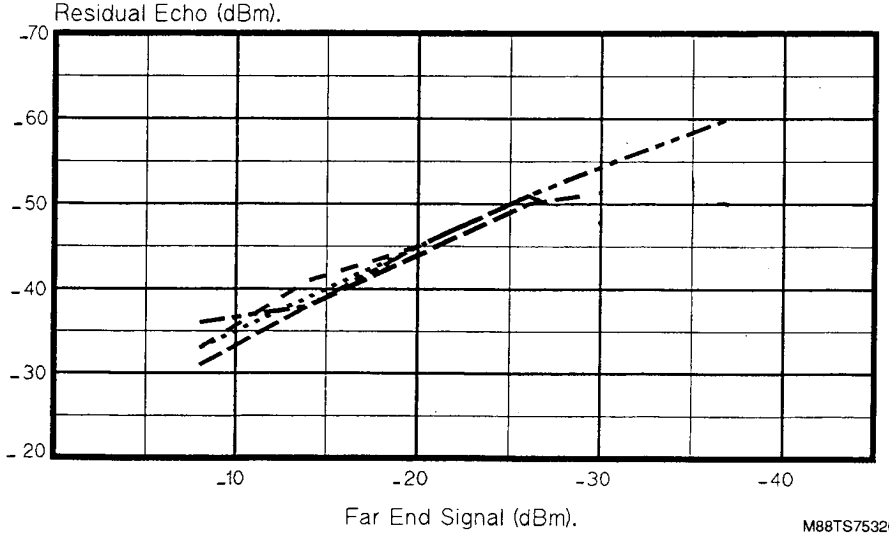
TYPICAL PERFORMANCE

TS75320 : Residual Echo without Far-end Signal.



M88TS75320-07

TS75320 : Residual Echo versus Far End Signal (with far-end echo level 8dB below far-end signal).



M88TS75320-08

ORDERING INFORMATION

Part Number	Temperature RAnge	Package
TS75320CP	0 °C to + 70 °C	48 Pin Plastic Dil

PACKAGE MECHANICAL DATA

48 PINS – PLASTIC DIP