PRELIMINARY DATA SHEET

NEC

MOS INTEGRATED CIRCUIT

μPD720133

USB2.0 to IDE Bridge

The μPD720133 is designed to function as a bridge between USB 2.0 and ATA/ATAPI. The μPD720133 complies with the Universal Serial Bus Specification Revision 2.0 full-/high-speed signaling and works up to 480 Mbps. The μPD720133 consists of a CISC processor, an ATA/ATAPI controller, an endpoint controller (EPC), a serial interface engine (SIE), and an USB2.0 transceiver. The USB2.0 protocol and class specific protocols (bulk only protocol) are handled by the USB2.0 transceiver, the SIE and the EPC. The V30MZ CISC processor in the μPD720133 takes care of the activities in the transport layer. The firmware controlling the μPD720133 is located in an embedded ROM.

FEATURES

- Compliant with Universal Serial Bus Specification Revision 2.0 (Data Rate 12/480 Mbps)
- Compliant with ATA/ATAPI-6 (LBA48, PIO Mode 0-4, Multi Word DMA Mode 0-2, Ultra DMA Mode 0-4)
- USB2.0 high-speed bus powered device capability
★ • Certified by USB implementers forum and granted with USB 2.0 high-speed Logo (TID: 40001985)
- One USB2.0 high-speed transceiver / receiver with full-speed transceiver / receiver
- USB2.0 High-speed or Full-speed packet protocol sequencer (Serial Interface Engine)
- Automatic chirp assertion and full-/high-speed mode change
- USB Reset, Suspend and Resume signaling detection
- Supports power control functionality for IDE device as CD-ROM and HDD
- Supports set feature (TEST_MODE) functionality
- System Clock is generated by 30 MHz X'tal
- 2.5 V and 3.3 V power supply

★ ORDERING INFORMATION

Part Number	Package
μPD720133GB-YEU-A	64-pin plastic TQFP (fine pitch) (10 × 10) Lead-free product
μPD720133GB-YEU-Y	64-pin plastic TQFP (fine pitch) (10 × 10) High heat-resistance product

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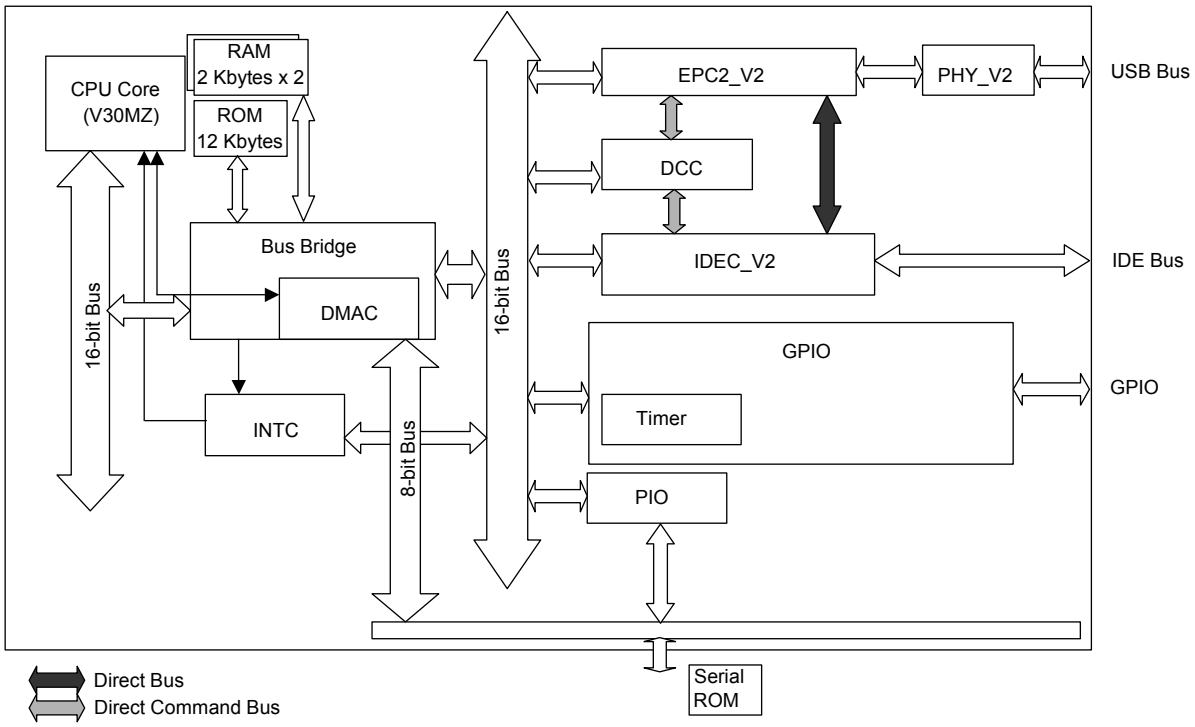
The mark ★ shows major revised points.

BLOCK DIAGRAM



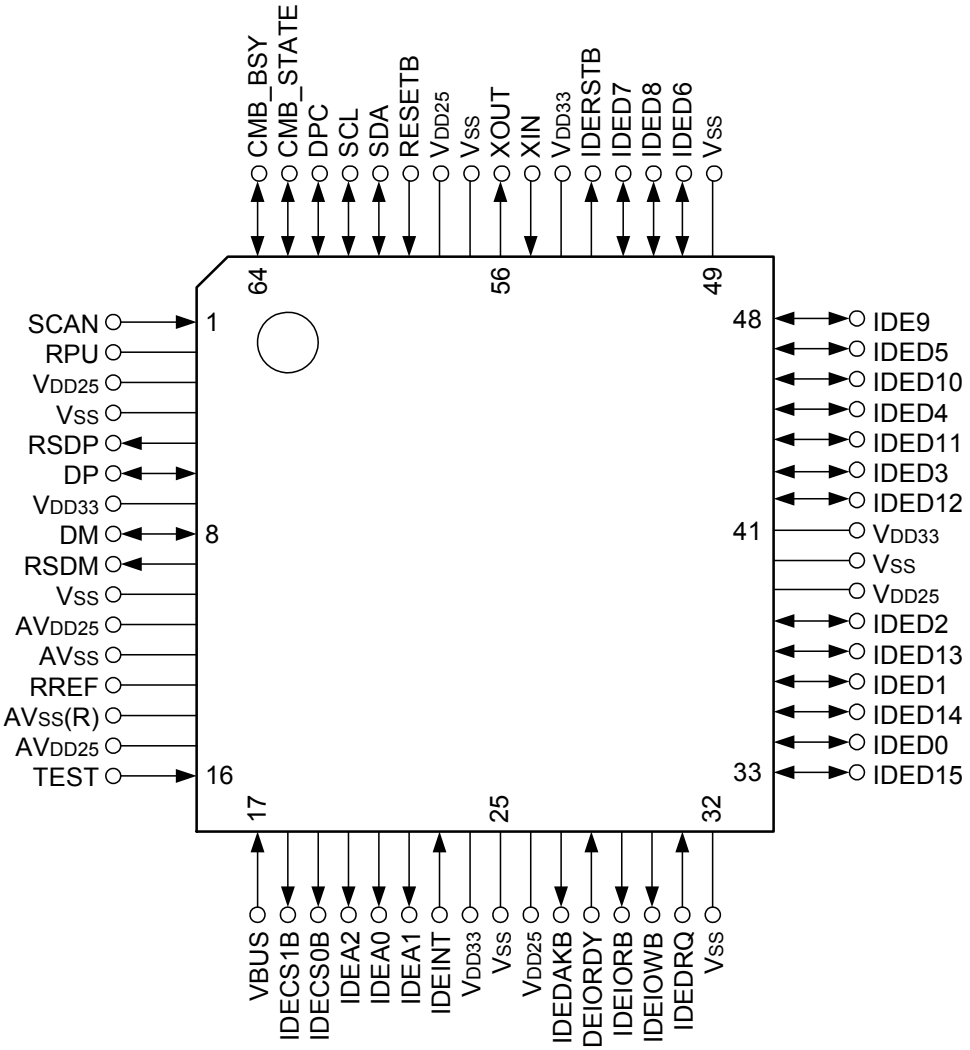
V30MZ	: CISC CPU core
RAM	: 4-Kbyte work RAM for firmware
ROM	: 12-Kbyte ROM for built-in firmware
PHY_V2	: USB2.0 transceiver with serial interface engine
EPC2_V2	: Endpoint controller
IDEC_V2	: IDE controller
DCC	: ATA direct command controller
Bus Bridge	: Internal / external bus controller and DMA controller
INTC	: Interrupt controller (82C59 like)
GPIO	: General purpose 3-bit I/O controller
PIO	: Multipurpose 2-bit I/O controller

PIN CONFIGURATION (TOP VIEW)

- **64-pin plastic TQFP (fine pitch) (10 × 10)**

★ μPD720133GB-YEU-A

μPD720133GB-YEU-Y



Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name
1	SCAN	17	VBUS	33	IDED15	49	V_{SS}
2	RPU	18	IDECS1B	34	IDED0	50	IDED6
3	V_{DD25}	19	IDECS0B	35	IDED14	51	IDED8
4	V_{SS}	20	IDEA2	36	IDED1	52	IDED7
5	RSDP	21	IDEA0	37	IDED13	53	IDERSTB
6	DP	22	IDEA1	38	IDED2	54	V_{DD33}
7	V_{DD33}	23	IDEINT	39	V_{DD25}	55	XIN
8	DM	24	V_{DD33}	40	V_{SS}	56	XOUT
9	RSDM	25	V_{SS}	41	V_{DD33}	57	V_{SS}
10	V_{SS}	26	V_{DD25}	42	IDED12	58	V_{DD25}
11	AV_{DD25}	27	IDEDAKB	43	IDED3	59	RESETB
12	AV_{SS}	28	IDEIORDY	44	IDED11	60	SDA (PIO0)
13	RREF	29	IDEIORB	45	IDED4	61	SCL (PIO1)
14	AV_{SS}(R)	30	IDEIOWB	46	IDED10	62	DPC(GPIO5)
15	AV_{DD25}	31	IDEDRQ	47	IDED5	63	CMB_STATE(GPIO6)
16	TEST	32	V_{SS}	48	IDED9	64	CMB_BSY(GPIO7)

Remark AV_{SS}(R) should be used to connect RREF through 1 % precision reference resistor of 2.43 kΩ.

1. PIN INFORMATION

Pin Name	I/O	Buffer Type	Active Level	Function
XIN	I	2.5 V Input		System clock input or oscillator In
XOUT	O	2.5 V Output		Oscillator out
RESETB	I	3.3 V Schmitt Input	Low	Asynchronous reset signaling
IDECS(1:0)B	O (I/O)	5 V tolerant Output	Low	IDE host chip select
IDEA(2:0)	O (I/O)	5 V tolerant Output		IDE address bus
IDEINT	I	5 V tolerant Input	High	IDE interrupt request from device to host
IDEDAKB	O (I/O)	5 V tolerant Output	Low	IDE DMA acknowledge
IDEIORDY	I	5 V tolerant Input	High	IDE IO channel ready
IDEIORB	O (I/O)	5 V tolerant Output	Low	IDE IO read strobe
IDEIOWB	O (I/O)	5 V tolerant Output	Low	IDE IO write strobe
IDEDRQ	I	5 V tolerant Input	High	IDE DMA request from device to host
IDED(15:0)	I/O	5 V tolerant I/O		IDE data bus
IDERSTB	O (I/O)	5 V tolerant Output	Low	IDE reset from host to device
CMB_BSY (GPIO7)	I/O	3.3 V I/O		Combo IDE bus busy
CMB_STATE (GPIO6)	I/O	3.3 V I/O		Combo IDE bus state
DPC (GPIO5)	I/O	3.3 V I/O		Power control signaling for IDE device
SDA (PIO0)	I/O	3.3 V I/O		Serial ROM data signaling
SCL (PIO1)	I/O	3.3 V I/O		Serial ROM clock signaling
VBUS	I	5 V Schmitt Input [Note]		VBUS monitoring
DP	I/O	USB high speed D+ I/O		USB's high speed D+ signal
DM	I/O	USB high speed D– I/O		USB's high speed D– signal
RSDP	O	USB full speed D+ Output		USB's full speed D+ signal
RSDM	O	USB full speed D– Output		USB's full speed D– signal
RPU	A	USB Pull-up control		USB's 1.5 kΩ pull-up resistor control
RREF	A	Analog		Reference resistor
SCAN	I	3.3 V Input		Scan mode control
TEST	I	3.3 V Input		Test mode setting
AV_{DD25}				2.5 V V_{DD} for Analog circuit
V_{DD25}				2.5 V V_{DD}
V_{DD33}				3.3 V V_{DD}
AV_{SS}				V_{SS} for Analog circuit
V_{SS}				V_{SS}

Note VBUS pin may be used to monitor for VBUS line even if V_{DD33}, V_{DD25}, and AV_{DD25} are shut off. The System Designer must ensure that the input voltage level for VBUS pin is less than 3.0 V. [that is the absolute maximum rating].

Remarks 1. "5 V tolerant" means that the buffer is a 3.3 V buffer with 5 V tolerant circuit.

2. The signal marked as "(I/O)" in the above table operates as I/O signals during testing. They should be ignored under normal operation.

2. FUNCTION INFORMATION

The USB to IDE system can be realized by μPD720133. If the customizations of data such as USB vendor ID and USB product ID are required, an external serial ROM can be used. The μPD720133 also has power circuit to turn on and off the system power supply. The μPD720133 can operate in either bus-powered mode or self-powered mode. If the total power consumption of the USB to IDE system within the USB 2.0 specification of a bus powered device, it will be possible to realize a high-speed capable bus powered system. In addition, μPD720133 has a feature of IDE bus arbitration. This enables system, which has two IDE controllers to control a single IDE device. In this case, another IDE controller also must have a feature of IDE bus arbitration.

The setting of IDE controller in the μPD720133 is controlled by data in serial ROM.

2.1 Data in Serial ROM

The μPD720133 loads some data such as Vendor ID, Product ID and some additional USB related information, etc from serial ROM during μPD720133 initialization.

Table 2-1. Data in Serial ROM

Offset (H)	Data Size	Symbol	Description
+00	1 Word	idMark	Validation Mark of 55AAH
+02	1 Word	CheckSum	Check sum of serial ROM
+04	1 Word	Flags	Control for descriptor overwrite
+06	1 Byte	ModeReset	PWR, CLC, DCC, DV[1:0], DPC Reset bit map field
+07	1 Byte	ModeSet	PWR, CLC, DCC, DV[1:0], DPC Set bit map field
+08	1 Word	idVendor	idVendor field in Device descriptor
+0A	1 Word	idProduct	idProduct field in Device descriptor
+0C	1 Word	bcdDevice	bcdDevice field in Device descriptor
+0E	1 Word	Reserved	Reserved for future use.
+10	1 Byte	MaxPower Bus	bMaxPower field in Configuration descriptor for Bus powered mode
+11	1 Byte	MaxPower Self	bMaxPower field in Configuration descriptor for Self powered mode
+12	1 Byte	bInterfaceClass	bInterfaceClass field in Interface descriptor
+13	1 Byte	bInterfaceSubClass	bInterfaceSubClass field in Interface descriptor
+14	1 Byte	bInterfaceProtocol	bInterfaceProtocol field in Interface descriptor
+15	1 Byte	Reserved	Reserved for future use.
+16	1Word	TxModeReset	IDE transmission type such as Ultra DMA 66 Reset bit map field
+18	1Word	TxModeSet	IDE transmission type such as Ultra DMA 66 Set bit map field
+1A	1Word	RompatchSW	ROM Patch information (Patch On or Off) of External Function
+1C	4 Bytes	Reserved	Reserved for future use.
+20	32 Bytes	ManufactureString	String descriptor for Manufacturer
+40	32 Bytes	ProductString	String descriptor for Product
+60	32 Bytes	SerialString	String descriptor for Device serial number
+80	128 × n Bytes	FW Patch	Firmware patch module for self-powered/bus-powered mode

2.2 Pin Setting

Settings of the SCL, SDA and unused pins (TEST and SCAN) are recommended as follows. Please note that the setting of the SCL depends on size of Serial ROM.

Table 2-2. Pin Settings

Pin Name	Setting
SCL	Pull Up [Note]
SDA	Pull Up
TEST	Low Clamp
SCAN	Low Clamp

Note If serial ROM size is more than 2 Kbytes, SCL should be pull down.

The settings for any other pins such as the CMB_BSY and the CMB_STATE depend on USB2.0 to IDE Bridge system. For example, if two IDE controllers are implemented in the system to control one target IDE device and one of the two IDE controllers is the μPD720133, then both the CMB_BSY and the CMB_STATE are used to handshake between the two IDE controller chips. On the other hand, when the system uses the μPD720133 as the only IDE controller to control a target IDE device, then both the CMB_BSY and the CMB_STATE should be connected to ground.

2.3 Control Bit in Serial ROM

The following tables show IDE status and control bit in serial ROM.

Table 2-3. DV1/DV0, CLC, PWR Setting

No.	Device Power	Internal Clock	ATA/ATAPI	PWR	CLC	DV1	DV0
0	Bus Powered	7.5 MHz	No device connected	1	1	1	1
1			ATA	1	1	1	0
2			ATAPI	1	1	0	1
3			Reserved	1	1	0	0
4		60 MHz	No device connected	1	0	1	1
5			ATA	1	0	1	0
6			ATAPI	1	0	0	1
7			Reserved	1	0	0	0
8	Self Powered	60 MHz	No device connected	0	1	1	1
9			Combo (ATA)	0	1	1	0
10			Combo (ATAPI)	0	1	0	1
11			Combo auto device detect	0	1	0	0
12			No device connected	0	0	1	1
13			ATA	0	0	1	0
14			ATAPI	0	0	0	1
15			Auto device detect	0	0	0	0

Remarks 1. Setting of no. 0, 3, 4, 7, 8, and 12 are not allowed.

2. For bus powered setting, some critical considerations such as power consumption for the total system should be observed.

3. The slave device function cannot use Auto device detect.

Table 2-4. DV1/DV0, DCC Setting

Condition				DCC setting in Serial ROM	Description
DV1	DV0	Mode	Target Device		
1	0	ATA	ATA	Reset	Ultra, Multi Word DMA are disabled.
				Set	Ultra, Multi Word DMA are enabled.
0	1	ATAPI	ATAPI	Reset	Ultra DMA are disabled.
				Set	Ultra, Multi Word DMA are enabled.
0	0	Auto device detect	ATA	Reset	Ultra, Multi Word DMA are disabled.
				Set	Ultra, Multi Word DMA are enabled.
			ATAPI	Reset	Ultra DMA are disabled.
				Set	Ultra, Multi Word DMA are enabled.

Remark PIO mode 0-4 are always enabled.

2.4 Combo Mode Function

The μPD720133 can be used to realize that two IDE controller chips control one target IDE device in one system. In order to realize IDE bus arbitration between two IDE controller chips, the μPD720133 has the CMB_BSY and the CMB_STATE. Combo mode is enabled when PWR = 0 and CLC = 1.

CMB_BSY and CMB_STATE are connected to another IDE controller chip as shown below.

Figure 2-1. CMB_BSY and CMB_STATE Connection between Two IDE Controller Chips

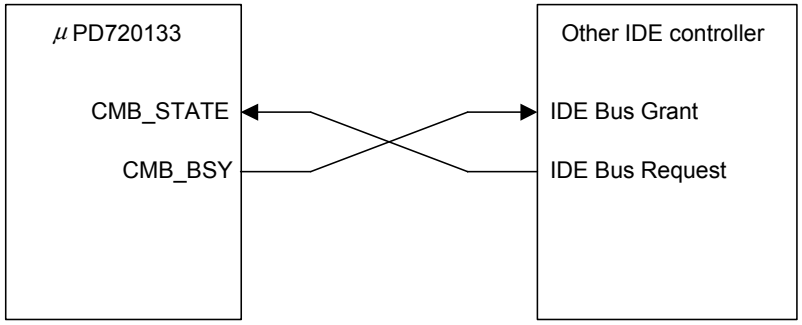
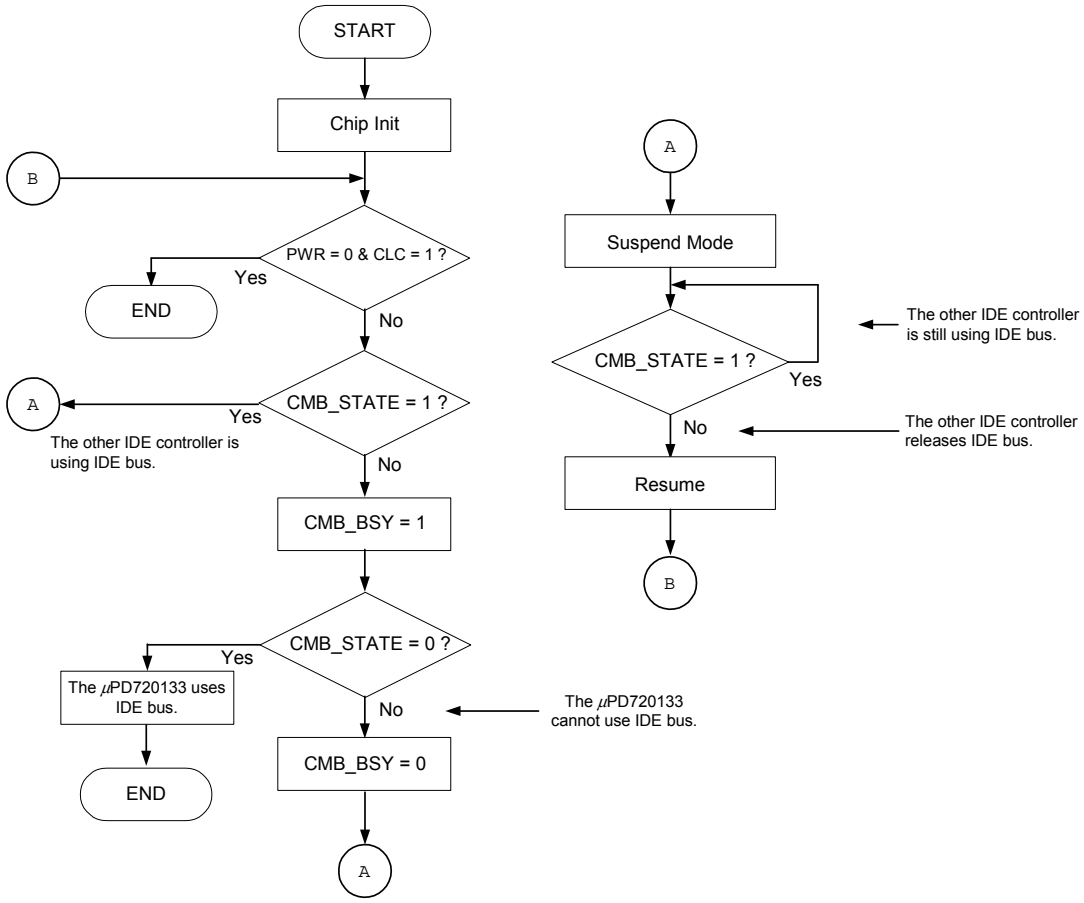


Table 2-5. Description of CMB_BSY and CMB_STATE

Pin Name	Direction	Value	Description
CMB_STATE	IN	0	Other IDE controller does not require or does not use IDE bus.
		1	Other IDE controller requires or is using IDE bus.
CMB_BSY	OUT	0	The μPD720133 does not require or does not use IDE bus.
		1	The μPD720133 requires or is using IDE bus.

The IDE bus arbitration will be performed in the following sequence. The μPD720133 will check if the other IDE controller is using the IDE bus. If the other IDE controller is not using the IDE bus, the μPD720133 will be able to use the IDE bus. On the other hand, if the other IDE controller is using the IDE bus, the μPD720133 transmits to the suspend mode. And the μPD720133 resumes on condition that the CMB_STATE becomes low level. After that, the arbitration will restart from the beginning of the sequence.

Figure 2-2. IDE Bus Arbitration Sequence

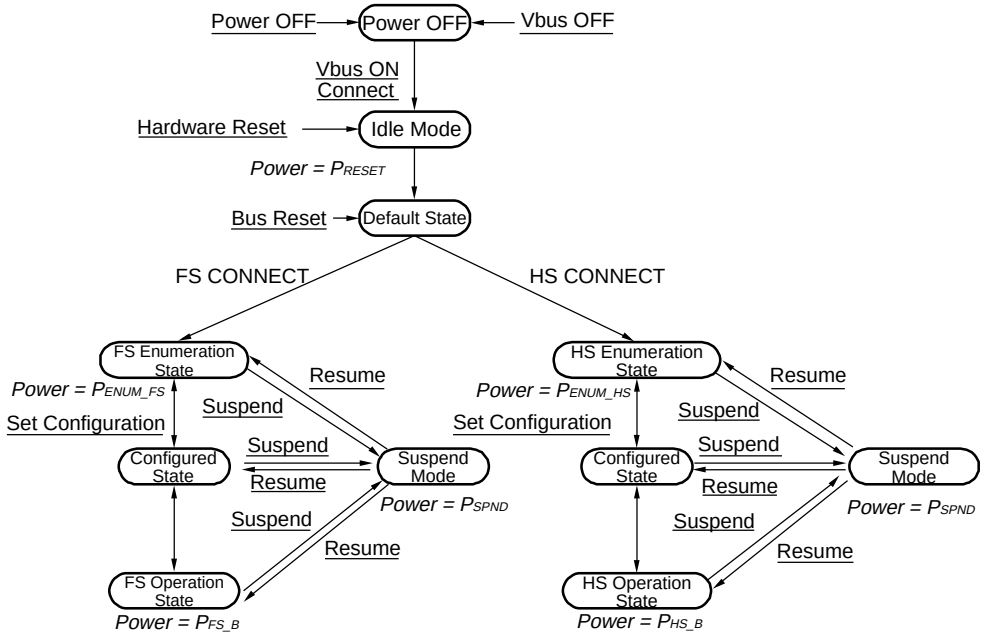


2.5 Power Control

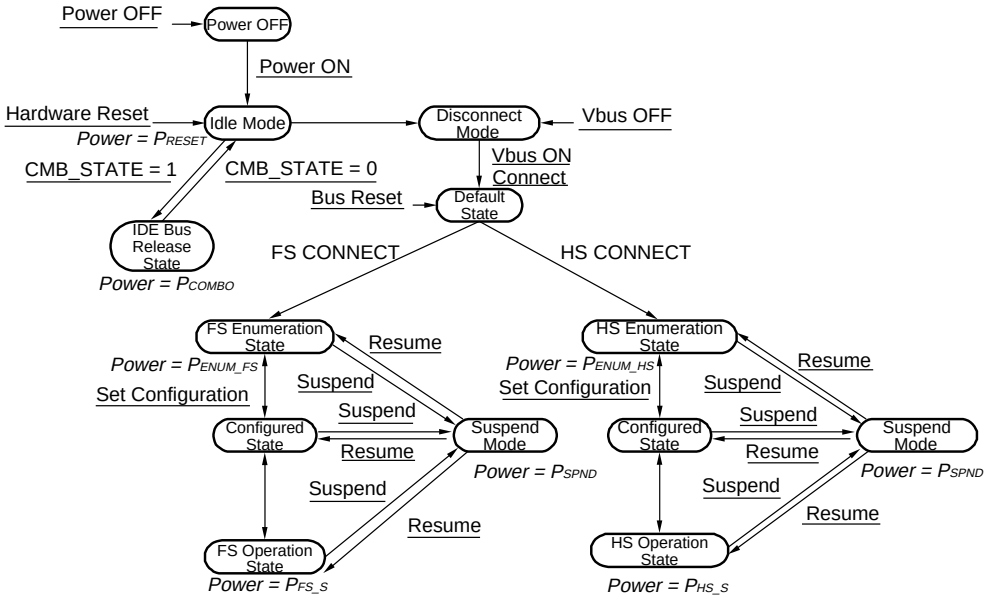
To realize bus-powered or high performance self-powered USB2.0 to IDE Bridge system, the μPD720133 has two internal system clock mode. One is 7.5 MHz for bus-powered mode and another is 60 MHz for self-powered mode. The μPD720133 controls the power state by events as follows. The word with under line indicates event. The Italic word indicates the power state.

Figure 2-3. Power State Control

(a) Bus-powered Mode

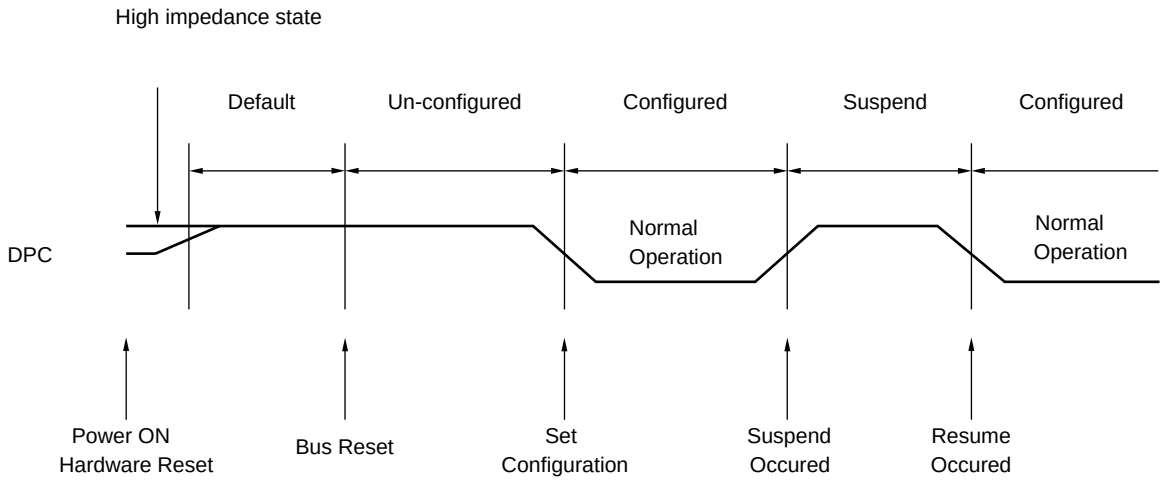


(b) Self-powered Mode



To realize bus-powered USB2.0 to IDE Bridge system, μPD720133 has a DPC pin to control the on and off of the IDE device's power supply according to the USB device states. DPC should be pull-up to 3.3 V because DPC output becomes high impedance state until the μPD720133 is initialized.

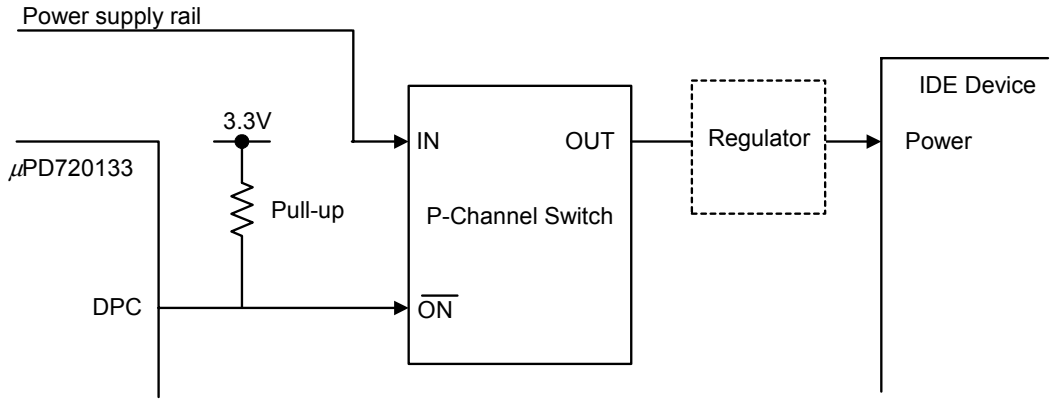
Figure 2-4. DPC Pin to Control IDE Device's Power Circuit



The following example is a circuit for controlling the power supplies to IDE device while the μPD720133 is under default and un-configured state. Also, the power supply to IDE device is disabled during suspend state.

Power consumption of total system under default, un-configured, and suspend state can be reduced by DPC pin.

Figure 2-5. Power Control Circuit Example



3. ELECTRICAL SPECIFICATIONS

3.1 Buffer List

- 2.5 V oscillator interface

  XIN, XOUT
- 3.3 V input buffer

  TEST, SCAN
- 3.3 V schmitt input buffer

  RESETB
- 3.3 V I_{OL} = 3 mA bi-directional buffer with input enable (OR-type)

  SDA, SCL, DPC (GPIO5), CMB_STATE (GPIO6), CMB_BSY (GPIO7)
- 5 V schmitt input buffer

  VBUS
- 5 V I_{OL} = 6 mA bi-directional buffer with input enable (OR-type)

  IDED(15:0), IDEINT, IDEIORDY, IDEDRQ, IDECS(1:0)B, IDEA(2:0), IDEDAKB, IDEIORB, IDEIOWB, IDERSTB
- USB interface

  DP, DM, RSDP, RSDM, RREF, RPU

Remark "5 V" refers to a 3.3 V buffer with 5-V tolerant circuit. Therefore, it is possible to have a 5-V connection for an external bus, but the output level will be only up to 3.3 V, which is the V_{DD33} voltage.

3.2 Terminology

Terms Used in Absolute Maximum Ratings

Parameter	Symbol	Meaning
Power supply voltage	V_{DD33}, V_{DD25}	Indicates voltage range within which damage or reduced reliability will not result when power is applied to a V_{DD} pin.
Input voltage	V_I	Indicates voltage range within which damage or reduced reliability will not result when power is applied to an input pin.
Output voltage	V_O	Indicates voltage range within which damage or reduced reliability will not result when power is applied to an output pin.
Output current	I_O	Indicates absolute tolerance value for DC current to prevent damage or reduced reliability when a current flows out of or into an output pin.
Operating temperature	T_A	Indicates the ambient temperature range for normal logic operations.
Storage temperature	T_{stg}	Indicates the element temperature range within which damage or reduced reliability will not result while no voltage or current are applied to the device.

Terms Used in Recommended Operating Range

Parameter	Symbol	Meaning
Power supply voltage	V_{DD33}, V_{DD25}	Indicates the voltage range for normal logic operations occur when V_{SS} = 0 V.
High-level input voltage	V_{IH}	Indicates the voltage, which is applied to the input pins of the device, is the voltage indicates that the high level states for normal operation of the input buffer. * If a voltage that is equal to or greater than the “Min.” value is applied, the input voltage is guaranteed as high level voltage.
Low-level input voltage	V_{IL}	Indicates the voltage, which is applied to the input pins of the device, is the voltage indicates that the low level states for normal operation of the input buffer. * If a voltage that is equal to or lesser than the “Max.” value is applied, the input voltage is guaranteed as low level voltage.
Hysteresys voltage	V_H	Indicates the differential between the positive trigger voltage and the negative trigger voltage.
Input rise time	t_{ri}	Indicates allowable input rise time to input pins. Input rise time is transition time from $0.1 \times V_{DD}$ to $0.9 \times V_{DD}$.
Input fall time	t_{fi}	Indicates allowable input fall time to input pins. Input fall time is transition time from $0.9 \times V_{DD}$ to $0.1 \times V_{DD}$.

Terms Used in DC Characteristics

Parameter	Symbol	Meaning
Off-state output leakage current	I_{OZ}	Indicates the current that flows from the power supply pins when the rated power supply voltage is applied when a 3-state output has high impedance.
Output short circuit current	I_{OS}	Indicates the current that flows when the output pin is shorted (to GND pins) when output is at high-level.
Input leakage current	I_I	Indicates the current that flows when the input voltage is supplied to the input pin.
Low-level output current	I_{OL}	Indicates the current that flows to the output pins when the rated low-level output voltage is being applied.
High-level output current	I_{OH}	Indicates the current that flows from the output pins when the rated high-level output voltage is being applied.

3.3 Electrical Specifications

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage	V_{DD33}	3.3 V power supply rail	–0.5 to +4.6	V
	V_{DD25}	2.5 V power supply rail	–0.5 to +3.6	V
Input voltage, 5 V buffer	V_I	3.0 V ≤ V_{DD33} ≤ 3.6 V V_I < V_{DD33} + 3.0 V	–0.5 to +6.6	V
Input voltage, 3.3 V buffer	V_I	3.0 V ≤ V_{DD33} ≤ 3.6 V V_I < V_{DD33} + 1.0 V	–0.5 to +4.6	V
Input voltage, 2.5 V buffer	V_I	2.3 V ≤ V_{DD25} ≤ 2.7 V V_I < V_{DD25} + 0.9 V	–0.5 to +3.6	V
Output voltage, 5 V buffer	V_O	3.0 V ≤ V_{DD33} ≤ 3.6 V V_O < V_{DD33} + 3.0 V	–0.5 to +6.6	V
Output voltage, 3.3 V buffer	V_O	3.0 V ≤ V_{DD33} ≤ 3.6 V V_O < V_{DD33} + 1.0 V	–0.5 to +4.6	V
Output voltage, 2.5 V buffer	V_O	2.3 V ≤ V_{DD25} ≤ 2.7 V V_O < V_{DD25} + 0.9 V	–0.5 to +3.6	V
Output current, 5 V buffer	I_O	I_{OL} = 6 mA	20	mA
Output current, 3.3 V buffer	I_O	I_{OL} = 6 mA	20	mA
		I_{OL} = 3 mA	10	mA
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		–65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameters. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

The ratings and conditions indicated for DC characteristics and AC characteristics represent the quality assurance range during normal operation.

Two Power Supply Rails Limitation

The μPD720133 has two power supply rails (2.5 V, 3.3 V). The system will require the power supply rail to be stable at V_{DD} level by a specified time. However, there are difference between the time of V_{DD25} and V_{DD33} becoming stable. The μPD720133 requires that V_{DD25} becomes stable before V_{DD33}. Also, it is necessary that V_{DD33} be powered within 100 ms after V_{DD25} became stable. In any case, the system must ensure that the absolute maximum ratings for V_I / V_O are not exceeded. System reset signaling must be asserted after the specified time of which both V_{DD25} and V_{DD33} become stable.

Recommended Operating Ranges

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating voltage	V_{DD33}	3.3 V for V_{DD33} pins	3.0	3.3	3.6	V
	V_{DD25}	2.5 V for V_{DD25} pins	2.3	2.5	2.7	V
	V_{DD25}	2.5 V for AV_{DD25} pins	2.3	2.5	2.7	V
High-level input voltage	V_{IH}					
5.0 V high-level input voltage			2.0		5.5	V
3.3 V high-level input voltage			2.0		V_{DD33}	V
2.5 V high-level input voltage			1.7		V_{DD25}	V
Low-level input voltage	V_{IL}					
5.0 V low-level input voltage			0		0.8	V
3.3 V low-level input voltage			0		0.8	V
2.5 V low-level input voltage			0		0.7	V
Hysteresis voltage	V_H					
5 V hysteresis voltage			0.3		1.5	V
3.3 V hysteresis voltage			0.2		1.0	V
Input rise time	t_{ri}					
Normal buffer			0		200	ns
Schmitt buffer			0		10	ms
Input fall time	t_{fi}					
Normal buffer			0		200	ns
Schmitt buffer			0		10	ms

DC Characteristics (V_{DD33} = 3.0 to 3.6 V, V_{DD25} = 2.3 to 2.7 V, T_A = 0 to +70°C)

Control Pin Block

Parameter	Symbol	Condition	Min.	Max.	Unit
Off-state output current	I_{OZ}	$V_O = V_{DD33}, V_{DD25}$ or V_{SS}		±10	μA
Output short circuit current	I_{OS} Note			−250	mA
Low-level output current	I_{OL}				
5.0 V low-level output current		V_{OL} = 0.4 V	6.0		mA
3.3 V low-level output current		V_{OL} = 0.4 V	6.0		mA
3.3 V low-level output current		V_{OL} = 0.4 V	3.0		mA
High-level output current	I_{OH}				
5.0 V high-level output current		V_{OH} = 2.4 V	−2.0		mA
3.3 V high-level output current		V_{OH} = 2.4 V	−6.0		mA
3.3 V high-level output current		V_{OH} = 2.4 V	−3.0		mA
Input leakage current	I_I				
3.3 V buffer		$V_I = V_{DD}$ or V_{SS}		±10	μA
5.0 V buffer		$V_I = V_{DD}$ or V_{SS}		±10	μA

Note It is specified under the assumption that only one pin on the LSI is short-circuited for not more than one second.

USB Interface Block

Parameter	Symbol	Conditions	Min.	Max.	Unit
Serial Resistor between DP (DM) and RSDP (RSDM)	R_S		38.61	39.39	Ω
Output pin impedance	Z_{HSDRV}	Includes R_S resistor	40.5	49.5	Ω
Bus pull-up resistor on upstream facing port	R_{PU}	1.5 kΩ ±5% consists of resistance of transistor and pull-up resistor	1.485	1.515	Ω
Termination voltage for upstream facing port pull-up	V_{TERM}		3.0	3.6	V
Input Levels for Full-speed:					
High-level input voltage (drive)	V_{IH}		2.0		V
High-level input voltage (floating)	V_{IHZ}		2.7	3.6	
Low-level input voltage	V_{IL}			0.8	V
Differential input sensitivity	V_{DI}	|(D+) – (D–)|	0.2		V
Differential common mode range	V_{CM}	Includes V_{DI} range	0.8	2.5	V
Output Levels for Full-speed:					
High-level output voltage	V_{OH}	R_L of 14.25 kΩ to V_{SS}	2.8	3.6	V
Low-level output voltage	V_{OL}	R_L of 1.425 kΩ to 3.6 V	0.0	0.3	V
SE1	V_{OSE1}		0.8		V
Output signal crossover point voltage	V_{CRS}		1.3	2.0	V
Input Levels for High-speed:					
High-speed squelch detection threshold (differential signal)	V_{HSSQ}		100	150	mV
High-speed disconnect detection threshold (differential signal)	V_{HSDSC}		525	625	mV
High-speed data signaling common mode voltage range	V_{HSCM}		–50	+500	mV
High-speed differential input signaling level	See **Figure 3-4**.				
Output Levels for High-speed:					
High-speed idle state	V_{HSOI}		–10.0	+10.0	mV
High-speed data signaling high	V_{HSOH}		360	440	mV
High-speed data signaling low	V_{HSOL}		–10.0	+10.0	mV
Chirp J level (differential signal)	V_{CHIRPJ}		700	1100	mV
Chirp K level (differential signal)	V_{CHIRPK}		–900	–500	mV

Figure 3-1. Differential Input Sensitivity Range for Low-/full-speed

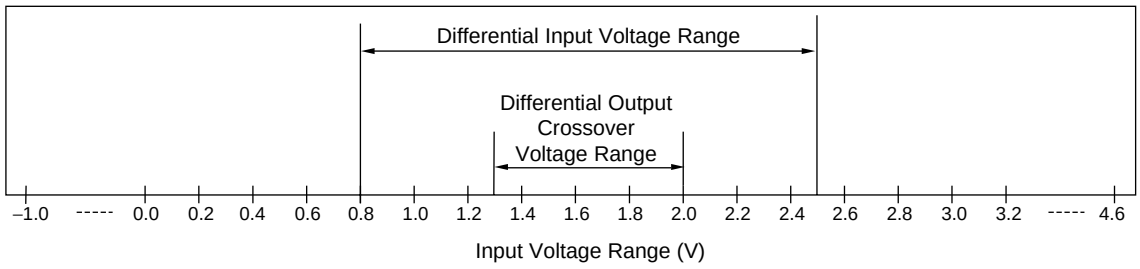


Figure 3-2. Full-speed Buffer V_{OH}/I_{OH} Characteristics for High-speed Capable Transceiver

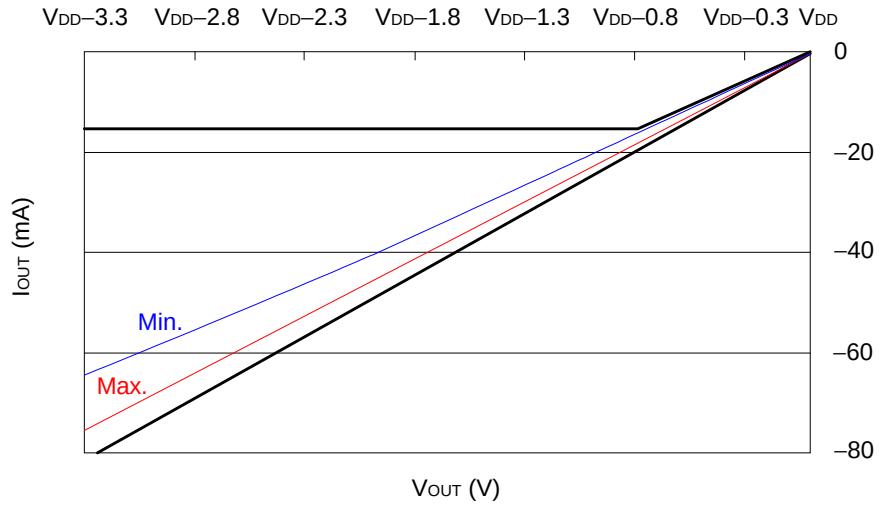


Figure 3-3. Full-speed Buffer V_{OL}/I_{OL} Characteristics for High-speed Capable Transceiver

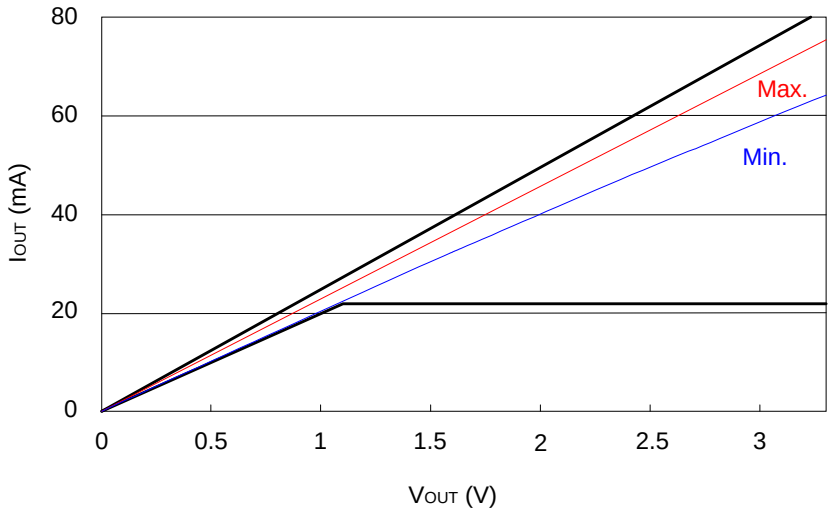


Figure 3-4. Receiver Sensitivity for Transceiver at DP/DM

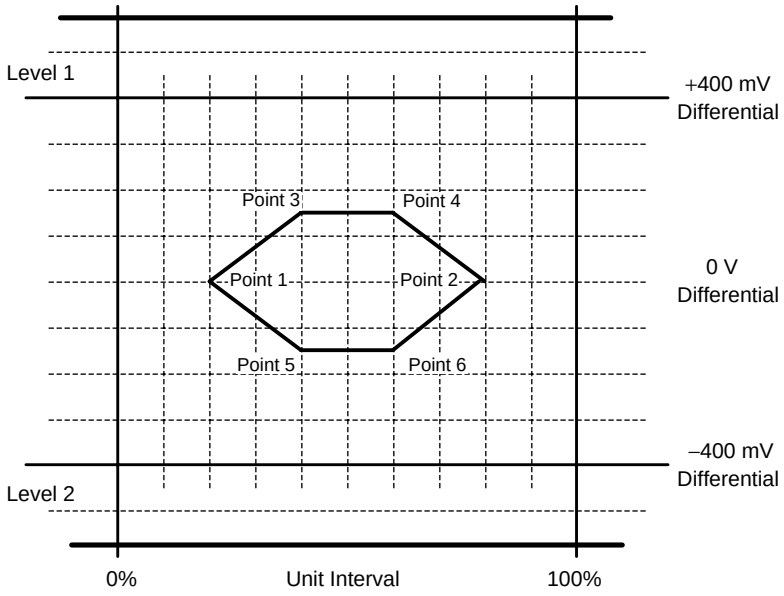
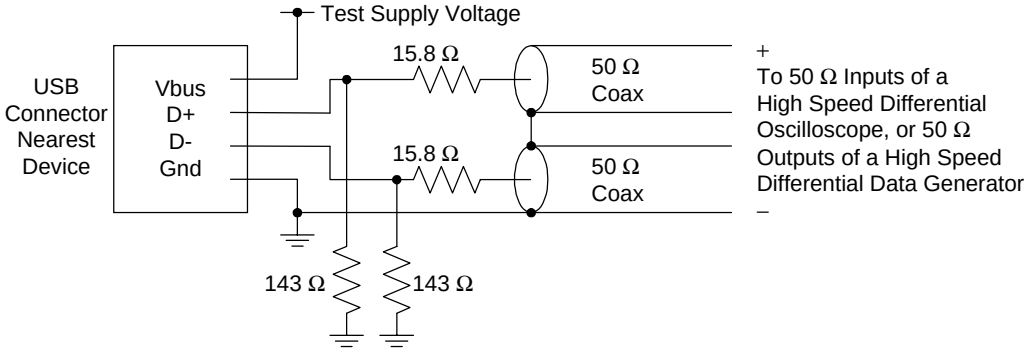


Figure 3-5. Receiver Measurement Fixtures



Pin Capacitance

Parameter	Symbol	Condition	Min.	Max.	Unit
Input capacitance	C_{IN}	V_{DD} = 0 V, T_A = 25°C	4	6	pF
Output capacitance	C_{OUT}	f_C = 1 MHz	4	6	pF
I/O capacitance	C_{IO}	Unmeasured pins returned to 0 V	4	6	pF

★ **Power Consumption**

(1) The power consumption when device works as bus-powered mode

Symbol	Condition	Max.			Unit
		V_{DD25}	V_{DD33}	AV_{DD25}	
$P_{ENUM-BUS}$	The power consumption during device unconfigured stage				
	High-speed operating	55	3	10	mA
	Full-speed operating	25	4	10	mA
P_{W-BUS}	The power consumption during device configured stage				
	High-speed operating	100	22	10	mA
	Full-speed operating	75	13	10	mA
$P_{W\_SPD-BUS}$	The power consumption under suspend state	15	235	5	μA

(2) The power consumption when device works as self-powered mode

Symbol	Condition	Max.			Unit
		V_{DD25}	V_{DD33}	AV_{DD25}	
$P_{ENUM-SELF}$	The power consumption during device unconfigured stage				
	High-speed operating	90	5	10	mA
	Full-speed operating	60	5	10	mA
P_{W-SELF}	The power consumption during device configured stage				
	High-speed operating	100	25	10	mA
	Full-speed operating	75	13	10	mA
$P_{W\_SPD-SELF}$	The power consumption under suspend state	50	500	15	μA
P_{W_UNP}	The power consumption under unplug state	50	500	15	μA
P_{W_COM}	The power consumption under combo mode The device is releasing the IDE bus.	50	500	15	μA

AC Characteristics (V_{DD33} = 3.0 to 3.6 V, V_{DD25} = 2.3 to 2.7 V, T_A = 0 to +70°C)

System Clock Ratings

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Clock frequency	f_{CLK}	X'tal	−500 ppm	30	+500 ppm	MHz
		Oscillator block	−500 ppm	30	+500 ppm	MHz
Clock duty cycle	t_{DUTY}		45	50	55	%

Remarks 1. Recommended accuracy of clock frequency is ± 100 ppm.

2. Required accuracy of X'tal or Oscillator block is including initial frequency accuracy, the spread of X'tal capacitor loading, supply voltage, temperature, and aging, etc.

System Reset signaling

Parameter	Symbol	Conditions	Min.	Max.	Unit
Reset active time	t_{rst}		2		μs

USB Interface Block

(1/2)

Parameter	Symbol	Conditions	Min.	Max.	Unit
Full-speed Source Electrical Characteristics					
Rise time (10% - 90%)	t_{FR}	C_L = 50 pF, R_S = 36 Ω	4	20	ns
Fall time (90% - 10%)	t_{FF}	C_L = 50 pF, R_S = 36 Ω	4	20	ns
Differential rise and fall time matching	t_{FRFM}	(t_{FR}/t_{FF})	90	111.11	%
Full-speed data rate for device which are high-speed capable	$t_{FDRATHS}$	Average bit rate	11.9940	12.0060	Mbps
Frame interval	t_{FRAME}		0.9995	1.0005	ms
Consecutive frame interval jitter	t_{RFI}	No clock adjustment		42	ns
Source jitter total (including frequency tolerance): To next transition For paired transitions	 t_{DJ1} t_{DJ2}		 −3.5 −4.0	 +3.5 +4.0	 ns ns
Source jitter for differential transition to SE0 transition	t_{FDEOP}		−2	+5	ns
Receiver jitter: To next transition For paired transitions	 t_{JR1} t_{JR2}		 −18.5 −9	 +18.5 +9	 ns ns
Source SE0 interval of EOP	t_{FEOPT}		160	175	ns
Receiver SE0 interval of EOP	t_{FEOPR}		82		ns
Width of SE0 interval during differential transition	t_{FST}			14	ns

(2/2)

Parameter	Symbol	Conditions	Min.	Max.	Unit
High-speed Source Electrical Characteristics					
Rise time (10% - 90%)	t_{HSR}		500		ps
Fall time (90% - 10%)	t_{HSF}		500		ps
Driver waveform	See **Figure 3-6**.				
High-speed data rate	t_{HSDRAT}		479.760	480.240	Mbps
Microframe interval	t_{HSFRAM}		124.9375	125.0625	μs
Consecutive microframe interval difference	t_{HSRFI}			4 high-speed	Bit times
Data source jitter	See **Figure 3-6**.				
Receiver jitter tolerance	See **Figure 3-4**.				
Device Event Timings					
Time from internal power good to device pulling D+ beyond V_{IHZ} (min.) (signaling attached)	t_{SIGATT}			100	ms
Debounce interval provided by USB system software after attach	t_{ATTDB}			100	ms
Inter-packet delay for full-speed	t_{IPD}		2		Bit times
Inter-packet delay for device response w/detachable cable for full-speed	$t_{RSPIPD1}$			6.5	Bit times
High-speed detection start time from suspend	t_{SCA}		2.5		μs
Sample time for suspend vs reset	t_{CSR}		100	875	μs
Time to detect bus suspend state	t_{SPD}		3.000	3.125	ms
Power down under suspend	t_{SUS}			10	ms
Reversion time from suspend to high-speed	t_{RHS}			1.333	μs
Drive Chirp K width	t_{CKO}		1		ms
Finish Chirp K assertion	t_{FCA}			7	ms
Start sequencing Chirp K-J-K-J-K-J	t_{SSC}			100	μs
Finish sequencing Chirp K-J	t_{FSC}		−500	−100	μs
Detect sequencing Chirp K-J width	t_{CSI}		2.5		μs
Sample time for sequencing Chirp	t_{SCS}		1	2.5	ms
Reversion time to high-speed	t_{RHA}			500	μs
High-speed detection start time	t_{HDS}		2.5	3000	μs
Reset completed time	t_{DRS}		10		ms

IDE Interface Block

PIO mode

Parameter	Symbol	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Unit
Cycle time (min.)	t_0	600	383	240	180	120	ns
Address setup time (min.)	t_1	70	50	30	30	25	ns
16 bits DIOR/DIOW pulse width (min.)	t_2	165	125	100	80	70	ns
8 bits DIOR/DIOW pulse width (min.)		290	290	290	80	70	ns
DIOR/DIOW recovery time (min.)	t_{2i}	–	–	–	70	25	ns
DIOW data setup time (min.)	t_3	60	45	30	30	20	ns
DIOW data hold time (min.)	t_4	30	20	15	10	10	ns
DIOR data setup time (min.)	t_5	50	35	20	20	20	ns
DIOR data hold time (min.)	t_6	5	5	5	5	5	ns
DIOR 3-state delay time (max.)	t_{6Z}	30	30	30	30	30	ns
Address hold time (min.)	t_9	20	15	10	10	10	ns
IORDY read data valid time (min.) Note	t_{RD}	0	0	0	0	0	ns
IORDY setup time (min.) Note	t_A	35	35	35	35	35	ns
IORDY pulse width (max.) Note	t_B	1250	1250	1250	1250	1250	ns
IORDY Inactive to Hi-Z time (max.) Note	t_C	5	5	5	5	5	ns

Note IORDY is an option in mode 0 - 2. IORDY is essential in modes 3 and 4.

Multi Word DMA mode

Parameter	Symbol	Mode 0	Mode 1	Mode 2	Unit
Cycle time (min.)	t_0	480	150	120	ns
DIOR/DIOW pulse width (min.)	t_D	215	80	70	ns
DIOR data access time (max.)	t_E	150	60	50	ns
DIOR data hold time (min.)	t_F	5	5	5	ns
DIOR data setup time (min.)	t_{Gr}	100	30	20	ns
DIOW data setup time (min.)	t_{Gw}	100	30	20	ns
DIOW data hold time (min.)	t_H	20	15	10	ns
DMACK setup time (min.)	t_I	0	0	0	ns
DMACK hold time (min.)	t_J	20	5	5	ns
DIOR negate pulse width (min.)	t_{Kr}	50	50	25	ns
DIOW negate pulse width (min.)	t_{Kw}	215	50	25	ns
DIOR-DMARQ delay time (max.)	t_{Lr}	120	40	35	ns
DIOW-DMARQ delay time (max.)	t_{Lw}	40	40	35	ns
DMACK 3-state delay time (max.)	t_Z	20	25	25	ns
CS setup time (min.)	t_M	50	30	25	ns
CS hold time (min.)	t_N	15	10	10	ns

Ultra DMA mode

Parameter	Symbol	Mode 0		Mode 1		Mode 2		Mode 3		Mode 4		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Average cycle time for 2 cycles	t_{2CYC}	240	-	160	-	120	-	90	-	60	-	ns
Minimum cycle time for 2 cycles	t_{2CYC}	235	-	156	-	117	-	86	-	57	-	ns
Cycle time for 1 cycle	t_{CYC}	114	-	75	-	55	-	39	-	25	-	ns
Data setup time on receive side	t_{DS}	15	-	10	-	7	-	7	-	5	-	ns
Data hold time on receive side	t_{DH}	5	-	5	-	5	-	5	-	5	-	ns
Data setup time on transmit side	t_{DVS}	70	-	48	-	34	-	20	-	6	-	ns
Data hold time on transmit side	t_{DVH}	6	-	6	-	6	-	6	-	6	-	ns
First STROBE time	t_{FS}	0	230	0	200	0	170	0	130	0	120	ns
Interlock time with limitation	t_{LI}	0	150	0	150	0	150	0	100	0	100	ns
Minimum interlock time	t_{MLI}	20	-	20	-	20	-	20	-	20	-	ns
Interlock time without limitation	t_{UI}	0	-	0	-	0	-	0	-	0	-	ns
Output release time	t_{AZ}	-	10	-	10	-	10	-	10	-	10	ns
Output delay time	t_{ZAH}	20	-	20	-	20	-	20	-	20	-	ns
Output stabilization time (from release)	t_{ZAD}	0	-	0	-	0	-	0	-	0	-	ns
Envelope time	t_{ENV}	20	70	20	70	20	70	20	55	20	55	ns
STROBE DMARDY delay time	t_{SR}	-	50	-	30	-	20	-	NA	-	NA	ns
Last STROBE time	t_{RFS}	-	75	-	60	-	50	-	60	-	60	ns
Pause time	t_{RP}	160	-	125	-	100	-	100	-	100	-	ns
IORDY pull-up time	t_{IORYZ}	-	20	-	20	-	20	-	20	-	20	ns
IORDY wait time	t_{ZIORY}	0	-	0	-	0	-	0	-	0	-	ns
DMACK setup/hold time	t_{ACK}	20	-	20	-	20	-	20	-	20	-	ns
STROBE STOP time	t_{SS}	50	-	50	-	50	-	50	-	50	-	ns

Serial ROM interface Block

Parameter	Symbol	Conditions	Min.	Max.	Unit
Clock frequency	t_{SCL}			100	KHz
Clock pulse width low	t_{LOW}		4.7		μs
Clock pulse width high	t_{HIGH}		4.0		μs
Clock Low to data valid	t_{AA}		100	4500	ns
Start hold time	$t_{HD.STA}$		4.0		μs
Start setup time	$t_{SU.STA}$		4.7		μs
Data in hold time	$t_{HD.DAT}$		0		ns
Data in setup time	$t_{SU.DAT}$		0.2		μs
Data out hold time	t_{DH}		50		ns
Stop setup time	$t_{SU.STO}$		4.7		μs
Time the bus must be free before a new transmission can start	t_{BUF}		10		μs
Write cycle time	t_{WR}		10		ms

Figure 3-6. Transmit Waveform for Transceiver at DP/DM

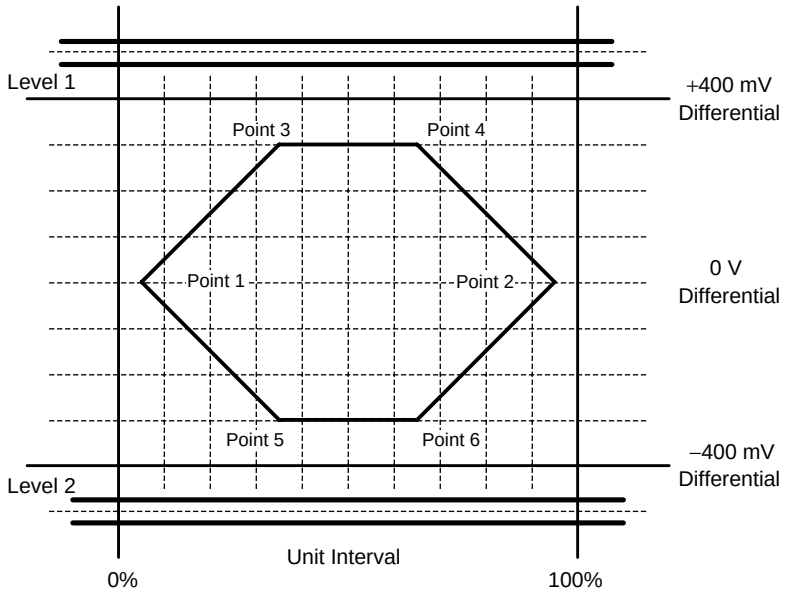
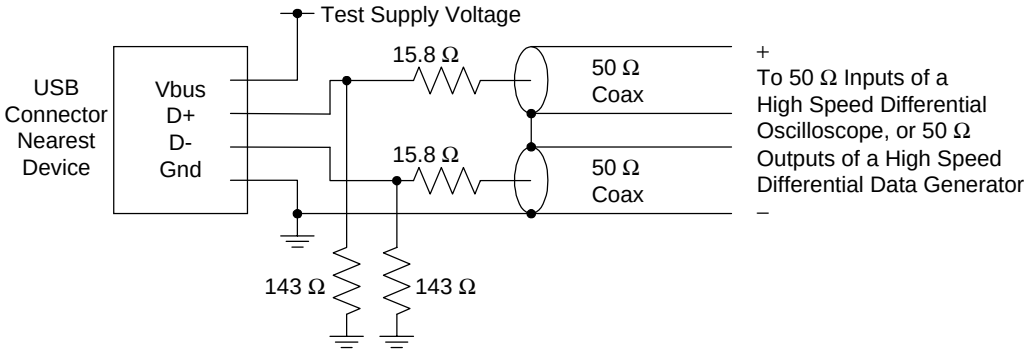
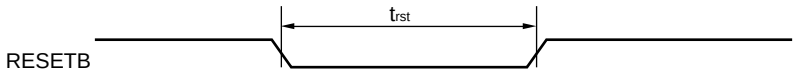


Figure 3-7. Transmitter Measurement Fixtures



Timing Diagram

System reset timing

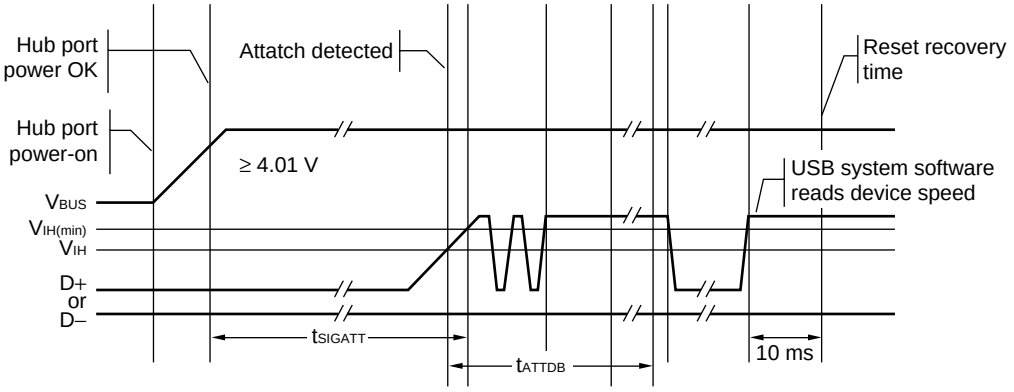


Remark After chip RESET, this chip reads the serial ROM first. Do not reset while the serial ROM is read. The read operation is completed in the period, which is calculated with the following expression.

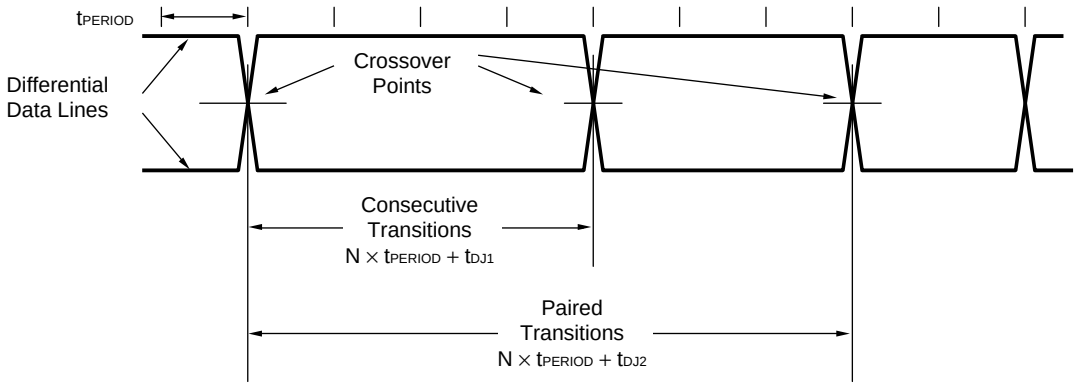
$5 + 0.1197 \times$ bytes (serial ROM size) $+ 0.5678$ (ms)

Example In the case of 512 bytes: 66.855 ms, in the case of 8 Kbytes: 986.15 ms

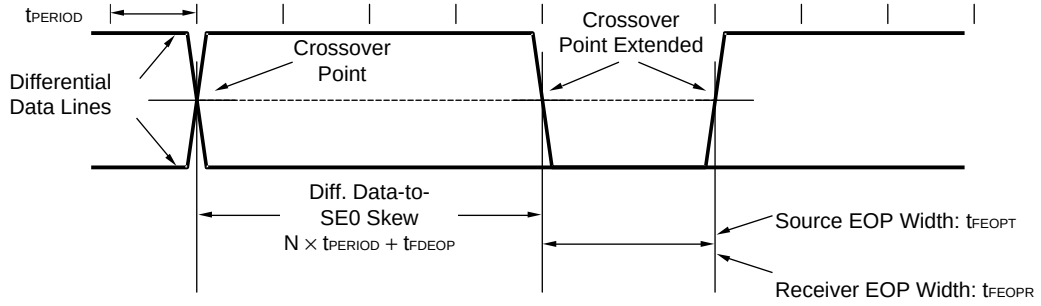
USB power-on and connection events



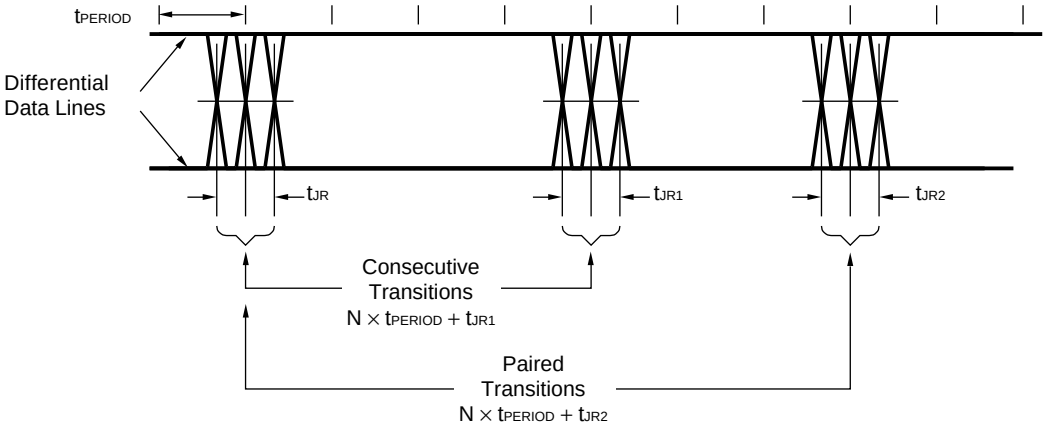
USB differential data jitter for full-speed



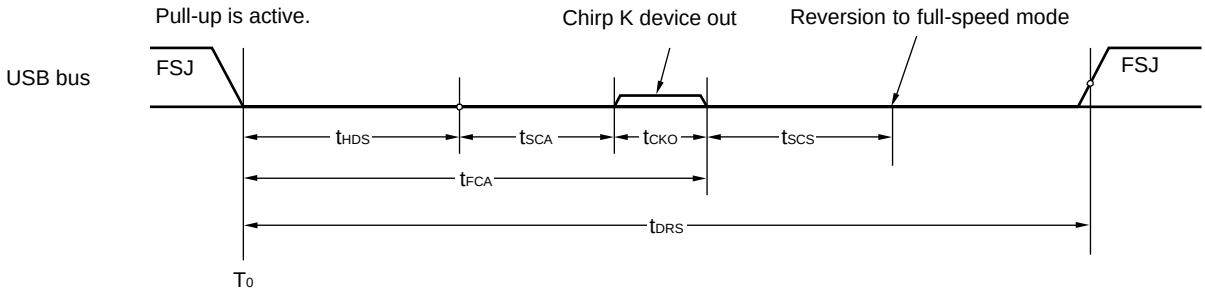
USB differential-to-EOP transition skew and EOP width for full-speed



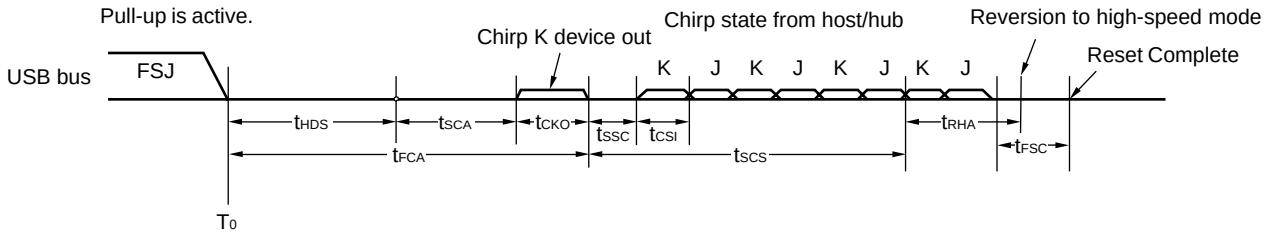
USB receiver jitter tolerance for full-speed



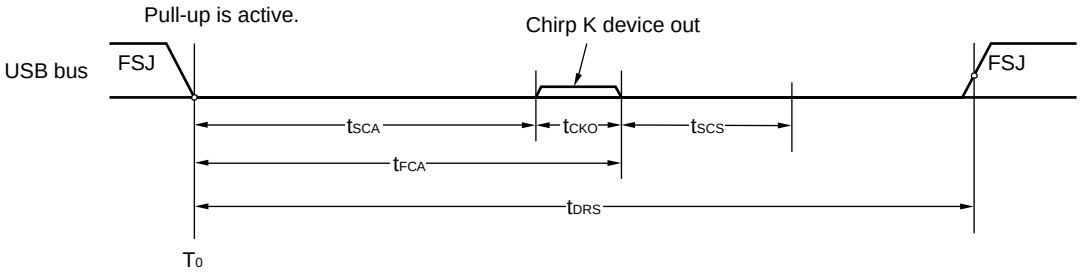
USB connection sequence on full-speed system bus



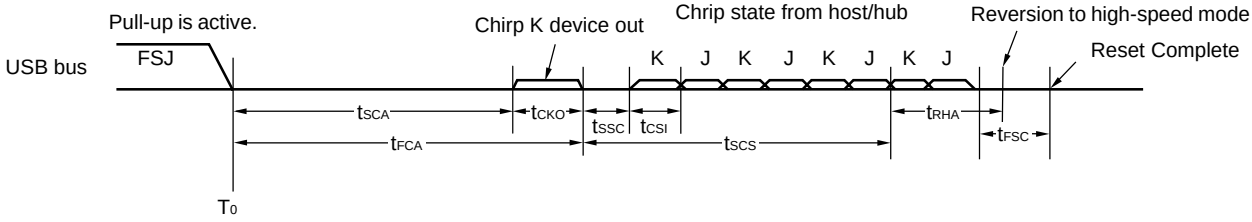
USB connection sequence on high-speed system bus



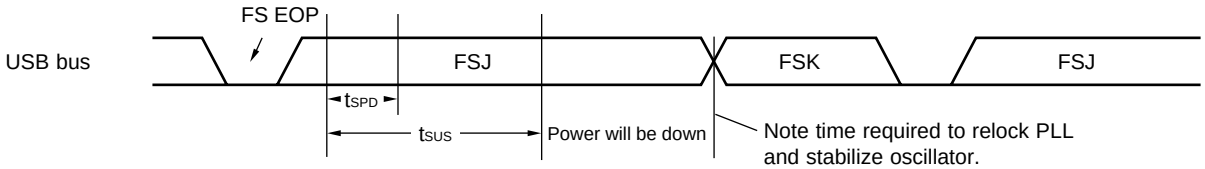
USB reset sequence from suspend state on full-speed system bus



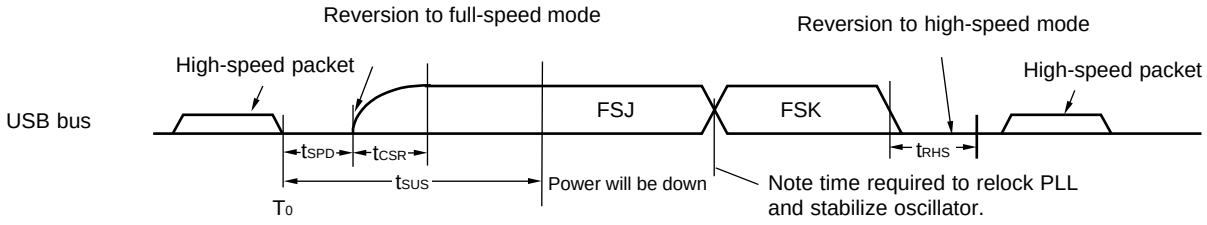
USB reset sequence from suspend state on high-speed system bus



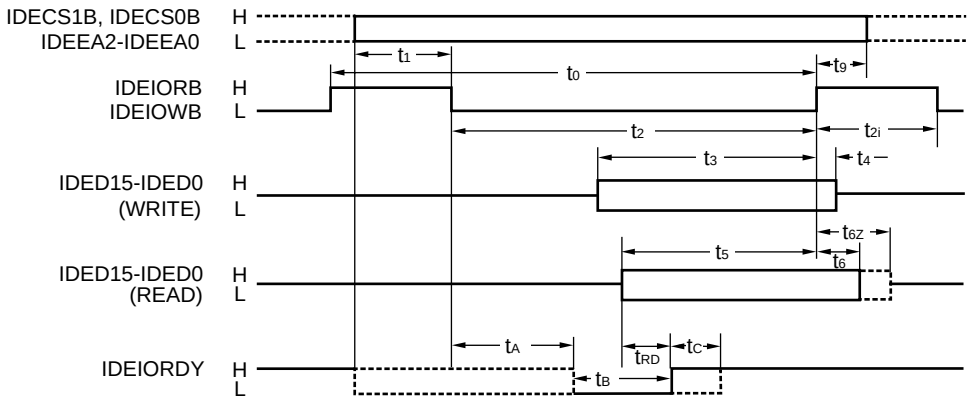
USB suspend and resume on full-speed system bus



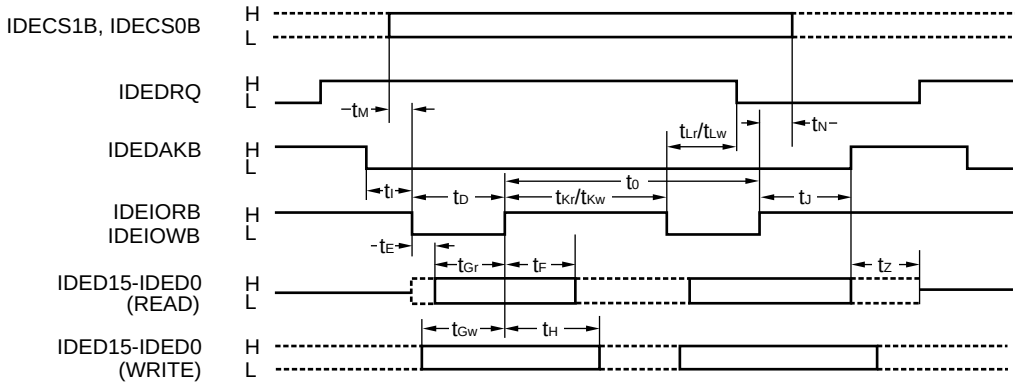
USB suspend and resume on high-speed system bus



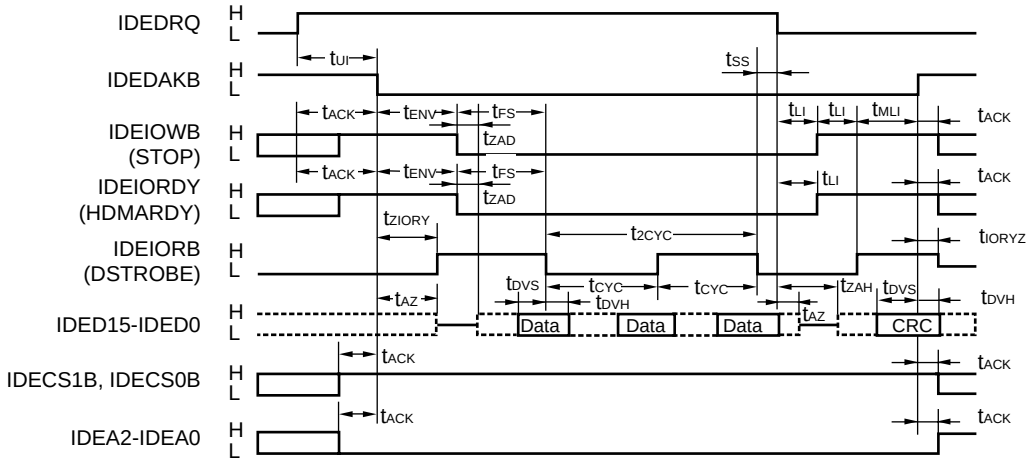
IDE PIO mode timing



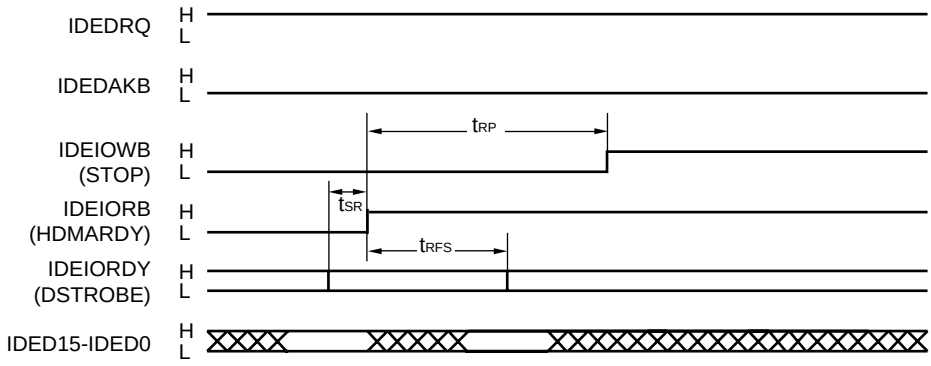
IDE multi word DMA mode timing



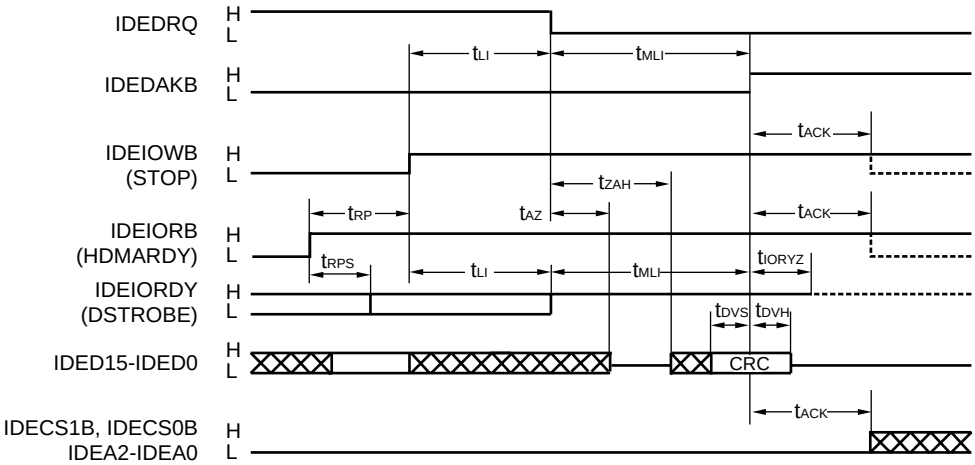
IDE ultra DMA mode data-in timing



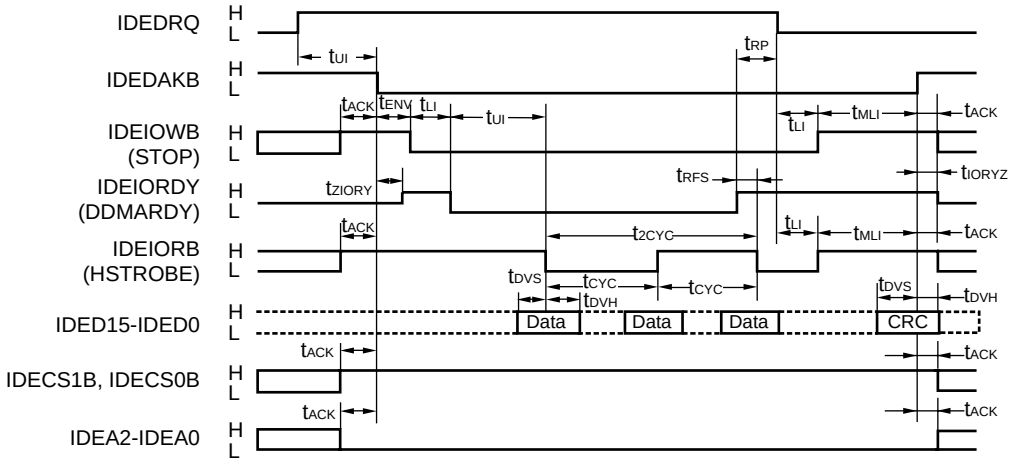
IDE ultra DMA mode data-in stop timing



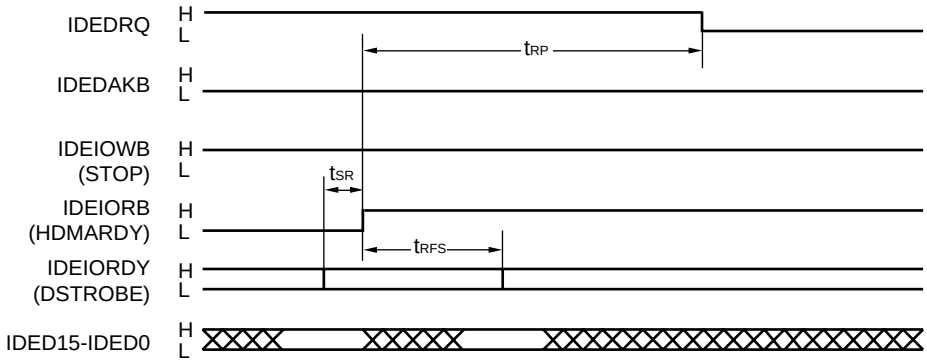
IDE ultra DMA mode data-in end timing



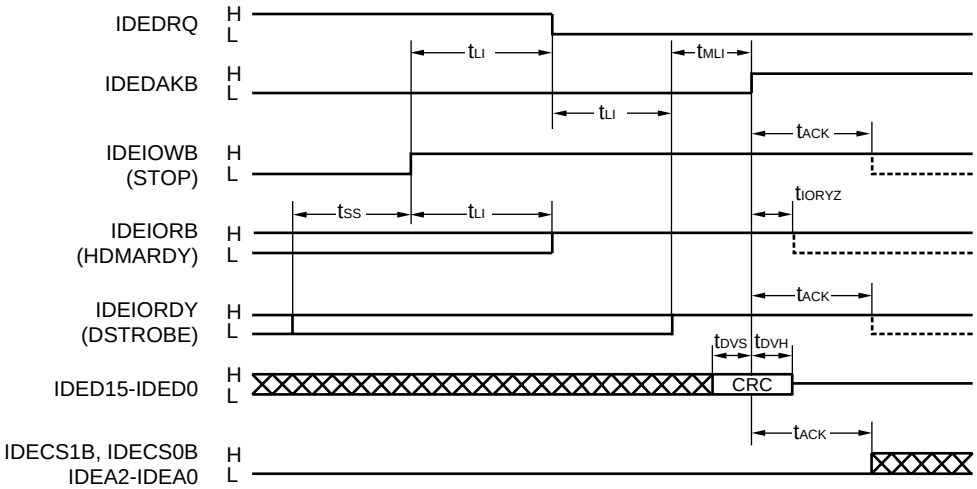
IDE ultra DMA mode data-out timing



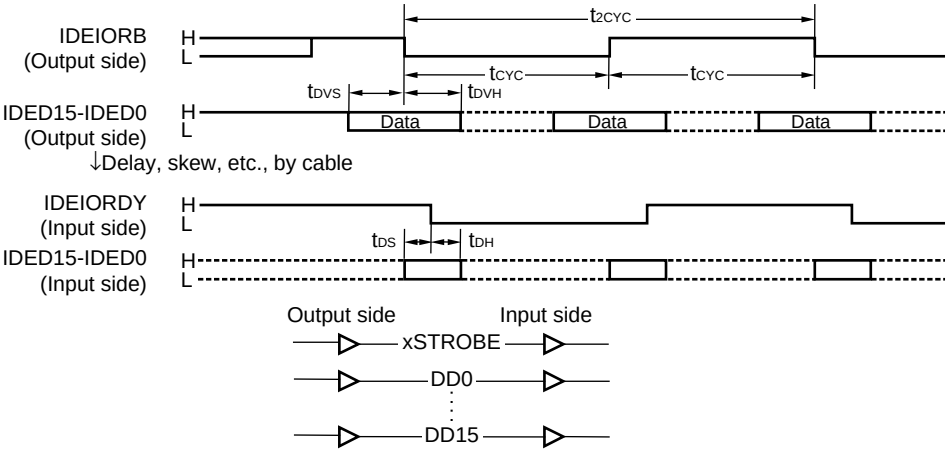
IDE ultra DMA mode data-out stop timing



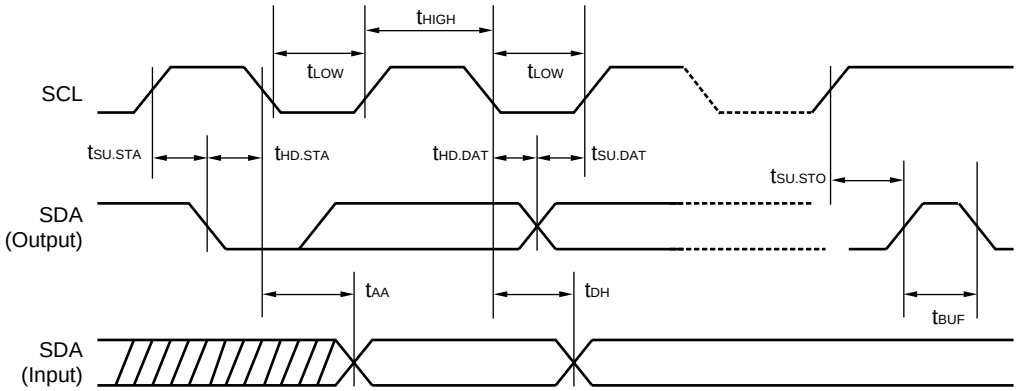
IDE ultra DMA mode data-out end timing



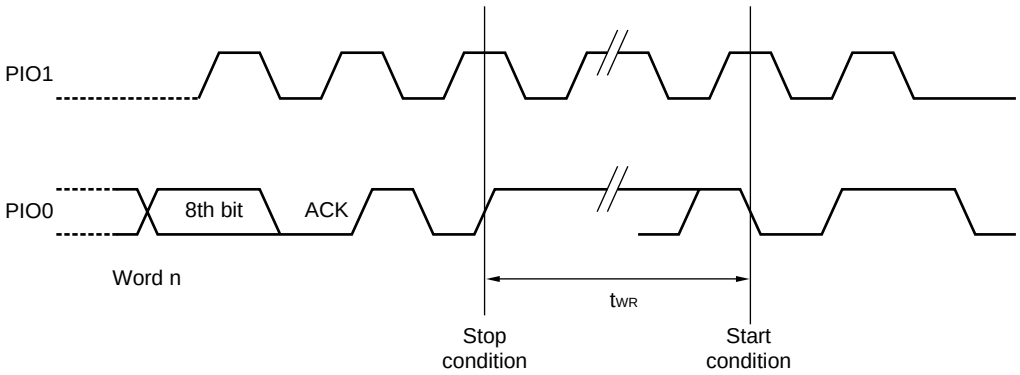
IDE ultra DMA mode data skew timing



Serial ROM access timing



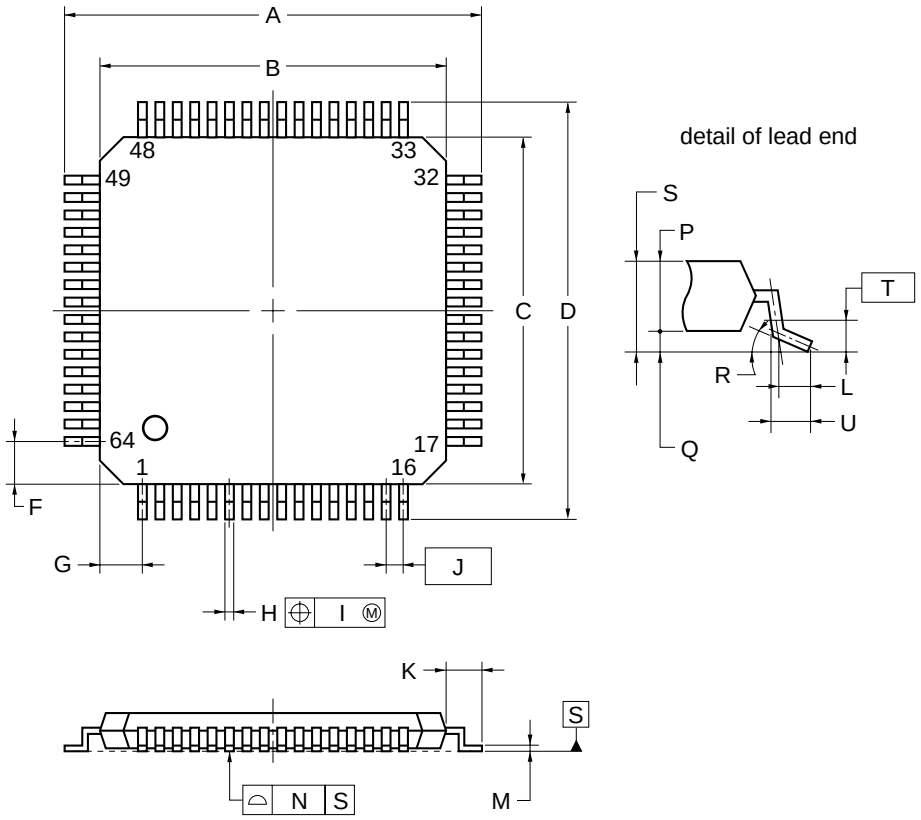
Serial ROM write cycle timing



4. PACKAGE DRAWING

- μPD720133GB-YEU-A
- μPD720133GB-YEU-Y

64-PIN PLASTIC TQFP (FINE PITCH) (10x10)



NOTE

Each lead centerline is located within 0.08 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	12.0±0.2
B	10.0±0.2
C	10.0±0.2
D	12.0±0.2
F	1.25
G	1.25
H	0.22±0.05
I	0.08
J	0.5 (T.P.)
K	1.0±0.2
L	0.5
M	$0.17^{+0.03}_{-0.07}$
N	0.08
P	1.0
Q	0.1±0.05
R	$3^{\circ}{}^{+4^{\circ}}_{-3^{\circ}}$
S	1.10±0.10
T	0.25
U	0.6±0.15

S64GB-50-YEU-1

5. RECOMMENDED SOLDERING CONDITIONS

The μPD720133 should be soldered and mounted under the following recommended conditions.

For soldering methods and conditions other than those recommended below, please contact your NEC Electronics sales representative.

For technical information, please refer to the following website.

Semiconductor Device Mount Manual (http://www.necel.com/pkg/en/mount/index.html)

★ **μPD720133GB-YEU-A / μPD720133GB-YEU-Y:64-pin plastic TQFP (Fine pitch) (10 × 10)**

Soldering Method	Soldering Conditions	Symbol
Infrared reflow	Package peak temperature : 260°C Time at peak temperature : within 10 seconds Time at 220°C or higher : within 60 seconds Preheat time (160 to 180°C) : 60 to 120 seconds Maximum count : 3 times or less Exposure limit : 3 days[Note] (after that, prebake at 125°C for 10 hours)	IR60-103-3
Partial heating	Pin temperature: 300°C max., Time: 3 seconds or less (per pin row)	–

Note After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

[MEMO]

NOTES FOR CMOS DEVICES

① VOLTAGE APPLICATION WAVEFORM AT INPUT PIN

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).

② HANDLING OF UNUSED INPUT PINS

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ PRECAUTION AGAINST ESD

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

④ STATUS BEFORE INITIALIZATION

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

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