



MCP23017/MCP23S17

16-Bit I/O Expander with Serial Interface

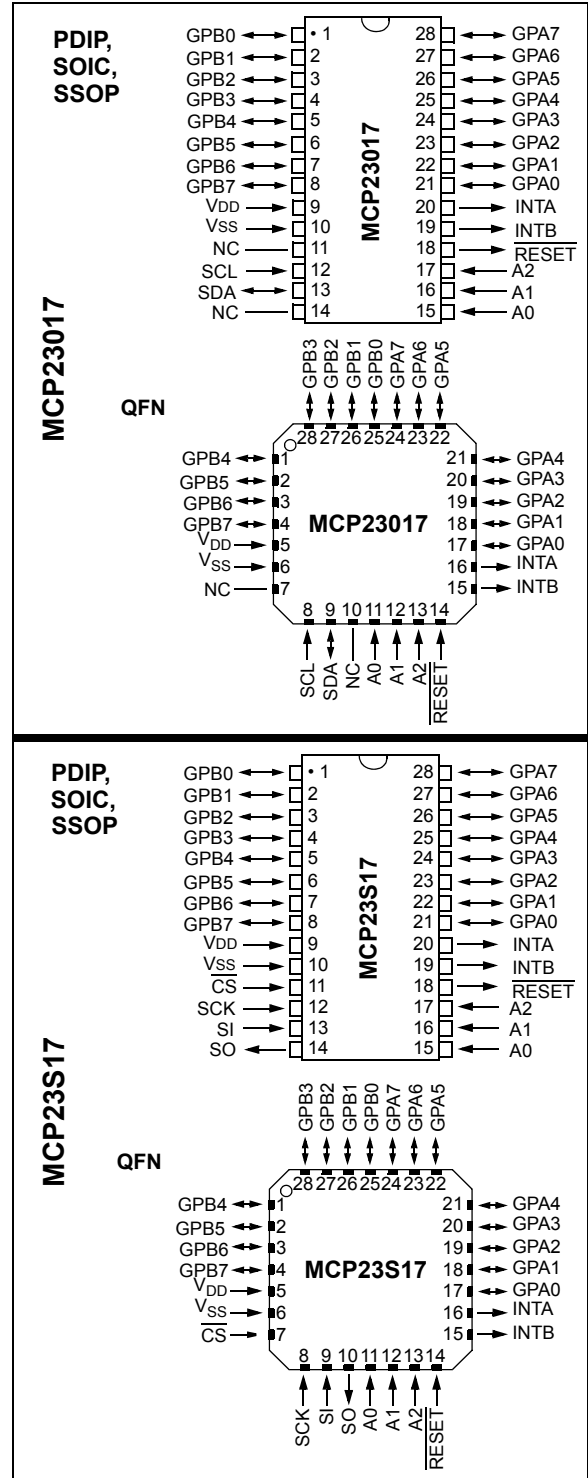
Features

- 16-bit remote bidirectional I/O port
 - I/O pins default to input
- High-speed I²C™ interface (**MCP23017**)
 - 100 kHz
 - 400 kHz
 - 1.7 MHz
- High-speed SPI interface (**MCP23S17**)
 - 10 MHz (max.)
- Three hardware address pins to allow up to eight devices on the bus
- Configurable interrupt output pins
 - Configurable as active-high, active-low or open-drain
- INTA and INTB can be configured to operate independently or together
- Configurable interrupt source
 - Interrupt-on-change from configured register defaults or pin changes
- Polarity Inversion register to configure the polarity of the input port data
- External Reset input
- Low standby current: 1 μA (max.)
- Operating voltage:
 - 1.8V to 5.5V @ -40°C to +85°C
 - 2.7V to 5.5V @ -40°C to +85°C
 - 4.5V to 5.5V @ -40°C to +125°C

Packages

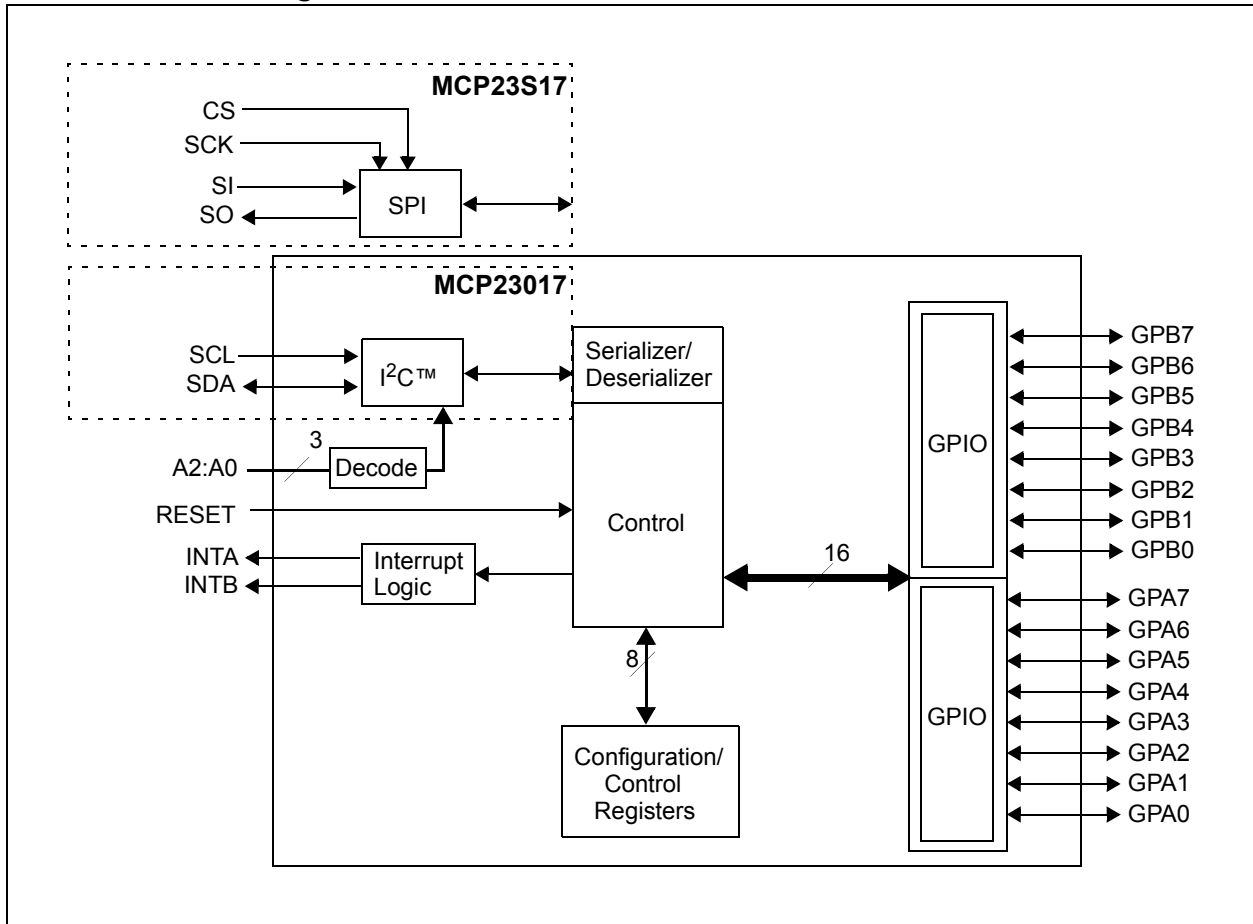
- 28-pin PDIP (300 mil)
- 28-pin SOIC (300 mil)
- 28-pin SSOP
- 28-pin QFN

Package Types



MCP23017/MCP23S17

Functional Block Diagram



1.0 DEVICE OVERVIEW

The MCP23017/MCP23S17 (MCP23X17) device family provides 16-bit, general purpose parallel I/O expansion for I²C bus or SPI applications. The two devices differ only in the serial interface.

- MCP23017 – I²C interface
- MCP23S17 – SPI interface

The MCP23X17 consists of multiple 8-bit configuration registers for input, output and polarity selection. The system master can enable the I/Os as either inputs or outputs by writing the I/O configuration bits (IODIRA/B). The data for each input or output is kept in the corresponding input or output register. The polarity of the Input Port register can be inverted with the Polarity Inversion register. All registers can be read by the system master.

The 16-bit I/O port functionally consists of two 8-bit ports (PORTA and PORTB). The MCP23X17 can be configured to operate in the 8-bit or 16-bit modes via IOCON.BANK.

There are two interrupt pins, INTA and INTB, that can be associated with their respective ports, or can be logically OR'ed together so that both pins will activate if either port causes an interrupt.

The interrupt output can be configured to activate under two conditions (mutually exclusive):

1. When any input state differs from its corresponding Input Port register state. This is used to indicate to the system master that an input state has changed.
2. When an input state differs from a preconfigured register value (DEFVAL register).

The Interrupt Capture register captures port values at the time of the interrupt, thereby saving the condition that caused the interrupt.

The Power-on Reset (POR) sets the registers to their default values and initializes the device state machine.

The hardware address pins are used to determine the device address.

MCP23017/MCP23S17

1.1 Pin Descriptions

TABLE 1-1: PINOUT DESCRIPTION

| Pin Name | PDIP/ SOIC/ SSOP | QFN | Pin Type | Function |
|----------------------------|------------------------|-----|----------|--|
| GPB0 | 1 | 25 | I/O | Bidirectional I/O pin. Can be enabled for interrupt-on-change and/or internal weak pull-up resistor. |
| GPB1 | 2 | 26 | I/O | Bidirectional I/O pin. Can be enabled for interrupt-on-change and/or internal weak pull-up resistor. |
| GPB2 | 3 | 27 | I/O | Bidirectional I/O pin. Can be enabled for interrupt-on-change and/or internal weak pull-up resistor. |
| GPB3 | 4 | 28 | I/O | Bidirectional I/O pin. Can be enabled for interrupt-on-change and/or internal weak pull-up resistor. |
| GPB4 | 5 | 1 | I/O | Bidirectional I/O pin. Can be enabled for interrupt-on-change and/or internal weak pull-up resistor. |
| GPB5 | 6 | 2 | I/O | Bidirectional I/O pin. Can be enabled for interrupt-on-change and/or internal weak pull-up resistor. |
| GPB6 | 7 | 3 | I/O | Bidirectional I/O pin. Can be enabled for interrupt-on-change and/or internal weak pull-up resistor. |
| GPB7 | 8 | 4 | I/O | Bidirectional I/O pin. Can be enabled for interrupt-on-change and/or internal weak pull-up resistor. |
| V _{DD} | 9 | 5 | P | Power |
| V _{SS} | 10 | 6 | P | Ground |
| NC/ $\overline{\text{CS}}$ | 11 | 7 | I | NC (MCP23017), Chip Select (MCP23S17) |
| SCL/SCK | 12 | 8 | I | Serial clock input |
| SDA/SI | 13 | 9 | I/O | Serial data I/O (MCP23017), Serial data input (MCP23S17) |
| NC/SO | 14 | 10 | O | NC (MCP23017), Serial data out (MCP23S17) |
| A0 | 15 | 11 | I | Hardware address pin. Must be externally biased. |
| A1 | 16 | 12 | I | Hardware address pin. Must be externally biased. |
| A2 | 17 | 13 | I | Hardware address pin. Must be externally biased. |
| $\overline{\text{RESET}}$ | 18 | 14 | I | Hardware reset. Must be externally biased. |
| INTB | 19 | 15 | O | Interrupt output for PORTB. Can be configured as active-high, active-low or open-drain. |
| INTA | 20 | 16 | O | Interrupt output for PORTA. Can be configured as active-high, active-low or open-drain. |
| GPA0 | 21 | 17 | I/O | Bidirectional I/O pin. Can be enabled for interrupt-on-change and/or internal weak pull-up resistor. |
| GPA1 | 22 | 18 | I/O | Bidirectional I/O pin. Can be enabled for interrupt-on-change and/or internal weak pull-up resistor. |
| GPA2 | 23 | 19 | I/O | Bidirectional I/O pin. Can be enabled for interrupt-on-change and/or internal weak pull-up resistor. |
| GPA3 | 24 | 20 | I/O | Bidirectional I/O pin. Can be enabled for interrupt-on-change and/or internal weak pull-up resistor. |
| GPA4 | 25 | 21 | I/O | Bidirectional I/O pin. Can be enabled for interrupt-on-change and/or internal weak pull-up resistor. |
| GPA5 | 26 | 22 | I/O | Bidirectional I/O pin. Can be enabled for interrupt-on-change and/or internal weak pull-up resistor. |
| GPA6 | 27 | 23 | I/O | Bidirectional I/O pin. Can be enabled for interrupt-on-change and/or internal weak pull-up resistor. |
| GPA7 | 28 | 24 | I/O | Bidirectional I/O pin. Can be enabled for interrupt-on-change and/or internal weak pull-up resistor. |

1.2 Power-on Reset (POR)

The on-chip POR circuit holds the device in reset until VDD has reached a high enough voltage to deactivate the POR circuit (i.e., release the device from reset). The maximum VDD rise time is specified in **Section 2.0 “Electrical Characteristics”**.

When the device exits the POR condition (releases reset), device operating parameters (i.e., voltage, temperature, serial bus frequency, etc.) must be met to ensure proper operation.

1.3 Serial Interface

This block handles the functionality of the I²C (MCP23017) or SPI (MCP23S17) interface protocol. The MCP23X17 contains 22 individual registers (11 register pairs) that can be addressed through the Serial Interface block, as shown in [Table 1-2](#).

TABLE 1-2: REGISTER ADDRESSES

| Address IOCON.BANK = 1 | Address IOCON.BANK = 0 | Access to: |
|---------------------------|---------------------------|------------|
| 00h | 00h | IODIRA |
| 10h | 01h | IODIRB |
| 01h | 02h | IPOLA |
| 11h | 03h | IPOLB |
| 02h | 04h | GPINTENA |
| 12h | 05h | GPINTENB |
| 03h | 06h | DEFVALA |
| 13h | 07h | DEFVALB |
| 04h | 08h | INTCONA |
| 14h | 09h | INTCONB |
| 05h | 0Ah | IOCON |
| 15h | 0Bh | IOCON |
| 06h | 0Ch | GPPUA |
| 16h | 0Dh | GPPUB |
| 07h | 0Eh | INTFA |
| 17h | 0Fh | INTFB |
| 08h | 10h | INTCAPA |
| 18h | 11h | INTCAPB |
| 09h | 12h | GPIOA |
| 19h | 13h | GPIOB |
| 0Ah | 14h | OLATA |
| 1Ah | 15h | OLATB |

1.3.1 BYTE MODE AND SEQUENTIAL MODE

The MCP23X17 family has the ability to operate in Byte mode or Sequential mode (IOCON.SEQOP).

Byte Mode disables automatic Address Pointer incrementing. When operating in Byte mode, the MCP23X17 family does not increment its internal address counter after each byte during the data transfer. This gives the ability to continually access the same address by providing extra clocks (without additional control bytes). This is useful for polling the GPIO register for data changes or for continually writing to the output latches.

A special mode (**Byte mode with IOCON.BANK = 0**) causes the address pointer to toggle between associated A/B register pairs. For example, if the BANK bit is cleared and the Address Pointer is initially set to address 12h (GPIOA) or 13h (GPIOB), the pointer will toggle between GPIOA and GPIOB. Note that the Address Pointer can initially point to either address in the register pair.

Sequential mode enables automatic address pointer incrementing. When operating in Sequential mode, the MCP23X17 family increments its address counter after each byte during the data transfer. The Address Pointer automatically rolls over to address 00h after accessing the last register.

These two modes are not to be confused with single writes/reads and continuous writes/reads that are serial protocol sequences. For example, the device may be configured for Byte mode and the master may perform a continuous read. In this case, the MCP23X17 would not increment the Address Pointer and would repeatedly drive data from the same location.

1.3.2 I²C INTERFACE

1.3.2.1 I²C Write Operation

The I²C write operation includes the control byte and register address sequence, as shown in the bottom of [Figure 1-1](#). This sequence is followed by eight bits of data from the master and an Acknowledge (ACK) from the MCP23017. The operation is ended with a Stop (P) or Restart (SR) condition being generated by the master.

Data is written to the MCP23017 after every byte transfer. If a Stop or Restart condition is generated during a data transfer, the data will not be written to the MCP23017.

Both “byte writes” and “sequential writes” are supported by the MCP23017. If Sequential mode is enabled (IOCON, SEQOP = 0) (default), the MCP23017 increments its address counter after each ACK during the data transfer.

MCP23017/MCP23S17

1.3.2.2 I²C Read Operation

I²C Read operations include the control byte sequence, as shown in the bottom of [Figure 1-1](#). This sequence is followed by another control byte (including the Start condition and ACK) with the R/W bit set (R/W = 1). The MCP23017 then transmits the data contained in the addressed register. The sequence is ended with the master generating a Stop or Restart condition.

1.3.2.3 I²C Sequential Write/Read

For sequential operations (Write or Read), instead of transmitting a Stop or Restart condition after the data transfer, the master clocks the next byte pointed to by the address pointer (see [Section 1.3.1 “Byte Mode and Sequential Mode”](#) for details regarding sequential operation control).

The sequence ends with the master sending a Stop or Restart condition.

The MCP23017 Address Pointer will roll over to address zero after reaching the last register address.

Refer to [Figure 1-1](#).

1.3.3 SPI INTERFACE

1.3.3.1 SPI Write Operation

The SPI write operation is started by lowering \overline{CS} . The Write command (slave address with R/W bit cleared) is then clocked into the device. The opcode is followed by an address and at least one data byte.

1.3.3.2 SPI Read Operation

The SPI read operation is started by lowering \overline{CS} . The SPI read command (slave address with R/W bit set) is then clocked into the device. The opcode is followed by an address, with at least one data byte being clocked out of the device.

1.3.3.3 SPI Sequential Write/Read

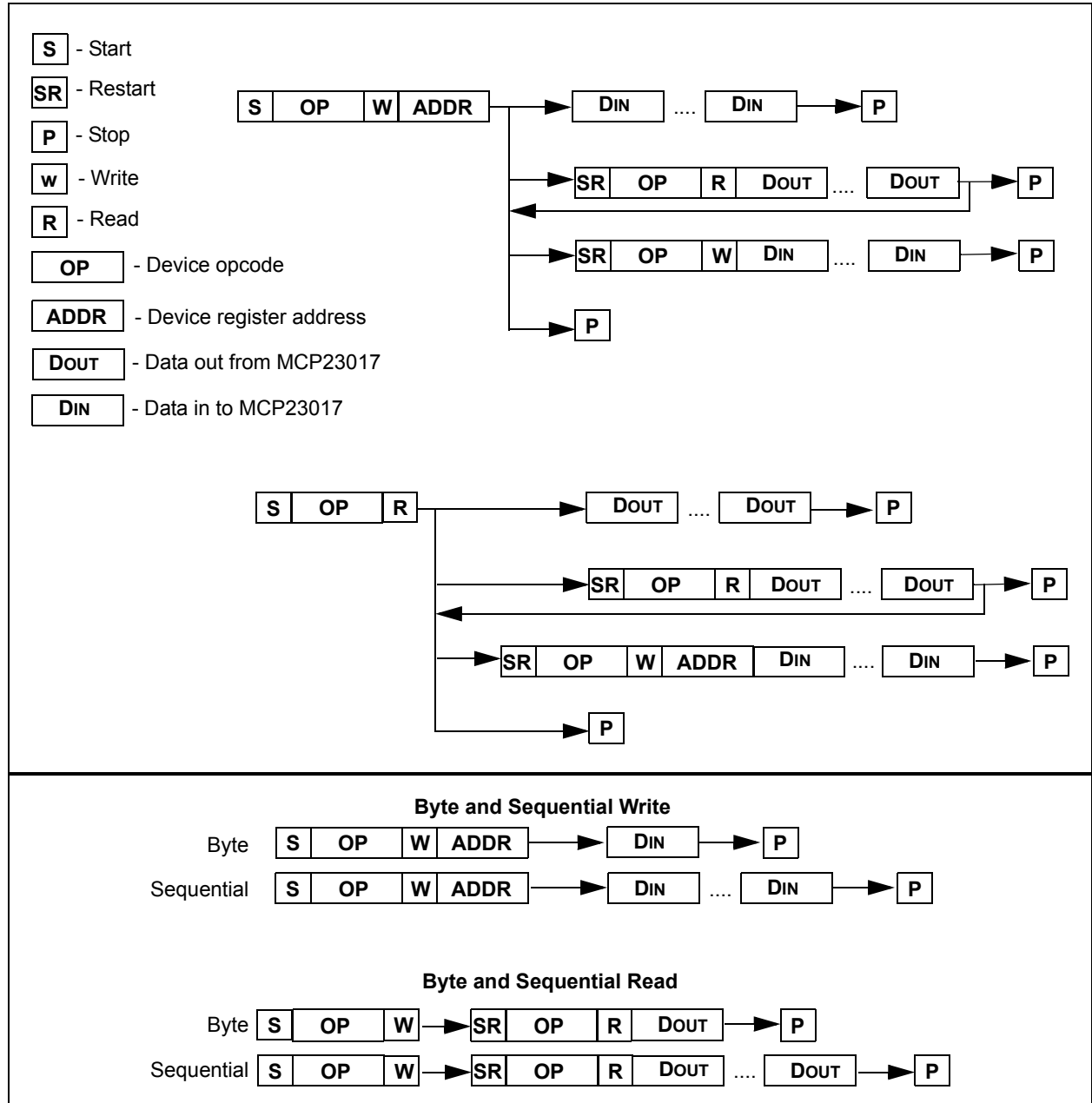
For sequential operations, instead of deselecting the device by raising \overline{CS} , the master clocks the next byte pointed to by the Address Pointer. (see [Section 1.3.1 “Byte Mode and Sequential Mode”](#) for details regarding sequential operation control).

The sequence ends by the raising of \overline{CS} .

The MCP23S17 Address Pointer will roll over to address zero after reaching the last register address.

MCP23017/MCP23S17

FIGURE 1-1: MCP23017 I²C™ DEVICE PROTOCOL



MCP23017/MCP23S17

1.4 Hardware Address Decoder

The hardware address pins are used to determine the device address. To address a device, the corresponding address bits in the control byte must match the pin state. The pins must be biased externally.

1.4.1 ADDRESSING I²C DEVICES (MCP23017)

The MCP23017 is a slave I²C interface device that supports 7-bit slave addressing, with the read/write bit filling out the control byte. The slave address contains four fixed bits and three user-defined hardware address bits (pins A2, A1 and A0). Figure 1-2 shows the control byte format.

1.4.2 ADDRESSING SPI DEVICES (MCP23S17)

The MCP23S17 is a slave SPI device. The slave address contains four fixed bits and three user-defined hardware address bits (if enabled via IOCON.HAEN) (pins A2, A1 and A0) with the read/write bit filling out the control byte. Figure 1-3 shows the control byte format. The address pins should be externally biased even if disabled (IOCON.HAEN = 0).

FIGURE 1-2: I²C™ CONTROL BYTE FORMAT

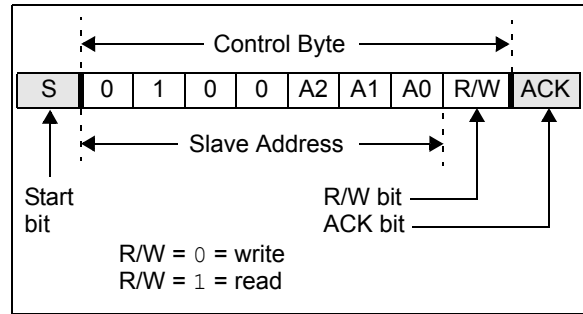


FIGURE 1-3: SPI CONTROL BYTE FORMAT

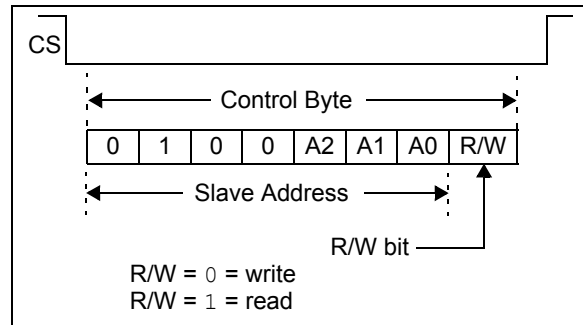


FIGURE 1-4: I²C™ ADDRESSING REGISTERS

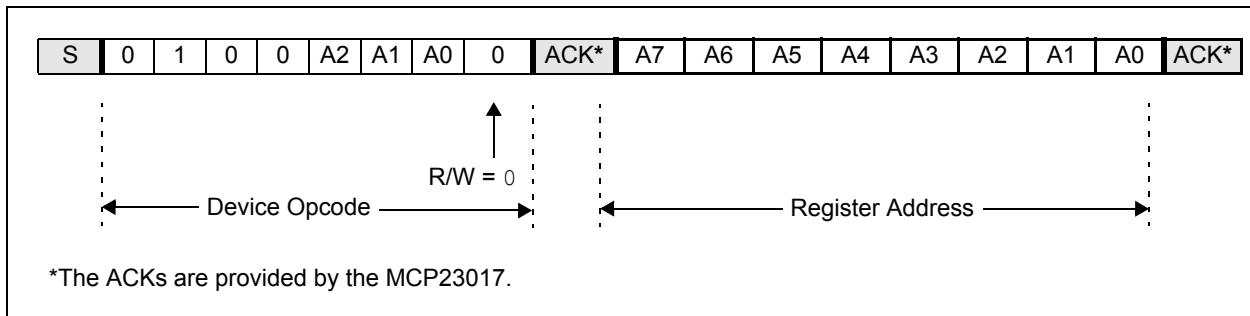
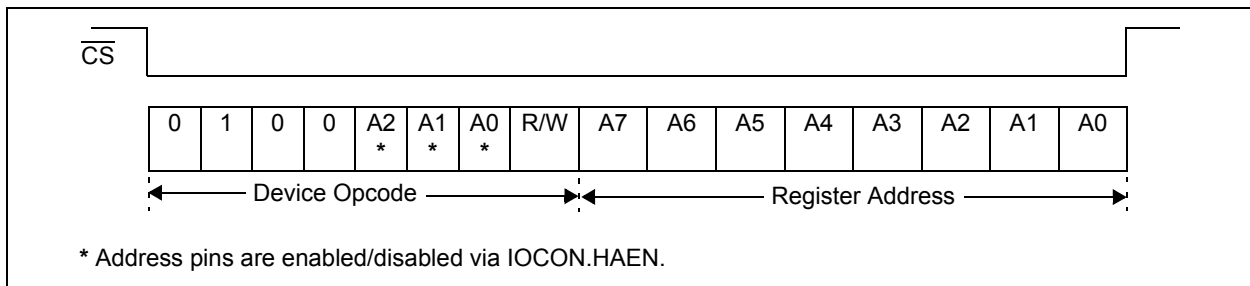


FIGURE 1-5: SPI ADDRESSING REGISTERS



MCP23017/MCP23S17

1.5 GPIO Port

The GPIO module is a general purpose, 16-bit wide, bidirectional port that is functionally split into two 8-bit wide ports.

The GPIO module contains the data ports (GPIO_n), internal pull-up resistors and the output latches (OLAT_n).

Reading the GPIO_n register reads the value on the port. Reading the OLAT_n register only reads the latches, not the actual value on the port.

Writing to the GPIO_n register actually causes a write to the latches (OLAT_n). Writing to the OLAT_n register forces the associated output drivers to drive to the level in OLAT_n. Pins configured as inputs turn off the associated output driver and put it in high-impedance.

TABLE 1-3: SUMMARY OF REGISTERS ASSOCIATED WITH THE GPIO PORTS (BANK = 1)

| Register Name | Address (hex) | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | POR/RST value |
|---------------|---------------|--------|--------|--------|--------|--------|--------|--------|--------|---------------|
| IODIRA | 00 | IO7 | IO6 | IO5 | IO4 | IO3 | IO2 | IO1 | IO0 | 1111 1111 |
| IPOLA | 01 | IP7 | IP6 | IP5 | IP4 | IP3 | IP2 | IP1 | IP0 | 0000 0000 |
| GPINTENA | 02 | GPINT7 | GPINT6 | GPINT5 | GPINT4 | GPINT3 | GPINT2 | GPINT1 | GPINT0 | 0000 0000 |
| GPPUA | 06 | PU7 | PU6 | PU5 | PU4 | PU3 | PU2 | PU1 | PU0 | 0000 0000 |
| GPIOA | 09 | GP7 | GP6 | GP5 | GP4 | GP3 | GP2 | GP1 | GP0 | 0000 0000 |
| OLATA | 0A | OL7 | OL6 | OL5 | OL4 | OL3 | OL2 | OL1 | OL0 | 0000 0000 |
| IODIRB | 10 | IO7 | IO6 | IO5 | IO4 | IO3 | IO2 | IO1 | IO0 | 1111 1111 |
| IPOLB | 11 | IP7 | IP6 | IP5 | IP4 | IP3 | IP2 | IP1 | IP0 | 0000 0000 |
| GPINTENB | 12 | GPINT7 | GPINT6 | GPINT5 | GPINT4 | GPINT3 | GPINT2 | GPINT1 | GPINT0 | 0000 0000 |
| GPPUB | 16 | PU7 | PU6 | PU5 | PU4 | PU3 | PU2 | PU1 | PU0 | 0000 0000 |
| GPIOB | 19 | GP7 | GP6 | GP5 | GP4 | GP3 | GP2 | GP1 | GP0 | 0000 0000 |
| OLATB | 1A | OL7 | OL6 | OL5 | OL4 | OL3 | OL2 | OL1 | OL0 | 0000 0000 |

TABLE 1-4: SUMMARY OF REGISTERS ASSOCIATED WITH THE GPIO PORTS (BANK = 0)

| Register Name | Address (hex) | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | POR/RST value |
|---------------|---------------|--------|--------|--------|--------|--------|--------|--------|--------|---------------|
| IODIRA | 00 | IO7 | IO6 | IO5 | IO4 | IO3 | IO2 | IO1 | IO0 | 1111 1111 |
| IODIRB | 01 | IO7 | IO6 | IO5 | IO4 | IO3 | IO2 | IO1 | IO0 | 1111 1111 |
| IPOLA | 02 | IP7 | IP6 | IP5 | IP4 | IP3 | IP2 | IP1 | IP0 | 0000 0000 |
| IPOLB | 03 | IP7 | IP6 | IP5 | IP4 | IP3 | IP2 | IP1 | IP0 | 0000 0000 |
| GPINTENA | 04 | GPINT7 | GPINT6 | GPINT5 | GPINT4 | GPINT3 | GPINT2 | GPINT1 | GPINT0 | 0000 0000 |
| GPINTENB | 05 | GPINT7 | GPINT6 | GPINT5 | GPINT4 | GPINT3 | GPINT2 | GPINT1 | GPINT0 | 0000 0000 |
| GPPUA | 0C | PU7 | PU6 | PU5 | PU4 | PU3 | PU2 | PU1 | PU0 | 0000 0000 |
| GPPUB | 0D | PU7 | PU6 | PU5 | PU4 | PU3 | PU2 | PU1 | PU0 | 0000 0000 |
| GPIOA | 12 | GP7 | GP6 | GP5 | GP4 | GP3 | GP2 | GP1 | GP0 | 0000 0000 |
| GPIOB | 13 | GP7 | GP6 | GP5 | GP4 | GP3 | GP2 | GP1 | GP0 | 0000 0000 |
| OLATA | 14 | OL7 | OL6 | OL5 | OL4 | OL3 | OL2 | OL1 | OL0 | 0000 0000 |
| OLATB | 15 | OL7 | OL6 | OL5 | OL4 | OL3 | OL2 | OL1 | OL0 | 0000 0000 |

MCP23017/MCP23S17

1.6 Configuration and Control Registers

There are 21 registers associated with the MCP23X17, as shown in [Table 1-5](#) and [Table 1-6](#). The two tables show the register mapping with the two BANK bit values. Ten registers are associated with PortA and ten

are associated with PortB. One register (IOCON) is shared between the two ports. The PortA registers are identical to the PortB registers, therefore, they will be referred to without differentiating between the port designation (i.e., they will not have the “A” or “B” designator assigned) in the register tables.

TABLE 1-5: CONTROL REGISTER SUMMARY (IOCON.BANK = 1)

| Register Name | Address (hex) | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | POR/RST value |
|---------------|---------------|--------|--------|--------|--------|--------|--------|--------|--------|---------------|
| IODIRA | 00 | IO7 | IO6 | IO5 | IO4 | IO3 | IO2 | IO1 | IO0 | 1111 1111 |
| IPOLA | 01 | IP7 | IP6 | IP5 | IP4 | IP3 | IP2 | IP1 | IP0 | 0000 0000 |
| GPINTENA | 02 | GPINT7 | GPINT6 | GPINT5 | GPINT4 | GPINT3 | GPINT2 | GPINT1 | GPINT0 | 0000 0000 |
| DEFVALA | 03 | DEF7 | DEF6 | DEF5 | DEF4 | DEF3 | DEF2 | DEF1 | DEF0 | 0000 0000 |
| INTCONA | 04 | IOC7 | IOC6 | IOC5 | IOC4 | IOC3 | IOC2 | IOC1 | IOC0 | 0000 0000 |
| IOCON | 05 | BANK | MIRROR | SEQOP | DISSLW | HAEN | ODR | INTPOL | — | 0000 0000 |
| GPPUA | 06 | PU7 | PU6 | PU5 | PU4 | PU3 | PU2 | PU1 | PU0 | 0000 0000 |
| INTFA | 07 | INT7 | INT6 | INT5 | INT4 | INT3 | INT2 | INT1 | INT0 | 0000 0000 |
| INTCAPA | 08 | ICP7 | ICP6 | ICP5 | ICP4 | ICP3 | ICP2 | ICP1 | ICP0 | 0000 0000 |
| GPIOA | 09 | GP7 | GP6 | GP5 | GP4 | GP3 | GP2 | GP1 | GP0 | 0000 0000 |
| OLATA | 0A | OL7 | OL6 | OL5 | OL4 | OL3 | OL2 | OL1 | OL0 | 0000 0000 |
| IODIRB | 10 | IO7 | IO6 | IO5 | IO4 | IO3 | IO2 | IO1 | IO0 | 1111 1111 |
| IPOLB | 11 | IP7 | IP6 | IP5 | IP4 | IP3 | IP2 | IP1 | IP0 | 0000 0000 |
| GPINTENB | 12 | GPINT7 | GPINT6 | GPINT5 | GPINT4 | GPINT3 | GPINT2 | GPINT1 | GPINT0 | 0000 0000 |
| DEFVALB | 13 | DEF7 | DEF6 | DEF5 | DEF4 | DEF3 | DEF2 | DEF1 | DEF0 | 0000 0000 |
| INTCONB | 14 | IOC7 | IOC6 | IOC5 | IOC4 | IOC3 | IOC2 | IOC1 | IOC0 | 0000 0000 |
| IOCON | 15 | BANK | MIRROR | SEQOP | DISSLW | HAEN | ODR | INTPOL | — | 0000 0000 |
| GPPUB | 16 | PU7 | PU6 | PU5 | PU4 | PU3 | PU2 | PU1 | PU0 | 0000 0000 |
| INTFB | 17 | INT7 | INT6 | INT5 | INT4 | INT3 | INT2 | INT1 | INT0 | 0000 0000 |
| INTCAPB | 18 | ICP7 | ICP6 | ICP5 | ICP4 | ICP3 | ICP2 | ICP1 | ICP0 | 0000 0000 |
| GPIOB | 19 | GP7 | GP6 | GP5 | GP4 | GP3 | GP2 | GP1 | GP0 | 0000 0000 |
| OLATB | 1A | OL7 | OL6 | OL5 | OL4 | OL3 | OL2 | OL1 | OL0 | 0000 0000 |

MCP23017/MCP23S17

TABLE 1-6: CONTROL REGISTER SUMMARY (IOCON.BANK = 0)

| Register Name | Address (hex) | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | POR/RST value |
|---------------|---------------|--------|--------|--------|--------|--------|--------|--------|--------|---------------|
| IODIRA | 00 | IO7 | IO6 | IO5 | IO4 | IO3 | IO2 | IO1 | IO0 | 1111 1111 |
| IODIRB | 01 | IO7 | IO6 | IO5 | IO4 | IO3 | IO2 | IO1 | IO0 | 1111 1111 |
| IPOLA | 02 | IP7 | IP6 | IP5 | IP4 | IP3 | IP2 | IP1 | IP0 | 0000 0000 |
| IPOLB | 03 | IP7 | IP6 | IP5 | IP4 | IP3 | IP2 | IP1 | IP0 | 0000 0000 |
| GPINTENA | 04 | GPINT7 | GPINT6 | GPINT5 | GPINT4 | GPINT3 | GPINT2 | GPINT1 | GPINT0 | 0000 0000 |
| GPINTENB | 05 | GPINT7 | GPINT6 | GPINT5 | GPINT4 | GPINT3 | GPINT2 | GPINT1 | GPINT0 | 0000 0000 |
| DEFVALA | 06 | DEF7 | DEF6 | DEF5 | DEF4 | DEF3 | DEF2 | DEF1 | DEF0 | 0000 0000 |
| DEFVALB | 07 | DEF7 | DEF6 | DEF5 | DEF4 | DEF3 | DEF2 | DEF1 | DEF0 | 0000 0000 |
| INTCONA | 08 | IOC7 | IOC6 | IOC5 | IOC4 | IOC3 | IOC2 | IOC1 | IOC0 | 0000 0000 |
| INTCONB | 09 | IOC7 | IOC6 | IOC5 | IOC4 | IOC3 | IOC2 | IOC1 | IOC0 | 0000 0000 |
| IOCON | 0A | BANK | MIRROR | SEQOP | DISSLW | HAEN | ODR | INTPOL | — | 0000 0000 |
| IOCON | 0B | BANK | MIRROR | SEQOP | DISSLW | HAEN | ODR | INTPOL | — | 0000 0000 |
| GPPUA | 0C | PU7 | PU6 | PU5 | PU4 | PU3 | PU2 | PU1 | PU0 | 0000 0000 |
| GPPUB | 0D | PU7 | PU6 | PU5 | PU4 | PU3 | PU2 | PU1 | PU0 | 0000 0000 |
| INTFA | 0E | INT7 | INT6 | INT5 | INT4 | INT3 | INT2 | INT1 | INT0 | 0000 0000 |
| INTFB | 0F | INT7 | INT6 | INT5 | INT4 | INT3 | INT2 | INT1 | INT0 | 0000 0000 |
| INTCAPA | 10 | ICP7 | ICP6 | ICP5 | ICP4 | ICP3 | ICP2 | ICP1 | ICP0 | 0000 0000 |
| INTCAPB | 11 | ICP7 | ICP6 | ICP5 | ICP4 | ICP3 | ICP2 | ICP1 | ICP0 | 0000 0000 |
| GPIOA | 12 | GP7 | GP6 | GP5 | GP4 | GP3 | GP2 | GP1 | GP0 | 0000 0000 |
| GPIOB | 13 | GP7 | GP6 | GP5 | GP4 | GP3 | GP2 | GP1 | GP0 | 0000 0000 |
| OLATA | 14 | OL7 | OL6 | OL5 | OL4 | OL3 | OL2 | OL1 | OL0 | 0000 0000 |
| OLATB | 15 | OL7 | OL6 | OL5 | OL4 | OL3 | OL2 | OL1 | OL0 | 0000 0000 |

MCP23017/MCP23S17

1.6.1 I/O DIRECTION REGISTER

Controls the direction of the data I/O.

When a bit is set, the corresponding pin becomes an input. When a bit is clear, the corresponding pin becomes an output.

REGISTER 1-1: IODIR – I/O DIRECTION REGISTER (ADDR 0x00)

| R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| IO7 | IO6 | IO5 | IO4 | IO3 | IO2 | IO1 | IO0 |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7-0

IO7:IO0: These bits control the direction of data I/O <7:0>

1 = Pin is configured as an input.

0 = Pin is configured as an output.

1.6.2 INPUT POLARITY REGISTER

This register allows the user to configure the polarity on the corresponding GPIO port bits.

If a bit is set, the corresponding GPIO register bit will reflect the inverted value on the pin.

REGISTER 1-2: IPOL – INPUT POLARITY PORT REGISTER (ADDR 0x01)

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| IP7 | IP6 | IP5 | IP4 | IP3 | IP2 | IP1 | IP0 |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7-0

IP7:IP0: These bits control the polarity inversion of the input pins <7:0>

1 = GPIO register bit will reflect the opposite logic state of the input pin.

0 = GPIO register bit will reflect the same logic state of the input pin.

MCP23017/MCP23S17

1.6.3 INTERRUPT-ON-CHANGE CONTROL REGISTER

The GPINTEN register controls the interrupt-on-change feature for each pin.

If a bit is set, the corresponding pin is enabled for interrupt-on-change. The DEFVAL and INTCON registers must also be configured if any pins are enabled for interrupt-on-change.

REGISTER 1-3: GPINTEN – INTERRUPT-ON-CHANGE PINS (ADDR 0x02)

| | | | | | | | |
|--------|--------|--------|--------|--------|--------|--------|--------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| GPINT7 | GPINT6 | GPINT5 | GPINT4 | GPINT3 | GPINT2 | GPINT1 | GPINT0 |
| bit 7 | | | | | | | bit 0 |

| | | | |
|-------------------|------------------|------------------------------------|--------------------|
| Legend: | | | |
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 7-0 **GPINT7:GPINT0:** General purpose I/O interrupt-on-change bits <7:0>
1 = Enable GPIO input pin for interrupt-on-change event.
0 = Disable GPIO input pin for interrupt-on-change event.

Refer to INTCON and GPINTEN.

1.6.4 DEFAULT COMPARE REGISTER FOR INTERRUPT-ON-CHANGE

The default comparison value is configured in the DEFVAL register. If enabled (via GPINTEN and INTCON) to compare against the DEFVAL register, an opposite value on the associated pin will cause an interrupt to occur.

REGISTER 1-4: DEFVAL – DEFAULT VALUE REGISTER (ADDR 0x03)

| | | | | | | | |
|-------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| DEF7 | DEF6 | DEF5 | DEF4 | DEF3 | DEF2 | DEF1 | DEF0 |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7-0

DEF7:DEF0: These bits set the compare value for pins configured for interrupt-on-change from defaults <7:0>. Refer to INTCON.

If the associated pin level is the opposite from the register bit, an interrupt occurs.

Refer to INTCON and GPINTEN.

MCP23017/MCP23S17

1.6.5 INTERRUPT CONTROL REGISTER

The INTCON register controls how the associated pin value is compared for the interrupt-on-change feature. If a bit is set, the corresponding I/O pin is compared against the associated bit in the DEFVAL register. If a bit value is clear, the corresponding I/O pin is compared against the previous value.

REGISTER 1-5: INTCON – INTERRUPT-ON-CHANGE CONTROL REGISTER (ADDR 0x04)

| | | | | | | | |
|-------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| IOC7 | IOC6 | IOC5 | IOC4 | IOC3 | IOC2 | IOC1 | IOC0 |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7-0 **IOC7:IOC0:** These bits control how the associated pin value is compared for interrupt-on-change <7:0>

1 = Controls how the associated pin value is compared for interrupt-on-change.

0 = Pin value is compared against the previous pin value.

Refer to INTCON and GPINTEN.

1.6.6 CONFIGURATION REGISTER

The IOCON register contains several bits for configuring the device:

The **BANK** bit changes how the registers are mapped (see [Table 1-5](#) and [Table 1-6](#) for more details).

- If **BANK** = 1, the registers associated with each port are segregated. Registers associated with PORTA are mapped from address 00h - 0Ah and registers associated with PORTB are mapped from 10h - 1Ah.
- If **BANK** = 0, the A/B registers are paired. For example, IODIRA is mapped to address 00h and IODIRB is mapped to the next address (address 01h). The mapping for all registers is from 00h - 15h.

It is important to take care when changing the **BANK** bit as the address mapping changes after the byte is clocked into the device. The address pointer may point to an invalid location after the bit is modified.

For example, if the device is configured to automatically increment its internal Address Pointer, the following scenario would occur:

- **BANK** = 0
- Write 80h to address 0Ah (IOCON) to set the **BANK** bit
- Once the write completes, the internal address now points to 0Bh which is an invalid address when the **BANK** bit is set.

For this reason, it is advised to only perform byte writes to this register when changing the **BANK** bit.

The **MIRROR** bit controls how the INTA and INTB pins function with respect to each other.

- When **MIRROR** = 1, the INTn pins are functionally OR'ed so that an interrupt on either port will cause both pins to activate.
- When **MIRROR** = 0, the INT pins are separated. Interrupt conditions on a port will cause its respective INT pin to activate.

The Sequential Operation (**SEQOP**) controls the incrementing function of the Address Pointer. If the address pointer is disabled, the Address Pointer does not automatically increment after each byte is clocked during a serial transfer. This feature is useful when it is desired to continuously poll (read) or modify (write) a register.

The Slew Rate (**DISSLW**) bit controls the slew rate function on the SDA pin. If enabled, the SDA slew rate will be controlled when driving from a high to low.

The Hardware Address Enable (**HAEN**) bit enables/disables hardware addressing on the MCP23S17 only. The address pins (A2, A1 and A0) must be externally biased, regardless of the **HAEN** bit value.

If enabled (**HAEN** = 1), the device's hardware address matches the address pins.

If disabled (**HAEN** = 0), the device's hardware address is A2 = A1 = A0 = 0.

The Open-Drain (**ODR**) control bit enables/disables the INT pin for open-drain configuration. Erasing this bit overrides the **INTPOL** bit.

The Interrupt Polarity (**INTPOL**) sets the polarity of the INT pin. This bit is functional only when the **ODR** bit is cleared, configuring the INT pin as active push-pull.

MCP23017/MCP23S17

REGISTER 1-6: IOCON – I/O EXPANDER CONFIGURATION REGISTER (ADDR 0x05)

| | | | | | | | |
|-------|--------|-------|--------|-------|-------|--------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 |
| BANK | MIRROR | SEQOP | DISSLW | HAEN | ODR | INTPOL | — |
| bit 7 | | | | | | | bit 0 |

| | | | |
|-------------------|------------------|------------------------------------|--------------------|
| Legend: | | | |
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

- bit 7 **BANK:** Controls how the registers are addressed
 - 1 = The registers associated with each port are separated into different banks
 - 0 = The registers are in the same bank (addresses are sequential)

- bit 6 **MIRROR:** INT Pins Mirror bit
 - 1 = The INT pins are internally connected
 - 0 = The INT pins are not connected. INTA is associated with PortA and INTB is associated with PortB

- bit 5 **SEQOP:** Sequential Operation mode bit.
 - 1 = Sequential operation disabled, address pointer does not increment.
 - 0 = Sequential operation enabled, address pointer increments.

- bit 4 **DISSLW:** Slew Rate control bit for SDA output.
 - 1 = Slew rate disabled.
 - 0 = Slew rate enabled.

- bit 3 **HAEN:** Hardware Address Enable bit (MCP23S17 only).
Address pins are always enabled on MCP23017.
 - 1 = Enables the MCP23S17 address pins.
 - 0 = Disables the MCP23S17 address pins.

- bit 2 **ODR:** This bit configures the INT pin as an open-drain output.
 - 1 = Open-drain output (overrides the INTPOL bit).
 - 0 = Active driver output (INTPOL bit sets the polarity).

- bit 1 **INTPOL:** This bit sets the polarity of the INT output pin.
 - 1 = Active-high.
 - 0 = Active-low.

- bit 0 **Unimplemented:** Read as '0'.

1.6.7 PULL-UP RESISTOR CONFIGURATION REGISTER

The GPPU register controls the pull-up resistors for the port pins. If a bit is set and the corresponding pin is configured as an input, the corresponding port pin is internally pulled up with a 100 k Ω resistor.

REGISTER 1-7: GPPU – GPIO PULL-UP RESISTOR REGISTER (ADDR 0x06)

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| PU7 | PU6 | PU5 | PU4 | PU3 | PU2 | PU1 | PU0 |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7-0 **PU7:PU0:** These bits control the weak pull-up resistors on each pin (when configured as an input) <7:0>.

1 = Pull-up enabled.

0 = Pull-up disabled.

MCP23017/MCP23S17

1.6.8 INTERRUPT FLAG REGISTER

The INTF register reflects the interrupt condition on the port pins of any pin that is enabled for interrupts via the GPINTEN register. A 'set' bit indicates that the associated pin caused the interrupt.

This register is 'read-only'. Writes to this register will be ignored.

REGISTER 1-8: INTF – INTERRUPT FLAG REGISTER (ADDR 0x07)

| | | | | | | | |
|-------|------|------|------|------|------|------|-------|
| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| INT7 | INT6 | INT5 | INT4 | INT3 | INT2 | INT1 | INT0 |
| bit 7 | | | | | | | bit 0 |

Legend:

| | | | |
|-------------------|------------------|------------------------------------|--------------------|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 7-0 **INT7:INT0:** These bits reflect the interrupt condition on the port. Will reflect the change only if interrupts are enabled (GPINTEN) <7:0>.
1 = Pin caused interrupt.
0 = Interrupt not pending.

1.6.9 INTERRUPT CAPTURE REGISTER

The INTCAP register captures the GPIO port value at the time the interrupt occurred. The register is 'read only' and is updated only when an interrupt occurs. The register will remain unchanged until the interrupt is cleared via a read of INTCAP or GPIO.

REGISTER 1-9: INTCAP – INTERRUPT CAPTURED VALUE FOR PORT REGISTER (ADDR 0x08)

| | | | | | | | |
|-------|------|------|------|------|------|------|-------|
| R-x | R-x | R-x | R-x | R-x | R-x | R-x | R-x |
| ICP7 | ICP6 | ICP5 | ICP4 | ICP3 | ICP2 | ICP1 | ICP0 |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7-0

ICP7:ICP0: These bits reflect the logic level on the port pins at the time of interrupt due to pin change <7:0>

1 = Logic-high.

0 = Logic-low.

MCP23017/MCP23S17

1.6.10 PORT REGISTER

The GPIO register reflects the value on the port. Reading from this register reads the port. Writing to this register modifies the Output Latch (OLAT) register.

REGISTER 1-10: GPIO – GENERAL PURPOSE I/O PORT REGISTER (ADDR 0x09)

| | | | | | | | |
|-------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| GP7 | GP6 | GP5 | GP4 | GP3 | GP2 | GP1 | GP0 |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7-0

GP7:GP0: These bits reflect the logic level on the pins <7:0>

1 = Logic-high.

0 = Logic-low.

1.6.11 OUTPUT LATCH REGISTER (OLAT)

The OLAT register provides access to the output latches. A read from this register results in a read of the OLAT and not the port itself. A write to this register modifies the output latches that modifies the pins configured as outputs.

REGISTER 1-11: OLAT – OUTPUT LATCH REGISTER 0 (ADDR 0x0A)

| | | | | | | | |
|-------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| OL7 | OL6 | OL5 | OL4 | OL3 | OL2 | OL1 | OL0 |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7-0

OL7:OL0: These bits reflect the logic level on the output latch <7:0>

1 = Logic-high.

0 = Logic-low.

MCP23017/MCP23S17

1.7 Interrupt Logic

If enabled, the MCP23X17 activates the INTn interrupt output when one of the port pins changes state or when a pin does not match the preconfigured default. Each pin is individually configurable as follows:

- Enable/disable interrupt via GPINTEN
- Can interrupt on either pin change or change from default as configured in DEFVAL

Both conditions are referred to as Interrupt-on-Change (IOC).

The interrupt control module uses the following registers/bits:

- IOCON.MIRROR – controls if the two interrupt pins mirror each other
- GPINTEN – Interrupt enable register
- INTCON – Controls the source for the IOC
- DEFVAL – Contains the register default for IOC operation

1.7.1 INTA AND INTB

There are two interrupt pins: INTA and INTB. By default, INTA is associated with GPAn pins (PortA) and INTB is associated with GPBn pins (PortB). Each port has an independent signal which is cleared if its associated GPIO or INTCAP register is read.

1.7.1.1 Mirroring the INT pins

Additionally, the INTn pins can be configured to mirror each other so that any interrupt will cause both pins to go active. This is controlled via IOCON.MIRROR.

If IOCON.MIRROR = 0, the internal signals are routed independently to the INTA and INTB pads.

If IOCON.MIRROR = 1, the internal signals are OR'ed together and routed to the INTn pads. In this case, the interrupt will only be cleared if the associated GPIO or INTCAP is read (see [Table 1-7](#)).

TABLE 1-7: INTERRUPT OPERATION (IOCON.MIRROR = 1)

| Interrupt Condition | Read Portn * | Interrupt Result |
|---------------------|----------------------|------------------|
| GPIOA | PortA | Clear |
| | PortB | Unchanged |
| GPIOB | PortA | Unchanged |
| | PortB | Clear |
| GPIOA and GPIOB | PortA | Unchanged |
| | PortB | Unchanged |
| | Both PortA and PortB | Clear |

* Port n = GPIO_n or INTCAP_n

1.7.2 IOC FROM PIN CHANGE

If enabled, the MCP23X17 will generate an interrupt if a mismatch condition exists between the current port value and the previous port value. Only IOC enabled pins will be compared. Refer to [Register 1-3](#) and [Register 1-5](#).

1.7.3 IOC FROM REGISTER DEFAULT

If enabled, the MCP23X17 will generate an interrupt if a mismatch occurs between the DEFVAL register and the port. Only IOC enabled pins will be compared. Refer to [Register 1-3](#), [Register 1-5](#) and [Register 1-4](#).

1.7.4 INTERRUPT OPERATION

The INTn interrupt output can be configured as active-low, active-high or open-drain via the IOCON register.

Only those pins that are configured as an input (IODIR register) with Interrupt-On-Change (IOC) enabled (IOINTEN register) can cause an interrupt. Pins defined as an output have no effect on the interrupt output pin.

Input change activity on a port input pin that is enabled for IOC will generate an internal device interrupt and the device will capture the value of the port and copy it into INTCAP. The interrupt will remain active until the INTCAP or GPIO register is read. Writing to these registers will not affect the interrupt. The interrupt condition will be cleared after the LSB of the data is clocked out during a read command of GPIO or INTCAP.

The first interrupt event will cause the port contents to be copied into the INTCAP register. Subsequent interrupt conditions on the port will not cause an interrupt to occur as long as the interrupt is not cleared by a read of INTCAP or GPIO.

Note: The value in INTCAP can be lost if GPIO is read before INTCAP while another IOC is pending. After reading GPIO, the interrupt will clear and then set due to the pending IOC, causing the INTCAP register to update.

1.7.5 INTERRUPT CONDITIONS

There are two possible configurations that cause interrupts (configured via INTCON):

1. Pins configured for **interrupt-on-pin change** will cause an interrupt to occur if a pin changes to the opposite state. The default state is reset after an interrupt occurs and after clearing the interrupt condition (i.e., after reading GPIO or INTCAP). For example, an interrupt occurs by an input changing from '1' to '0'. The new initial state for the pin is a logic 0 after the interrupt is cleared.
2. Pins configured for **interrupt-on-change from register value** will cause an interrupt to occur if the corresponding input pin differs from the register bit. The interrupt condition will remain as long as the condition exists, regardless if the INTCAP or GPIO is read.

See [Figure 1-6](#) and [Figure 1-7](#) for more information on interrupt operations.

FIGURE 1-6: INTERRUPT-ON-PIN CHANGE

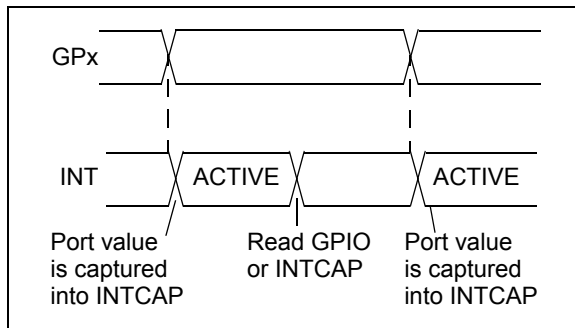
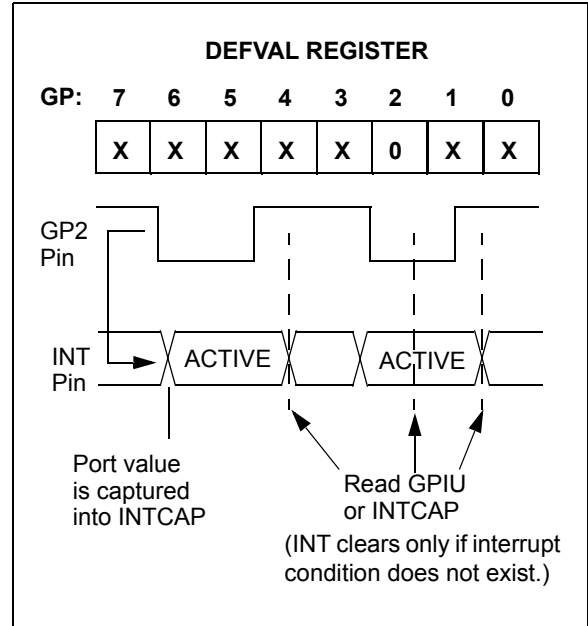


FIGURE 1-7: INTERRUPT-ON-CHANGE FROM REGISTER DEFAULT



MCP23017/MCP23S17

NOTES:

2.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

| | |
|---|-----------------------|
| Ambient temperature under bias | -40°C to +125°C |
| Storage temperature | -65°C to +150°C |
| Voltage on VDD with respect to VSS | -0.3V to +5.5V |
| Voltage on all other pins with respect to VSS (except VDD)..... | -0.6V to (VDD + 0.6V) |
| Total power dissipation (Note) | 700 mW |
| Maximum current out of VSS pin | 150 mA |
| Maximum current into VDD pin | 125 mA |
| Input clamp current, I _{IK} (V _I < 0 or V _I > V _{DD})..... | ±20 mA |
| Output clamp current, I _{OK} (V _O < 0 or V _O > V _{DD}) | ±20 mA |
| Maximum output current sunk by any output pin | 25 mA |
| Maximum output current sourced by any output pin | 25 mA |

Note: Power dissipation is calculated as follows:

$$P_{DIS} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD} - V_{OH}) \times I_{OH}\} + \sum (V_{OL} \times I_{OL})$$

† **NOTE:** The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

MCP23017/MCP23S17

2.1 DC Characteristics

| DC Characteristics | | Operating Conditions (unless otherwise indicated): $1.8V \leq V_{DD} \leq 5.5V$ at $-40^{\circ}C \leq T_A \leq +85^{\circ}C$ (I-Temp) $4.5V \leq V_{DD} \leq 5.5V$ at $-40^{\circ}C \leq T_A \leq +125^{\circ}C$ (E-Temp) (Note 1) | | | | | |
|--|--|--|----------------|--------------|----------|-------|---|
| Param No. | Characteristic | Sym | Min | Typ (Note 1) | Max | Units | Conditions |
| D001 | Supply Voltage | VDD | 1.8 | — | 5.5 | V | |
| D002 | VDD Start Voltage to Ensure Power-on Reset | VPOR | — | VSS | — | V | |
| D003 | VDD Rise Rate to Ensure Power-on Reset | SVDD | 0.05 | — | — | V/ms | Design guidance only. Not tested. |
| D004 | Supply Current | IDD | — | — | 1 | mA | SCL/SCK = 1 MHz |
| D005 | Standby current | IDDS | — | — | 1 | μA | |
| | | | — | — | 3 | μA | 4.5V-5.5V @ +125°C (Note 1) |
| Input Low Voltage | | | | | | | |
| D030 | A0, A1 (TTL buffer) | VIL | VSS | — | 0.15 VDD | V | |
| D031 | \overline{CS} , GPIO, SCL/SCK, SDA, A2, \overline{RESET} (Schmitt Trigger) | | VSS | — | 0.2 VDD | V | |
| Input High Voltage | | | | | | | |
| D040 | A0, A1 (TTL buffer) | VIH | 0.25 VDD + 0.8 | — | VDD | V | |
| D041 | \overline{CS} , GPIO, SCL/SCK, SDA, A2, \overline{RESET} (Schmitt Trigger) | | 0.8 VDD | — | VDD | V | For entire VDD range |
| Input Leakage Current | | | | | | | |
| D060 | I/O port pins | IIL | — | — | ±1 | μA | VSS ≤ VPIN ≤ VDD |
| Output Leakage Current | | | | | | | |
| D065 | I/O port pins | ILO | — | — | ±1 | μA | VSS ≤ VPIN ≤ VDD |
| D070 | GPIO weak pull-up current | IPU | 40 | 75 | 115 | μA | VDD = 5V, GP Pins = VSS -40°C ≤ TA ≤ +85°C |
| Output Low-Voltage | | | | | | | |
| D080 | GPIO | VOL | — | — | 0.6 | V | IOL = 8.0 mA, VDD = 4.5V |
| | INT | | — | — | 0.6 | V | IOL = 1.6 mA, VDD = 4.5V |
| | SO, SDA | | — | — | 0.6 | V | IOL = 3.0 mA, VDD = 1.8V |
| | SDA | | — | — | 0.8 | V | IOL = 3.0 mA, VDD = 4.5V |
| Output High-Voltage | | | | | | | |
| D090 | GPIO, INT, SO | VOH | VDD - 0.7 | — | — | V | I _{OH} = -3.0 mA, VDD = 4.5V |
| | | | VDD - 0.7 | — | — | | I _{OH} = -400 μA, VDD = 1.8V |
| Capacitive Loading Specs on Output Pins | | | | | | | |
| D101 | GPIO, SO, INT | CIO | — | — | 50 | pF | |
| D102 | SDA | CB | — | — | 400 | pF | |

Note 1: This parameter is characterized, not 100% tested.

MCP23017/MCP23S17

FIGURE 2-1: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS

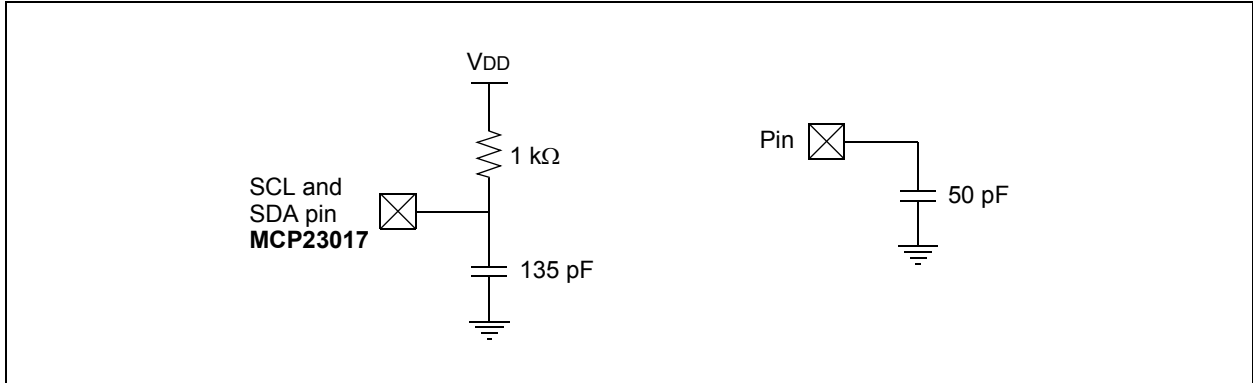
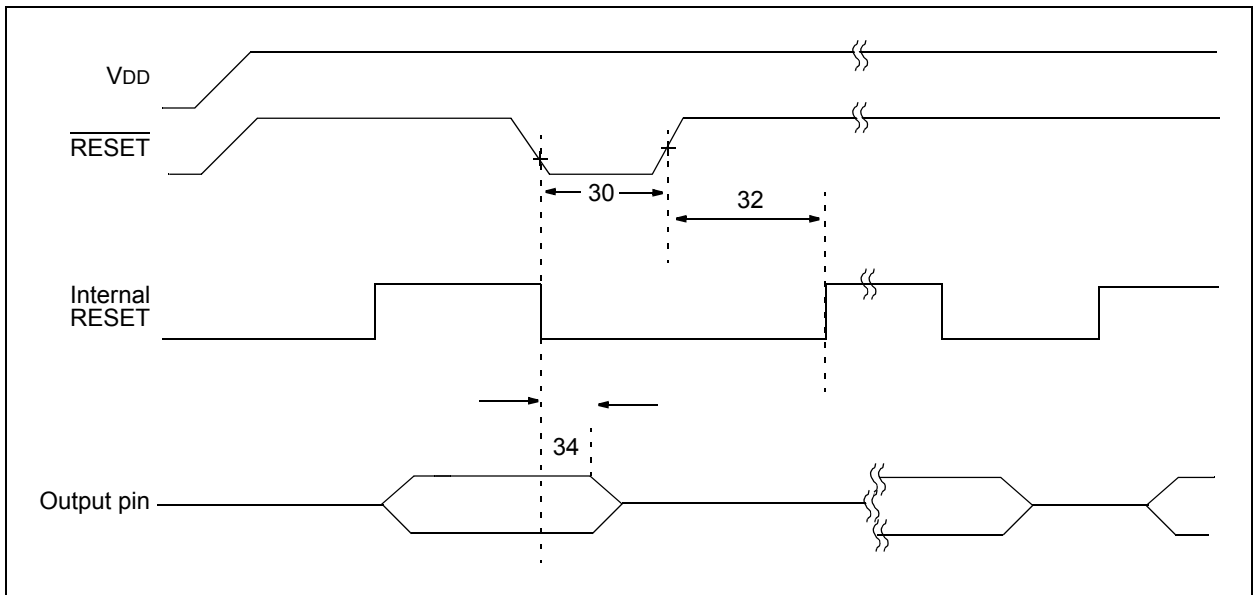


FIGURE 2-2: RESET AND DEVICE RESET TIMER TIMING



MCP23017/MCP23S17

TABLE 2-1: DEVICE RESET SPECIFICATIONS

| AC Characteristics | | Operating Conditions (unless otherwise indicated): 1.8V ≤ VDD ≤ 5.5V at -40°C ≤ TA ≤ +85°C (I-Temp) 4.5V ≤ VDD ≤ 5.5V at -40°C ≤ TA ≤ +125°C (E-Temp) (Note 1) | | | | | |
|--------------------|--------------------------------------|--|-----|--------------------|-----|-------|------------|
| Param No. | Characteristic | Sym | Min | Typ ⁽¹⁾ | Max | Units | Conditions |
| 30 | RESET Pulse Width (Low) | TRSTL | 1 | — | — | μs | |
| 32 | Device Active After Reset high | THLD | — | 0 | — | ns | VDD = 5.0V |
| 34 | Output High-Impedance From RESET Low | TIOZ | — | — | 1 | μs | |

Note 1: This parameter is characterized, not 100% tested.

FIGURE 2-3: I²C™ BUS START/STOP BITS TIMING

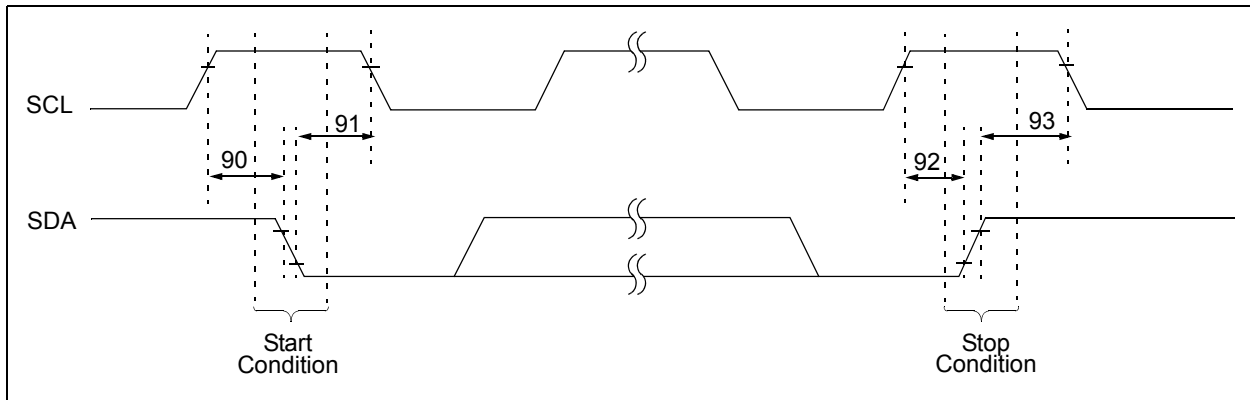
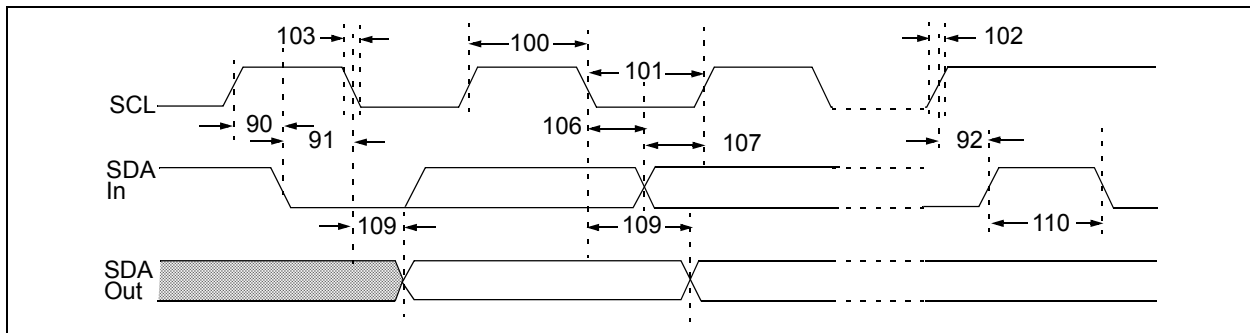


FIGURE 2-4: I²C™ BUS DATA TIMING



MCP23017/MCP23S17

TABLE 2-2: I²C™ BUS DATA REQUIREMENTS

| I ² C™ AC Characteristics | | Operating Conditions (unless otherwise indicated): 1.8V ≤ VDD ≤ 5.5V at -40°C ≤ TA ≤ +85°C (I-Temp) 4.5V ≤ VDD ≤ 5.5V at -40°C ≤ TA ≤ +125°C (E-Temp) (Note 1) RPU (SCL, SDA) = 1 kΩ, CL (SCL, SDA) = 135 pF | | | | | |
|--------------------------------------|-----------------------------|---|----------------------------|-----|------|-------|--------------------|
| Param No. | Characteristic | Sym | Min | Typ | Max | Units | Conditions |
| 100 | Clock High Time: | THIGH | | | | | |
| | 100 kHz mode | | 4.0 | — | — | μs | 1.8V–5.5V (I-Temp) |
| | 400 kHz mode | | 0.6 | — | — | μs | 2.7V–5.5V (I-Temp) |
| | 1.7 MHz mode | | 0.12 | — | — | μs | 4.5V–5.5V (E-Temp) |
| 101 | Clock Low Time: | TLOW | | | | | |
| | 100 kHz mode | | 4.7 | — | — | μs | 1.8V–5.5V (I-Temp) |
| | 400 kHz mode | | 1.3 | — | — | μs | 2.7V–5.5V (I-Temp) |
| | 1.7 MHz mode | | 0.32 | — | — | μs | 4.5V–5.5V (E-Temp) |
| 102 | SDA and SCL Rise Time: | TR (Note 1) | | | | | |
| | 100 kHz mode | | — | — | 1000 | ns | 1.8V–5.5V (I-Temp) |
| | 400 kHz mode | | 20 + 0.1 CB ⁽²⁾ | — | 300 | ns | 2.7V–5.5V (I-Temp) |
| | 1.7 MHz mode | | 20 | — | 160 | ns | 4.5V–5.5V (E-Temp) |
| 103 | SDA and SCL Fall Time: | TF (Note 1) | | | | | |
| | 100 kHz mode | | — | — | 300 | ns | 1.8V–5.5V (I-Temp) |
| | 400 kHz mode | | 20 + 0.1 CB ⁽²⁾ | — | 300 | ns | 2.7V–5.5V (I-Temp) |
| | 1.7 MHz mode | | 20 | — | 80 | ns | 4.5V–5.5V (E-Temp) |
| 90 | START Condition Setup Time: | TSU:STA | | | | | |
| | 100 kHz mode | | 4.7 | — | — | μs | 1.8V–5.5V (I-Temp) |
| | 400 kHz mode | | 0.6 | — | — | μs | 2.7V–5.5V (I-Temp) |
| | 1.7 MHz mode | | 0.16 | — | — | μs | 4.5V–5.5V (E-Temp) |
| 91 | START Condition Hold Time: | THD:STA | | | | | |
| | 100 kHz mode | | 4.0 | — | — | μs | 1.8V–5.5V (I-Temp) |
| | 400 kHz mode | | 0.6 | — | — | μs | 2.7V–5.5V (I-Temp) |
| | 1.7 MHz mode | | 0.16 | — | — | μs | 4.5V–5.5V (E-Temp) |
| 106 | Data Input Hold Time: | THD:DAT | | | | | |
| | 100 kHz mode | | 0 | — | 3.45 | μs | 1.8V–5.5V (I-Temp) |
| | 400 kHz mode | | 0 | — | 0.9 | μs | 2.7V–5.5V (I-Temp) |
| | 1.7 MHz mode | | 0 | — | 0.15 | μs | 4.5V–5.5V (E-Temp) |
| 107 | Data Input Setup Time: | TSU:DAT | | | | | |
| | 100 kHz mode | | 250 | — | — | ns | 1.8V–5.5V (I-Temp) |
| | 400 kHz mode | | 100 | — | — | ns | 2.7V–5.5V (I-Temp) |
| | 1.7 MHz mode | | 0.01 | — | — | μs | 4.5V–5.5V (E-Temp) |
| 92 | Stop Condition Setup Time: | TSU:STO | | | | | |
| | 100 kHz mode | | 4.0 | — | — | μs | 1.8V–5.5V (I-Temp) |
| | 400 kHz mode | | 0.6 | — | — | μs | 2.7V–5.5V (I-Temp) |
| | 1.7 MHz mode | | 0.16 | — | — | μs | 4.5V–5.5V (E-Temp) |

Note 1: This parameter is characterized, not 100% tested.

Note 2: CB is specified to be from 10 to 400 pF.

MCP23017/MCP23S17

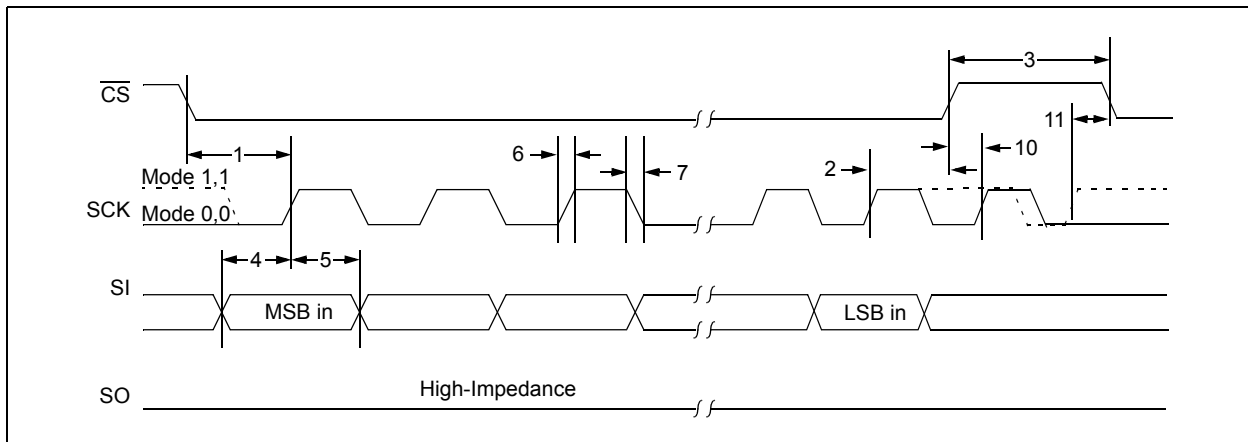
TABLE 2-2: I²C™ BUS DATA REQUIREMENTS (CONTINUED)

| I ² C™ AC Characteristics | | Operating Conditions (unless otherwise indicated): 1.8V ≤ VDD ≤ 5.5V at -40°C ≤ TA ≤ +85°C (I-Temp) 4.5V ≤ VDD ≤ 5.5V at -40°C ≤ TA ≤ +125°C (E-Temp) (Note 1) RPU (SCL, SDA) = 1 kΩ, CL (SCL, SDA) = 135 pF | | | | | | |
|--------------------------------------|--|---|-----|------|------|----------------------|-----------------------|--|
| Param No. | Characteristic | Sym | Min | Typ | Max | Units | Conditions | |
| 109 | Output Valid From Clock: | TAA | | | | | | |
| | 100 kHz mode | | — | — | 3.45 | μs | 1.8V–5.5V (I-Temp) | |
| | 400 kHz mode | | — | — | 0.9 | μs | 2.7V–5.5V (I-Temp) | |
| | 1.7 MHz mode | — | — | 0.18 | μs | 4.5V–5.5V (E-Temp) | | |
| 110 | Bus Free Time: | TBUF | | | | | | |
| | 100 kHz mode | | 4.7 | — | — | μs | 1.8V–5.5V (I-Temp) | |
| | 400 kHz mode | | 1.3 | — | — | μs | 2.7V–5.5V (I-Temp) | |
| | 1.7 MHz mode | N/A | — | N/A | μs | 4.5V – 5.5V (E-Temp) | | |
| | Bus Capacitive Loading: | CB | | | | | | |
| | 100 kHz and 400 kHz | | — | — | 400 | pF | Note 1 | |
| | 1.7 MHz | — | — | 100 | pF | Note 1 | | |
| | Input Filter Spike Suppression (SDA and SCL) | TSP | | | | | | |
| | 100 kHz and 400 kHz | | — | — | 50 | ns | | |
| | 1.7 MHz | | — | — | 10 | ns | Spike suppression off | |

Note 1: This parameter is characterized, not 100% tested.

Note 2: CB is specified to be from 10 to 400 pF.

FIGURE 2-5: SPI INPUT TIMING



MCP23017/MCP23S17

FIGURE 2-6: SPI OUTPUT TIMING

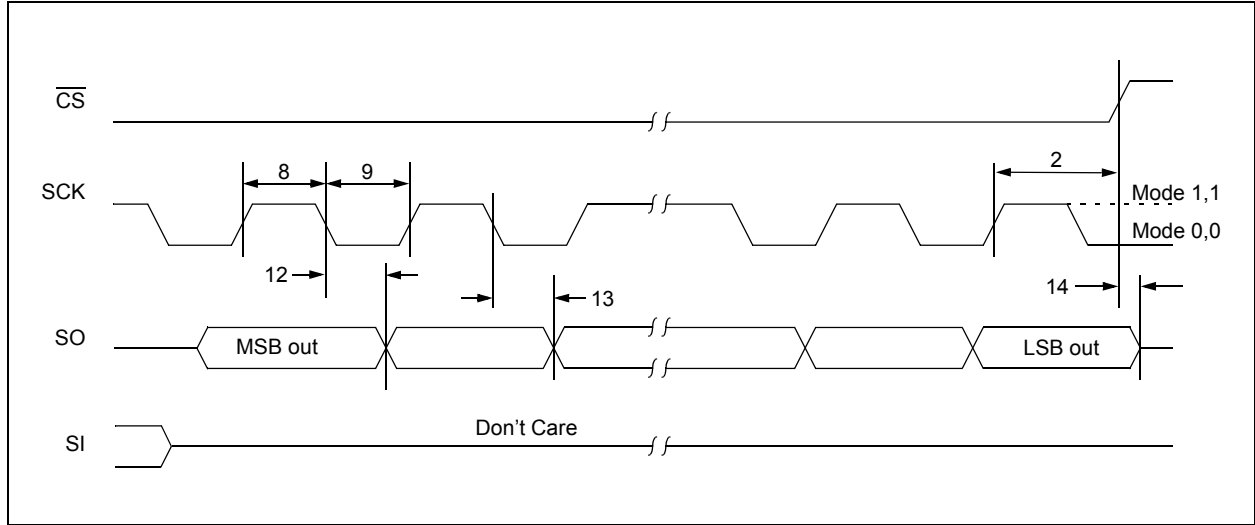


TABLE 2-3: SPI INTERFACE AC CHARACTERISTICS

| SPI Interface AC Characteristics | | Operating Conditions (unless otherwise indicated): 1.8V ≤ VDD ≤ 5.5V at -40°C ≤ TA ≤ +85°C (I-Temp) 4.5V ≤ VDD ≤ 5.5V at -40°C ≤ TA ≤ +125°C (E-Temp) (Note 1) | | | | | |
|----------------------------------|-----------------|--|-----|-----|-----|-------|--------------------|
| Param No. | Characteristic | Sym | Min | Typ | Max | Units | Conditions |
| | Clock Frequency | FCLK | — | — | 5 | MHz | 1.8V–5.5V (I-Temp) |
| | | | — | — | 10 | MHz | 2.7V–5.5V (I-Temp) |
| | | | — | — | 10 | MHz | 4.5V–5.5V (E-Temp) |
| 1 | CS Setup Time | T _{CSS} | 50 | — | — | ns | |
| 2 | CS Hold Time | T _{CSH} | 100 | — | — | ns | 1.8V–5.5V (I-Temp) |
| | | | 50 | — | — | ns | 2.7V–5.5V (I-Temp) |
| | | | 50 | — | — | ns | 4.5V–5.5V (E-Temp) |
| 3 | CS Disable Time | T _{CSD} | 100 | — | — | ns | 1.8V–5.5V (I-Temp) |
| | | | 50 | — | — | ns | 2.7V–5.5V (I-Temp) |
| | | | 50 | — | — | ns | 4.5V–5.5V (E-Temp) |
| 4 | Data Setup Time | T _{SU} | 20 | — | — | ns | 1.8V–5.5V (I-Temp) |
| | | | 10 | — | — | ns | 2.7V–5.5V (I-Temp) |
| | | | 10 | — | — | ns | 4.5V–5.5V (E-Temp) |
| 5 | Data Hold Time | T _{HD} | 20 | — | — | ns | 1.8V–5.5V (I-Temp) |
| | | | 10 | — | — | ns | 2.7V–5.5V (I-Temp) |
| | | | 10 | — | — | ns | 4.5V–5.5V (E-Temp) |
| 6 | CLK Rise Time | T _R | — | — | 2 | μs | Note 1 |
| 7 | CLK Fall Time | T _F | — | — | 2 | μs | Note 1 |
| 8 | Clock High Time | T _{HI} | 90 | — | — | ns | 1.8V–5.5V (I-Temp) |
| | | | 45 | — | — | ns | 2.7V–5.5V (I-Temp) |
| | | | 45 | — | — | ns | 4.5V–5.5V (E-Temp) |

Note 1: This parameter is characterized, not 100% tested.

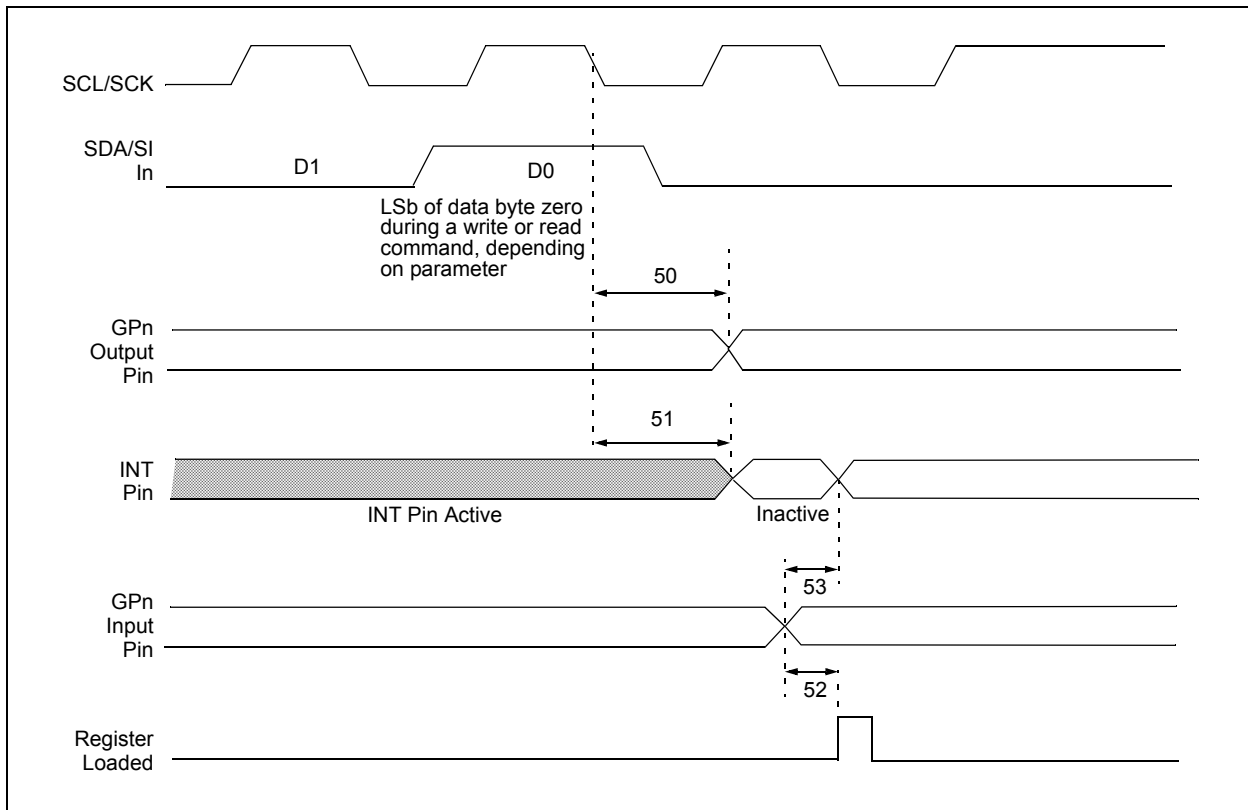
MCP23017/MCP23S17

TABLE 2-3: SPI INTERFACE AC CHARACTERISTICS (CONTINUED)

| SPI Interface AC Characteristics | | Operating Conditions (unless otherwise indicated): 1.8V ≤ VDD ≤ 5.5V at -40°C ≤ TA ≤ +85°C (I-Temp) 4.5V ≤ VDD ≤ 5.5V at -40°C ≤ TA ≤ +125°C (E-Temp) (Note 1) | | | | | |
|----------------------------------|-----------------------------|--|-----|-----|-----|-------|--------------------|
| Param No. | Characteristic | Sym | Min | Typ | Max | Units | Conditions |
| 9 | Clock Low Time | TLO | 90 | — | — | ns | 1.8V–5.5V (I-Temp) |
| | | | 45 | — | — | ns | 2.7V–5.5V (I-Temp) |
| | | | 45 | — | — | ns | 4.5V–5.5V (E-Temp) |
| 10 | Clock Delay Time | TCLD | 50 | — | — | ns | |
| 11 | Clock Enable Time | TCLE | 50 | — | — | ns | |
| 12 | Output Valid from Clock Low | TV | — | — | 90 | ns | 1.8V–5.5V (I-Temp) |
| | | | — | — | 45 | ns | 2.7V–5.5V (I-Temp) |
| | | | — | — | 45 | ns | 4.5V–5.5V (E-Temp) |
| 13 | Output Hold Time | THO | 0 | — | — | ns | |
| 14 | Output Disable Time | TDIS | — | — | 100 | ns | |

Note 1: This parameter is characterized, not 100% tested.

FIGURE 2-7: GPIO AND INT TIMING



MCP23017/MCP23S17

TABLE 2-4: GP AND INT PINS

| AC Characteristics | | Operating Conditions (unless otherwise indicated): 1.8V ≤ VDD ≤ 5.5V at -40°C ≤ TA ≤ +85°C (I-Temp) 4.5V ≤ VDD ≤ 5.5V at -40°C ≤ TA ≤ +125°C (E-Temp) (Note 1) | | | | | |
|--------------------|-----------------------------------|--|-----|-----|-----|-------|---------------|
| Param No. | Characteristic | Sym | Min | Typ | Max | Units | Conditions |
| 50 | Serial Data to Output Valid | TGPOV | — | — | 500 | ns | |
| 51 | Interrupt Pin Disable Time | TINTD | — | — | 600 | ns | |
| 52 | GP Input Change to Register Valid | TGPIV | — | — | 450 | ns | |
| 53 | IOC Event to INT Active | TGPINT | — | — | 600 | ns | |
| | Glitch Filter on GP Pins | TGLITCH | — | — | 150 | ns | Note 1 |

Note 1: This parameter is characterized, not 100% tested

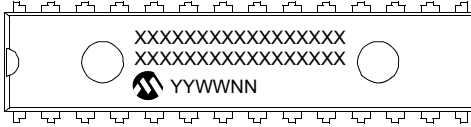
MCP23017/MCP23S17

NOTES:

3.0 PACKAGING INFORMATION

3.1 Package Marking Information

28-Lead PDIP (Skinny DIP)



Example:



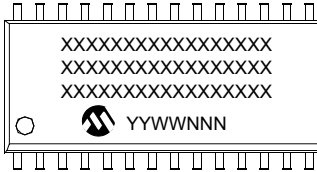
28-Lead QFN



Example:



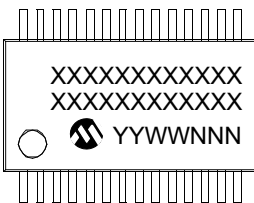
28-Lead SOIC



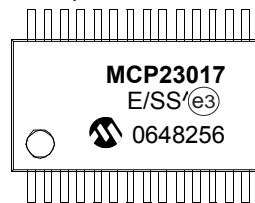
Example:



28-Lead SSOP



Example:



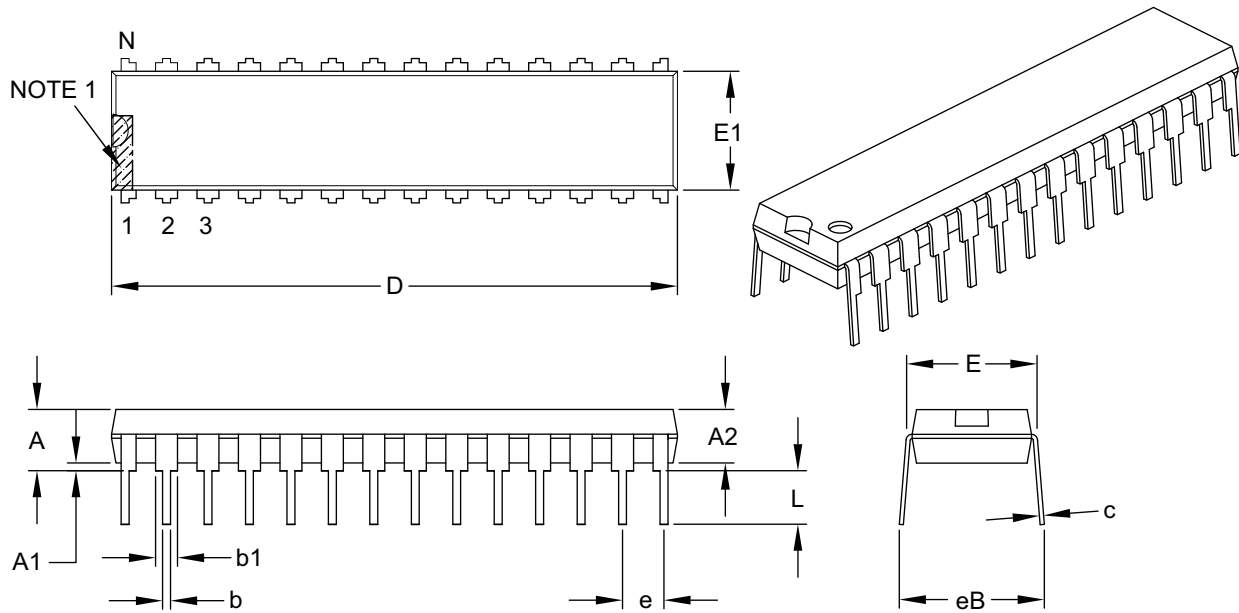
| | | |
|----------------|--------|--|
| Legend: | XX...X | Customer-specific information |
| | Y | Year code (last digit of calendar year) |
| | YY | Year code (last 2 digits of calendar year) |
| | WW | Week code (week of January 1 is week '01') |
| | NNN | Alphanumeric traceability code |
| | (e3) | Pb-free JEDEC designator for Matte Tin (Sn) |
| | * | This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package. |

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

MCP23017/MCP23S17

28-Lead Skinny Plastic Dual In-Line (SP) – 300 mil Body [SPDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



| Dimension Limits | Units | INCHES | | |
|----------------------------|-------|----------|-------|-------|
| | | MIN | NOM | MAX |
| Number of Pins | N | 28 | | |
| Pitch | e | .100 BSC | | |
| Top to Seating Plane | A | – | – | .200 |
| Molded Package Thickness | A2 | .120 | .135 | .150 |
| Base to Seating Plane | A1 | .015 | – | – |
| Shoulder to Shoulder Width | E | .290 | .310 | .335 |
| Molded Package Width | E1 | .240 | .285 | .295 |
| Overall Length | D | 1.345 | 1.365 | 1.400 |
| Tip to Seating Plane | L | .110 | .130 | .150 |
| Lead Thickness | c | .008 | .010 | .015 |
| Upper Lead Width | b1 | .040 | .050 | .070 |
| Lower Lead Width | b | .014 | .018 | .022 |
| Overall Row Spacing § | eB | – | – | .430 |

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- § Significant Characteristic.
- Dimensions D and $E1$ do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
- Dimensioning and tolerancing per ASME Y14.5M.

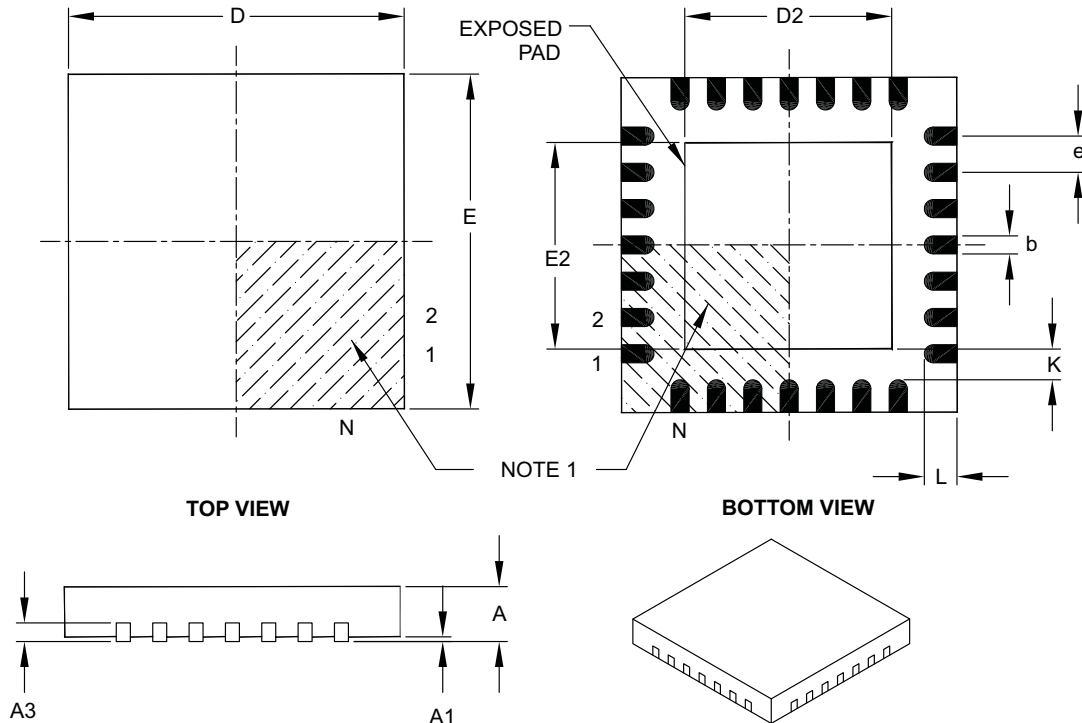
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-070B

MCP23017/MCP23S17

28-Lead Plastic Quad Flat, No Lead Package (ML) – 6x6 mm Body [QFN] with 0.55 mm Contact Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



| Dimension Limits | Units | MILLIMETERS | | |
|------------------------|-------|-------------|------|------|
| | | MIN | NOM | MAX |
| Number of Pins | N | 28 | | |
| Pitch | e | 0.65 BSC | | |
| Overall Height | A | 0.80 | 0.90 | 1.00 |
| Standoff | A1 | 0.00 | 0.02 | 0.05 |
| Contact Thickness | A3 | 0.20 REF | | |
| Overall Width | E | 6.00 BSC | | |
| Exposed Pad Width | E2 | 3.65 | 3.70 | 4.20 |
| Overall Length | D | 6.00 BSC | | |
| Exposed Pad Length | D2 | 3.65 | 3.70 | 4.20 |
| Contact Width | b | 0.23 | 0.30 | 0.35 |
| Contact Length | L | 0.50 | 0.55 | 0.70 |
| Contact-to-Exposed Pad | K | 0.20 | – | – |

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Package is saw singulated.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

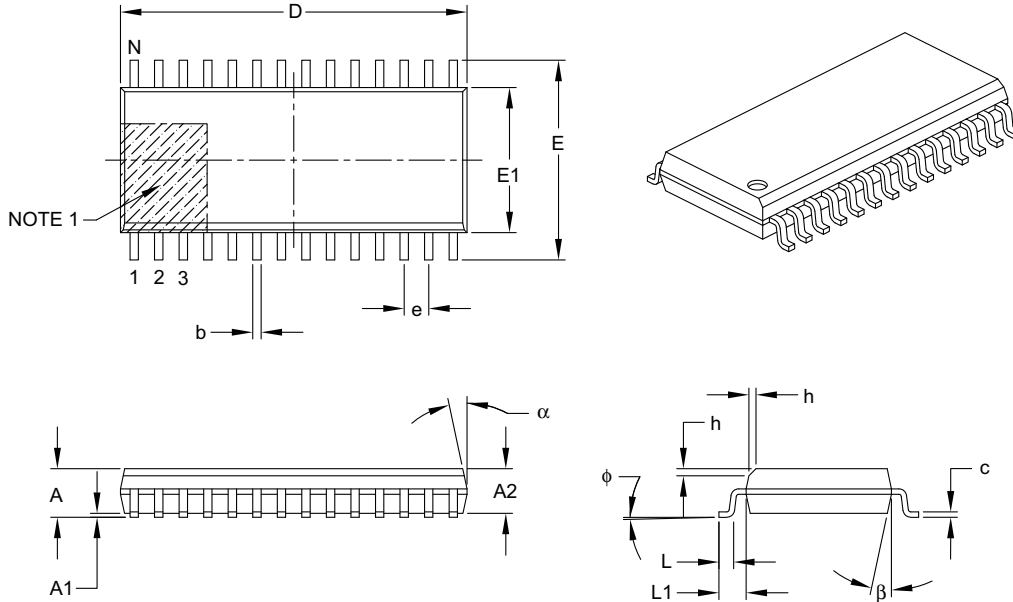
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-105B

MCP23017/MCP23S17

28-Lead Plastic Small Outline (SO) – Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



| Dimension Limits | Units | MILLMETERS | | |
|--------------------------|----------|------------|-----|------|
| | | MIN | NOM | MAX |
| Number of Pins | N | 28 | | |
| Pitch | e | 1.27 BSC | | |
| Overall Height | A | – | – | 2.65 |
| Molded Package Thickness | A2 | 2.05 | – | – |
| Standoff § | A1 | 0.10 | – | 0.30 |
| Overall Width | E | 10.30 BSC | | |
| Molded Package Width | E1 | 7.50 BSC | | |
| Overall Length | D | 17.90 BSC | | |
| Chamfer (optional) | h | 0.25 | – | 0.75 |
| Foot Length | L | 0.40 | – | 1.27 |
| Footprint | L1 | 1.40 REF | | |
| Foot Angle Top | ϕ | 0° | – | 8° |
| Lead Thickness | c | 0.18 | – | 0.33 |
| Lead Width | b | 0.31 | – | 0.51 |
| Mold Draft Angle Top | α | 5° | – | 15° |
| Mold Draft Angle Bottom | β | 5° | – | 15° |

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- § Significant Characteristic.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

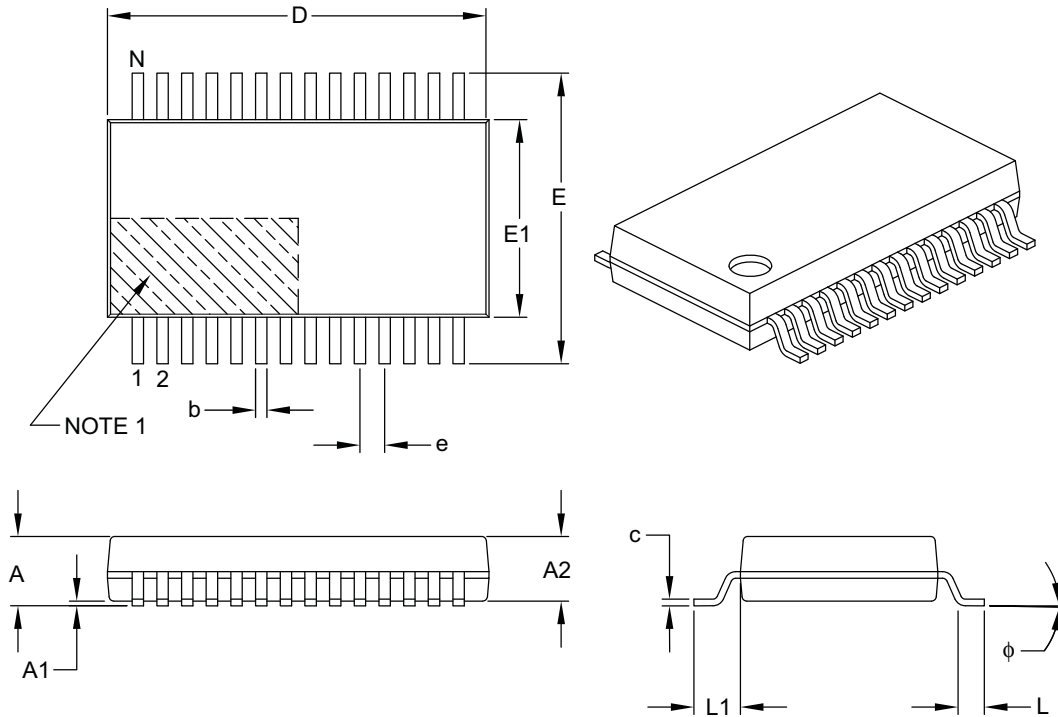
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-052B

MCP23017/MCP23S17

28-Lead Plastic Shrink Small Outline (SS) – 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



| Dimension Limits | Units | MILLIMETERS | | |
|--------------------------|-------|-------------|-------|-------|
| | | MIN | NOM | MAX |
| Number of Pins | N | 28 | | |
| Pitch | e | 0.65 BSC | | |
| Overall Height | A | – | – | 2.00 |
| Molded Package Thickness | A2 | 1.65 | 1.75 | 1.85 |
| Standoff | A1 | 0.05 | – | – |
| Overall Width | E | 7.40 | 7.80 | 8.20 |
| Molded Package Width | E1 | 5.00 | 5.30 | 5.60 |
| Overall Length | D | 9.90 | 10.20 | 10.50 |
| Foot Length | L | 0.55 | 0.75 | 0.95 |
| Footprint | L1 | 1.25 REF | | |
| Lead Thickness | c | 0.09 | – | 0.25 |
| Foot Angle | φ | 0° | 4° | 8° |
| Lead Width | b | 0.22 | – | 0.38 |

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.20 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-073B

MCP23017/MCP23S17

NOTES:

APPENDIX A: REVISION HISTORY

Revision B (February 2007)

1. Changed Byte and Sequential Read in [Figure 1-1](#) from “R” to “W”.
2. Table 2-4, Param No. 51 and 53: Changed from 450 to 600 and 500 to 600, respectively.
3. Added disclaimers to package outline drawings.
4. Updated package outline drawings.

Revision A (June 2005)

- Original Release of this Document.

MCP23017/MCP23S17

NOTES:

MCP23017/MCP23S17

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

| <u>PART NO.</u> | - | <u>X</u> | <u>/XX</u> | |
|-------------------|----|-------------------|--|--|
| Device | | Temperature Range | Package | |
| Device | | MCP23017: | 16-Bit I/O Expander w/I ² C™ Interface | |
| | | MCP23017T: | 16-Bit I/O Expander w/I ² C Interface (Tape and Reel) | |
| | | MCP23S17: | 16-Bit I/O Expander w/SPI Interface | |
| | | MCP23S17T: | 16-Bit I/O Expander w/SPI Interface (Tape and Reel) | |
| Temperature Range | E | = | -40°C to +125°C (Extended) | |
| Package | ML | = | Plastic Quad, Flat No Leads (QFN), 28-lead | |
| | SP | = | Plastic DIP (300 mil Body), 28-Lead | |
| | SO | = | Plastic SOIC (300 mil Body), 28-Lead | |
| | SS | = | SSOP, (209 mil Body, 5.30 mm), 28-Lead | |

| Examples: | |
|------------------|---|
| a) | MCP23017-E/SP: Extended Temp., 28LD PDIP package. |
| b) | MCP23017-E/SO: Extended Temp., 28LD SOIC package. |
| c) | MCP23017T-E/SO: Tape and Reel, Extended Temp., 28LD SOIC package. |
| d) | MCP23017-E/SS: Extended Temp., 28LD SSOP package. |
| e) | MCP23017T-E/SS: Tape and Reel, Extended Temp., 28LD SSOP package. |
| a) | MCP23S17-E/SP: Extended Temp., 28LD PDIP package. |
| b) | MCP23S17-E/SO: Extended Temp., 28LD SOIC package. |
| c) | MCP23S17T-E/SO: Tape and Reel, Extended Temp., 28LD SOIC package. |
| d) | MCP23S17-E/SS: Extended Temp., 28LD SSOP package. |
| e) | MCP23S17T-E/SS: Tape and Reel, Extended Temp., 28LD SSOP package. |

MCP23017/MCP23S17

NOTES:

Note the following details of the code protection feature on Microchip devices:

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- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
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