# PCF8531

**34 x 128 pixel matrix driver**

Rev. 6 — 16 May 2011

**Product data sheet**

## 1. General description

The PCF8531 is a low-power CMOS[1] LCD row and column driver, designed to drive dot matrix graphic displays at multiplex rates of 1:17, 1:26, and 1:34. Furthermore, it can drive up to 128 icons. All necessary functions for the display are provided in a single chip, including on-chip generation of $V_{LCD}$ and the LCD bias voltages, resulting in a minimum of external components and low power consumption. The PCF8531 is compatible with most microcontrollers and communicates via a two-line bidirectional $I^2C$-bus. All inputs are CMOS compatible.

**Remark:** The icon mode is used to reduce current consumption. When only icons are displayed, a much lower operating voltage ($V_{LCD}$) can be used and the switching frequency of the LCD outputs is reduced. In most applications it is possible to use $V_{DD}$ as $V_{LCD}$.

## 2. Features and benefits

- Single-chip LCD controller and driver
- 34 row and 128 column outputs
- Display data RAM $34 \times 128$ bits
- 128 icons (last row is used for icons)
- Fast-mode $I^2C$-bus interface (400 kbit/s)
- Software selectable multiplex rates: 1:17, 1:26, and 1:34
- Icon mode with multiplex rate 1:2:
    - ◆ Featuring reduced current consumption while displaying icons only
- On-chip:
    - ◆ Generation of $V_{LCD}$ (external supply also possible)
    - ◆ Selectable linear temperature compensation
    - ◆ Oscillator requires no external components (external clock also possible)
    - ◆ Generation of intermediate LCD bias voltages
    - ◆ Power-On Reset (POR)
- No external components required
- Software selectable bias configuration
- Logic supply voltage range $V_{DD1}$ to $V_{SS1}$: 1.8 V to 5.5 V
- Supply voltage range for on-chip voltage generator $V_{DD2}$ and $V_{DD3}$ to $V_{SS1}$ and $V_{SS2}$: 2.5 V to 4.5 V
- Display supply voltage range $V_{LCD}$ to $V_{SS}$:
    - ◆ Normal mode: 4 V to 9 V

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1. The definition of the abbreviations and acronyms used in this data sheet can be found in .

◆ Icon mode: 3 V to 9 V
■ Low-power consumption, suitable for battery operated systems
■ CMOS compatible inputs
■ Manufactured in silicon gate CMOS process

# 3. Applications

■ Telecommunication systems
■ Automotive information systems
■ Point-of-sale terminals
■ Instrumentation

# 4. Ordering information

**Table 1.    Ordering information**

| Type number | Package | | |
| --- | --- | --- | --- |
| | **Name** | **Description** | **Version** |
| PCF8531U/2DA/1 | - | chip with bumps in tray | - |

## 5. Block diagram



**Fig 1.    Block diagram of PCF8531**

PCF8531

Product data sheet

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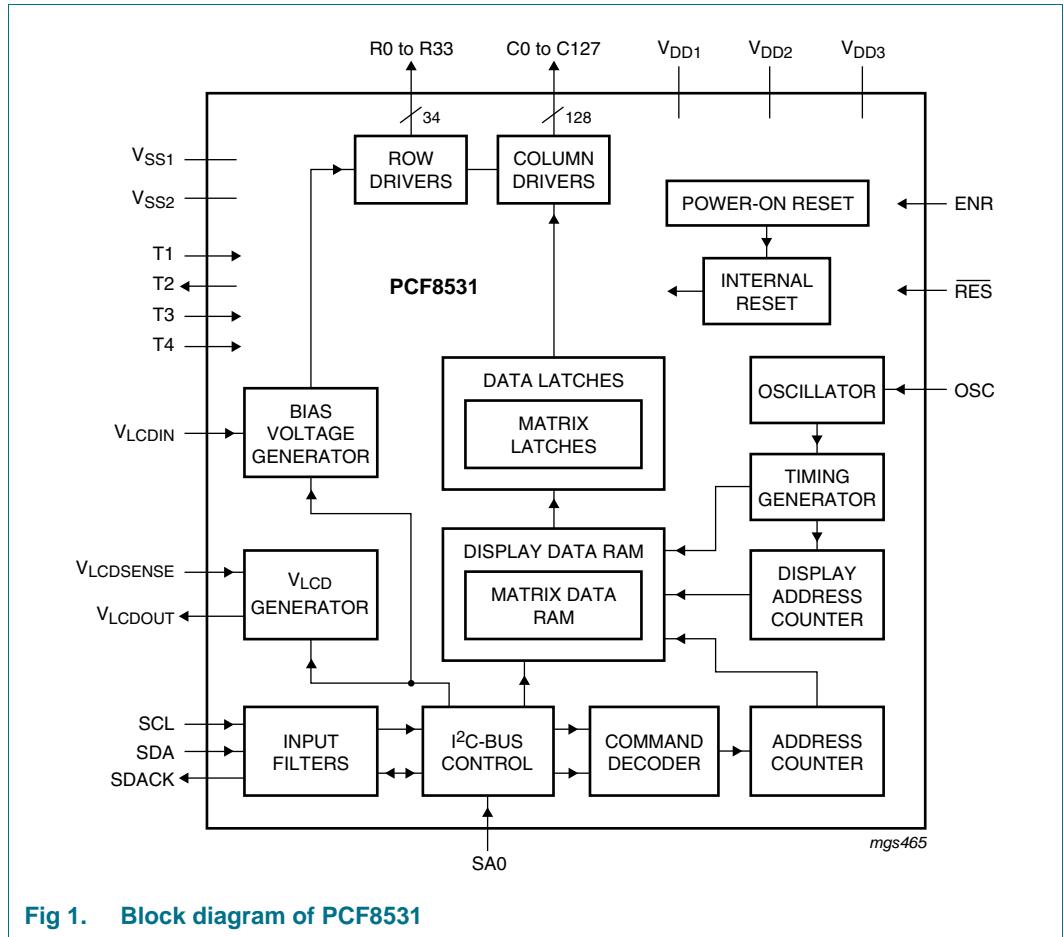
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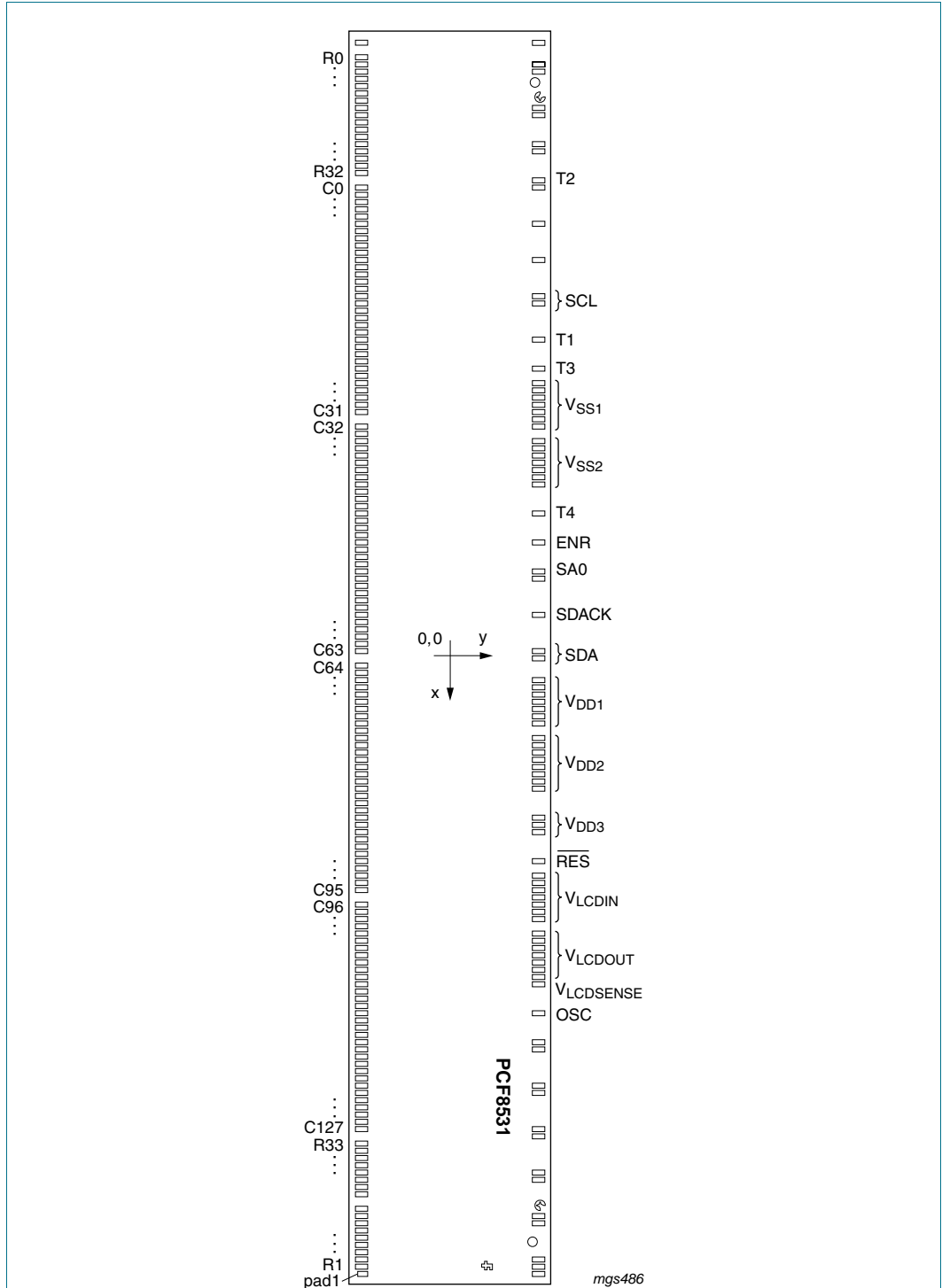
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# 6. Pinning information

## 6.1 Pinning



Viewed from active side. The positioning of the bonding pads is not to scale.

**Fig 2.    Bonding pad location for PCF8531**

**Table 2.** **Pad allocation table**

| Pad | Symbol | Pad | Symbol |
|---|---|---|---|
| 15 | OSC | 55 | ENR |
| 16 | $V_{LCDSENSE}$ | 56 | T4 |
| 17 to 23 | $V_{LCDOUT}$ | 57 to 63 | $V_{SS2}$ |
| 24 to 30 | $V_{LCDIN}$ | 64 to 70 | $V_{SS1}$ |
| 31 | $\overline{RES}$ | 71 | T3 |
| 32 to 34 | $V_{DD3}$ | 72 | T1 |
| 35 to 42 | $V_{DD2}$ | 73 to 74 | SCL |
| 43 to 49 | $V_{DD1}$ | 78 | T2 |
| 50 to 51 | SDA | 87 to 103 | R0, R2, R4, R6, R8, R10, R12, R14, R16, R18, R20, R22, R24, R26, R28, R30, R32 |
| 52 | SDACK | 104 to 231 | C0 to C127 |
| 54 | SA0 | 232 to 248 | R33, R31, R29, R27, R25, R23, R21, R19, R17, R15, R13, R11, R9, R7, R5, R3, R1 |



**Fig 3.** **Alignment markers**
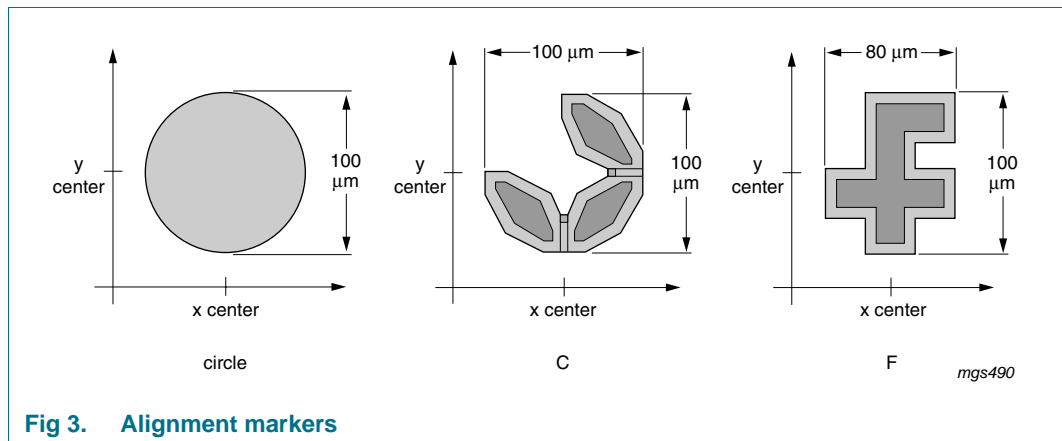
**Table 3.** **Alignment markers for PCF8531**

*All x/y coordinates represent the position of the center of each pad with respect to the center (x/y = 0) of the chip (see Figure 2).*

| Alignment marks | x ($\mu$m) | y ($\mu$m) |
|---|---|---|
| C1 | −5402.0 | 823.1 |
| C2 | 5292.4 | 950.0 |
| F | 5890.3 | 401.9 |
| circle 1 | −5543.0 | 798.4 |
| circle 2 | 5637.4 | 798.4 |
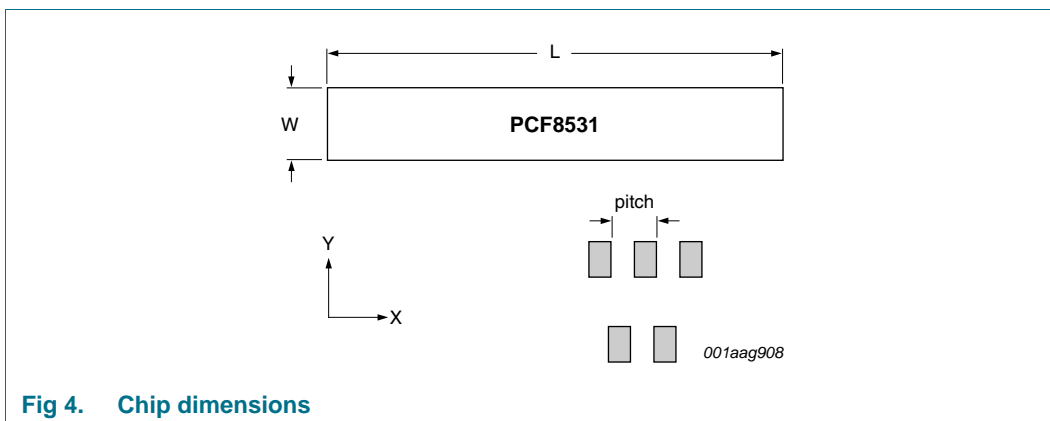
**Fig 4.** **Chip dimensions**

**Table 4.** **Bonding pad dimensions**

| Pad | Size | Unit |
|---|---|---|
| pad pitch (minimum) | 70 | $\mu$m |
| bump dimensions | $50 \times 90 \times 17.5$ ($\pm3$) | $\mu$m |
| wafer thickness (excluding bumps) | 381 | $\mu$m |
| die size L $\times$ W | $12.14 \times 1.86$[1] | mm |

[1] Die size including saw lane of 70 $\mu$m.

## 6.2 Pin description

**Table 5.** **Bonding pad description**

*All x/y coordinates represent the position of the center of each pad with respect to the center (x/y = 0) of the chip (see Figure 2).*

| Symbol | Pad | X ($\mu$m) | Y ($\mu$m) | Description | |
|---|---|---|---|---|---|
| - | 1 | 5973.6 | −821.7 | dummy | |
| - | 2 | 5969.5 | 823.4 | | |
| - | 3 | 5899.5 | 823.4 | | |
| - | 4 | 5829.5 | 823.4 | | |
| - | 5 | 5479.5 | 823.4 | | |
| - | 6 | 5409.5 | 823.4 | | |
| - | 7 | 5059.5 | 823.4 | | |
| - | 8 | 4989.5 | 823.4 | | |
| - | 9 | 4639.5 | 823.4 | | |
| - | 10 | 4569.5 | 823.4 | | |
| - | 11 | 4219.5 | 823.4 | | |
| - | 12 | 4149.5 | 823.4 | | |
| - | 13 | 3799.5 | 823.4 | | |
| - | 14 | 3729.5 | 823.4 | | |
| OSC | 15 | 3449.5 | 823.4 | oscillator input | [1] |
| $V_{LCDSENSE}$ | 16 | 3169.5 | 823.4 | voltage multiplier regulation input ($V_{LCD}$) | [2] |

**Table 5.** **Bonding pad description** *…continued*
*All x/y coordinates represent the position of the center of each pad with respect to the center (x/y = 0) of the chip (see Figure 2).*

| Symbol | Pad | X ($\mu$m) | Y ($\mu$m) | Description | |
|---|---|---|---|---|---|
| $V_{LCDOUT}$ | 17 | 3099.5 | 823.4 | voltage multiplier output ($V_{LCD}$) | [3] |
| $V_{LCDOUT}$ | 18 | 3029.5 | 823.4 | | |
| $V_{LCDOUT}$ | 19 | 2959.5 | 823.4 | | |
| $V_{LCDOUT}$ | 20 | 2889.5 | 823.4 | | |
| $V_{LCDOUT}$ | 21 | 2819.5 | 823.4 | | |
| $V_{LCDOUT}$ | 22 | 2749.5 | 823.4 | | |
| $V_{LCDOUT}$ | 23 | 2679.5 | 823.4 | | |
| $V_{LCDIN}$ | 24 | 2539.5 | 823.4 | LCD supply voltage ($V_{LCD}$) | [2] |
| $V_{LCDIN}$ | 25 | 2469.5 | 823.4 | | |
| $V_{LCDIN}$ | 26 | 2399.5 | 823.4 | | |
| $V_{LCDIN}$ | 27 | 2329.5 | 823.4 | | |
| $V_{LCDIN}$ | 28 | 2259.5 | 823.4 | | |
| $V_{LCDIN}$ | 29 | 2189.5 | 823.4 | | |
| $V_{LCDIN}$ | 30 | 2119.5 | 823.4 | | |
| $\overline{RES}$ | 31 | 1979.5 | 823.4 | external reset input (active LOW) | [4] |
| $V_{DD3}$ | 32 | 1699.5 | 823.4 | supply voltage 3 | [5] |
| $V_{DD3}$ | 33 | 1629.5 | 823.4 | | |
| $V_{DD3}$ | 34 | 1559.5 | 823.4 | | |
| $V_{DD2}$ | 35 | 1279.5 | 823.4 | supply voltage 2 | [5] |
| $V_{DD2}$ | 36 | 1209.5 | 823.4 | | |
| $V_{DD2}$ | 37 | 1139.5 | 823.4 | | |
| $V_{DD2}$ | 38 | 1069.5 | 823.4 | | |
| $V_{DD2}$ | 39 | 999.5 | 823.4 | | |
| $V_{DD2}$ | 40 | 929.5 | 823.4 | | |
| $V_{DD2}$ | 41 | 859.5 | 823.4 | | |
| $V_{DD2}$ | 42 | 789.5 | 823.4 | | |
| $V_{DD1}$ | 43 | 649.5 | 823.4 | supply voltage 1 | [5] |
| $V_{DD1}$ | 44 | 579.5 | 823.4 | | |
| $V_{DD1}$ | 45 | 509.5 | 823.4 | | |
| $V_{DD1}$ | 46 | 439.5 | 823.4 | | |
| $V_{DD1}$ | 47 | 369.5 | 823.4 | | |
| $V_{DD1}$ | 48 | 299.5 | 823.4 | | |
| $V_{DD1}$ | 49 | 229.5 | 823.4 | | |
| SDA | 50 | 19.5 | 823.4 | serial data line input of the I²C-bus | |
| SDA | 51 | −50.5 | 823.4 | | |
| SDACK | 52 | −400.5 | 823.4 | serial data acknowledge output | [6] |
| - | 53 | −750.5 | 823.4 | dummy | |
| SA0 | 54 | −820.5 | 823.4 | I²C-bus slave address input; bit 0 | |
| ENR | 55 | −1100.5 | 823.4 | enable internal Power-On Reset (POR) input | [7] |

**Table 5.** **Bonding pad description** *…continued*

*All x/y coordinates represent the position of the center of each pad with respect to the center (x/y = 0) of the chip (see Figure 2).*

| Symbol | Pad | X ($\mu$m) | Y ($\mu$m) | Description | |
|---|---|---|---|---|---|
| T4 | 56 | −1380.5 | 823.4 | test input 4 | [8] |
| $V_{SS2}$ | 57 | −1660.5 | 823.4 | ground 2 | [9] |
| $V_{SS2}$ | 58 | −1730.5 | 823.4 | | |
| $V_{SS2}$ | 59 | −1800.5 | 823.4 | | |
| $V_{SS2}$ | 60 | −1870.5 | 823.4 | | |
| $V_{SS2}$ | 61 | −1940.5 | 823.4 | | |
| $V_{SS2}$ | 62 | −2010.5 | 823.4 | | |
| $V_{SS2}$ | 63 | −2080.5 | 823.4 | | |
| $V_{SS1}$ | 64 | −2220.5 | 823.4 | ground 1 | [9] |
| $V_{SS1}$ | 65 | −2290.5 | 823.4 | | |
| $V_{SS1}$ | 66 | −2360.5 | 823.4 | | |
| $V_{SS1}$ | 67 | −2430.5 | 823.4 | | |
| $V_{SS1}$ | 68 | −2500.5 | 823.4 | | |
| $V_{SS1}$ | 69 | −2570.5 | 823.4 | | |
| $V_{SS1}$ | 70 | −2640.5 | 823.4 | | |
| T3 | 71 | −2780.5 | 823.4 | test 3 | [8] |
| T1 | 72 | −3060.5 | 823.4 | test 1 | [8] |
| SCL | 73 | −3410.5 | 823.4 | serial clock line input of the I2C-bus | |
| SCL | 74 | −3480.5 | 823.4 | | |
| - | 75 | −3830.5 | 823.4 | dummy | |
| - | 76 | −4180.5 | 823.4 | | |
| - | 77 | −4530.5 | 823.4 | | |
| T2 | 78 | −4600.5 | 823.4 | test 2 output | [10] |
| - | 79 | −4880.5 | 823.4 | dummy | |
| - | 80 | −4950.5 | 823.4 | | |
| - | 81 | −5230.5 | 823.4 | | |
| - | 82 | −5300.5 | 823.4 | | |
| - | 83 | −5650.5 | 823.4 | | |
| - | 84 | −5720.5 | 823.4 | | |
| - | 85 | −5930.5 | 823.4 | | |
| - | 86 | −5926.4 | −821.7 | | |
| R0 | 87 | −5786.4 | −821.7 | LCD row driver output | |
| R2 | 88 | −5716.4 | −821.7 | | |
| R4 | 89 | −5646.4 | −821.7 | | |
| R6 | 90 | −5576.4 | −821.7 | | |
| R8 | 91 | −5506.4 | −821.7 | | |
| R10 | 92 | −5436.4 | −821.7 | | |

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**Table 5.** **Bonding pad description** *…continued*

*All x/y coordinates represent the position of the center of each pad with respect to the center (x/y = 0) of the chip (see Figure 2).*

| Symbol | Pad | X ($\mu$m) | Y ($\mu$m) | Description |
|---|---|---|---|---|
| R12 | 93 | −5366.4 | −821.7 | LCD row driver output |
| R14 | 94 | −5296.4 | −821.7 | |
| R16 | 95 | −5226.4 | −821.7 | |
| R18 | 96 | −5156.4 | −821.7 | |
| R20 | 97 | −5086.4 | −821.7 | |
| R22 | 98 | −5016.4 | −821.7 | |
| R24 | 99 | −4946.4 | −821.7 | |
| R26 | 100 | −4876.4 | −821.7 | |
| R28 | 101 | −4806.4 | −821.7 | |
| R30 | 102 | −4736.4 | −821.7 | |
| R32 | 103 | −4666.4 | −821.7 | |
| C0 | 104 | −4526.4 | −821.7 | LCD column driver output |
| C1 | 105 | −4456.4 | −821.7 | |
| C2 | 106 | −4386.4 | −821.7 | |
| C3 | 107 | −4316.4 | −821.7 | |
| C4 | 108 | −4246.4 | −821.7 | |
| C5 | 109 | −4176.4 | −821.7 | |
| C6 | 110 | −4106.4 | −821.7 | |
| C7 | 111 | −4036.4 | −821.7 | |
| C8 | 112 | −3966.4 | −821.7 | |
| C9 | 113 | −3896.4 | −821.7 | |
| C10 | 114 | −3826.4 | −821.7 | |
| C11 | 115 | −3756.4 | −821.7 | |
| C12 | 116 | −3688.4 | −821.7 | |
| C13 | 117 | −3616.4 | −821.7 | |
| C14 | 118 | −3546.4 | −821.7 | |
| C15 | 119 | −3476.4 | −821.7 | |
| C16 | 120 | −3406.4 | −821.7 | |
| C17 | 121 | −3336.4 | −821.7 | |
| C18 | 122 | −3266.4 | −821.7 | |
| C19 | 123 | −3196.4 | −821.7 | |
| C20 | 124 | −3126.4 | −821.7 | |
| C21 | 125 | −3056.4 | −821.7 | |
| C22 | 126 | −2986.4 | −821.7 | |
| C23 | 127 | −2916.4 | −821.7 | |
| C24 | 128 | −2846.4 | −821.7 | |
| C25 | 129 | −2776.4 | −821.7 | |
| C26 | 130 | −2706.4 | −821.7 | |
| C27 | 131 | −2636.4 | −821.7 | |

**Table 5.** **Bonding pad description** *…continued*
*All x/y coordinates represent the position of the center of each pad with respect to the center (x/y = 0) of the chip (see Figure 2).*

| Symbol | Pad | X ($\mu$m) | Y ($\mu$m) | Description |
|---|---|---|---|---|
| C28 | 132 | −2566.4 | −821.7 | LCD column driver output |
| C29 | 133 | −2496.4 | −821.7 | |
| C30 | 134 | −2426.4 | −821.7 | |
| C31 | 135 | −2356.4 | −821.7 | |
| C32 | 136 | −2216.4 | −821.7 | |
| C33 | 137 | −2146.4 | −821.7 | |
| C34 | 138 | −2076.4 | −821.7 | |
| C35 | 139 | −2006.4 | −821.7 | |
| C36 | 140 | −1936.4 | −821.7 | |
| C37 | 141 | −1866.4 | −821.7 | |
| C38 | 142 | −1796.4 | −821.7 | |
| C39 | 143 | −1726.4 | −821.7 | |
| C40 | 144 | −1656.4 | −821.7 | |
| C41 | 145 | −1586.4 | −821.7 | |
| C42 | 146 | −1516.4 | −821.7 | |
| C43 | 147 | −1446.4 | −821.7 | |
| C44 | 148 | −1376.4 | −821.7 | |
| C45 | 149 | −1306.4 | −821.7 | |
| C46 | 150 | −1236.4 | −821.7 | |
| C47 | 151 | −1166.4 | −821.7 | |
| C48 | 152 | −1096.4 | −821.7 | |
| C49 | 153 | −1026.4 | −821.7 | |
| C50 | 154 | −956.4 | −821.7 | |
| C51 | 155 | −886.4 | −821.7 | |
| C52 | 156 | −816.4 | −821.7 | |
| C53 | 157 | −746.4 | −821.7 | |
| C54 | 158 | −676.4 | −821.7 | |
| C55 | 159 | −606.4 | −821.7 | |
| C56 | 160 | −534.6 | −821.7 | |
| C57 | 161 | −466.4 | −821.7 | |
| C58 | 162 | −396.4 | −821.7 | |
| C59 | 163 | −326.4 | −821.7 | |
| C60 | 164 | −256.4 | −821.7 | |
| C61 | 165 | −186.4 | −821.7 | |
| C62 | 166 | −116.6 | −821.7 | |
| C63 | 167 | −46.4 | −821.7 | |
| C64 | 168 | 93.6 | −821.7 | |
| C65 | 169 | 163.6 | −821.7 | |
| C66 | 170 | 233.6 | −821.7 | |

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**Table 5.** **Bonding pad description** *…continued*
*All x/y coordinates represent the position of the center of each pad with respect to the center (x/y = 0) of the chip (see* Figure 2*).*

| Symbol | Pad | X ($\mu$m) | Y ($\mu$m) | Description |
|---|---|---|---|---|
| C67 | 171 | 303.6 | −821.7 | LCD column driver output |
| C68 | 172 | 373.3 | −821.7 | |
| C69 | 173 | 443.6 | −821.7 | |
| C70 | 174 | 513.6 | −821.7 | |
| C71 | 175 | 583.6 | −821.7 | |
| C72 | 176 | 653.6 | −821.7 | |
| C73 | 177 | 723.6 | −821.7 | |
| C74 | 178 | 793.6 | −821.7 | |
| C75 | 179 | 863.6 | −821.7 | |
| C76 | 180 | 933.6 | −821.7 | |
| C77 | 181 | 1003.6 | −821.7 | |
| C78 | 182 | 1073.6 | −821.7 | |
| C79 | 183 | 1143.6 | −821.7 | |
| C80 | 184 | 1213.6 | −821.7 | |
| C81 | 185 | 1283.6 | −821.7 | |
| C82 | 186 | 1353.6 | −821.7 | |
| C83 | 187 | 1423.6 | −821.7 | |
| C84 | 188 | 1493.6 | −821.7 | |
| C85 | 189 | 1563.6 | −821.7 | |
| C86 | 190 | 1633.6 | −821.7 | |
| C87 | 191 | 1703.6 | −821.7 | |
| C88 | 192 | 1773.6 | −821.7 | |
| C89 | 193 | 1843.6 | −821.7 | |
| C90 | 194 | 1913.6 | −821.7 | |
| C91 | 195 | 1983.6 | −821.7 | |
| C92 | 196 | 2053.6 | −821.7 | |
| C93 | 197 | 2123.6 | −821.7 | |
| C94 | 198 | 2193.6 | −821.7 | |
| C95 | 199 | 2263.6 | −821.7 | |
| C96 | 200 | 2403.6 | −821.7 | |
| C97 | 201 | 2473.6 | −821.7 | |
| C98 | 202 | 2543.6 | −821.7 | |
| C99 | 203 | 2613.6 | −821.7 | |
| C100 | 204 | 2683.6 | −821.7 | |
| C101 | 205 | 2753.6 | −821.7 | |
| C102 | 206 | 2823.6 | −821.7 | |
| C103 | 207 | 2893.6 | −821.7 | |
| C104 | 208 | 2963.6 | −821.7 | |
| C105 | 209 | 3033.6 | −821.7 | |

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**Table 5.    Bonding pad description** …*continued*

*All x/y coordinates represent the position of the center of each pad with respect to the center (x/y = 0) of the chip (see Figure 2).*

| Symbol | Pad | X (μm) | Y (μm) | Description |
|---|---|---|---|---|
| C106 | 210 | 3103.6 | −821.7 | LCD column driver output |
| C107 | 211 | 3173.6 | −821.7 | |
| C108 | 212 | 3243.6 | −821.7 | |
| C109 | 213 | 3313.6 | −821.7 | |
| C110 | 214 | 3383.6 | −821.7 | |
| C111 | 215 | 3453.6 | −821.7 | |
| C112 | 216 | 3523.6 | −821.7 | |
| C113 | 217 | 3593.6 | −821.7 | |
| C114 | 218 | 3663.6 | −821.7 | |
| C115 | 219 | 3733.6 | −821.7 | |
| C116 | 220 | 3803.6 | −821.7 | |
| C117 | 221 | 3873.6 | −821.7 | |
| C118 | 222 | 3943.6 | −821.7 | |
| C119 | 223 | 4013.6 | −821.7 | |
| C120 | 224 | 4083.6 | −821.7 | |
| C121 | 225 | 4153.6 | −821.7 | |
| C122 | 226 | 4223.6 | −821.7 | |
| C123 | 227 | 4293.6 | −821.7 | |
| C124 | 228 | 4363.6 | −821.7 | |
| C125 | 229 | 4433.6 | −821.7 | |
| C126 | 230 | 4503.6 | −821.7 | |
| C127 | 231 | 4573.6 | −821.7 | |
| R33 | 232 | 4713.6 | −821.7 | LCD row driver output; icon row |
| R31 | 233 | 4783.6 | −821.7 | LCD row driver output |
| R29 | 234 | 4853.6 | −821.7 | |
| R27 | 235 | 4923.6 | −821.7 | |
| R25 | 236 | 4993.6 | −821.7 | |
| R23 | 237 | 5063.6 | −821.7 | |
| R21 | 238 | 5113.6 | −821.7 | |
| R19 | 239 | 5203.6 | −821.7 | |
| R17 | 240 | 5343.6 | −821.7 | |
| R15 | 241 | 5413.6 | −821.7 | |
| R13 | 242 | 5483.6 | −821.7 | |
| R11 | 243 | 5553.6 | −821.7 | |
| R9 | 244 | 5623.6 | −821.7 | |
| R7 | 245 | 5693.6 | −821.7 | |
| R5 | 246 | 5763.6 | −821.7 | |
| R3 | 247 | 5833.6 | −821.7 | |
| R1 | 248 | 5903.6 | −821.7 | |

[1] If the on-chip oscillator is used, this input must be connected to $V_{DD1}$.

[2] If the internal $V_{LCD}$ generation is used, $V_{LCDOUT}$, $V_{LCDIN}$, and $V_{LCDSENSE}$ must be connected together.

[3] If an external $V_{LCD}$ is used in the application, then pin $V_{LCDOUT}$ must be left open-circuit, otherwise the chip will be damaged.

[4] If only the internal Power-On Reset (POR) is used, this input must be connected to $V_{DD1}$.

[5] $V_{DD1}$ is for the logic supply, $V_{DD2}$ and $V_{DD3}$ are for the voltage multiplier. For split power supplies, $V_{DD2}$ and $V_{DD3}$ must be connected together. If only one supply voltage is available, $V_{DD1}$, $V_{DD2}$, and $V_{DD3}$ must be connected together.

[6] Serial data acknowledge for the I²C-bus. By connecting SDACK to SDA externally, the SDA line becomes fully I²C-bus compatible. Having the acknowledge output separated from the serial data line is advantageous in Chip-On-Glass (COG) applications. In COG applications where the track resistance from the SDACK pad to the system SDA line can be significant, a potential divider is generated by the bus pull-up resistor and the Indium Tin Oxide (ITO) track resistance. It is possible that the PCF8531 will not be able to create a valid logic 0 level during the acknowledge cycle. By splitting the SDA input from the SDACK output, the device could be used in a mode that ignores the acknowledge bit. In COG applications where the acknowledge cycle is required, it is necessary to minimize the track resistance from the SDACK pad to the system SDA line to guarantee a valid LOW level.

[7] If ENR is connected to $V_{SS}$, Power-On Reset (POR) is disabled; to enable Power-On Reset (POR) ENR must be connected to $V_{DD1}$.

[8] In the application, this input must be connected to $V_{SS}$.

[9] $V_{SS1}$ and $V_{SS2}$ must be connected together.

[10] In the application, T2 must be left open-circuit.

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# 7. Functional description

## 7.1 Oscillator

The on-chip oscillator provides the clock signal for the display system. No external components are required and the OSC input must be connected to $V_{DD}$. An external clock signal, if used, is connected to this input.

## 7.2 Power-On Reset (POR)

The on-chip Power-On Reset (POR) initializes the chip after power-on or power failure.

## 7.3 I²C-bus controller

The I²C-bus controller receives and executes the commands. The PCF8531 acts as an I²C-bus slave receiver and therefore it cannot control bus communication.

## 7.4 Input filters

To enhance noise immunity in electrically adverse environments, RC low-pass filters are provided on the SDA and SCL lines.

## 7.5 Display data RAM

The PCF8531 contains $34 \times 128$ bits static RAM for storing the display data, see Figure 7. The RAM is divided into 6 banks of 128 bytes ($6 \times 8 \times 128$ bits). Bank 5 is used for icon data. During RAM access, data is transferred to the RAM via the I²C-bus interface. There is a direct correspondence between the X address and column output number.

## 7.6 Timing generator

The timing generator produces the various signals required to drive the internal circuitry. Internal chip operation is not affected by operations on the data buses.

## 7.7 Address counter

The address counter sets the addresses of the display data RAM for writing.

## 7.8 Display address counter

The display address counter generates the addresses for read out of the display data.

## 7.9 Command decoder

The command decoder identifies command words that arrive on the I²C-bus and determines the destination for the following data bytes.

## 7.10 Bias voltage generator

The bias voltage generator generates four buffered intermediate bias voltages. This block contains the generator for the reference voltages and the four buffers. This block can operate in two voltage ranges:

- Normal mode: 4.0 V to 9.0 V
- Power save mode: 3.0 V to 9.0 V.

## 7.11 $V_{LCD}$ generator

The $V_{LCD}$ voltage generator contains a configurable 2 to 5 times voltage multiplier; this is programmed by software.

## 7.12 Reset

The PCF8531 has the possibility of two reset modes: internal Power-On Reset (POR) or external reset ($\overline{RES}$). The reset mode is selected using the ENR signal. After a reset, the chip has the following state:

- All row and column outputs are set to $V_{SS}$ (display off)
- RAM data is undefined
- Power-down mode

## 7.13 Power-down

During power-down, all static currents are switched off (no internal oscillator, no timing and no LCD segment drive system) and all LCD outputs are internally connected to $V_{SS}$. The I²C-bus function remains operational.

## 7.14 Column driver outputs

The LCD drive section includes 128 column outputs (C0 to C127) which must be connected directly to the LCD. The column output signals are generated in accordance with the multiplexed row signals and with the data in the display latch. When less than 128 columns are required, the unused column outputs must be left open-circuit.

## 7.15 Row driver outputs

The LCD drive section includes 34 row outputs (R0 to R33), which must be connected directly to the LCD. The row output signals are generated in accordance with the selected LCD drive mode. If less than 34 rows or lower multiplex rates are required, the unused outputs must be left open-circuit. The row signals are interlaced i.e. the selection order is R0, R2, ..., R1, R3, etc.

## 8. LCD waveforms and DDRAM to data mapping

The LCD waveforms and the DDRAM to display data mapping are shown in Figure 5, Figure 6 and Figure 7.



(1) $V_{state1}(t) = C1(t) - R0(t)$.

(2) $V_{state2}(t) = C1(t) - R1(t)$.

**Fig 5.    Typical LCD driver waveforms**
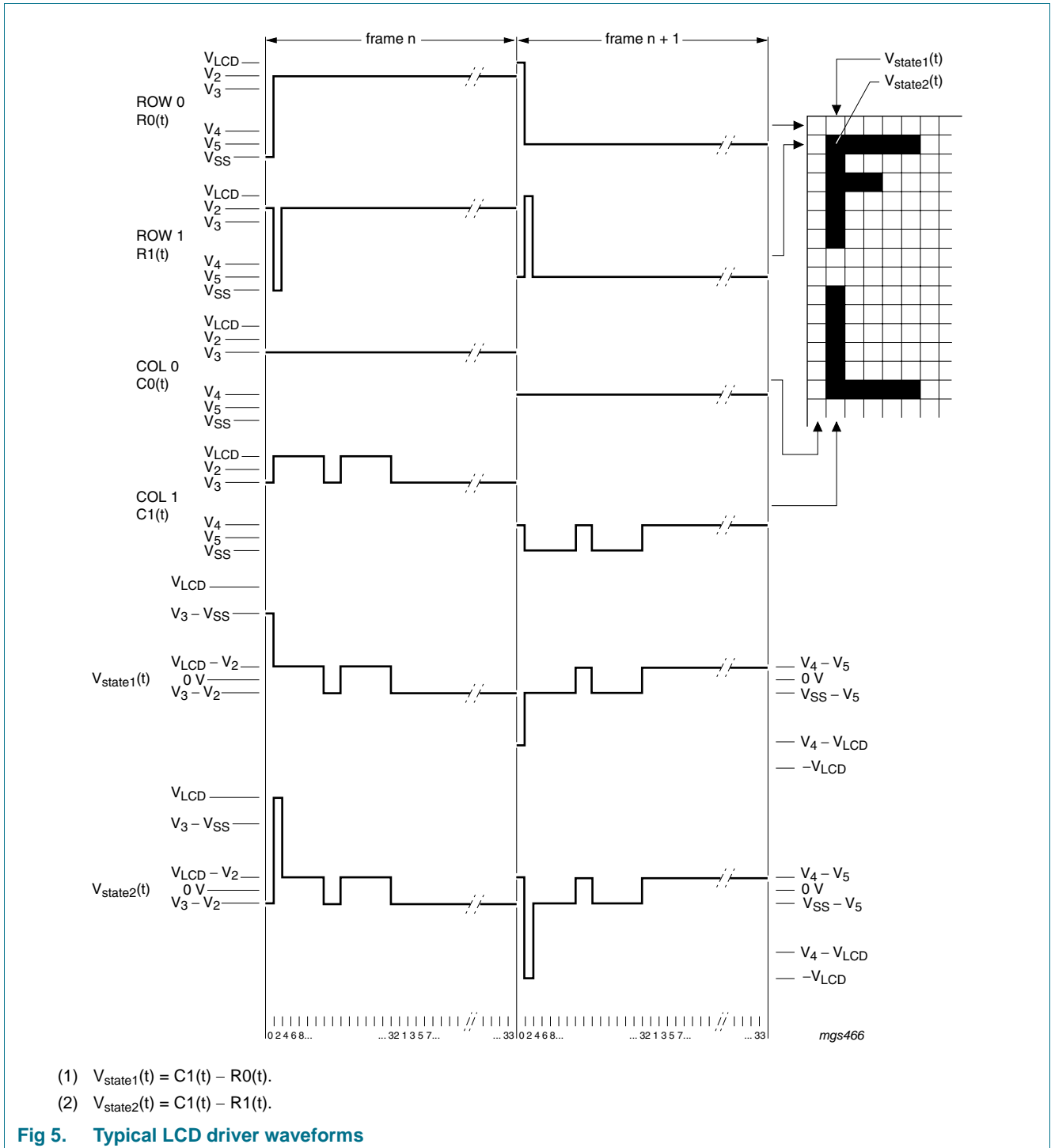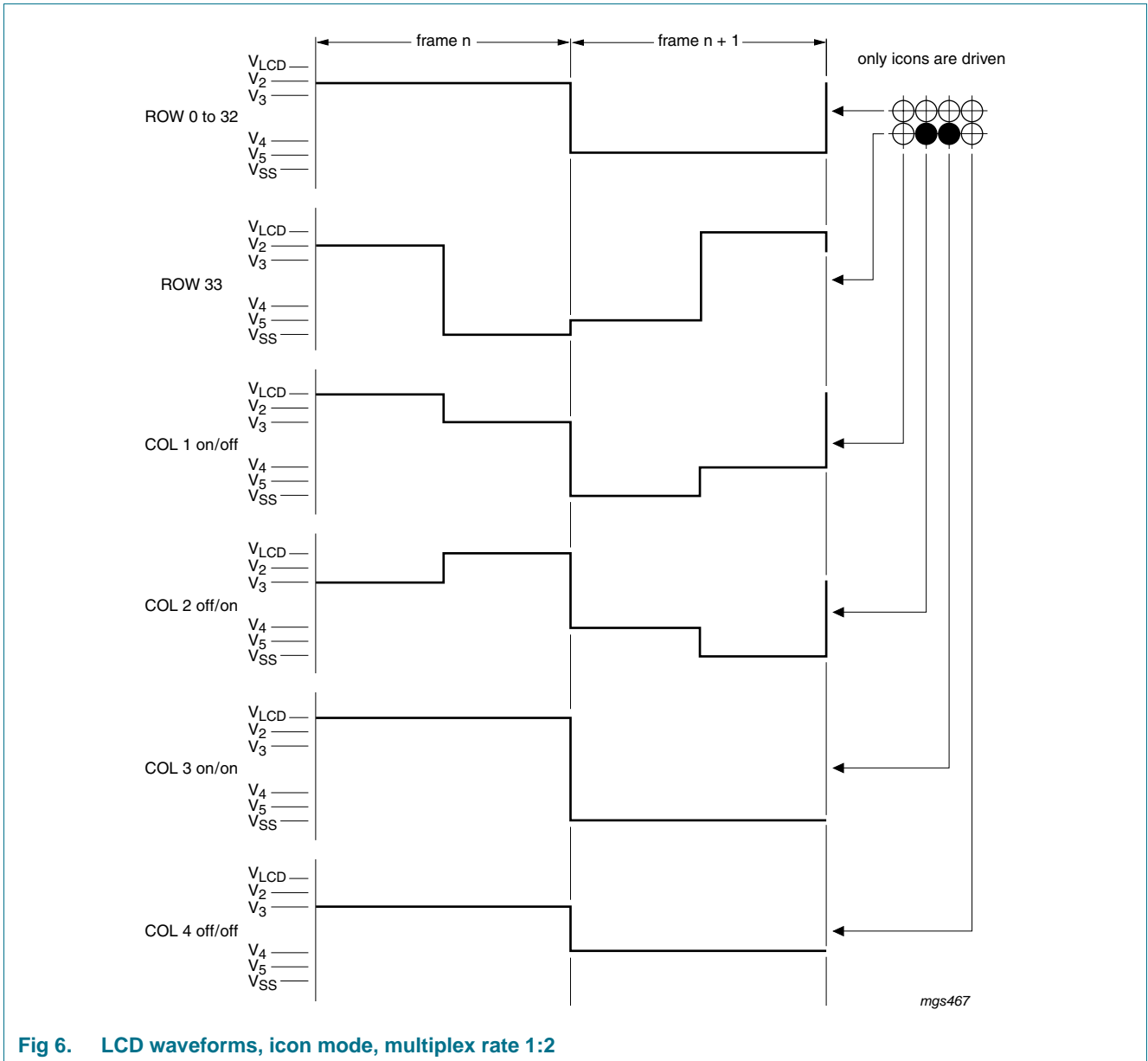
**Fig 6.    LCD waveforms, icon mode, multiplex rate 1:2**
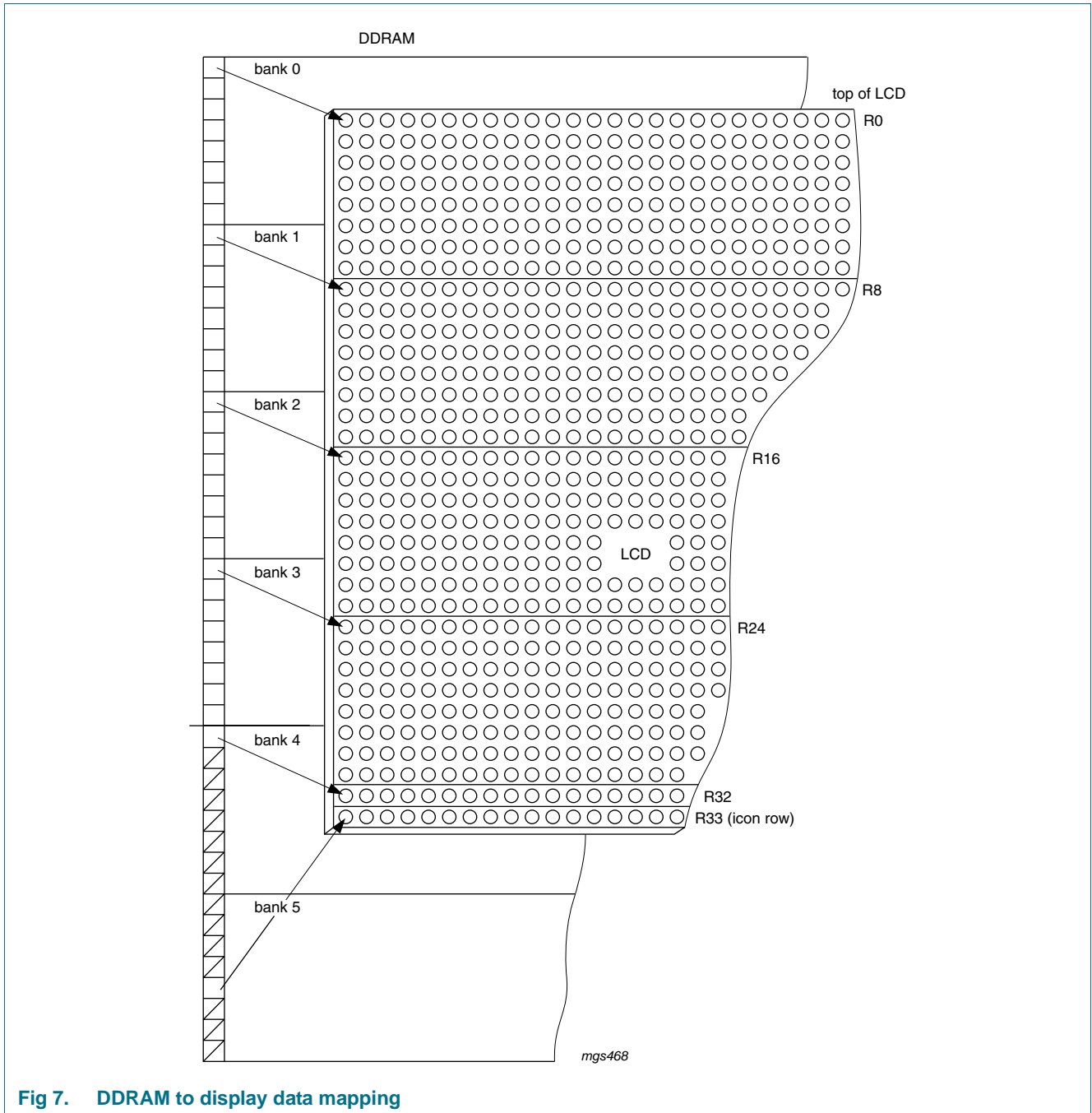
**Fig 7.    DDRAM to display data mapping**

## 8.1  Addressing

Data is written in bytes into the RAM matrix of the PCF8531 as shown in Figure 8, Figure 9 and Figure 10. The display RAM has a matrix of 34 × 128 bits. The columns are addressed by the address pointer. The address ranges are X 0 to X 127 (7Fh) and Y 0 to Y 5 (5h). Addresses outside of these ranges are not allowed. In vertical addressing mode (V = 1), the Y address increments after each byte (see Figure 9). After the last Y address (Y = 4), Y wraps around to 0 and X increments to address the next column. In horizontal addressing mode (V = 0), the X address increments after each byte (see Figure 10). After the last X address (X = 127), X wraps around to 0 and Y increments to address the next

row. After the very last address (X = 127 and Y = 4), the address pointers wrap around to address (X = 0 and Y = 0). The Y address 5 is reserved for icon data and is not affected by the addressing mode. Please note that in bank 4 only the LSB (DB0) of the data is written into the RAM and in bank 5 only the 5th data bit (DB4) is written into the RAM.
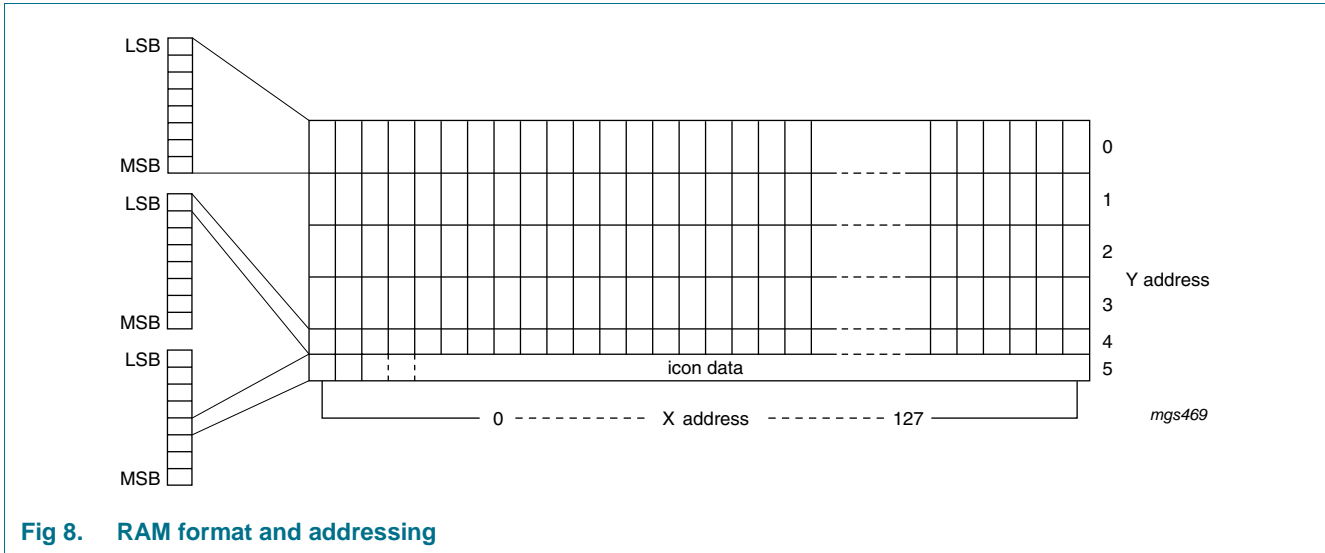


**Fig 8.    RAM format and addressing**
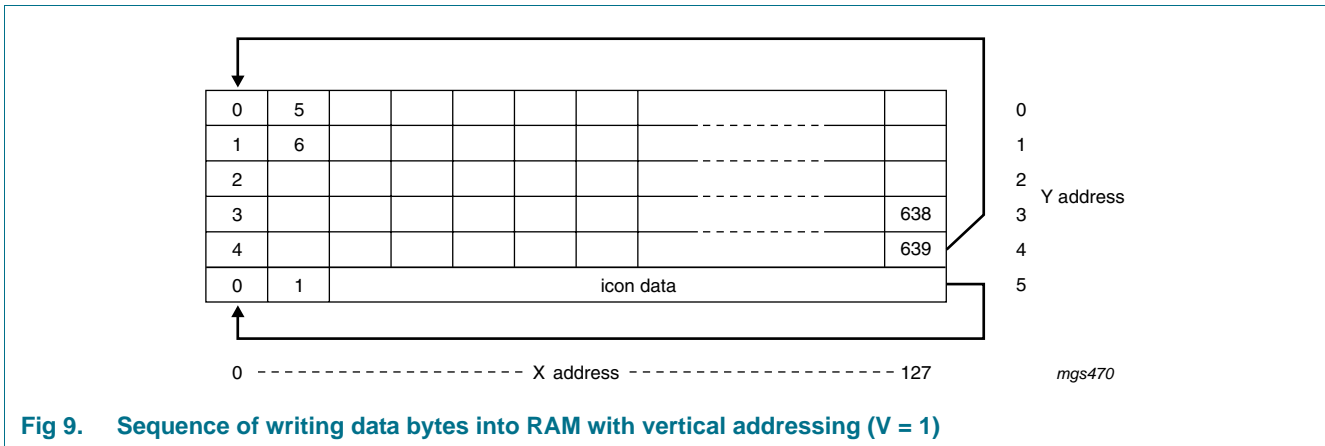


**Fig 9.    Sequence of writing data bytes into RAM with vertical addressing (V = 1)**
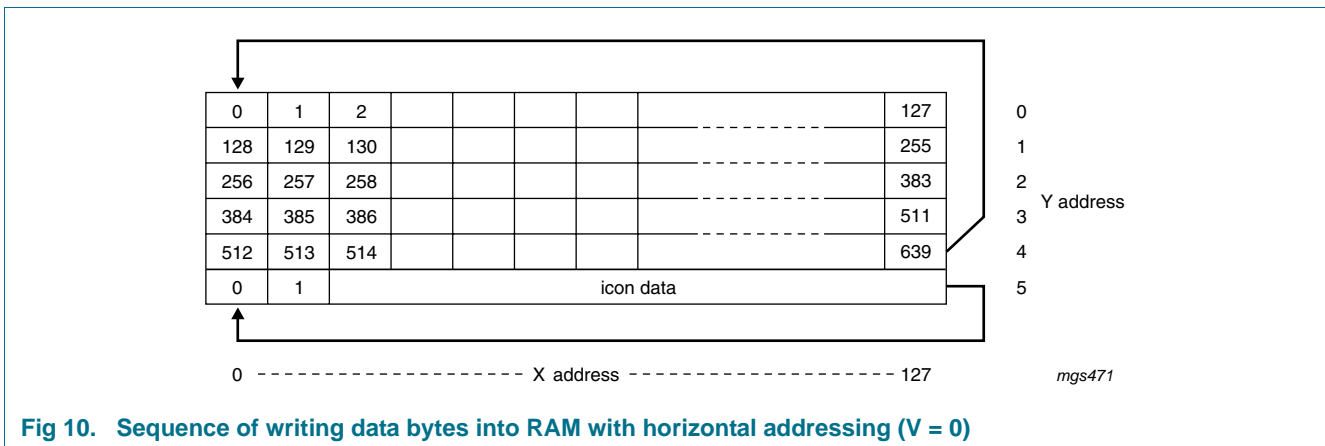


**Fig 10.   Sequence of writing data bytes into RAM with horizontal addressing (V = 0)**

## 9. Instructions

Only two PCF8531 registers, the instruction register and the data register can be directly controlled by the MPU. Before internal operation, control information is stored temporarily in these registers to allow interfacing to various types of MPUs which operate at different speeds or to allow interfacing to peripheral control ICs. The PCF8531 operation is controlled by the instructions given in Table 11.

Instructions are of four types:

- Those that define PCF8531 functions e.g. display configuration, etc.
- Those that set internal RAM addresses
- Those that perform data transfer to/from the internal RAM
- Others

In normal mode instructions which perform data transfer to/from the internal RAM are used most frequently. Automatic incrementing by 1 of internal RAM addresses after each data write reduces the MPU program load.

### 9.1 Reset

After reset or internal Power-On Reset (POR) (depending on the application), the LCD driver is set to the following state:

- Power-down mode (PD = 1)
- Horizontal addressing (V = 0)
- Display blank (D = 0; E = 0), no icon mode (IM = 0)
- Address counter X[6:0] = 0; Y[2:0] = 0
- Bias system BS[2:0] = 0
- Multiplex rate M[1:0] = 0 (multiplex rate 1:17)
- Temperature control mode TC[2:0] = 0
- HV-gen control, HVE = 0 the high voltage (HV) generator is switched off, PRS = 0 and S[1:0] = 0
- $V_{LCD}$ = 0 V
- RAM data is undefined
- Command page definition H[1:0] = 0

### 9.2 Function set

#### 9.2.1 PD

When PD = 1, the power-down mode of the LCD driver is active:

- All LCD outputs at $V_{SS}$ (display off)
- Power-On Reset (POR) detection active, oscillator off
- $V_{LCD}$ can be disconnected
- I²C-bus is operational, commands can be executed
- RAM contents not cleared; RAM data can be written
- Register settings remain unchanged

#### 9.2.2 V

When V = 0 the horizontal addressing is selected. The data is written into the DDRAM as shown in Figure 10. When V = 1 the vertical addressing is selected. The data is written into the DDRAM as shown in Figure 9. Icon data is written independently of V when Y address is 5.

### 9.3 Set Y address

Bits Y2, Y1, and Y0 define the Y address vector of the display RAM (see Table 6).

**Table 6.    Y address**

| Y2 | Y1 | Y0 | Bank |
|----|----|----|------|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 2 |
| 0 | 1 | 1 | 3 |
| 1 | 0 | 0 | 4 |
| 1 | 0 | 1 | 5 (icons) |

### 9.4 Set X address

The X address points to the columns. The range of X is 0 to 127 (7Fh).

### 9.5 Set multiplex rate

M[1:0] selects the multiplex rate (see Table 7).

**Table 7.    Multiplex rates**

| Multiplex rate | M1 | M0 |
|----------------|----|----|
| 1:17 | 0 | 0 |
| 1:26 | 1 | 0 |
| 1:34 | 0 | 1 |

### 9.6 Display control (D, E, and IM)

Bits D and E select the display mode (see Table 13). Bit IM (see Table 12) sets the display to icon mode.

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## 9.7 Set bias system

The bias voltage levels are set in the ratio of $R - R - n \times R - R - R$ (see Figure 11).



V$_1$ = V$_{LCD}$

R

V$_2$

R

V$_3$

n × R

V$_4$

R

V$_5$

R

V$_6$ = V$_{SS}$

013aaa183
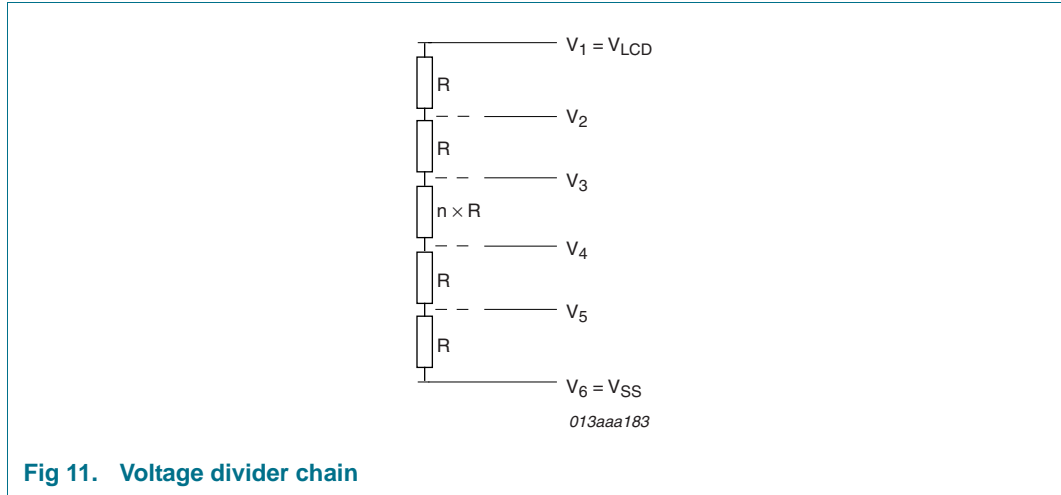
**Fig 11. Voltage divider chain**

Different multiplex rates require different bias settings. Bias settings are programmed by BS[2:0], which sets the binary number n. The optimum value for n is given by:

$$n = \sqrt{muxrate} - 3$$

Supported values of n are given in Table 8. Table 9 shows the intermediate bias voltages.

**Table 8. Programming the required bias system**

| BS[2:0] | n | Bias system | Comment |
|---|---|---|---|
| 000 | 7 | $\frac{1}{11}$ | - |
| 001 | 6 | $\frac{1}{10}$ | - |
| 010 | 5 | $\frac{1}{9}$ | - |
| 011 | 4 | $\frac{1}{8}$ | - |
| 100 | 3 | $\frac{1}{7}$ | recommended for 1:34 |
| 101 | 2 | $\frac{1}{6}$ | recommended for 1:26 |
| 110 | 1 | $\frac{1}{5}$ | recommended for 1:17 |
| 111 | 0 | $\frac{1}{4}$ | recommended for icon mode |

### 9.8 LCD bias voltage

**Table 9.** **Intermediate LCD bias voltages**

| Symbol | Bias voltage | Example for $\frac{1}{7}$ bias |
|---|---|---|
| V1 | $V_{LCD}$ | $V_{LCD}$ |
| V2 | $\dfrac{n+3}{n+4} \times V_{LCD}$ | $\frac{6}{7} \times V_{LCD}$ |
| V3 | $\dfrac{n+2}{n+4} \times V_{LCD}$ | $\frac{5}{7} \times V_{LCD}$ |
| V4 | $\dfrac{2}{n+4} \times V_{LCD}$ | $\frac{2}{7} \times V_{LCD}$ |
| V5 | $\dfrac{1}{n+4} \times V_{LCD}$ | $\frac{1}{7} \times V_{LCD}$ |
| V6 | $V_{SS}$ | $V_{SS}$ |

### 9.9 Set $V_{LCD}$ value

$V_{LCD}$ can be set by software. The voltage at intersection temperature [$V_{LCD}$ (T = $T_{ints}$)] can be calculated as: $V_{LCD}$ ($T_{ints}$) = a + $V_{LCD} \times$ b

The generated voltage is dependent on the temperature, programmed Temperature Coefficient (TC) and the programmed voltage at intersection temperature ($T_{ints}$).

$V_{LCD}$ = $V_{LCD}$ ($T_{ints}$) $\times$ [1 + TC $\times$ (T $-$ $T_{ints}$)]

The parameter values are given in Table 10. Two overlapping $V_{LCD}$ ranges can be selected via the command HV-gen control (see Table 10 and Figure 12). The maximum voltage which can be generated depends on the $V_{DD2}$ and $V_{DD3}$ voltages and the display load current. For multiplex rate 1:34, the optimum $V_{LCD}$ can be calculated as:

$$V_{LCD} = \frac{1 + \sqrt{34}}{\sqrt{2 \times \left(1 - \frac{1}{\sqrt{34}}\right)}} \times V_{th} = 5.30 \times V_{th}$$

Where $V_{th}$ is the threshold voltage of the liquid crystal material used.

The practical value for $V_{LCD}$ is determined by equating $V_{off(RMS)}$ with a defined LCD threshold voltage ($V_{th}$), typically when the LCD exhibits approximately 10 % contrast.

As the programming range for the internally generated $V_{LCD}$ allows values above the maximum allowed $V_{LCD}$, the user must ensure, while setting the VOP register and selecting the temperature compensation, that the $V_{LCD}$ limit maximum of 9.0 V is never exceeded under all conditions and including all tolerances.

**Table 10.** **Parameter values for the HV generator programming**

| Symbol | Value | | Unit |
|---|---|---|---|
| | **PRS = 0** | **PRS = 1** | |
| $T_{ints}$ | 27 | 27 | °C |
| a | 2.94 | 6.75 | V |
| b | 0.03 | 0.03 | V |
| programming range | 2.94 to 6.75 | 6.75 to 10.56 | V |



VOP[6:0] (programmed) [00h to 7Fh] program range LOW to HIGH.

**Fig 12.** $V_{LCD}$ **programming of PCF8531**
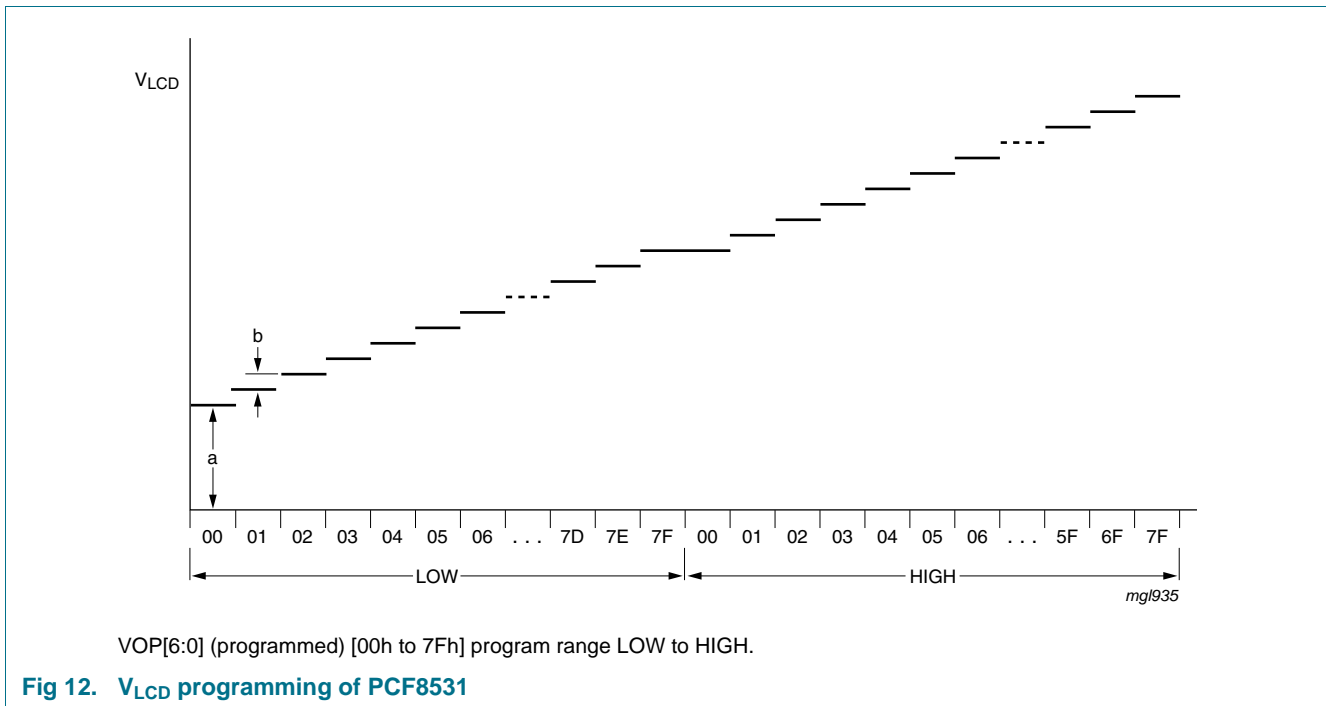
## 9.10 Voltage multiplier control S[1:0]

The PCF8531 incorporates a software configurable voltage multiplier. After reset (internal or external), the voltage multiplier is set to $2 \times V_{DD2}$. The voltage multiplier factors are set by setting bits S[1:0] (see Table 13).

## 9.11 Temperature compensation

Due to the temperature dependency of the viscosity of the liquid crystals, the LCD controlling voltage $V_{LCD}$ should usually be increased at lower temperatures to maintain optimum contrast. Figure 13 shows $V_{LCD}$ for high multiplex rates.

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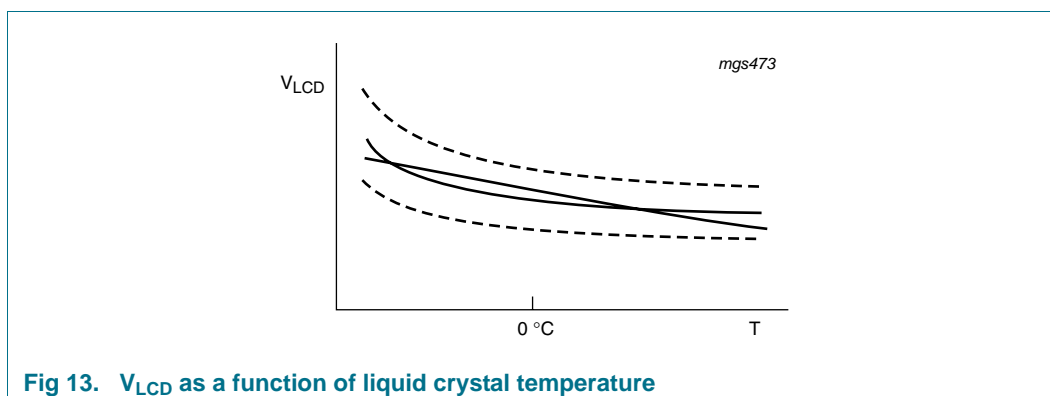
**Fig 13.** $V_{LCD}$ **as a function of liquid crystal temperature**

Linear temperature compensation is supported in the PCF8531. The temperature coefficient of $V_{LCD}$ can be selected from eight values by setting bits TC[2:0] (see Table 13).

**Table 11.    Instruction set**

| Instruction | I²C-bus command[1] | | I²C-bus command byte | | | | | | | | Description |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | |
| **H1 and H0 = don't care (H independent command page)** | | | | | | | | | | | |
| NOP | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | no operation |
| write data | 1 | 0 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | write data to display RAM |
| set default H[1:0] | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | select H[1:0] = 0 |
| **H1 = 0 and H0 = 0 (function and RAM command page)** | | | | | | | | | | | |
| instruction set | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | H1 | H0 | select command page |
| function set | 0 | 0 | 0 | 0 | 1 | 0 | 0 | PD | V | 0 | power-down control; entry mode |
| set Y address of RAM | 0 | 0 | 0 | 1 | 0 | 0 | 0 | Y2 | Y1 | Y0 | set Y address of RAM; $0 \leq Y \leq 5$ |
| set X address of RAM | 0 | 0 | 1 | X6 | X5 | X4 | X3 | X2 | X1 | X0 | set X address of RAM; $0 \leq X \leq 127$ |
| **H1 = 0 and H0 = 1 (display setting command page)** | | | | | | | | | | | |
| multiplex rate | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | M1 | M0 | set multiplex rate |
| display control | 0 | 0 | 0 | 0 | 0 | 0 | 1 | D | IM | E | set display configuration |
| bias system | 0 | 0 | 0 | 0 | 0 | 1 | 0 | BS2 | BS1 | BS0 | set bias system (BSx) |
| **H1 = 1 and H0 = 0 (HV-gen command page)** | | | | | | | | | | | |
| HV-gen control | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | PRS | HVE | set $V_{LCD}$ programming range |
| HV-gen configuration | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | S1 | S0 | set voltage multiplication factor |

**Table 11.  Instruction set** …*continued*

| Instruction | I²C-bus command[1] | | I²C-bus command byte | | | | | | | | Description |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | |
| temperature control | 0 | 0 | 0 | 0 | 1 | 0 | 0 | TC2 | TC1 | TC0 | set temperature coefficient |
| test modes | 0 | 0 | 0 | 1 | X | X | X | X | X | X | do not use (reserved for test) |
| V_LCD control | 0 | 0 | 1 | VOP6 | VOP5 | VOP4 | VOP3 | VOP2 | VOP1 | VOP0 | set V_LCD register |

[1]  R/W̄ is set to the slave address byte; Co and RS are set in the control byte.

**Table 12.  Explanation for symbols in Table 11**

| Bit | 0 | 1 |
|---|---|---|
| PD | chip is active | chip is in power-down mode |
| V | horizontal addressing | vertical addressing |
| IM | normal mode; full display + icons | icon mode; only icons are displayed |
| H[1:0] [1] | see Table 13 | |
| D and E | see Table 13 | |
| HVE | voltage multiplier disabled | voltage multiplier enabled |
| PRS | V_LCD programming range LOW | V_LCD programming range HIGH |
| TC[2:0] | see Table 13 | |
| S[1:0] | see Table 13 | |

[1]  The bits H[1:0] identify the command page (use set default H[1:0] command to set H[1:0] = 0).

**Table 13.  Description of bits H, D and E, TC and S**

| Bits | Value | Description |
|---|---|---|
| **Command page (H)** | | |
| H[1:0] | 00 | function and RAM command page |
| | 01 | display setting command page |
| | 10 | HV-gen command page |
| **Display modes (D, E)** | | |
| D and E | 00 | display blank |
| | 10 | normal mode |
| | 01 | all display segments |
| | 11 | inverse video mode |

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**Table 13.   Description of bits H, D and E, TC and S** *…continued*

| Bits | Value | Description |
|---|---|---|
| **Temperature coefficient (TC)** | | |
| TC[2:0] | 000 | temperature coefficient $TC_0$ |
| | 001 | temperature coefficient $TC_1$ |
| | 010 | temperature coefficient $TC_2$ |
| | 011 | temperature coefficient $TC_3$ |
| | 100 | temperature coefficient $TC_4$ |
| | 101 | temperature coefficient $TC_5$ |
| | 110 | temperature coefficient $TC_6$ |
| | 111 | temperature coefficient $TC_7$ |
| **Voltage multiplier factor (S)** | | |
| S[1:0] | 00 | $2 \times$ voltage multiplier |
| | 01 | $3 \times$ voltage multiplier |
| | 10 | $4 \times$ voltage multiplier |
| | 11 | $5 \times$ voltage multiplier |

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# 10. I²C-bus interface

## 10.1 Characteristics of the I²C-bus

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a Serial DAta line (SDA) and a Serial CLock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

### 10.1.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal (see Figure 14).
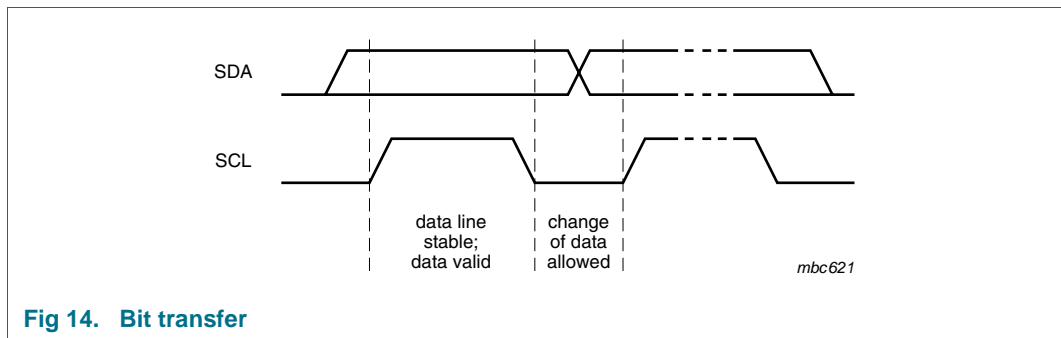


**Fig 14. Bit transfer**

### 10.1.2 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P). The START and STOP conditions are shown in Figure 15.
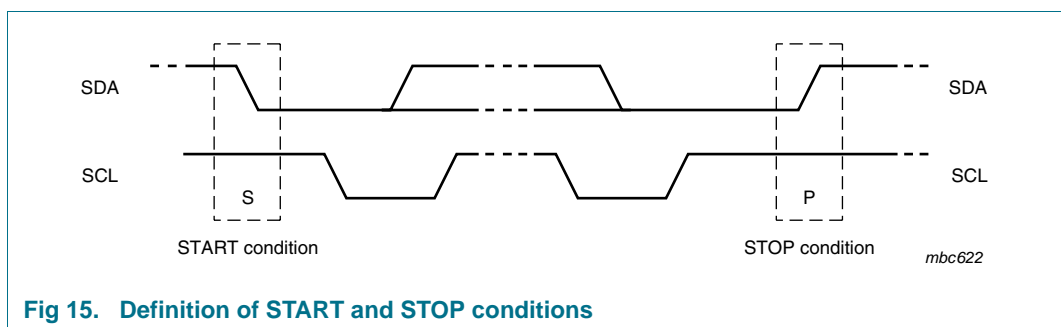


**Fig 15. Definition of START and STOP conditions**

### 10.1.3 System configuration

The system configuration is shown in Figure 16.

- Transmitter: the device that sends the data to the bus

- Receiver: the device that receives the data from the bus

- Master: the device that initiates a transfer, generates clock signals and terminates a transfer

- Slave: the device addressed by a master

- Multi-master: more than one master can attempt to control the bus at the same time without corrupting the message

- Arbitration: procedure to ensure that, if more than one master simultaneously tries to control the bus, only one is allowed to do so and the message is not corrupted

- Synchronization: procedure to synchronize the clock signals of two or more devices.
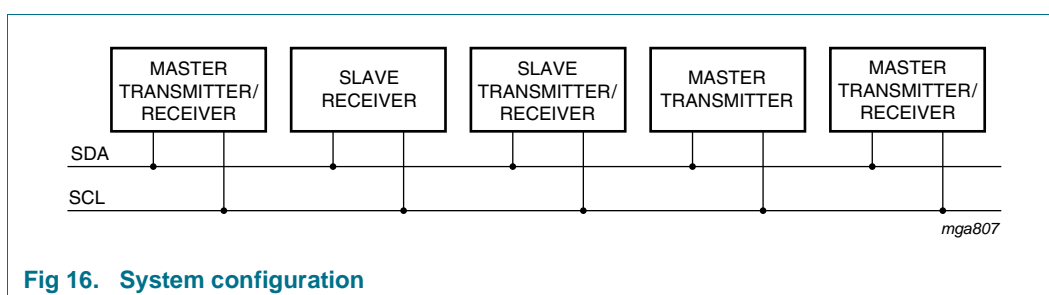


**Fig 16. System configuration**

### 10.1.4 Acknowledge

The number of data bytes transferred between the START and STOP conditions from transmitter to receiver is unlimited. Each byte of eight bits is followed by an acknowledge cycle.

- A slave receiver which is addressed must generate an acknowledge after the reception of each byte.

- Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

- The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration).

- A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

Acknowledgement on the I$^2$C-bus is shown in Figure 17.
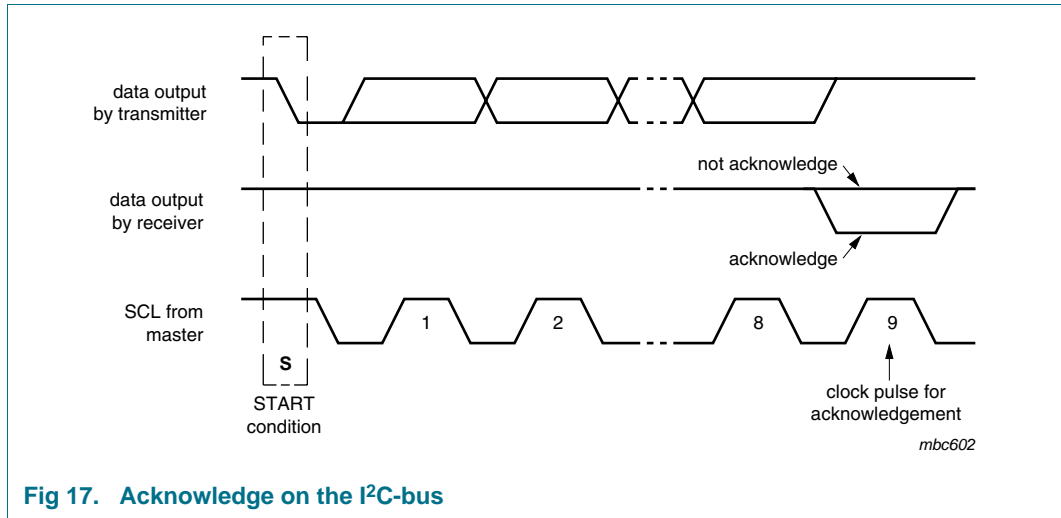
**Fig 17.  Acknowledge on the I²C-bus**

## 10.2  I²C-bus protocol

This driver does not support read. The PCF8531 is a slave receiver. Therefore, it only responds when R/$\overline{\text{W}}$ = 0 in the slave address byte.

Before any data is transmitted on the I²C-bus, the device that must respond is addressed first. Two 7-bit slave addresses (0111100 and 0111101) are reserved for the PCF8531. The least significant bit of the slave address is set by connecting the input SA0 to either logic 0 ($V_{SS}$) or logic 1 ($V_{DD}$).

The I²C-bus protocol is shown in Figure 18.

The sequence is initiated with a START condition (S) from the I²C-bus master, and is followed by the slave address. All slaves with the corresponding address acknowledge in parallel, all others ignore the I²C-bus transfer. After acknowledgement, one or more command words follow, which define the status of the addressed slaves. A command word consists of a control byte, which defines Co and RS, plus a data byte (see Figure 19 and Table 11).

The last control byte is tagged with a cleared most significant bit, the continuation bit Co. The control and data bytes are also acknowledged by all addressed slaves on the bus.

After the last control byte, depending on the RS bit setting, either a series of display data bytes or command data bytes may follow. If the RS bit was set logic 1, these display bytes are stored in the display RAM at the address specified by the data pointer.

The data pointer is automatically updated and the data is directed to the intended PCF8531 device. If the RS bit of the last control byte was set logic 0, these command bytes will be decoded and the setting of the device will be changed according to the received commands. The acknowledgement after each byte is made only by the addressed PCF8531. At the end of the transmission, the I²C-bus master issues a STOP condition (P).

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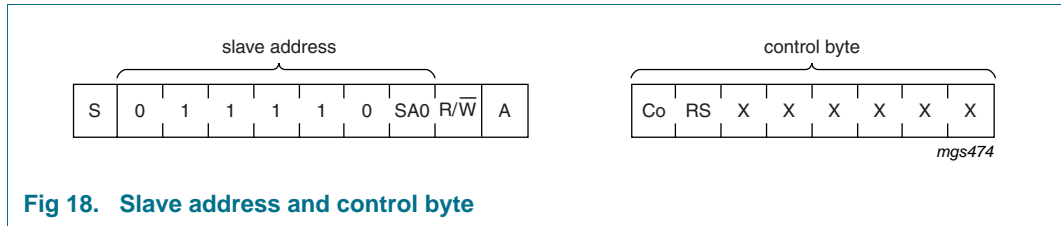
**Fig 18. Slave address and control byte**
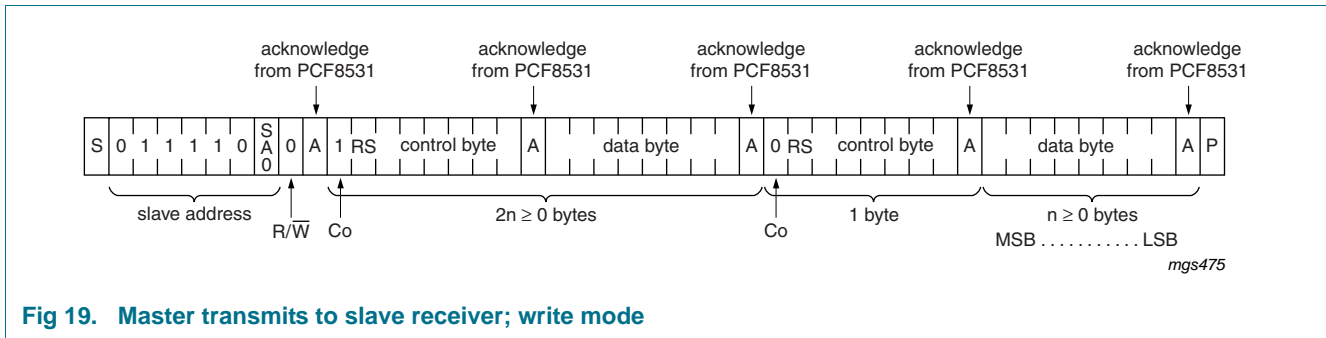


**Fig 19. Master transmits to slave receiver; write mode**

## 10.3 Command decoder

The command decoder identifies command words that arrive on the I$^2$C-bus. The most significant bit of a control byte is the continuation bit Co. If this bit is logic 1, it indicates that only one data byte (either command or RAM data) will follow. If this bit is logic 0, it indicates that a series of data bytes (either command or RAM data) may follow. The DB6 bit of a control byte is the RAM data/command bit RS. When this bit is logic 1, it indicates that another RAM data byte will be transferred next. If the bit is logic 0, it indicates that another command byte will be transferred next.

- Pairs of bytes; information in the second byte, the first byte determines whether information is display or instruction data
- Stream of information bytes after Co = 0; display or instruction data, depending on last RS.

## 11. Internal circuitry



For all diagrams the maximum forward current is 5 mA and the maximum reverse voltage is 5 V.

**Fig 20.  Device protection diagrams**
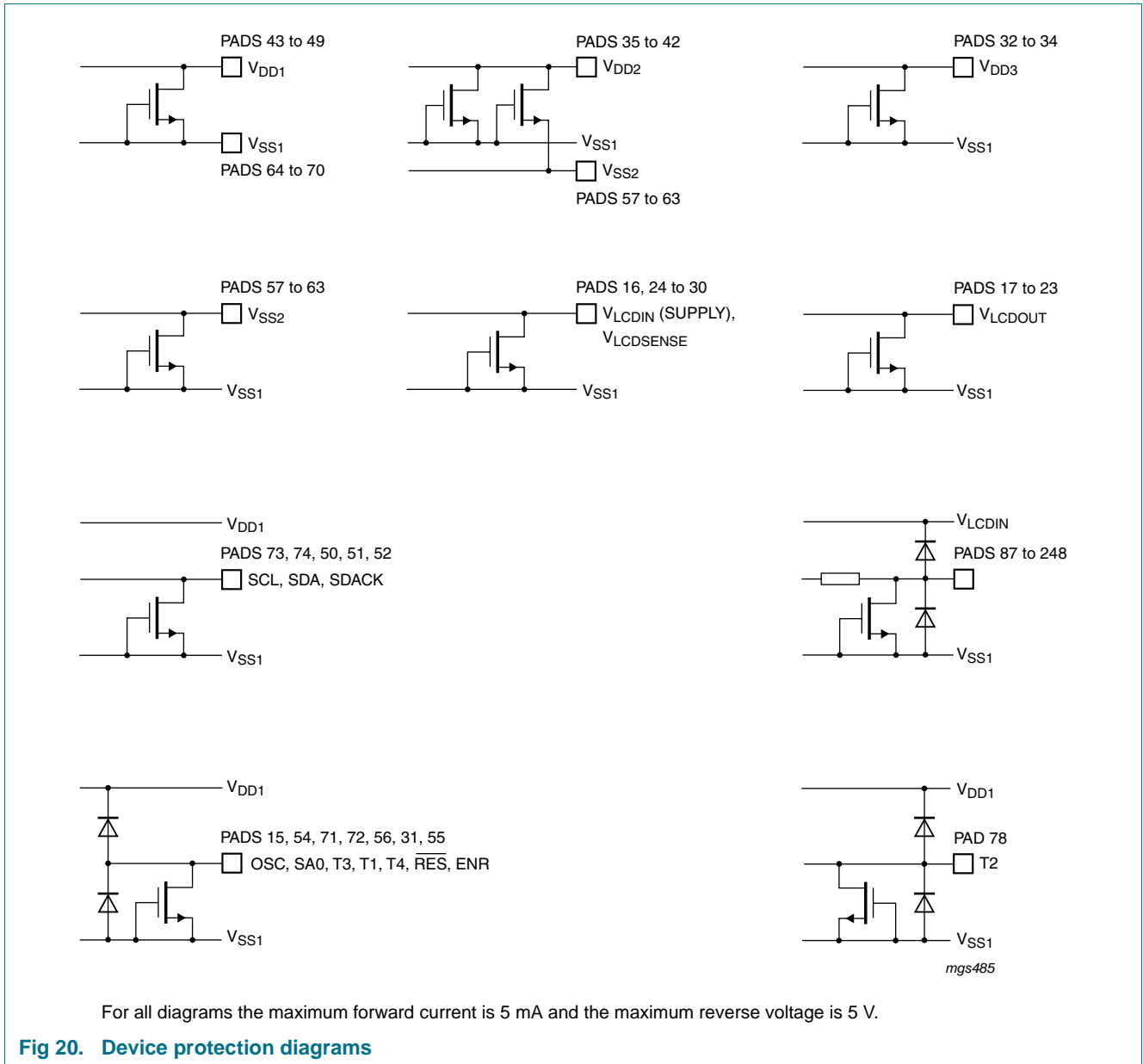
## 12. Limiting values

**Table 14. Limiting values [1]**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DD1}$ | supply voltage 1 | logic supply | | −0.5 | +5.5 | V |
| $V_{DD2}$ | supply voltage 2 | multiplier supply | | −0.5 | +4.5 | V |
| $V_{DD3}$ | supply voltage 3 | multiplier supply | | −0.5 | +4.5 | V |
| $V_{LCD}$ | LCD supply voltage | | | −0.5 | +9.0 | V |
| $V_I$ | input voltage | | | −0.5 | $V_{DD} + 0.5$ | V |
| $V_O$ | output voltage | | | −0.5 | $V_{DD} + 0.5$ | V |
| $I_{DD(LCD)}$ | LCD supply current | | | −50 | +50 | mA |
| $I_{SS}$ | ground supply current | | | −50 | +50 | mA |
| $I_I$ | input current | | | −10 | +10 | mA |
| $I_O$ | output current | | | −10 | +10 | mA |
| $P_{tot}$ | total power dissipation | | | - | 300 | mW |
| P/out | power dissipation per output | | | - | 30 | mW |
| $V_{ESD}$ | electrostatic discharge voltage | HBM | [2] | - | ±1500 | V |
| | | MM | [3] | - | ±200 | V |
| $I_{lu}$ | latch-up current | | [4] | - | 200 | mA |
| $T_j$ | junction temperature | | | - | +150 | °C |
| $T_{stg}$ | storage temperature | | [5] | −65 | +150 | °C |
| $T_{amb}$ | ambient temperature | operating device | | −40 | +85 | °C |

[1] Parameters are valid over the whole operating temperature range unless otherwise specified. All voltages are referenced to $V_{SS}$ unless otherwise specified.

[2] Pass level; Human Body Model (HBM), according to Ref. 6 "JESD22-A114".

[3] Pass level; Machine Model (MM), according to Ref. 7 "JESD22-A115".

[4] Pass level; latch-up testing according to Ref. 8 "JESD78" at maximum ambient temperature ($T_{amb(max)}$).

[5] According to the NXP store and transport requirements (see Ref. 10 "NX3-00092") the devices have to be stored at a temperature of +8 °C to +45 °C and a humidity of 25 % to 75 %. For long term storage products deviant conditions are described in that document.

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## 13. Static characteristics

**Table 15.   Static characteristics**

$V_{DD1}$ = 1.8 V (1.9 V) to 5.5 V; $V_{DD2}$ and $V_{DD3}$ = 2.5 V to 4.5 V; $V_{SS1}$ = $V_{SS2}$ = 0 V; $V_{DD1}$ to $V_{DD3}$ ≤ $V_{LCD}$ ≤ 9.0 V; $T_{amb}$ = −40 °C to +85 °C; unless otherwise specified.

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **Supplies** | | | | | | | |
| $V_{LCD}$ | LCD supply voltage | | [1] | 4.0 | - | 9.0 | V |
| | | icon mode | [1] | 3.0 | - | 9.0 | V |
| $V_{DD1}$ | supply voltage 1 | logic supply | | 1.9 | - | 5.5 | V |
| | | $T_{amb}$ ≥ −25 °C | | 1.8 | - | 5.5 | V |
| $V_{DD2}$ | supply voltage 2 | multiplier supply; LCD voltage internally generated | | 2.5 | - | 4.5 | V |
| $V_{DD3}$ | supply voltage 3 | multiplier supply; LCD voltage internally generated | | 2.5 | - | 4.5 | V |
| $I_{DD}$ | supply current | power-down mode; internal $V_{LCD}$ | | - | 2 | 10 | μA |
| | | normal mode; internal $V_{LCD}$ | [2][3] | - | 170 | 350 | μA |
| | | normal mode; external $V_{LCD}$ | [2] | - | 10 | 50 | μA |
| $I_{DD(LCD)}$ | LCD supply current | normal mode; external $V_{LCD}$ | [2][4] | - | 25 | 100 | μA |
| | | icon mode; external $V_{LCD}$ | [2][5] | - | 15 | 70 | μA |
| $V_{POR}$ | power-on reset voltage | | [6] | 0.9 | 1.2 | 1.6 | V |
| **Logic** | | | | | | | |
| $V_{IL}$ | LOW-level input voltage | | | $V_{SS}$ | - | 0.3$V_{DD}$ | V |
| $V_{IH}$ | HIGH-level input voltage | | | 0.7$V_{DD}$ | - | $V_{DD}$ | V |
| $I_{OL(SDA)}$ | LOW-level output current on pin SDA | $V_{OL}$ = 0.4 V; $V_{DD}$ = 5.0 V | | 3.0 | - | - | mA |
| $I_{LI}$ | input leakage current | $V_I$ = $V_{DD}$ or $V_{SS}$ | | −1 | - | +1 | μA |
| **Column and row outputs** | | | | | | | |
| $R_O$ | output resistance | column outputs: C0 to C127 | [7] | - | 12 | 20 | kΩ |
| | | row outputs: R0 to R33 | | - | 12 | 20 | kΩ |
| $ΔV_{bias}$ | bias voltage variation | outputs R0 to R33 and C0 to C127 | | −100 | 0 | +100 | mV |
| $ΔV_{LCD}$ | LCD voltage variation | $TC_1$ to $TC_7$ | [8] | - | - | ±3.9 | % |
| TC | temperature coefficient | $T_{amb}$ = −20 °C to +70 °C | | | | | |
| | | $TC_0$; TC[2:0] = 000 | | - | 0 | - | %/K |
| | | $TC_1$; TC[2:0] = 001 | | - | −0.026 | - | %/K |
| | | $TC_2$; TC[2:0] = 010 | | - | −0.039 | - | %/K |
| | | $TC_3$; TC[2:0] = 011 | | - | −0.052 | - | %/K |
| | | $TC_4$; TC[2:0] = 100 | | - | −0.078 | - | %/K |
| | | $TC_5$; TC[2:0] = 101 | | - | −0.13 | - | %/K |
| | | $TC_6$; TC[2:0] = 110 | | - | −0.19 | - | %/K |
| | | $TC_7$; TC[2:0] = 111 | | - | −0.26 | - | %/K |
| $T_{ints}$ | intersection temperature | | | - | 27 | - | °C |

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[1] As the programming range for the internally generated $V_{LCD}$ allows values above the maximum allowed $V_{LCD}$, the user must ensure, while setting the VOP register and selecting the temperature compensation, that the $V_{LCD}$ maximum limit of 9 V will never be exceeded under all conditions and including all tolerances.

[2] LCD outputs are open circuit, inputs at $V_{DD}$ or $V_{SS}$; bus inactive.

[3] $V_{DD1}$ to $V_{DD3}$ = 2.85 V; $V_{LCD}$ = 7.0 V; voltage multiplier = 3 × $V_{DD}$; $f_{osc}$ = 34 kHz.

[4] $V_{DD1}$ to $V_{DD3}$ = 2.75 V; $V_{LCD}$ = 9.0 V; $f_{osc}$ = 34 kHz.

[5] $V_{DD1}$ to $V_{DD3}$ = 2.75 V; $V_{LCD}$ = 3.5 V; $f_{osc}$ = 34 kHz.

[6] Resets all logic when $V_{DD1} < V_{POR}$.

[7] $I_{load} \le 50$ μA; outputs are tested one at a time.

[8] $V_{LCD} \le 7.7$ V.

# 14. Dynamic characteristics

**Table 16. Dynamic characteristics**

$V_{DD1}$ = 1.8 V (1.9 V) to 5.5 V; $V_{DD2}$ and $V_{DD3}$ = 2.5 V to 4.5 V; $V_{SS1} = V_{SS2}$ = 0 V; $V_{DD1}$ to $V_{DD3} \le V_{LCD} \le 9.0$ V; $T_{amb}$ = −40 °C to +85 °C; unless otherwise specified.

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $f_{fr(LCD)}$ | LCD frame frequency | $V_{DD}$ = 3.0 V | [1] | 40 | 66 | 135 | Hz |
| $f_{osc}$ | oscillator frequency | | | 20 | 34 | 65 | kHz |
| $f_{clk(ext)}$ | external clock frequency | | | 20 | - | 65 | kHz |
| $t_{w(RESL)}$ | RES LOW pulse width | | [2] | 300 | - | - | ns |
| $t_{su(RESL)}$ | RES LOW set-up time | | | - | - | 30 | μs |
| **Serial bus interface (see Figure 22)[3]** | | | | | | | |
| $f_{SCL}$ | SCL clock frequency | | | 0 | - | 400 | kHz |
| $t_{LOW}$ | LOW period of the SCL clock | | | 1.3 | - | - | μs |
| $t_{HIGH}$ | HIGH period of the SCL clock | | | 0.6 | - | - | μs |
| $t_{SU;DAT}$ | data set-up time | | | 100 | - | - | ns |
| $t_{HD;DAT}$ | data hold time | | | 0 | - | 0.9 | ns |
| $t_r$ | rise time of both SDA and SCL signals | | [4] | $20 + 0.1C_b$ | - | 0.3 | μs |
| $t_f$ | fall time of both SDA and SCL signals | | [4] | $20 + 0.1C_b$ | - | 0.3 | μs |
| $C_b$ | capacitive load for each bus line | | | - | - | 400 | pF |
| $t_{SU;STA}$ | set-up time for a repeated START condition | | | 0.6 | - | - | μs |
| $t_{HD;STA}$ | hold time (repeated) START condition | | | 0.6 | - | - | μs |
| $t_{SU;STO}$ | set-up time for STOP condition | | | 0.6 | - | - | μs |
| $t_{SP}$ | pulse width of spikes that must be suppressed by the input filter | on bus | | - | - | 50 | ns |
| $t_{BUF}$ | bus free time between a STOP and START condition | | | 1.3 | - | - | μs |

[1] $f_{fr} = f_{clk(ext)}/480$ or $f_{osc}/480$.

[2] A reset is generated if $t_{w(RESL)} > 3$ ns (see Figure 21).

[3] All timing values are valid within the operating supply voltage and ambient temperature range and are referenced to $V_{IL}$ and $V_{IH}$, with an input voltage swing of $V_{SS}$ to $V_{DD}$.

[4] $C_b$ = total capacitance of one bus line in pF.
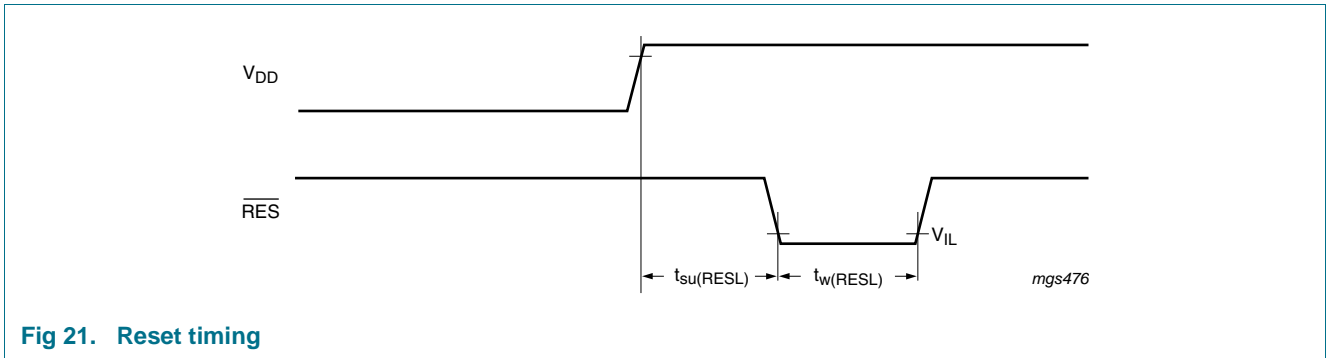
**Fig 21. Reset timing**
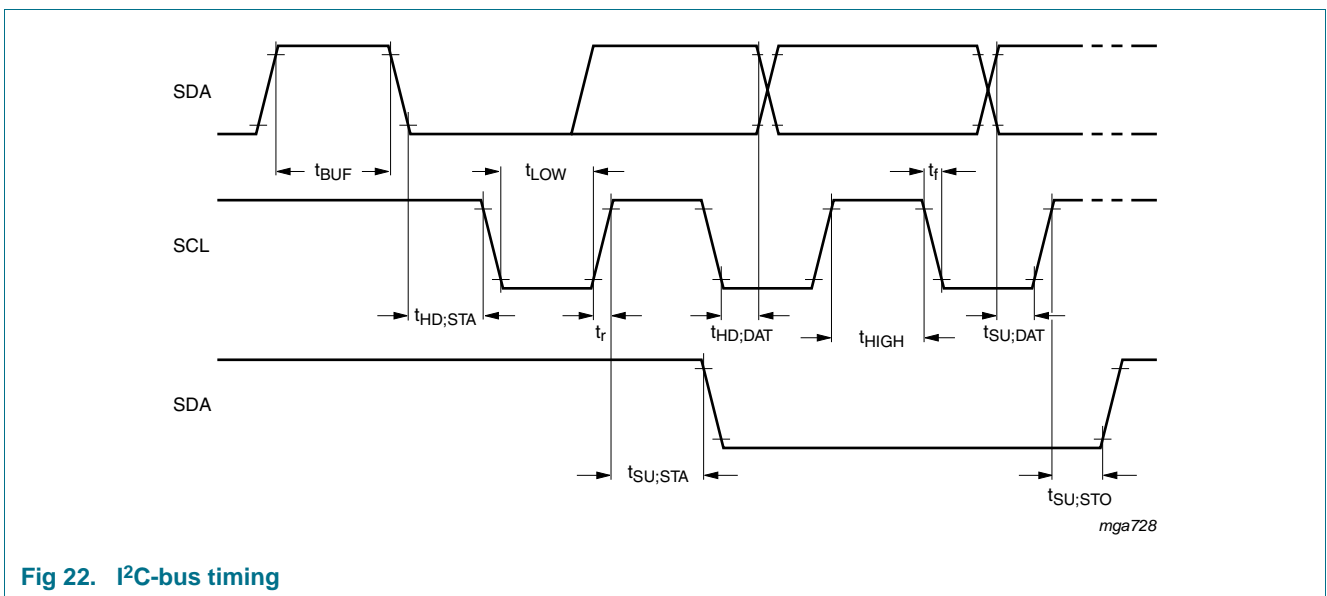


**Fig 22. I²C-bus timing**
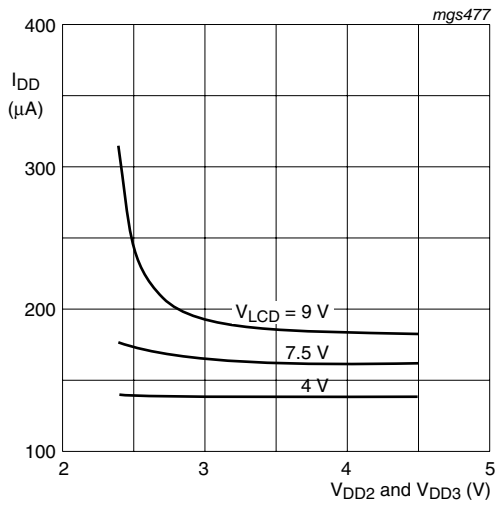
$V_{DD1}$ = 2 V; 4 × voltage multiplier; $T_{amb}$ = 27 °C; TC = 0;
BS = 100; no $V_{LCD}$ load.

**Fig 23.** **Supply current as a function of supply voltage 2 and supply voltage 3**
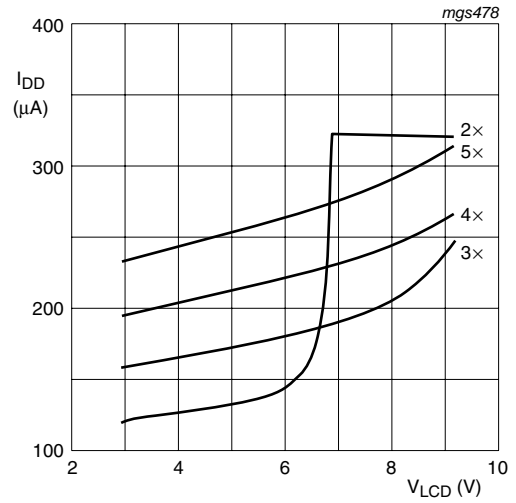


$V_{DD1}$ = 1.8 V; $V_{DD2}$ and $V_{DD3}$ = 2.6 V; $T_{amb}$ = 27 °C;
$f_{osc}$ = 34 kHz; no $V_{LCD}$ load.

**Fig 24.** **Supply current as a function of LCD supply voltage; different multiplication factors**
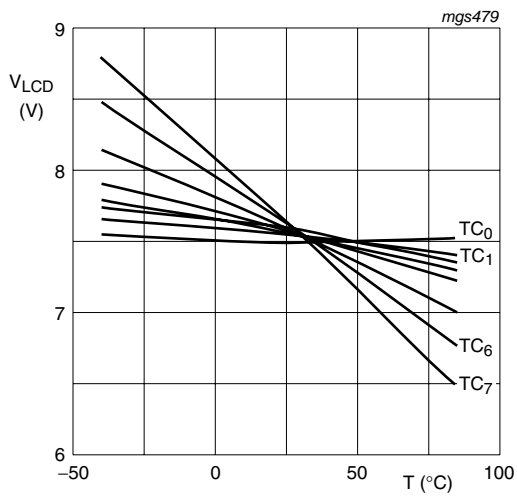


$V_{LCD}$ = 7.5 V; $V_{DD1}$ to $V_{DD3}$ = 2.7 V; $T_{amb}$ = 27 °C;
no $V_{LCD}$ load.

**Fig 25.** **LCD supply voltage as a function of temperature**
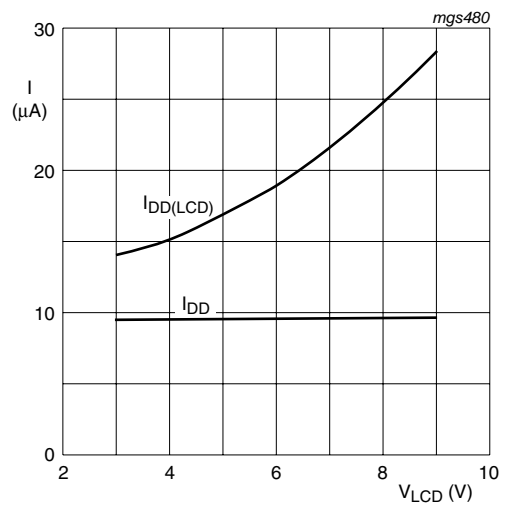


$V_{DD1}$ = 1.8 V; $V_{DD2}$ and $V_{DD3}$ = 2.5 V; external $V_{LCD}$;
$T_{amb}$ = 27 °C; TC = 0; BS = 100; no $V_{LCD}$ load.

**Fig 26.** **Supply current as a function of LCD supply voltage**
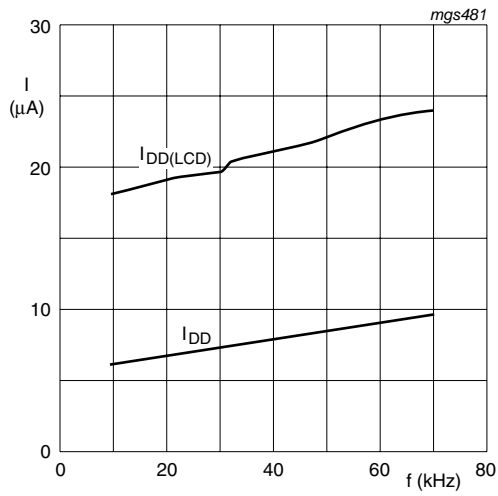
$V_{DD1}$ = 2.5 V; $V_{DD2}$ and $V_{DD3}$ = 2.5 V; external $V_{LCD}$;
$T_{amb}$ = 27 °C; TC = 0; BS = 100; no $V_{LCD}$ load.

**Fig 27.  Supply current as a function of frequency**
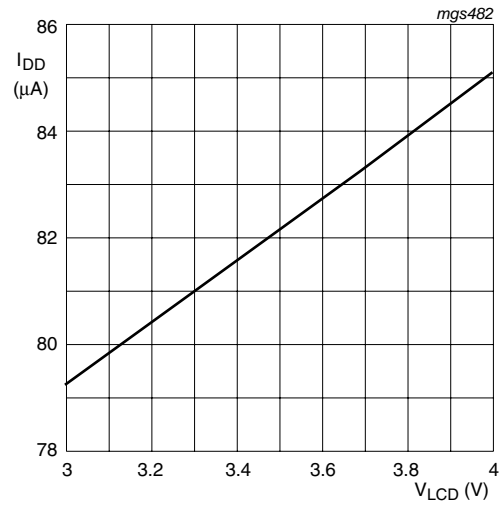


$V_{DD1}$ = 1.8 V; $V_{DD2}$ = 2.5 V; 2 × voltage multiplier;
$T_{amb}$ = 27 °C; TC = 0; BS = 111; no $V_{LCD}$ load.

**Fig 28.  Supply current as a function of LCD supply voltage**

# 15. Application information

## 15.1 Typical system configuration
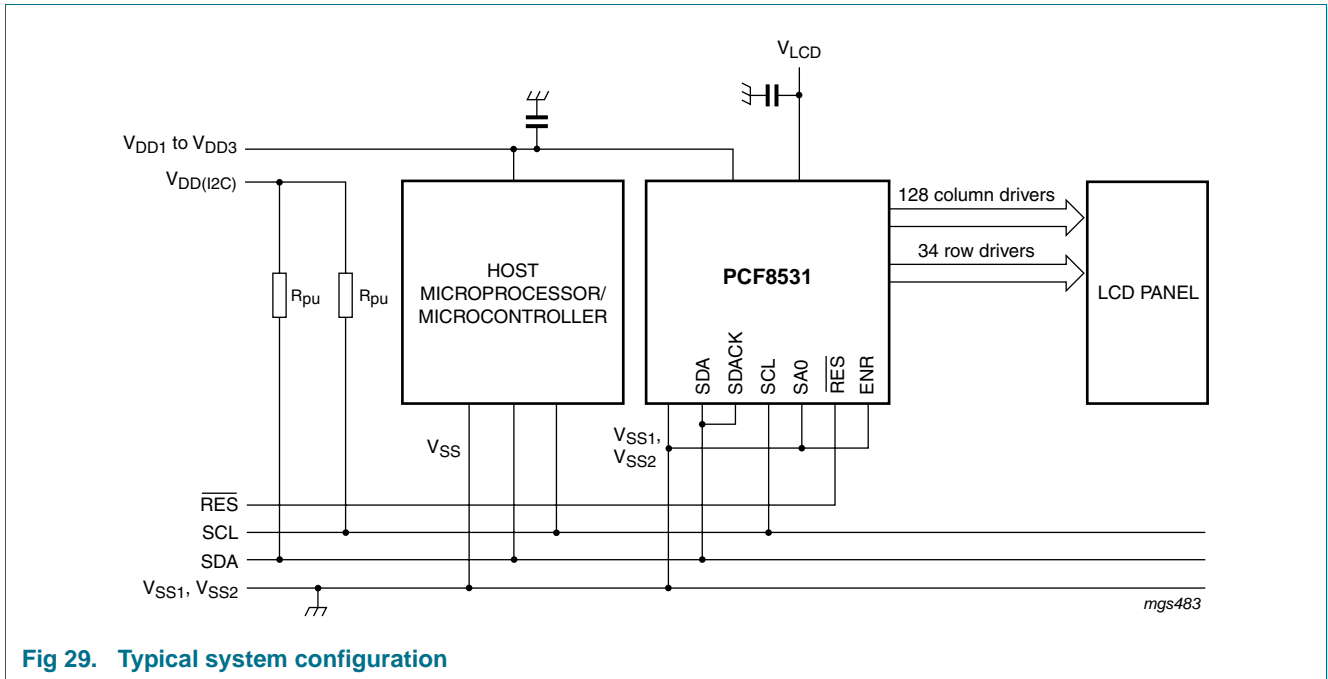


**Fig 29. Typical system configuration**

The host microprocessor/microcontroller and the PCF8531 are both connected to the I2C-bus. The SDA and SCL lines must be connected to the positive power supply via pull-up resistors. The internal oscillator requires no external components. The appropriate intermediate biasing voltage for the multiplexed LCD waveforms are generated on-chip. The only other connections required to complete the system are to the power supplies ($V_{DD}$, $V_{SS}$, and $V_{LCD}$) and suitable capacitors for decoupling $V_{LCD}$ and $V_{DD}$.

## 15.2 Power supply connections for internal $V_{LCD}$ generation
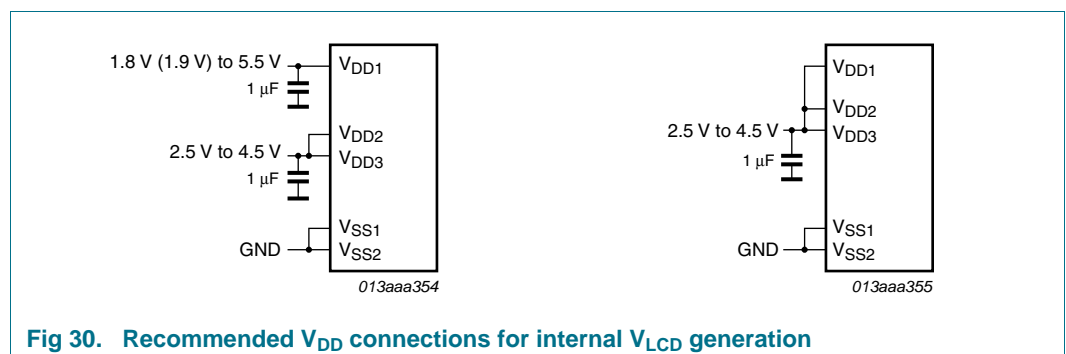


**Fig 30. Recommended $V_{DD}$ connections for internal $V_{LCD}$ generation**
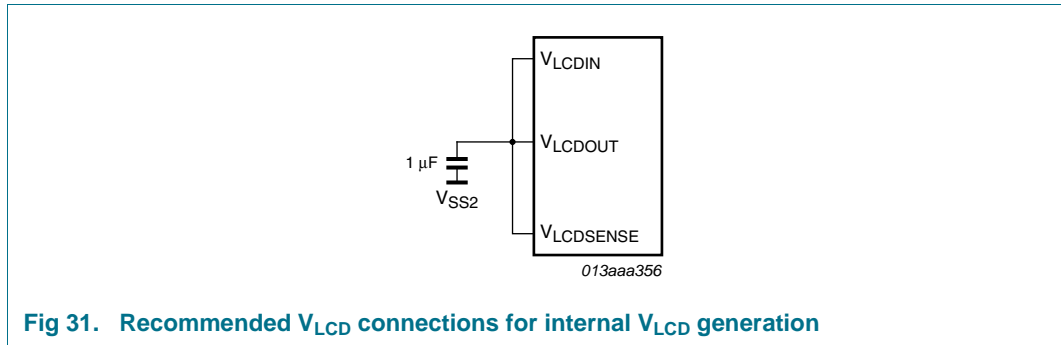
**Fig 31. Recommended $V_{LCD}$ connections for internal $V_{LCD}$ generation**

## 15.3 Power supply connections for external $V_{LCD}$ generation
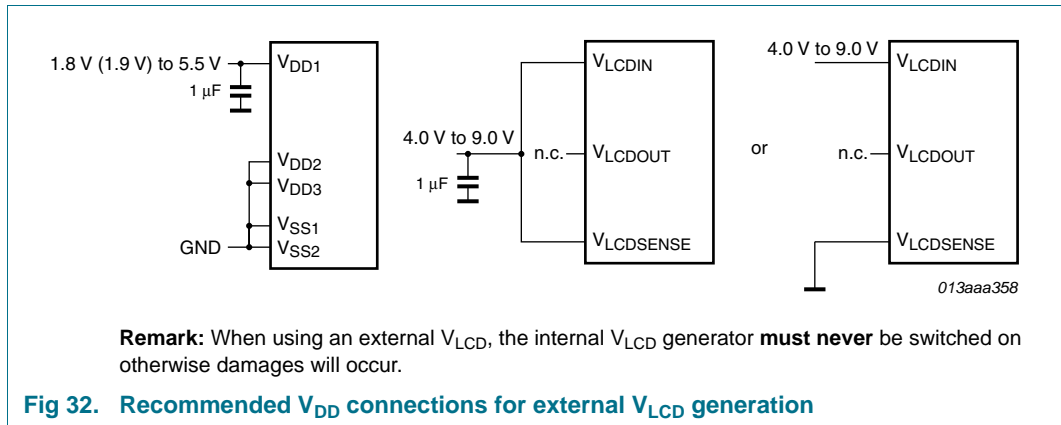


**Remark:** When using an external $V_{LCD}$, the internal $V_{LCD}$ generator **must never** be switched on otherwise damages will occur.

**Fig 32. Recommended $V_{DD}$ connections for external $V_{LCD}$ generation**

## 15.4 Information about $V_{LCD}$ connections

**$V_{LCDIN}$** — This input is used for generating the 5 LCD bias levels. It is the power supply for the bias level buffers.

**$V_{LCDOUT}$** — This is the $V_{LCD}$ output if $V_{LCD}$ is generated internally. It is the output of the charge pump. In this case pin $V_{LCDOUT}$ must be connected to $V_{LCDIN}$ and to $V_{LCDSENSE}$ (see Figure 31). $V_{LCDOUT}$ must be left open circuit when $V_{LCD}$ is supplied from an external source (see Figure 32).

**$V_{LCDSENSE}$** — When using the internal $V_{LCD}$ generation, this pin must be connected to $V_{LCDOUT}$ and $V_{LCDIN}$ (see Figure 31). When using an external $V_{LCD}$ supply it must be connected to $V_{LCDIN}$ or to ground (see Figure 32).

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### 15.5 Chip-on-glass application
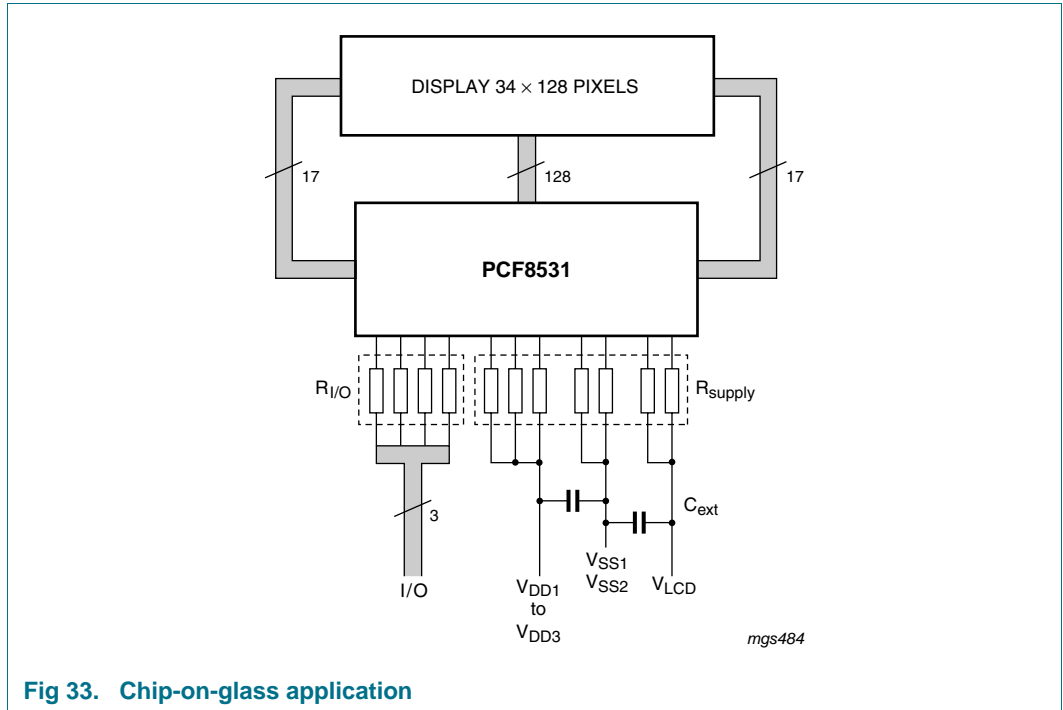


**Fig 33. Chip-on-glass application**

The required minimum values for the external capacitors in a chip-on-glass application are:

- $C_{ext}$ = 100 nF between $V_{LCD}$ and $V_{SS1}$, $V_{SS2}$; $C_{ext}$ = 470 nF between $V_{DD1}$, $V_{DD2}$, $V_{DD3}$ and $V_{SS1}$, $V_{SS2}$.
- Higher capacitor values are recommended for ripple reduction.
- For COG applications, the recommended ITO track resistance must be minimized for the I/O and supply connections. Optimized values for these tracks are below 50 $\Omega$ for the supply ($R_{supply}$) and below 100 $\Omega$ for the I/O connections ($R_{I/O}$).
- To reduce the sensitivity of the reset to ESD/EMC disturbances for a COG application, NXP strongly recommended implementing a series input resistance in the reset line (recommended minimum value 8 k$\Omega$) on the glass (ITO). If the reset input is not used, this input must be connected to $V_{DD1}$ using a short connection.

## 15.6 Programming example

**Table 17. Programming example for PCF8531**

| Step | Serial bus byte | | | | | | | | Display | Operation |
|------|-----|-----|-----|-----|-----|-----|-----|-----|---------|-----------|
| | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | | |
| 1 | 0 | 1 | 1 | 1 | 1 | 0 | SA0 | 0 | | start; slave address; R/$\overline{W}$ = 0 |
| 2 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | control byte; Co = 1; RS = 0 |
| 3 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | | H[1:0] independent command; select function and RAM command page (H[1:0] = 00) |
| 4 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | control byte; Co = 1; RS = 0 |
| 5 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | | function and RAM command page PD = 0 and V = 1 |
| 6 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | control byte; Co = 1; RS = 0 |
| 7 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | | function and RAM command page select display setting command page H[1:0] = 01 |
| 8 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | control byte; Co = 1; RS = 0 |
| 9 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | | display setting command page; set normal mode (D = 1; IM = 0 and E = 0) |
| 10 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | control byte; Co = 1; RS = 0 |
| 11 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | | select multiplex rate 1:34 |
| 12 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | control byte; Co = 1; RS = 0 |
| 13 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | | H[2:0] independent command; select function and RAM command page H[1:0] = 00 |
| 14 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | control byte; Co = 1; RS = 0 |
| 15 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | | function and RAM command page; select HV-gen command page H[1:0] = 10 |
| 16 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | control byte; Co = 1; RS = 0 |
| 17 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | | HV-gen command page; select voltage multiplication factor 5 S[1:0] = 11 |
| 18 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | control byte; Co = 1; RS = 0 |
| 19 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | | HV-gen command page; select temperature coefficient 2 TC[2:0] = 010 |
| 20 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | control byte; Co = 1; RS = 0 |
| 21 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | | HV-gen command page; select high $V_{LCD}$ programming range (PRS = 1); voltage multiplier off (HVE = 1) |
| 22 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | control byte; Co = 1; RS = 0 |

**Table 17.** **Programming example for PCF8531** *…continued*
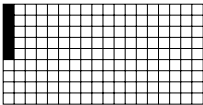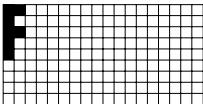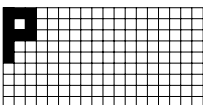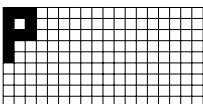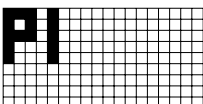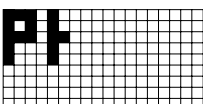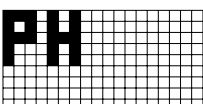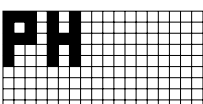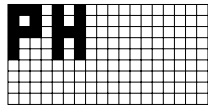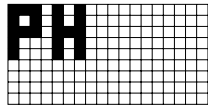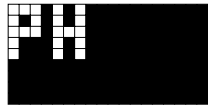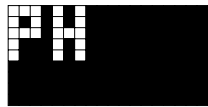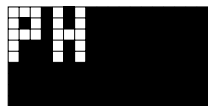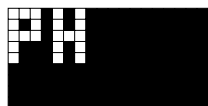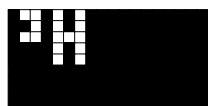
| Step | Serial bus byte | | | | | | | | Display | Operation |
|---|---|---|---|---|---|---|---|---|---|---|
| | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | | |
| 23 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | | HV-gen command page; set $V_{LCD}$ = 7.71 V; VOP[6:0] = 0100000 |
| 24 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | | control byte; Co = 0; RS = 1 |
| 25 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | mgs405 | data write; Y and X are initialized to 0 by default, so they are not set here |
| 26 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | mgs406 | data write |
| 27 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | mgs407 | data write |
| 28 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | mgs407 | data write |
| 29 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | mgs409 | data write |
| 30 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | mgs410 | data write |
| 31 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | mgs411 | data write; last data and stop transmission |
| 32 | 0 | 1 | 1 | 1 | 1 | 0 | SA0 | 0 | mgs411 | repeated start; slave address; R/$\overline{W}$ = 0 |

**Table 17.  Programming example for PCF8531** *…continued*

| Step | Serial bus byte | | | | | | | | Display | Operation |
|------|-----|-----|-----|-----|-----|-----|-----|-----|---------|-----------|
| | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | | |
| 33 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | mgs411 | control byte; Co = 1; RS = 0 |
| 34 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | | H[1:0] independent command; select function and RAM command page H[1:0] = 00 |
| 35 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | control byte; Co = 1; RS = 0 |
| 36 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | mgs411 | function and RAM command page; select display setting command page H[1:0] = 01 |
| 37 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | control byte; Co = 1; RS = 0 |
| 38 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | | H[1:0] independent command; select function and RAM command page H[1:0] = 00 |
| 39 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | control byte; Co = 1; RS = 0 |
| 40 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | mgs412 | display control; set inverse video mode (D = 1; E = 1 and IM = 0) |
| 41 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | mgs412 | control byte; Co = 1; RS = 0 |
| 42 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | mgs412 | set X address of RAM; set address to '0000000' |
| 43 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | mgs412 | control byte; Co = 0; RS = 1 |
| 44 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | mgs414 | data write |

## 16. Package outline

Not applicable.

## 17. Handling information

All input and output pins are protected against ElectroStatic Discharge (ESD) under normal handling. When handling Metal-Oxide Semiconductor (MOS) devices ensure that all normal precautions are taken as described in *JESD625-A*, *IEC 61340-5* or equivalent standards.

## 18. Packing information

**Table 18. Tray dimensions (see Figure 34)**

| Symbol | Description | Value |
|--------|-------------|-------|
| A | pocket pitch in x direction | 13.72 mm |
| B | pocket pitch in y direction | 4.17 mm |
| C | pocket width in x direction | 12.34 mm |
| D | pocket width in y direction | 2.05 mm |
| E | tray width in x direction | 50.8 mm |
| F | tray width in y direction | 50.8 mm |
| x | number of pockets, x direction | 3 |
| y | number of pockets, y direction | 10 |



**Fig 34. Tray details**

The orientation of the IC in a pocket is indicated by the position of the IC type name on the die surface with respect to the chamfer on the upper left corner of the tray. Refer to the bonding pad location diagram (Figure 2) for the orientation and position of the type name on the die surface.

**Fig 35.  Tray alignment**
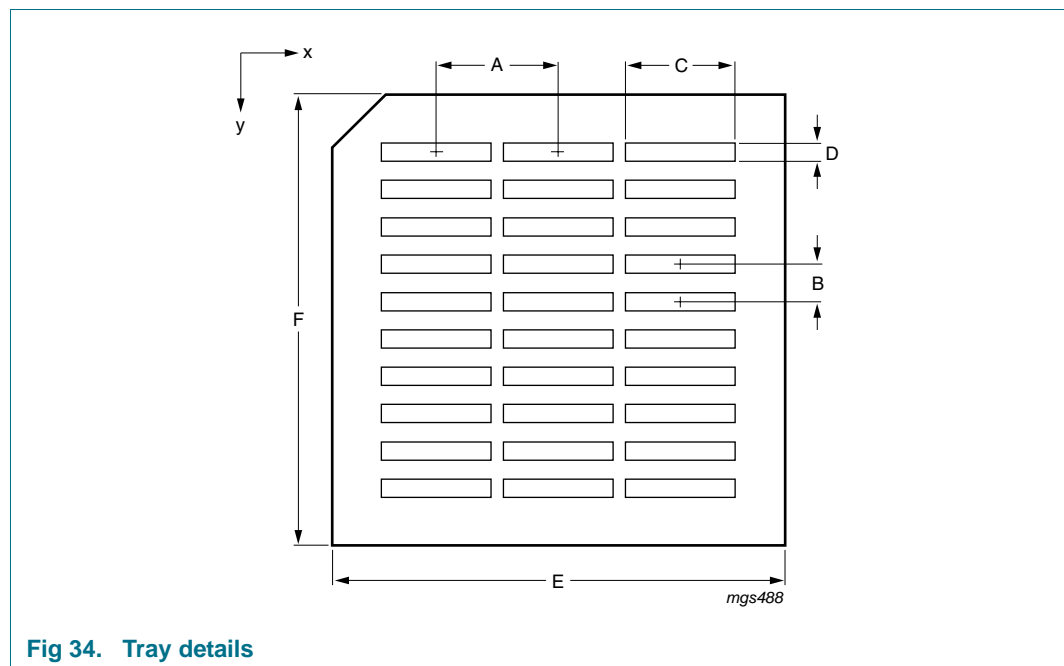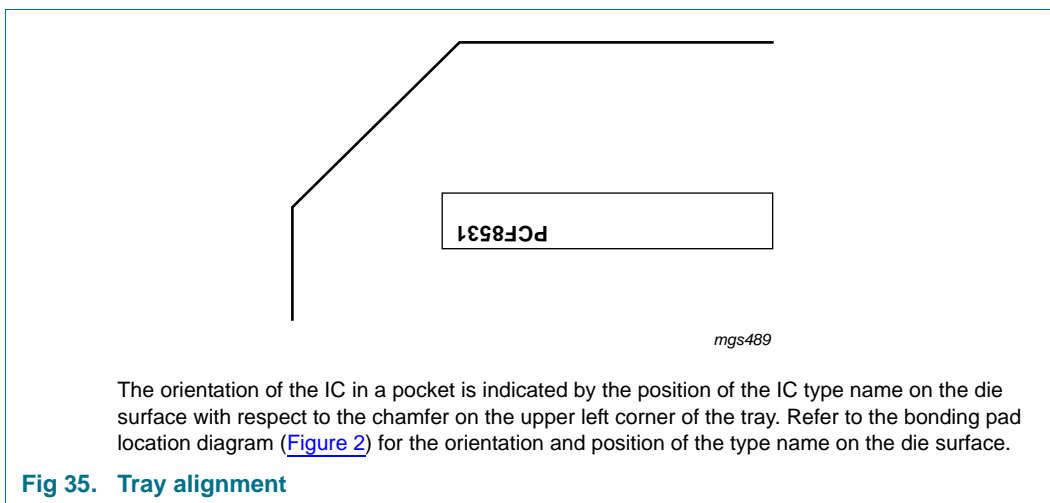
# 19. Abbreviations

**Table 19.   Abbreviations**

| Acronym | Description |
|---------|-------------|
| CDM | Charged Device Model |
| CMOS | Complementary Metal-Oxide Semiconductor |
| COG | Chip-On-Glass |
| DDRAM | Double Data Random Access Memory |
| EMC | ElectroMagnetic Compatibility |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| HV | High Voltage |
| IC | Integrated Circuit |
| ITO | Indium Tin Oxide |
| LCD | Liquid Crystal Display |
| LSB | Least Significant Bit |
| MM | Machine Model |
| MPU | MicroProcessor Unit |
| POR | Power-On Reset |
| RAM | Random Access Memory |
| RC | Resistance-Capacitance |
| TC | Temperature Coefficient |
| SCL | Serial CLock line |
| SDA | Serial DAta line |

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## 20. References

**[1]** **AN10170 —** Design guidelines for COG modules with NXP monochrome LCD drivers

**[2]** **AN10706 —** Handling bare die

**[3]** **AN10853 —** ESD and EMC sensitivity of IC

**[4]** **IEC 60134 —** Rating systems for electronic tubes and valves and analogous semiconductor devices

**[5]** **IEC 61340-5 —** Protection of electronic devices from electrostatic phenomena

**[6]** **JESD22-A114 —** Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)

**[7]** **JESD22-A115 —** Electrostatic Discharge (ESD) Sensitivity Testing Machine Model (MM)

**[8]** **JESD78 —** IC Latch-Up Test

**[9]** **JESD625-A —** Requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices

**[10]** **NX3-00092 —** NXP store and transport requirements

**[11]** **UM10204 —** $I^2C$-bus specification and user manual

## 21. Revision history

**Table 20.  Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| PCF8531 v.6 | 20110516 | Product data sheet | - | PCF8531 v.5 |
| Modifications: | • Specified for product type PCF8531U/2DA/1 | | | |
| PCF8531 v.5 | 20100810 | Product data sheet | - | PCF8531_4 |
| PCF8531_4 | 20080613 | Product data sheet | - | PCF8531_3 |
| PCF8531_3 | 20000211 | Product data sheet | - | PCF8531_2 |
| PCF8531_2 | 19990810 | Product data sheet | - | PCF8531_SDS_1 |
| PCF8531_SDS_1 | 19990322 | Product data sheet | - | - |

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### 22.1 Data sheet status

| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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