Xicor®

1M **X28C010** **128K x 8 Bit**

5 Volt, Byte Alterable E²PROM   F46-13-27

FEATURES

- **Access Time: 120 ns**
- **SIMPLE Byte and Page Write**
  - **—Single 5 Volt Supply**
  - **—No External High Voltages or V_{PP} Control Circuits**
  - **—Self Timed**
    - **—No Erase Before Write**
    - **—No Complex Programming Algorithms**
    - **—No Overerase Problem**
- **Low Power CMOS:**
  - **—Active: 50mA**
  - **—Standby: 500µA**
- **Software Data Protection**
  - **—Protects Data Against System Level Inadvertant Writes**
- **High Speed Page Write Capability**
- **Highly Reliable Direct Write™ Cell**
  - **—Endurance: 10,000 Write Cycles**
  - **—Data Retention: 100 Years**
- **Early End of Write Detection**
  - **—$\overline{DATA}$ Polling**
  - **—Toggle Bit Polling**

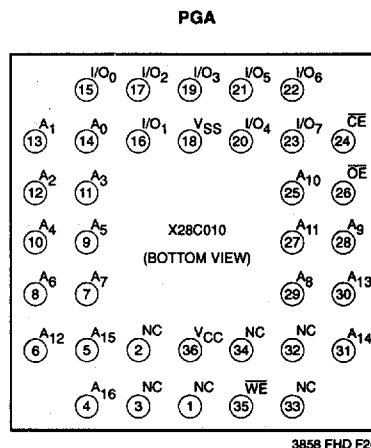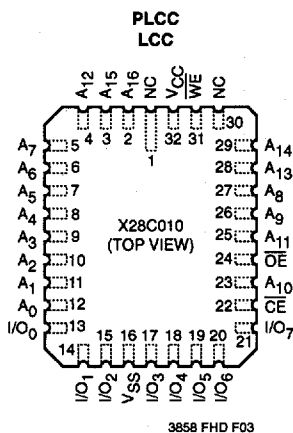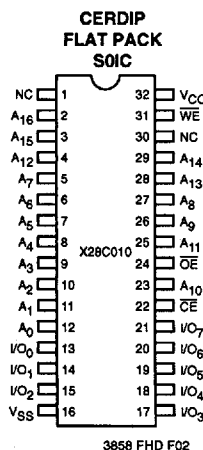## DESCRIPTION

The Xicor X28C010 is a 128K x 8 E²PROM, fabricated with Xicor's proprietary, high performance, floating gate CMOS technology. Like all Xicor programmable non-volatile memories the X28C010 is a 5V only device. The X28C010 features the JEDEC approved pinout for byte-wide memories, compatible with industry standard EPROMs.

The X28C010 supports a 256-byte page write operation, effectively providing a 19 µs/byte write cycle and enabling the entire memory to be typically written in less than 2.5 seconds. The X28C010 also features $\overline{DATA}$ Polling and Toggle Bit test, system software support schemes used to indicate the early completion of a write cycle. In addition, the X28C010 supports Software Data Protection option.

Xicor E²PROMs are designed and tested for applications requiring extended endurance. Data retention is specified to be greater than 100 years.

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PIN CONFIGURATION

3858 FHD F02

3858 FHD F03

3858 FHD F20

Characteristics subject to change without notice

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PIN DESCRIPTIONS

Addresses (A_0–A_{16})

The Address inputs select an 8-bit memory location during a read or write operation.

Chip Enable ($\overline{CE}$)

The Chip Enable input must be LOW to enable all read/write operations. When $\overline{CE}$ is HIGH, power consumption is reduced.

Output Enable ($\overline{OE}$)

The Output Enable input controls the data output buffers and is used to initiate read operations.

Data In/Data Out (I/O_0–I/O_7)

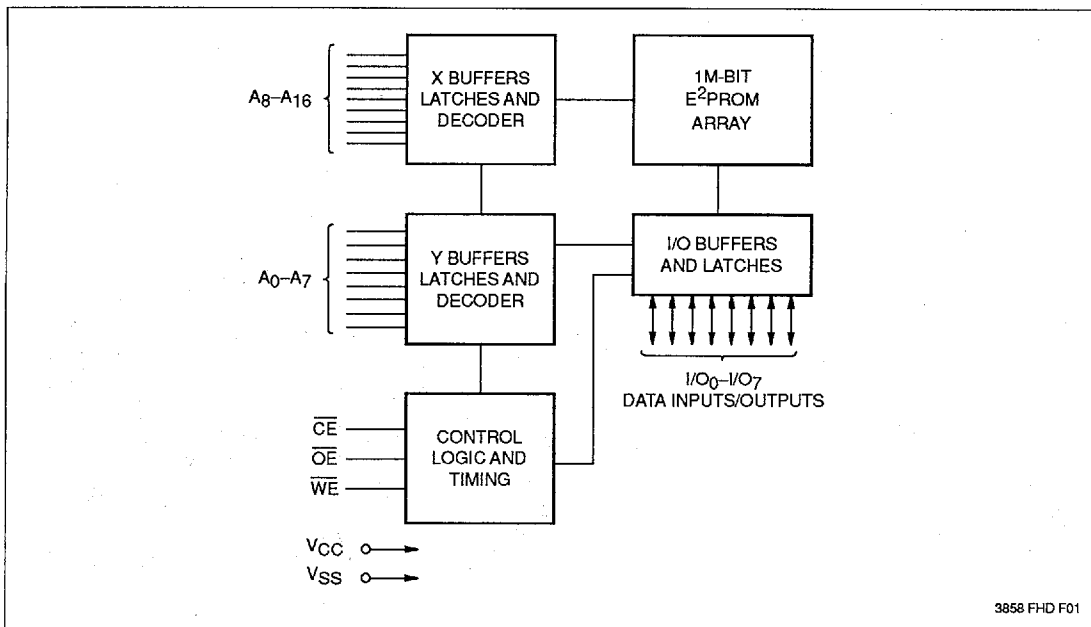Data is written to or read from the X28C010 through the I/O pins.

Write Enable ($\overline{WE}$)

The Write Enable input controls the writing of data to the X28C010.

PIN NAMES

Symbol	Description
A_0–A_{16}	Address Inputs
I/O_0–I/O_7	Data Input/Output
$\overline{WE}$	Write Enable
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
V_{CC}	+5V
V_{SS}	Ground
NC	No Connect

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FUNCTIONAL DIAGRAM

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DEVICE OPERATION

Read

Read operations are initiated by both $\overline{OE}$ and $\overline{CE}$ LOW. The read operation is terminated by either $\overline{CE}$ or $\overline{OE}$ returning HIGH. This 2-line control architecture eliminates bus contention in a system environment. The data bus will be in a high impedance state when either $\overline{OE}$ or $\overline{CE}$ is HIGH.

Write

Write operations are initiated when both $\overline{CE}$ and $\overline{WE}$ are LOW *and* $\overline{OE}$ is HIGH. The X28C010 supports both a $\overline{CE}$ and $\overline{WE}$ controlled write cycle. That is, the address is latched by the falling edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs last. Similarly, the data is latched internally by the rising edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs first. A byte write operation, once initiated, will automatically continue to completion, typically within 5 ms.
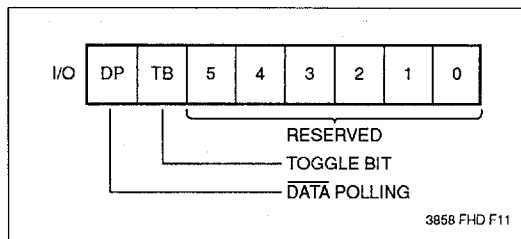
Page Write Operation

The page write feature of the X28C010 allows the entire memory to be written in 5 seconds. Page write allows two to two hundred fifty-six bytes of data to be consecutively written to the X28C010 prior to the commencement of the internal programming cycle. The host can fetch data from another location within the system during a page write operation (change the source address), but the page address (A_8 through A_{16}) for each subsequent valid write cycle to the part during this operation must be the same as the initial page address.

The page write mode can be initiated during any write operation. Following the initial byte write cycle, the host can write an additional one to two hundred fifty-six bytes in the same manner as the first byte was written. Each successive byte load cycle, started by the $\overline{WE}$ HIGH to LOW transition, must begin within 100 µs of the falling edge of the preceding $\overline{WE}$. If a subsequent $\overline{WE}$ HIGH to LOW transition is not detected within 100 µs, the internal automatic programming cycle will commence. There is no page write window limitation. Effectively the page write window is infinitely wide, so long as the host continues to access the device within the byte load cycle time of 100 µs.

Write Operation Status Bits

The X28C010 provides the user two write operation status bits. These can be used to optimize a system write cycle time. The status bits are mapped onto the I/O bus as shown in Figure 1.

Figure 1. Status Bit Assignment


```
I/O | DP | TB | 5 | 4 | 3 | 2 | 1 | 0 |
                 └──────────────────┘
                     RESERVED
              ──────── TOGGLE BIT
         ──────────── DATA POLLING
```
3858 FHD F11

$\overline{DATA}$ Polling (I/O$_7$)

The X28C010 features $\overline{DATA}$ Polling as a method to indicate to the host system that the byte write or page write cycle has completed. $\overline{DATA}$ Polling allows a simple bit test operation to determine the status of the X28C010, eliminating additional interrupt inputs or external hardware. During the internal programming cycle, any attempt to read the last byte written will produce the complement of that data on I/O$_7$ (i.e., write data = 0xxx xxxx, read data = 1xxx xxxx). Once the programming cycle is complete, I/O$_7$ will reflect true data. Note: If the X28C010 is in the protected state and an illegal write operation is attempted $\overline{DATA}$ Polling will not operate.

Toggle Bit (I/O$_6$)

The X28C010 also provides another method for determining when the internal write cycle is complete. During the internal programming cycle I/O$_6$ will toggle from one to zero and zero to one on subsequent attempts to read the device. When the internal cycle is complete the toggling will cease and the device will be accessible for additional read or write operations.

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$\overline{\text{DATA}}$ Polling I/O$_7$
Figure 2. $\overline{\text{DATA}}$ Polling Bus Sequence

3858 FHD F12
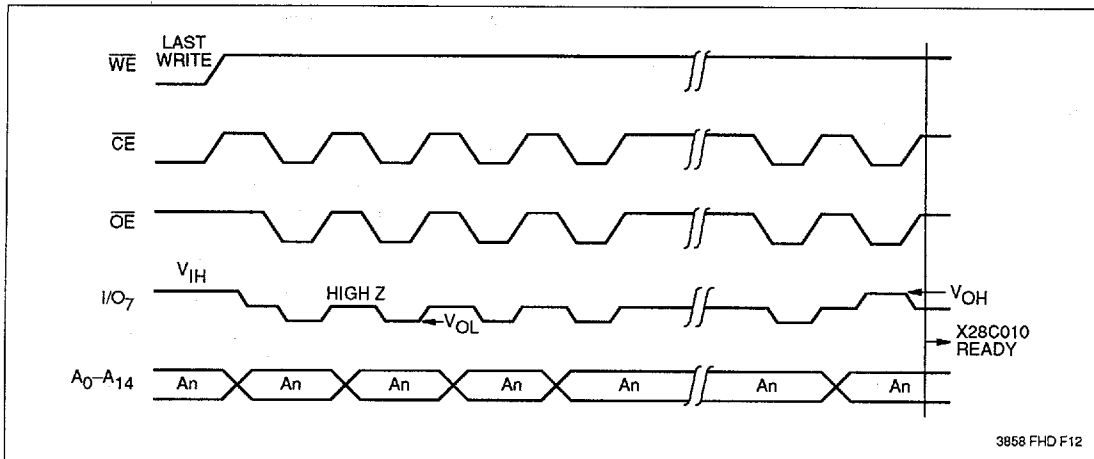
Figure 3. $\overline{\text{DATA}}$ Polling Software Flow

3858 FHD F13
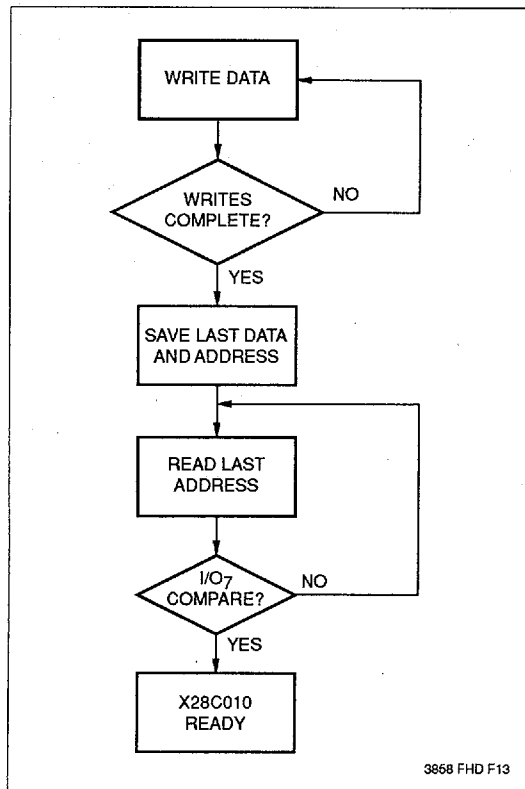
$\overline{\text{DATA}}$ Polling can effectively halve the time for writing to the X28C010. The timing diagram in Figure 2 illustrates the sequence of events on the bus. The software flow diagram in Figure 3 illustrates one method of implementing the routine.

X28C010

The Toggle Bit I/O$_6$
Figure 4. Toggle Bit Bus Sequence

* Beginning and ending state of I/O$_6$ will vary.

3858 FHD F14
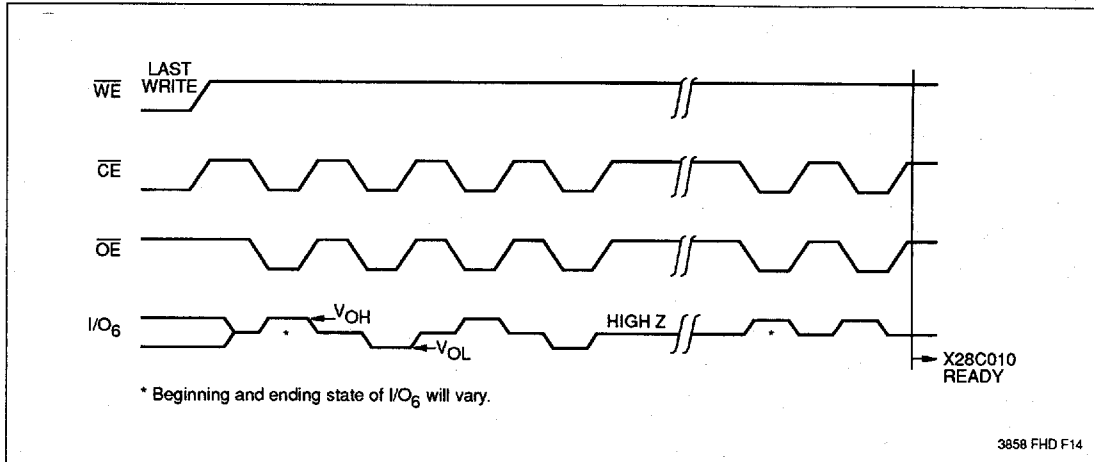
Figure 5. Toggle Bit Software Flow

3858 FHD F15
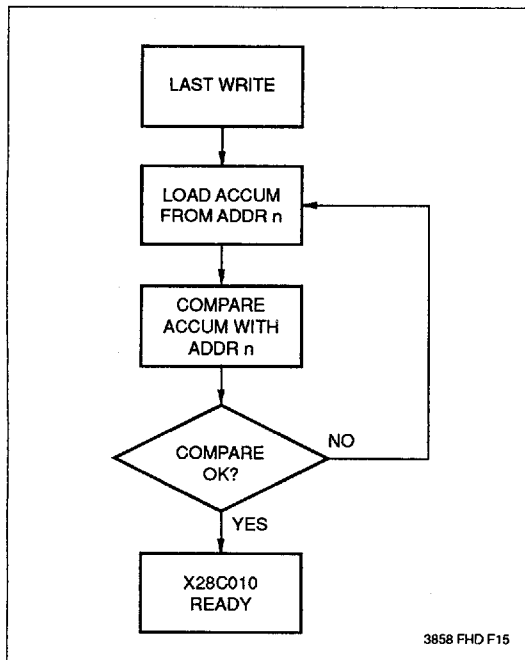
The Toggle Bit can eliminate the software housekeeping chore of saving and fetching the last address and data written to a device in order to implement $\overline{DATA}$ Polling. This can be especially helpful in an array comprised of multiple X28C010 memories that is frequently updated. Toggle Bit testing can also provide a method for status checking in multiprocessor applications. The timing diagram in Figure 4 illustrates the sequence of events on the bus. The software flow diagram in Figure 5 illustrates a method for testing the Toggle Bit.

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HARDWARE DATA PROTECTION

The X28C010 provides three hardware features that protect nonvolatile data from inadvertent writes.

- Noise Protection—A $\overline{WE}$ pulse less than 10 ns will not initiate a write cycle.

- Default V_{CC} Sense—All functions are inhibited when V_{CC} is ≤3.6V.

- Write inhibit—Holding either $\overline{OE}$ LOW, $\overline{WE}$ HIGH, or $\overline{CE}$ HIGH will prevent an inadvertent write cycle during power-on and power-off, maintaining data integrity.

SOFTWARE DATA PROTECTION

The X28C010 offers a software controlled data protection feature. The X28C010 is shipped from Xicor with the software data protection NOT ENABLED: that is the device will be in the standard operating mode. In this mode data should be protected during power-up/-down operations through the use of external circuits. The host would then have open read and write access of the device once V_{CC} was stable.

The X28C010 can be automatically protected during power-up and power-down without the need for external circuits by employing the software data protection feature. The internal software data protection circuit is enabled after the first write operation utilizing the software algorithm. This circuit is nonvolatile and will remain set for the life of the device unless the reset command is issued.

Once the software protection is enabled, the X28C010 is also protected from inadvertent and accidental writes in the powered-on state. That is, the software algorithm must be issued prior to writing additional data to the device.

SOFTWARE ALGORITHM

Selecting the software data protection mode requires the host system to precede data write operations by a series of three write operations to three specific addresses. Refer to Figures 6 and 7 for the sequence. The three byte sequence opens the page write window enabling the host to write from one to two hundred fifty-six bytes of data. Once the page load cycle has been completed, the device will automatically be returned to the data protected state.

X28C010
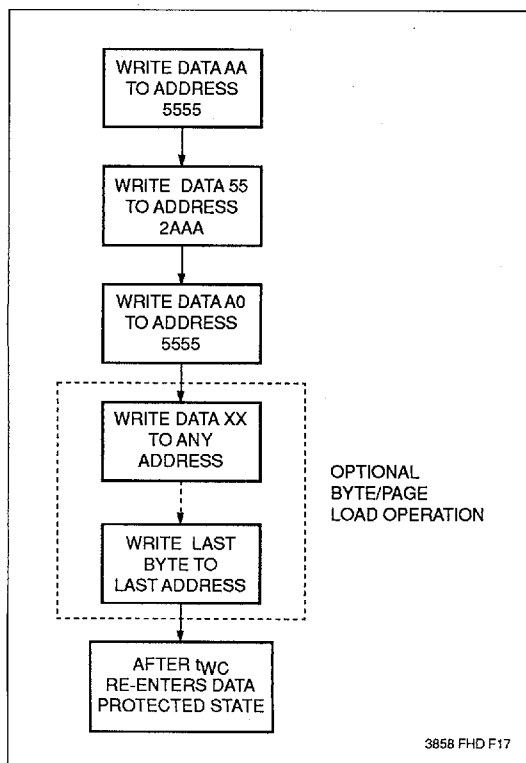
Software Data Protection
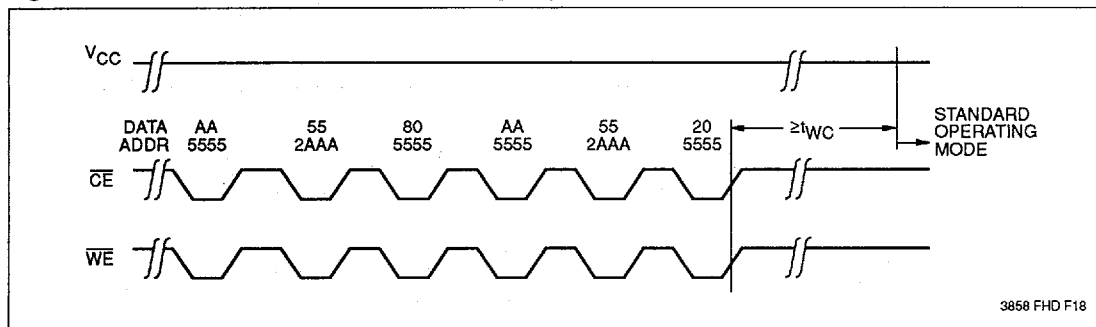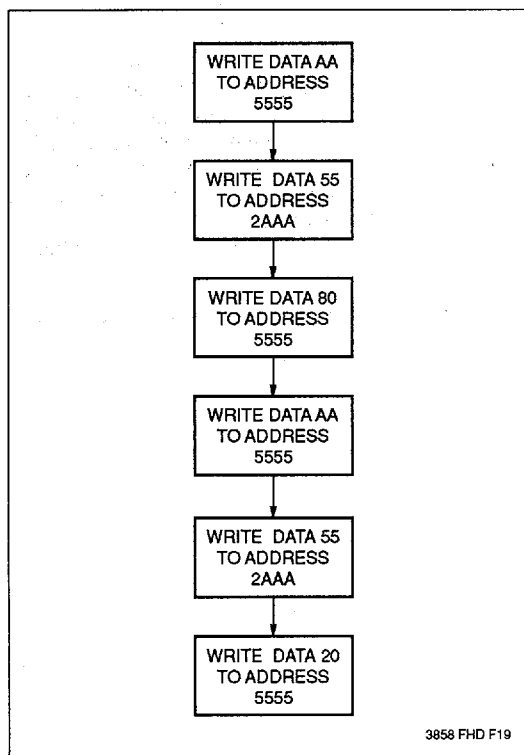### Figure 6. Timing Sequence—Byte or Page Write
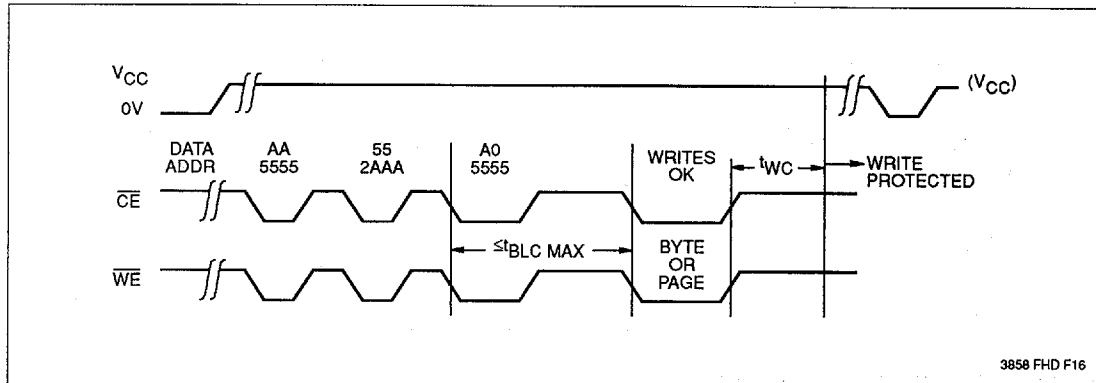
3858 FHD F16

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Figure 7. Write Sequence for Software Data Protection


```
WRITE DATA AA
TO ADDRESS
5555
        ↓
WRITE DATA 55
TO ADDRESS
2AAA
        ↓
WRITE DATA A0
TO ADDRESS
5555
        ↓
WRITE DATA XX
TO ANY
ADDRESS              OPTIONAL
                     BYTE/PAGE
                     LOAD OPERATION
WRITE LAST
BYTE TO
LAST ADDRESS
        ↓
AFTER tWC
RE-ENTERS DATA
PROTECTED STATE
```

3858 FHD F17

Regardless of whether the device has previously been protected or not, once the software data protection algorithm is used and data has been written, the X28C010 will automatically disable further writes unless another command is issued to cancel it. If no further commands are issued the X28C010 will be write protected during power-down and after any subsequent power-up. The state of A_{15} and A_{16} while executing the algorithm is don't care.

Note: Once initiated, the sequence of write operations should not be interrupted.

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Resetting Software Data Protection
Figure 8. Reset Software Data Protection Timing Sequence

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Figure 9. Software Sequence to Deactivate Software Data Protection

WRITE DATA AA TO ADDRESS 5555

WRITE DATA 55 TO ADDRESS 2AAA

WRITE DATA 80 TO ADDRESS 5555

WRITE DATA AA TO ADDRESS 5555

WRITE DATA 55 TO ADDRESS 2AAA

WRITE DATA 20 TO ADDRESS 5555

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In the event the user wants to deactivate the software data protection feature for testing or reprogramming in an E2PROM programmer, the following six step algorithm will reset the internal protection circuit. After t_{WC}, the X28C010 will be in standard operating mode.

Note: Once initiated, the sequence of write operations should not be interrupted.

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SYSTEM CONSIDERATIONS

Because the X28C010 is frequently used in large memory arrays it is provided with a two line control architecture for both read and write operations. Proper usage can provide the lowest possible power dissipation and eliminate the possibility of contention where multiple I/O pins share the same bus.

To gain the most benefit it is recommended that $\overline{CE}$ be decoded from the address bus and be used as the primary device selection input. Both $\overline{OE}$ and $\overline{WE}$ would then be common among all devices in the array. For a read operation this assures that all deselected devices are in their standby mode and that only the selected device(s) is outputting data on the bus.

Because the X28C010 has two power modes, standby and active, proper decoupling of the memory array is of prime concern. Enabling $\overline{CE}$ will cause transient current spikes. The magnitude of these spikes is dependent on the output capacitive loading of the I/Os. Therefore, the larger the array sharing a common bus, the larger the transient spikes. The voltage peaks associated with the current transients can be suppressed by the proper selection and placement of decoupling capacitors. As a minimum, it is recommended that a 0.1 μF high frequency ceramic capacitor be used between V_{CC} and GND at each device. Depending on the size of the array, the value of the capacitor may have to be larger.

In addition, it is recommended that a 4.7 μF electrolytic bulk capacitor be placed between V_{CC} and GND for each eight devices employed in the array. This bulk capacitor is employed to overcome the voltage droop caused by the inductive effects of the PC board traces.

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ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias
 X28C010 ....−10°C to +85°C
 X28C010I ....−65°C to +135°C
 X28C010M ....−65°C to +135°C
Storage Temperature ....−65°C to +150°C
Voltage on any Pin with
 Respect to Ground ....−1.0V to +7.0V
D.C. Output Current ....5 mA
Lead Temperature
 (Soldering, 10 Seconds) ....300°C

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMEND OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	+70°C
Industrial	−40°C	+85°C
Military	−55°C	+125°C

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Supply Voltage	Limits
X28C010	5V ±10%

3826 PGM T03

D.C. OPERATING CHARACTERISTICS (Over the recommended operating conditions, unless otherwise specified.)

Symbol	Parameter	Limits Min.	Limits Max.	Units	Test Conditions
I_{CC}	V_{CC} Current (Active) (TTL Inputs)		50	mA	$\overline{CE} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$, All I/O's = Open, Address Inputs = .4V/2.4V Levels @ f = 5MHz
I_{SB1}	V_{CC} Current (Standby) (TTL Inputs)		3	mA	$\overline{CE} = V_{IH}$, $\overline{OE} = V_{IL}$ All I/O's = Open, Other Inputs = V_{IH}
I_{SB2}	V_{CC} Current (Standby) (CMOS Inputs)		500	µA	$\overline{CE} = V_{CC} - 0.3V$, $\overline{OE} = V_{IL}$ All I/O's = Open, Other Inputs = V_{CC}
I_{LI}	Input Leakage Current		10	µA	V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current		10	µA	V_{OUT} = GND to V_{CC}, $\overline{CE} = V_{IH}$
V_{IL}[1]	Input Low Voltage	−1.0	0.8	V	
V_{IH}[1]	Input High Voltage	2.0	$V_{CC} + 1.0$	V	
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = −400 µA

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Notes: (1) V_{IL} min. and V_{IH} max. are for reference only and are not tested.

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POWER-UP TIMING

Symbol	Parameter	Max.	Units
t_{PUR}[2]	Power-up to Read Operation	100	µs
t_{PUW}[2]	Power-up to Write Operation	5	ms

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CAPACITANCE $T_A = 25°C$, f = 1.0 MHz, $V_{CC} = 5V$

Symbol	Parameter	Max.	Units	Test Conditions
$C_{I/O}$[2]	Input/Output Capacitance	10	pF	$V_{I/O} = 0V$
C_{IN}[2]	Input Capacitance	10	pF	$V_{IN} = 0V$

3858 PGM T04

ENDURANCE AND DATA RETENTION

Parameter	Min.	Max.	Units
Endurance	10,000		Cycles per Byte
Data Retention	100		Years

3858 PGM T05
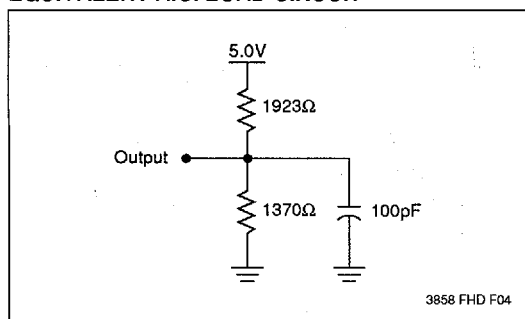
A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	10 ns
Input and Output Timing Levels	1.5V

3858 PGM T05

MODE SELECTION

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O	Power
L	L	H	Read	D_{OUT}	Active
L	H	L	Write	D_{IN}	Active
H	X	X	Standby and Write Inhibit	High Z	Standby
X	L	X	Write Inhibit	—	—
X	X	H	Write Inhibit	—	—

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EQUIVALENT A.C. LOAD CIRCUIT

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SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

Note: (2) This parameter is periodically sampled and not 100% tested.

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A.C. CHARACTERISTICS (Over the recommended operating conditions, unless otherwise specified.)

Read Cycle Limits

| Symbol	Parameter	X28C010-12 Min.	X28C010-12 Max.	X28C010-15 Min.	X28C010-15 Max.	X28C010-20 Min.	X28C010-20 Max.	X28C010-25 Min.	X28C010-25 Max.	Units
t_{RC}	Read Cycle Time	120		150		200		250		ns
t_{CE}	Chip Enable Access Time		120		150		200		250	ns
t_{AA}	Address Access Time		120		150		200		250	ns
t_{OE}	Output Enable Access Time		50		50		50		50	ns
t_{LZ}[3]	$\overline{CE}$ Low to Active Output	0		0		0		0		ns
t_{OLZ}[3]	$\overline{OE}$ Low to Active Output	0		0		0		0		ns
t_{HZ}[3]	$\overline{CE}$ High to High Z Output		50		50		50		50	ns
t_{OHZ}[3]	$\overline{OE}$ High to High Z Output		50		50		50		50	ns
t_{OH}	Output Hold from Address Change	0		0		0		0		ns

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Read Cycle
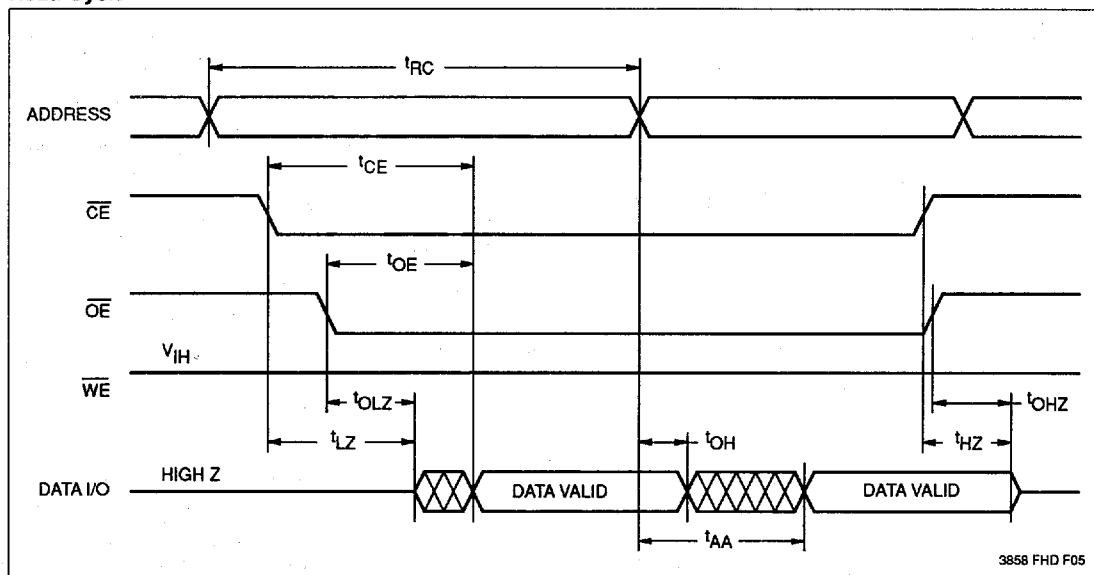
3858 FHD F05

Note: (3) t_{LZ} min., t_{HZ}, t_{OLZ} min., and t_{OHZ} are periodically sampled and not 100% tested. t_{HZ} max. and t_{OHZ} max. are measured, with C_L = 5pF, from the point when $\overline{CE}$ or $\overline{OE}$ return high (whichever occurs first) to the time when the outputs are no longer driven.

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Write Cycle Limits

Symbol	Parameter	Min.	Max.	Units
t_{WC}[4]	Write Cycle Time		10	ms
t_{AS}	Address Setup Time	0		ns
t_{AH}	Address Hold Time	50		ns
t_{CS}	Write Setup Time	0		ns
t_{CH}	Write Hold Time	0		ns
t_{CW}	$\overline{CE}$ Pulse Width	100		ns
t_{OES}	$\overline{OE}$ High Setup Time	10		ns
t_{OEH}	$\overline{OE}$ High Hold Time	10		ns
t_{WP}	$\overline{WE}$ Pulse Width	100		ns
t_{WPH}	$\overline{WE}$ High Recovery	100		ns
t_{DV}	Data Valid		1	μs
t_{DS}	Data Setup	50		ns
t_{DH}	Data Hold	10		ns
t_{DW}	Delay to Next Write	10		μs
t_{BLC}	Byte Load Cycle	0.2	100	μs

3858 PGM T09

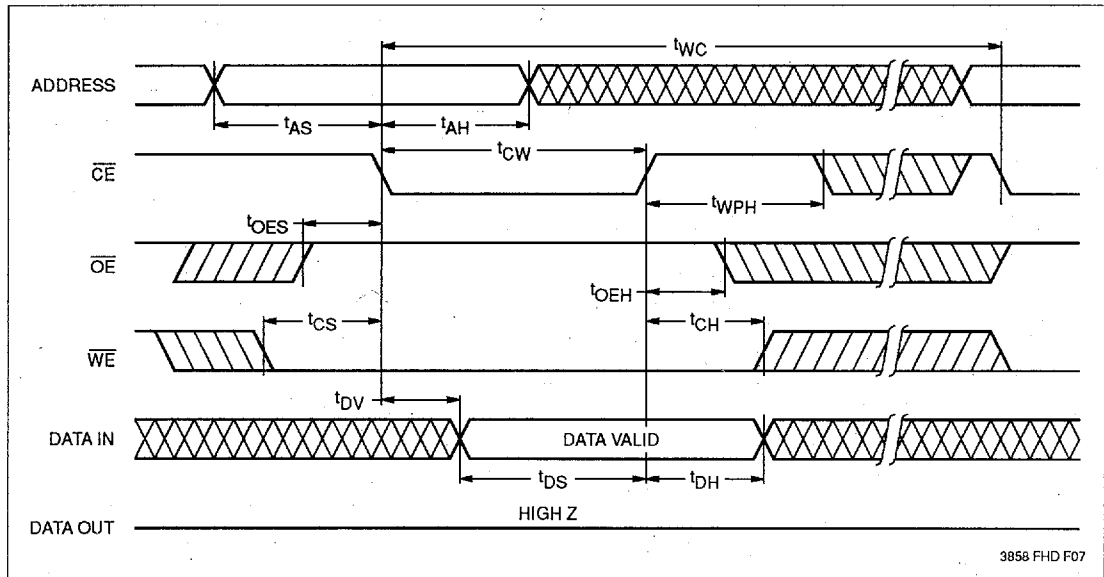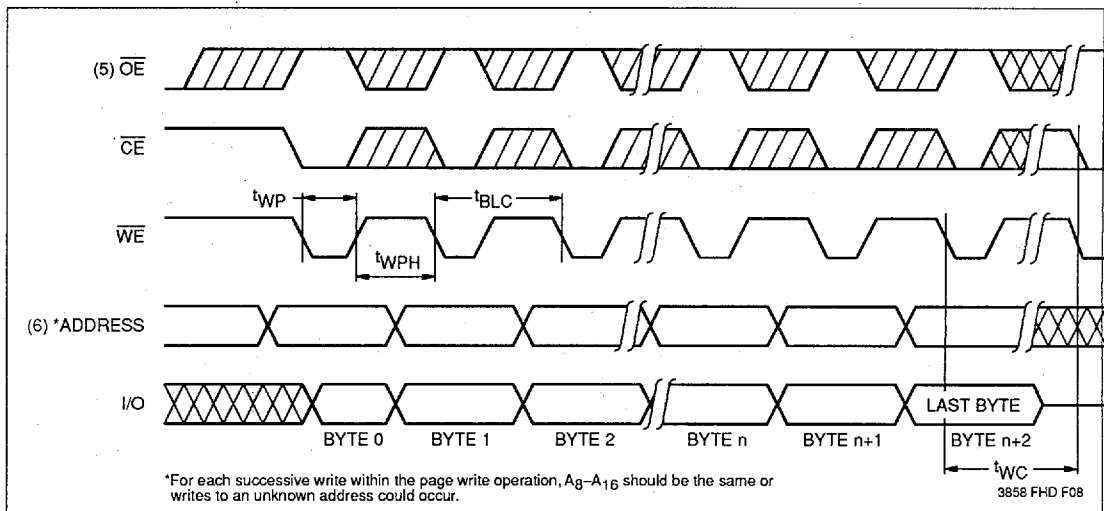### $\overline{WE}$ Controlled Write Cycle
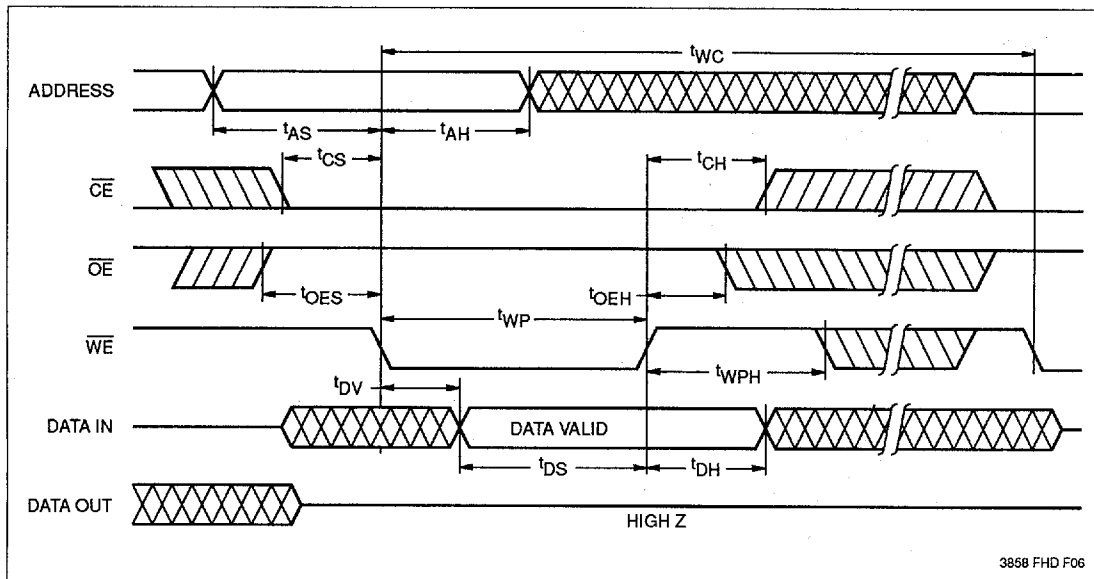
3858 FHD F06

Notes: (4) t_{WC} is the minimum cycle time to be allowed from the system perspective unless polling techniques are used. It is the maximum time the device requires to complete internal write operation.

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$\overline{CE}$ Controlled Write Cycle

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Page Write Cycle

*For each successive write within the page write operation, A_8–A_{16} should be the same or writes to an unknown address could occur.

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Notes: (5) Between successive byte writes within a page write operation, $\overline{OE}$ can be strobed LOW: e.g. this can be done with $\overline{CE}$ and $\overline{WE}$ HIGH to fetch data from another memory device within the system for the next write; or with $\overline{WE}$ HIGH and $\overline{CE}$ LOW effectively performing a polling operation.

(6) The timings shown above are unique to page write operations. Individual byte load operations within the page write must conform to either the $\overline{CE}$ or $\overline{WE}$ controlled write cycle timing.
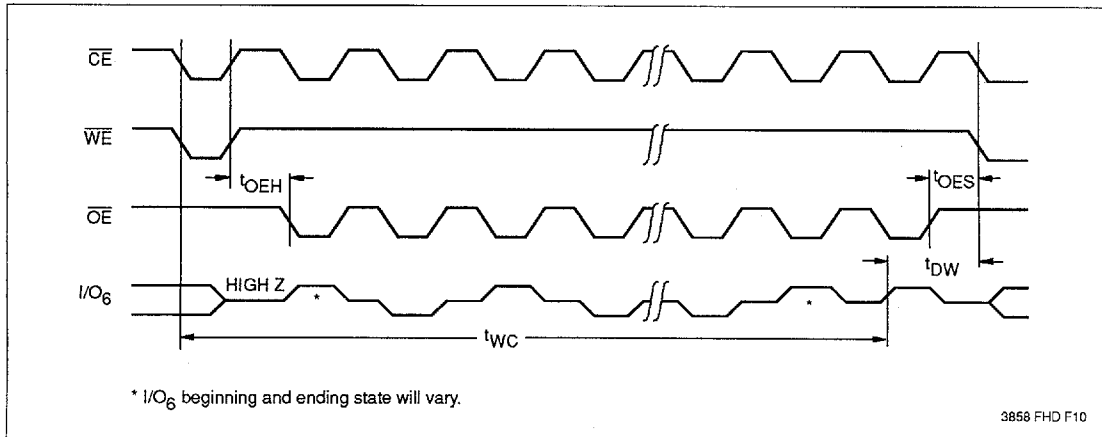
X28C010

$\overline{\text{DATA}}$ Polling Timing Diagram[7]

3858 FHD F09
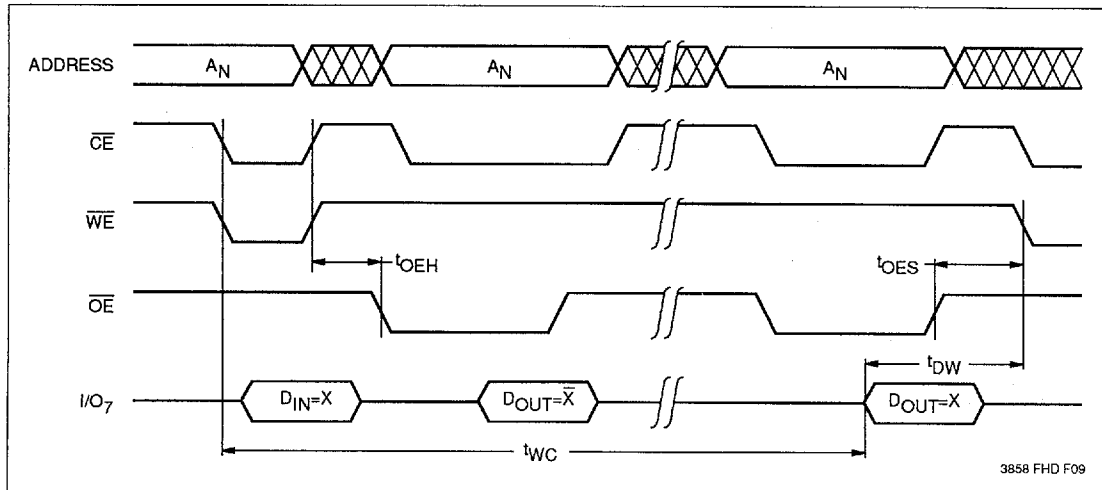
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Toggle Bit Timing Diagram

* I/O$_6$ beginning and ending state will vary.

3858 FHD F10

Note: (7) Polling operations are by definition read cycles and are therefore subject to read cycle timings.