

Am6072

Companding D-to-A Converter for PCM Communication Systems

Distinctive Characteristics

- Tested to D3 compandor tracking specification
- Absolute accuracy specified — includes all errors over temperature range
- Settling time 300ns typical
- Ideal for multiplexed PCM systems
- Output dynamic range of 72 dB

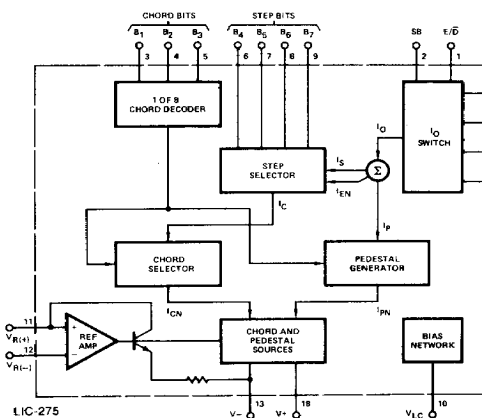
- Improved pin-for-pin replacement for DAC-86
- Microprocessor controlled operations
- Multiplying operation
- Negligible output noise
- Monotonicity guaranteed over entire dynamic range
- Wide output voltage compliance
- Low power consumption

GENERAL DESCRIPTION

The Am6072 is a monolithic 8-bit, companding digital-to-analog (D/A) data converter with true current outputs and large output voltage compliance for fast driving a variety of loads. The transfer function of the Am6072 complies with the Bell System μ -255 companding law, $Y = 0.18 \ln(1 + \mu x)$, and consists of 15 linear segments or chords. A particular chord is identified with the sign bit input, (SB), and three chord select input bits. Each chord contains 16 uniformly spaced linear steps which are determined by four step select input bits. The resulting dynamic range achieved with this 8-bit format is 72dB. Accuracy and monotonicity are assured by the internal circuit design and are guaranteed over the full temperature

range. The Am6072 is tested to the Bell D3 channel bank compandor tracking specification for pulse code modulation (PCM) transmission systems. The application of the Am6072 in communication systems provides an increased signal-to-noise ratio, reduces system signal distortion, and stimulates wider usage of computerized channel switching. Other application areas include digital audio recording, voice synthesis, and secure communications. When used in PCM communication systems, the Am6072 functions as a complete PCM decoder with additional encoding capabilities which make it ideal for implementation in CODEC circuits.

FUNCTIONAL BLOCK DIAGRAM



MAXIMUM RATINGS above which useful life may be impaired

V+ Supply to V- Supply	36V	Operating Temperature	
V _{LC} Swing	V- plus 8V to V+	MIL Grade	-55°C to +125°C
Output Voltage Swing	V- plus 8V to V- plus 36V	COM'L Grade	0°C to +70°C
Reference Inputs	V- to V+	Storage Temperature	-65°C to +150°C
Reference Input Differential Voltage	±18V	Power Dissipation T _A ≤ 100°C	500mW
Reference Input Current	1.25mA	For T _A > 100°C derate at	10mW/°C
Logic Inputs	V- plus 8V to V- plus 36V	Lead Soldering Temperature	300°C (60 sec)

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GUARANTEED FUNCTIONAL SPECIFICATIONS

Resolution	±128 Steps
Monotonicity	For both groups of 128 steps and over full operating temperature range
Dynamic Range	72 dB, (20 log (I ₇ , 15/I ₀ , 11))

ELECTRICAL CHARACTERISTICS (Note 1)

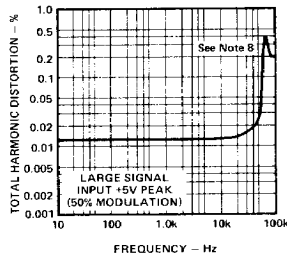
These specifications apply for V₊ = +15V, V₋ = -15V, I_{REF} = 528μA, 0°C ≤ T_A ≤ +70°C, for the commercial grade, -55°C ≤ T_A ≤ +125°C, for the military grade, and for all 4 outputs unless otherwise specified.

Parameter	Description		Test Conditions	Min.	Typ.	Max.	Unit	
t _s	Settling Time		To within ±1/2 step at T _A = 25° C, Output switched from I _{ZS} to I _{FS}	—	300	500	ns	
	Chord Endpoint Accuracy		V _{REF} = +10,000V R _{REF+} = 18.94kΩ R _{REF-} = 20kΩ -5V ≤ V _{OUT} ≤ +18V	See Table 1 for absolute accuracy limits which cover all errors related to the transfer characteristic.				
	Step Nonlinearity							
I _{EN}	Encode Current							
I _{FS(D)} I _{FS(E)}	Full Scale Current Deviation from Ideal							
I _{O(+)} -I _{O(-)}	Full Scale Current Symmetry Error							
I _{ZS}	Zero Scale Current							
ΔI _{FS}	Full Scale Current Drift							
V _{OC}	Output Voltage Compliance		Output within limits specified by Table 1	-5	—	+18	Volts	
I _{DIS}	Disable Current		Leakage of output disabled by E/D or SB	—	5.0	50	nA	
I _{FSR}	Output Current Range			0	2.0	4.2	mA	
V _{IL}	Logic Input Levels	Logic "0"	V _{LC} = 0V	—	—	0.8	Volts	
V _{IH}		Logic "1"		2.0	—	—	Volts	
I _{IN}	Logic Input Current		V _{IN} = -5V to +18V	—	—	40	μA	
V _{IS}	Logic Input Swing		V ₋ = -15V	-5	—	+18	Volts	
I _{BREF-}	Reference Bias Current			—	-1.0	-4.0	μA	
di/dt	Reference Input Slew Rate			0.12	0.25	—	mA/μs	
PSSI _{FS+} PSSI _{FS-}	Power Supply Sensitivity Over Supply Range (Refer to Characteristic Curves)		V ₊ = +4.5 to +18V, V ₋ = -15V	—	0.005	0.1	dB	
			V ₋ = -10.8V to -18V, V ₊ = +15V	—	0.01	0.1		
I ₊ I ₋	Power Supply Current		V ₊ = +5V to +15V, V ₋ = -15V, I _{FS} = 2.0mA	—	2.7	4.0	mA	
				—	-6.7	-8.8		
P _D	Power Dissipation		V ₋ = -15V, V _{OUT} = 0V I _{FS} = 2.0mA	V ₊ = +5V V ₊ = +15V	— —	114 141	152 192	mW

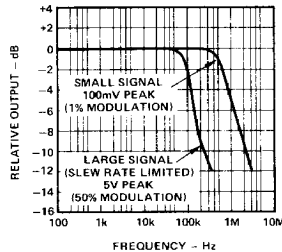
Note 1. In a companding DAC the term LSB is not used because the step size within each chord is different. For example, in the first chord around zero (C₀) the step size is 0.5μA, while in the last chord near full scale (C₇) the step size is 64μA.

TYPICAL PERFORMANCE CURVES

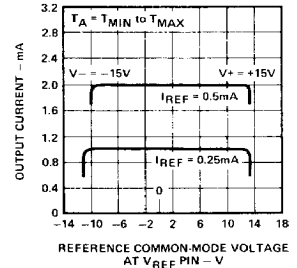
Reference Amplifier
Total Harmonic Distortion
Versus Frequency (80kHz Filter)
(Notes 6, 7, 8)



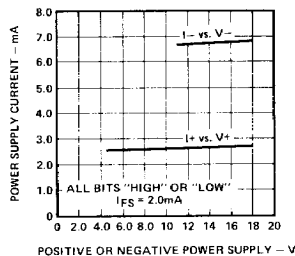
Reference Amplifier
Input Frequency Response



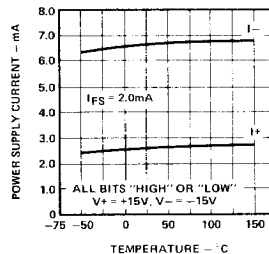
Reference Amplifier
Input Common-Mode Range
(Note 9)



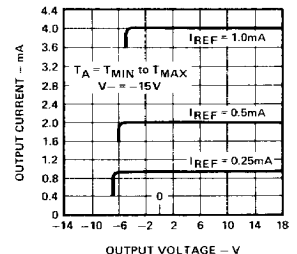
Power Supply Currents
Versus Power Supply Voltages



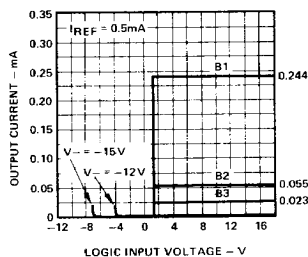
Power Supply Currents
Versus Temperature



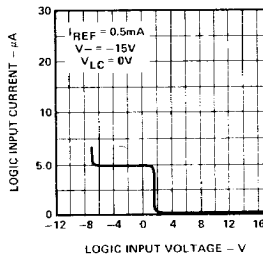
Output Current Versus
Output Voltage
(Output Voltage Compliance)



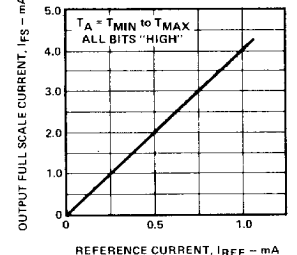
Bit Transfer Characteristics
(Note 10)



Logic Input Current
Versus Input Voltage
and Logic Input Range
(Note 11)



Output Full Scale Current
Versus Reference Input Current



Notes: 6. THD is nearly independent of the logic input code.

7. Similar results are obtained for a high input impedance connection using $V_{R(-)}$ as an input.

8. Increased distortion above 50kHz is due to a slew rate limiting effect which determines the large signal bandwidth. For an input of $\pm 2.5V$ peak (25% modulation), the bandwidth is 100kHz.

9. Positive common mode range is always $(V+) - 1.5V$.

10. All bits are fully switched with less than a half step error at switching points which are guaranteed to lie between 0.8V and 2.0V over the operating temperature range.

11. The logic input voltage range is independent of the positive power supply and logic inputs may swing above the supply.

ELECTRICAL CHARACTERISTICS (Cont.)

TABLE 1
ABSOLUTE DECODER OUTPUT CURRENT LEVELS IN μA

STEP NO.	CHORD NO.							
	0	1	2	3	4	5	6	7
0	-.250	7.789	24.048	56.112	120.24	248.49	505.00	1018.02
	.000	8.264	24.750	57.250	123.75	256.75	519.75	1047.75
	.250	8.739	25.473	59.438	127.36	263.22	534.93	1078.34
1	.250	8.733	25.991	59.998	128.01	264.04	536.10	1080.21
	.500	9.250	26.750	61.750	131.75	271.75	551.75	1111.75
	.750	9.798	27.531	63.553	135.60	279.69	567.86	1144.21
2	.750	9.677	27.934	63.885	135.79	278.59	567.19	1142.39
	1.000	10.250	28.750	65.750	139.75	287.75	583.75	1175.75
	1.250	10.857	29.590	67.670	143.83	296.15	600.80	1210.08
3	1.250	10.621	29.878	67.771	143.56	295.13	598.28	1204.58
	1.500	11.250	30.750	69.750	147.75	303.75	615.75	1239.75
	1.750	11.917	31.648	71.787	152.06	312.62	633.73	1275.95
4	1.750	11.566	31.821	71.658	151.33	310.68	629.37	1266.76
	2.000	12.250	32.750	73.750	155.75	319.75	647.75	1303.75
	2.250	12.976	33.706	75.904	160.30	329.09	666.66	1341.82
5	2.250	12.509	33.784	75.544	159.10	326.22	660.46	1328.94
	2.500	13.250	34.750	77.750	163.75	335.75	679.75	1367.75
	2.750	14.035	35.765	80.020	168.53	345.55	699.60	1407.69
6	2.750	13.453	35.707	79.431	166.98	341.77	691.56	1391.13
	3.000	14.250	36.750	81.750	171.75	351.75	711.75	1431.75
	3.250	15.094	37.823	84.137	176.77	362.02	732.53	1473.56
7	3.250	14.397	37.661	83.317	174.65	357.32	722.65	1453.31
	3.500	15.250	38.750	85.750	179.75	367.75	743.75	1495.75
	3.750	16.154	39.882	88.250	185.00	378.49	765.47	1539.43
8	3.750	15.341	39.594	87.204	182.42	372.86	753.74	1515.50
	4.000	16.250	40.750	89.750	187.75	383.75	775.75	1559.75
	4.250	17.213	41.940	92.371	193.23	394.96	798.40	1605.30
9	4.248	16.285	41.537	91.090	190.20	388.41	784.83	1577.68
	4.500	17.250	42.750	93.750	195.75	399.75	807.75	1623.75
	4.757	18.272	43.998	96.488	201.47	411.42	831.34	1671.16
10	4.720	17.229	43.480	94.977	197.97	403.95	815.92	1639.87
	5.000	18.250	44.750	97.750	203.75	415.75	839.75	1687.75
	5.296	19.331	46.057	100.604	209.70	427.89	864.27	1737.03
11	5.192	18.173	45.424	98.863	205.74	419.50	847.02	1702.05
	5.500	19.250	46.750	101.750	211.75	431.75	871.75	1751.75
	5.826	19.812	48.115	104.721	217.93	444.36	897.21	1802.90
12	5.664	19.675	47.367	102.750	213.52	436.05	878.11	1764.23
	6.000	20.250	48.750	105.750	219.75	447.75	903.75	1815.75
	6.366	20.841	50.174	108.838	226.17	460.82	930.14	1868.77
13	6.136	20.647	49.310	106.636	221.29	450.59	908.20	1826.42
	6.500	21.250	50.750	109.750	227.75	463.75	936.75	1879.75
	6.885	21.871	52.232	112.965	234.40	477.29	963.07	1934.64
14	6.808	21.619	51.253	110.523	229.06	466.14	940.29	1888.60
	7.000	22.250	52.750	113.750	235.75	479.75	967.75	1943.75
	7.415	22.900	54.290	117.072	242.63	493.76	996.01	2000.51
15	7.086	22.590	53.197	114.406	236.63	481.68	971.39	1950.79
	7.500	23.250	54.750	117.750	243.75	495.75	999.75	2007.75
	7.944	23.929	56.349	121.188	250.87	510.23	1028.94	2066.38
STEP SIZE	.5	1	2	4	8	16	32	64

Minimum, ideal and maximum values are specified for each step. The minimum and maximum values are specified to comply with the Bell D3 compandor tracking requirements. All four outputs are guaranteed, the encode outputs being specified to limits a half step higher than those shown above. This takes into account the combined effects of chord endpoint accuracy, step nonlinearity, encode current error, full scale current deviation from ideal, full scale symmetry error, zero scale current, full scale drift, and output impedance over the specified output voltage compliance range. Note that the guaranteed monotonicity ensures that adjacent step current levels will not overlap as might otherwise be implied from the minimum and maximum values shown in the above table.

TABLE 2
IDEAL DECODER OUTPUT VALUES EXPRESSED IN dB DOWN FROM OVERLOAD LEVEL (+3dBmo)

CHORD STEP	0	1	2	3	4	5	6	7
0	-	-44.73	-35.18	-27.82	-21.20	-14.90	-8.74	-2.65
1	-69.07	-43.73	-34.51	-27.24	-20.66	-14.37	-8.22	-2.13
2	-63.05	-42.84	-33.88	-26.70	-20.15	-13.87	-7.73	-1.66
3	-59.25	-42.03	-33.25	-26.18	-19.66	-13.40	-7.27	-1.19
4	-57.03	-41.29	-32.75	-25.70	-19.21	-12.96	-6.83	-0.75
5	-55.10	-40.61	-32.24	-25.24	-18.77	-12.53	-6.41	-0.33
6	-53.51	-39.98	-31.75	-24.80	-18.36	-12.13	-6.01	+0.06
7	-52.17	-39.39	-31.29	-24.39	-17.96	-11.74	-5.63	+0.44
8	-51.01	-38.84	-30.85	-23.99	-17.58	-11.37	-5.28	+0.81
9	-49.99	-38.32	-30.44	-23.61	-17.22	-11.02	-4.91	+1.16
10	-49.07	-37.83	-30.04	-23.25	-16.87	-10.68	-4.57	+1.49
11	-48.25	-37.37	-29.66	-22.90	-16.54	-10.35	-4.25	+1.82
12	-47.49	-36.93	-29.29	-22.57	-16.22	-10.03	-3.93	+2.13
13	-46.80	-36.51	-28.95	-22.25	-15.91	-9.73	-3.63	+2.43
14	-46.15	-36.11	-28.61	-21.94	-15.61	-9.43	-3.34	+2.72
15	-45.55	-35.73	-28.29	-21.63	-15.32	-9.15	-3.06	+3.00

The -37 dBmo and -50 dBmo output points significant for the Bell D3 system specification can be found between steps 11 and 12 on chord 1, and steps 8 and 9 on chord 0, respectively. Outputs corresponding to points below -50dB are specified in Table 1 for an accuracy of $\pm$ a half step.

THEORY OF OPERATION

Functional Description

The Am6072 is an 8-bit, nonlinear, digital-to-analog converter with high impedance current outputs. The output current value is proportional to the product of the digital inputs and the input reference current. The full scale output current, I_{FS} , is specified by the input binary code 111 1111, and is a linear function of the reference current, I_{REF} . There are two operating modes, encode and decode, which are controlled by the Encode/Decode, (E/D), input signal. A logic 1 applied to the E/D input places the Am6072 in the encode mode and current will flow into the $I_{OE(+)}$ or $I_{OD(-)}$ output, depending on the state of the Sign Bit (SB) input. A logic 0 at the E/D input places the Am6072 in the decode mode.

The transfer characteristic is a piece-wise linear approximation to the Bell System μ -225 logarithmic law which can be written as follows:

$$Y = 0.18 \ln(1 + \mu |X|) \operatorname{sgn}(X)$$

where: X = analog signal level normalized to unity
(encoder input or decoder output)

Y = digital signal level normalized to unity
(encoder output or decoder input)

$$\mu = 255$$

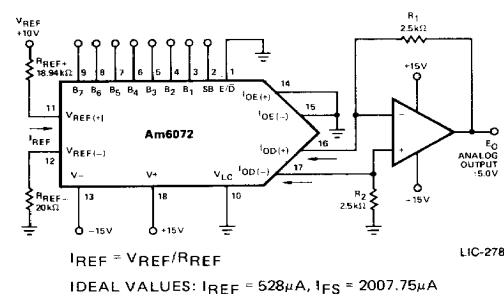
The current flows from the external circuit into one of four possible analog outputs determined by the SB and E/D inputs. The output current transfer function can be represented by a total of 16 segments or chords addressable through the SB input and three chord select bits. Each chord can be further divided into 16 steps, all of the same size. The step size changes from one chord to another, with the smallest step of $0.5\mu A$ found in the first chord near zero output current, and the largest step of $64\mu A$ found in the last chord near full scale output current. This nonlinear feature provides exceptional accuracy for small signal levels near zero output current. The accuracy for signal amplitudes corresponding to chord 0 is equivalent to that of a 12-bit linear, binary D/A converter. However, the ratio (in dB) between the chord

endpoint current, (Step 15), and the current which corresponds to the preceding step, (Step 14), is maintained at about 0.3dB over most of the dynamic range. The difference between the ratios of full scale current to chord endpoint currents of adjacent chords is similarly maintained at approximately 6dB over most of the dynamic range. Resulting signal-to-quantizing distortions due to non-uniform quantizing levels maintain an acceptably low value over a 40dB range of input speech signals. Note that the 72dB output dynamic range for the Am6072 corresponds to the dynamic range of a sign plus 12-bit linear, binary D/A converter.

In order to achieve a smoother transition between adjacent chords, the step size between these chord end points is equal to 1.5 times the step size of the lower chord. Monotonic operation is guaranteed by the internal device design over the entire output dynamic range by specifying and maintaining the chord end points and step size deviations within the allowable limits.

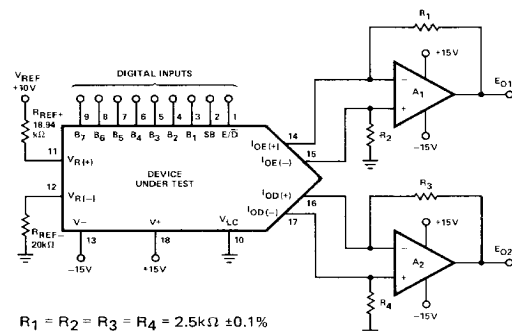
Operating Modes

The basic converter function is conversion of digital input data into a corresponding analog current signal, i.e., the basic function is digital-to-analog decoding. The basic decoder connection for a sign plus 7-bit input configuration is shown in Figure 1. The corresponding dynamic range is 72dB, and input-output characteristics conform to the standard decoder transfer function with output current values specified in Table 1. The E/D input enables switching between the encode, $I_{OE(+)}$ or $I_{OD(-)}$, and the decode, $I_{OD(+)}$ or $I_{OD(-)}$, outputs. A typical encode/decode test circuit is shown in Figure 2. This circuit is used for output current measurements. When the E/D input is high, (a logic 1), the converter will assume the encode operating mode and the output current will flow into one of the I_{OE} outputs (as determined by the SB input). When operating in the decode mode as shown in Figure 3, an offset current equal to a half step in each chord is required to obtain the correct encoder transfer characteristic. Since the size of this step varies from one chord to another, it cannot easily be added externally. As indicated in the block diagram this required half step of encode current,



	E/D	SB	B1	B2	B3	B4	B5	B6	B7	E0
POSITIVE FULL SCALE	0	1	1	1	1	1	1	1	1	5.019V
(+) ZERO SCALE +1 STEP	0	1	0	0	0	0	0	0	0	0.0012V
(+) ZERO SCALE	0	1	0	0	0	0	0	0	0	0V
(-) ZERO SCALE	0	0	0	0	0	0	0	0	0	0V
(-) ZERO SCALE +1 STEP	0	0	0	0	0	0	0	0	1	-0.0012V
NEGATIVE FULL SCALE	0	0	1	1	1	1	1	1	1	-5.019V

Figure 1. Detailed Decoder Connections.



LINE SELECTION TABLE

TEST GROUP	E/D	SB	OUTPUT MEASUREMENT
1	1	1	$I_{OE}(+)$ (E_{01}/R_1)
2	1	0	$I_{OE}(-)$ (E_{01}/R_2)
3	0	1	$I_{OD}(+)$ (E_{02}/R_3)
4	0	0	$I_{OD}(-)$ (E_{02}/R_4)

Figure 2. Output Current DC Test Circuit.

I_{EN} is automatically added to the I_{OE} output through the internal chip design. This additional current will, for example, make the ideal full scale current in the encode mode larger than the same current in the decode mode by $32\mu A$. Similarly, the current levels in the first chord near the origin will be offset by $0.25\mu A$, which will bring the ideal encode current value for step 0 on chord 0 to $\pm 0.25\mu A$ with respect to the corresponding decode current value of $0.0\mu A$. This additional encode half step of current can be used for extension of the output dynamic range from 72dB to 78dB, when the converter is performing only the decode function. The corresponding decoder connection utilizes the $E/\bar{D}$ input as a ninth digital input and has the outputs $I_{OD}(+)$ and $I_{OE}(+)$ and the outputs $I_{OD}(-)$ and $I_{OE}(-)$ tied together, respectively.

When encoding or compression of an analog signal is required, the Am6072 can be used together with a Successive Approximation Register (SAR), comparator, and additional SSI logic elements to perform the A/D data conversion, as shown in Figure 3. The encoder transfer function, shown on page 1, characterizes this A/D converter system. The first task of this system is to determine the polarity of the incoming analog signal and to generate a corresponding SB input value. When the proper Start, $\bar{S}$, and Conversion Complete, CC, signal levels are set, the first clock pulse sets the MSB output of the SAR, Am2502, to a logic 0 and sets all other parallel digital outputs to logic 1 levels. At the same time, the flip-flop is triggered, and its output provides the $E/\bar{D}$ input with a logic 0 level. No current flows into the I_{OE} outputs. This disconnects the converter from the comparator inputs, and the incoming analog signal can be compared with the ground applied to the opposite comparator input. The resulting comparator output is fed to the Am2502 serial data input, D, through an exclusive-or gate. At the same time, the second input to the same exclusive-or gate is held at a logic 0 level by the additional successive approximation logic shown in Figure 3. This exclusive-or gate inverts the comparator's outputs whenever a negative signal polarity is detected. This maintains the proper output current coding, i.e., all ones for full scale and all zeros for zero scale.

The second clock pulse changes the $E/\bar{D}$ input back to a logic 1 level because the CC signal changed. It also clocks the D

input signal of the Am2502 to its MSB output, and transfers it to the SB input of the Am6072. Depending upon the SB input level, current will flow into the $I_{OE}(+)$ or $I_{OE}(-)$ output of the Am6072.

Nine total clock pulses are required to obtain a digital binary representation of the incoming analog signal at the eight Am2502 digital outputs. The resulting Am6072 analog output signal is compared with the analog input signal after each of the nine successive clock pulses. The analog signal should not be allowed to change its value during the data conversion time. In high speed systems, fast changes of the analog signals at the A/D system input are usually prevented by using sample and hold circuitry.

Additional Considerations and Recommendations

In Figure 1, an optional operational amplifier converts the Am6072 output current to a bipolar voltage output. When the SB input is a logic 1, sink current appears at the amplifier's negative input, and the amplifier acts as a current to voltage converter, yielding a positive voltage output. With the SB value at a logic 0, sink current appears at the amplifier's positive input. The amplifier behaves as a voltage follower, and the true current outputs will swing below ground with essentially no change in output current. The SB input steers current into the appropriate (+) or (-) output of the Am6072. The resulting operational amplifier's output in Figure 2 should ideally be symmetrical with resistors R1 and R2 matched.

In Figure 2, two operational amplifiers measure the currents of each of the four Am6072 analog outputs. Resistor tolerances of 0.1% give 0.1% output measurement error (approximately $2\mu A$ at full scale). The input offset currents of the A1 and A2 devices also increase output measurement error and this error is most significant near zero scale. The Am101A and 308 devices, for example, may be used for A1 and A2 since their maximum offset currents, which would add directly to the measurement error, are only 10nA and 1nA, respectively. The input offset voltages of the A1 and A2 devices, with output resistor values of

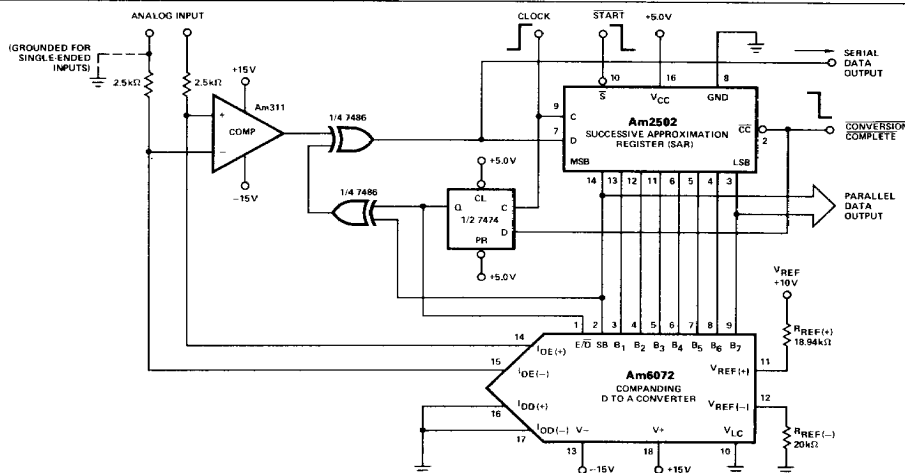


Figure 3. Detailed Encoder Connections.

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2.5k Ω , also contribute to the output measurement error by a factor of 400nA for every mV of offset at the A1 and A2 outputs. Therefore, to minimize error, the offset voltages of A1 and A2 should be nulled.

The recommended operating range for the reference current I_{REF} is from 0.1mA to 1.0mA. The full scale output current, I_{FS} , is a linear function of the reference current, and may be calculated from the equation $I_{FS} = 3.8 I_{REF}$. This tight relationship between I_{REF} and I_{FS} alleviates the requirement for trimming the I_{REF} current if the R_{REF} resistor values are within $\pm 1\%$ of the calculated value. Lower values of I_{REF} will reduce the negative power supply current, (I_-), and will increase the reference amplifier negative common mode input voltage range.

The ideal value for the reference current $I_{REF} = V_{REF}/R_{REF}$ is 528 μ A. The corresponding ideal full scale decode and encode current values are 2007.75 μ A and 2039.75 μ A, respectively. A percentage change from the ideal I_{REF} value produced by changes in V_{REF} or R_{REF} values produces the same percentage change in decode and encode output current values. The positive voltage supply, V_+ , may be used, with certain precautions, for the positive reference voltage V_{REF} . In this case, the reference resistor $R_{REF(+)}$ should be split into two resistors and their junction bypassed to ground with a capacitor of 0.01 μ F. The total resistor value should provide the reference current $I_{REF} = 528\mu$ A. The resistor $R_{REF(-)}$ value should be approximately equal to the $R_{REF(+)}$ value in order to compensate for the errors caused by the reference amplifier's input offset current.

An alternative to the positive reference voltage applications shown in Figures 1, 2 and 3 is the application of a negative voltage to the $V_{R(-)}$ terminal through the resistor $R_{REF(-)}$ with the $R_{REF(+)}$ resistor tied to ground. The advantage of this arrangement is the presence of very high impedance at the $V_{R(-)}$ terminal while the reference current flows from ground through $R_{REF(+)}$ into the $V_{R(+)}$ terminal.

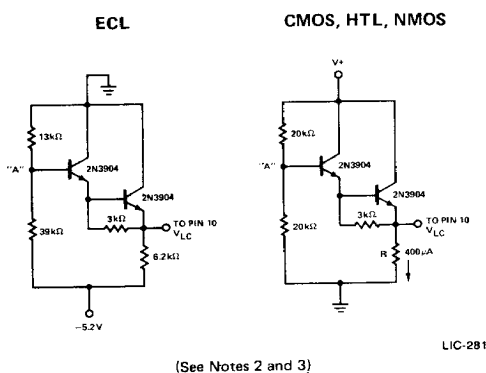


Figure 4. Interfacing Circuits for ECL, CMOS, HTL, and NMOS Logic Inputs.

The Am6072 has a wide output voltage compliance suitable for driving a variety of loads. With $I_{REF} = 528\mu$ A and $V_- = -15$ V, positive voltage compliance is +18V and negative voltage compliance is -5.0V. For other values of I_{REF} and V_- , the negative voltage compliance, $V_{OC(-)}$, may be calculated as follows:

$$V_{OC(-)} = (V_-) + (2 \cdot I_{REF} \cdot 1.5k\Omega) + 8.4V.$$

The following table contains $V_{OC(-)}$ values for some specific V_- , I_{REF} , and I_{FS} values.

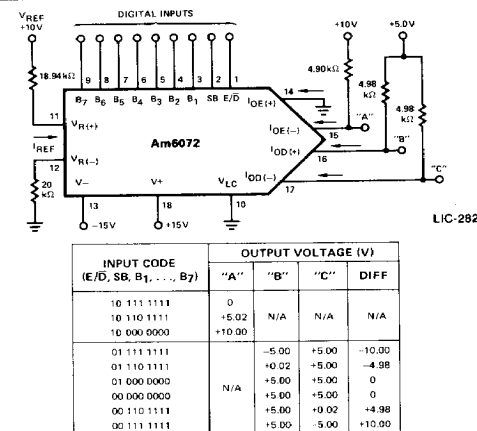
Negative Output Voltage Compliance $V_{OC(-)}$

V_-	I_{REF} (I_{FS})	264 μ A (1mA)	528 μ A (2mA)	1056 μ A (4mA)
-12V		-2.8V	-2.0V	-0.4V
-15V		-5.8V	-5.0V	-3.4V
-18V		-8.8V	-8.0V	-6.4V

The V_{LC} input can accommodate various logic input switching threshold voltages allowing the Am6072 to interface with various logic families. This input should be placed at a potential which is 1.4V below the desired logic input switching threshold. Two external discrete circuits which provide this function for non-TTL driven inputs are shown in Figure 4. For TTL-driven logic inputs, the V_{LC} input should be grounded. If negative voltages are applied at the digital logic inputs, they must have a value which is more positive than the sum of the chosen V_- value and +10V.

With a V_- value chosen between -15V and -11V, the $V_{OC(-)}$, the input reference common mode voltage range, and the logic input negative voltage range are reduced by an amount equivalent to the difference between -15V and the V_- value chosen.

With a V_+ value chosen between +5V and +15V, the reference amplifier common mode positive voltage range and the V_{LC} input values are reduced by an amount equivalent to the difference between +15V and the V_+ value chosen.



INPUT CODE (E/D, SB, B1, ..., B7)	"A"	"B"	"C"	DIFF
10 111 1111	0	N/A	N/A	N/A
10 110 1111	+5.02	N/A	N/A	N/A
10 000 0000	+10.00	N/A	N/A	N/A
01 111 1111	-5.00	+5.00	-10.00	
01 110 1111	+0.02	+5.00	-4.98	
01 000 0000	+5.00	+5.00	0	
00 000 0000	N/A	+5.00	+5.00	0
00 110 1111	+5.00	+0.02	+4.98	
00 111 1111	+5.00	-5.00	+10.00	

Figure 5. Resistive Output Connections.

Notes: 2. Set the voltage "A" to the desired logic input switching threshold.

3. Allowable range of logic threshold is typically -5V to +13.5V when operating the companding DAC on ± 15 V supplies.

ADDITIONAL DECODE OUTPUT CURRENT TABLES

Table 3
Normalized Decoder Output (Sign Bit Excluded)

Chord (C)		0	1	2	3	4	5	6	7
Step (S)		000	001	010	011	100	101	110	111
0	0000	0	33	99	231	495	1023	2079	4191
1	0001	2	37	107	247	527	1087	2207	4447
2	0010	4	41	115	263	559	1151	2335	4703
3	0011	6	45	123	279	591	1215	2463	4959
4	0100	8	49	131	295	623	1279	2591	5215
5	0101	10	53	139	311	655	1343	2719	5471
6	0110	12	57	147	327	687	1407	2847	5727
7	0111	14	61	155	343	719	1471	2975	5983
8	1000	16	65	163	359	751	1535	3103	6239
9	1001	18	69	171	375	783	1599	3231	6495
10	1010	20	73	179	391	815	1663	3359	6751
11	1011	22	77	187	407	847	1727	3487	7007
12	1100	24	81	195	423	879	1791	3615	7263
13	1101	26	85	203	439	911	1855	3743	7519
14	1110	28	89	211	455	943	1919	3871	7775
15	1111	30	93	219	471	975	1983	3999	8031
Step Size		2	4	8	16	32	64	128	256

The normalized decode current, ($I_{C,S}$), is calculated using:

$$I_{C,S} = 2(2^C(S + 16.5) - 16.5)$$

where C = chord number; S = step number. The ideal decode current, (I_{OD}), in μA is calculated using:

$$I_{OD} = (I_{C,S} / 17, 15(\text{norm.})) \cdot I_{FS} (\mu A)$$

where $I_{C,S}$ is the corresponding normalized current. To obtain normalized encode current values the corresponding normalized half-step value should be added to all entries in Table 3.

Table 4
Decoder Step Size Summary

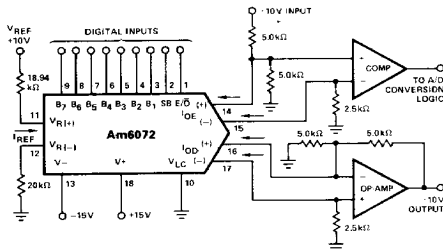
Chord	Step Size Normalized to Full Scale	Step Size in μA with 2007.75 μA FS	Step Size as a % of Full Scale	Step Size in dB at Chord Endpoints	Step Size as a % of Reading at Chord Endpoints	Resolution & Accuracy of Equivalent Binary DAC
0	2	0.5	0.025%	0.60	6.67%	Sign + 12 Bits
1	4	1.0	0.05%	0.38	4.30%	Sign + 11 Bits
2	8	2.0	0.1%	0.32	3.65%	Sign + 10 Bits
3	16	4.0	0.2%	0.31	3.40%	Sign + 9 Bits
4	32	8.0	0.4%	0.29	3.28%	Sign + 8 Bits
5	64	16.0	0.8%	0.28	3.23%	Sign + 7 Bits
6	128	32.0	1.6%	0.28	3.20%	Sign + 6 Bits
7	256	64.0	3.2%	0.28	3.19%	Sign + 5 Bits

Table 5
Decoder Chord Size Summary

Chord	Chord Endpoints Normalized to Full Scale	Chord Endpoints in μA with 2007.75 μA FS	Chord Endpoints as a % of Full Scale	Chord Endpoints in dB Down from Full Scale
0	30	7.5	0.37%	-48.55
1	93	23.25	1.16%	-38.73
2	219	54.75	2.73%	-31.29
3	471	117.75	5.86%	-24.63
4	975	243.75	12.1%	-18.32
5	1983	495.75	24.7%	-12.15
6	3999	999.75	49.8%	-6.06
7	8031	2007.75	100%	0

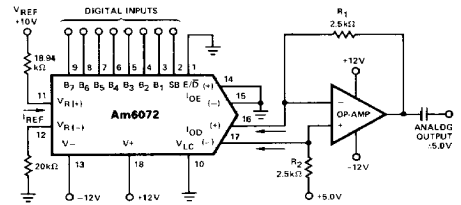
BASIC CIRCUIT CONNECTIONS

±10V RANGE ENCODER/DECODER CONNECTIONS



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COMPLIANCE EXTENSION USING AC COUPLED OUTPUT



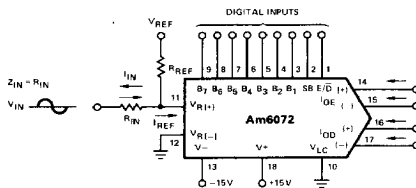
IDEAL VALUES:

$$I_{REF} = 528\mu A$$

$$I_{FS} = 2007.75\mu A$$

LIC-284

LOW INPUT IMPEDANCE CONNECTION

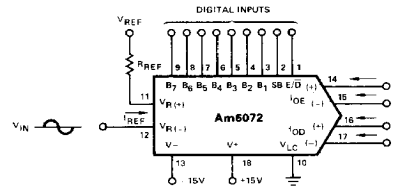


$$I_{REF} = V_{IN}/R_{IN} + V_{REF}/R_{REF}$$

$$I_{FS} \approx 4 \cdot I_{REF}$$

LIC-285

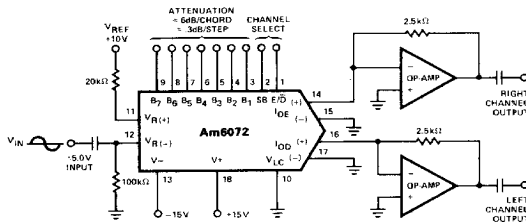
HIGH INPUT IMPEDANCE CONNECTION



$$I_{REF} = (V_{REF} - V_{IN})/R_{REF}$$

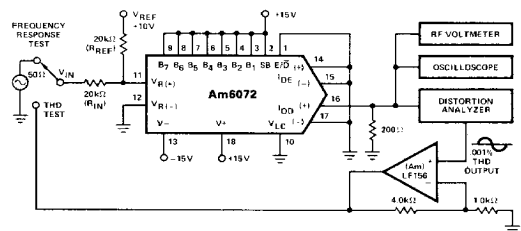
$$I_{FS} \approx 4 \cdot I_{REF}$$

LIC-286

LOGARITHMIC DIGITAL GAIN CONTROL
(Notes 4 & 5)

LIC-287

REFERENCE AMPLIFIER DYNAMIC TEST CIRCUIT



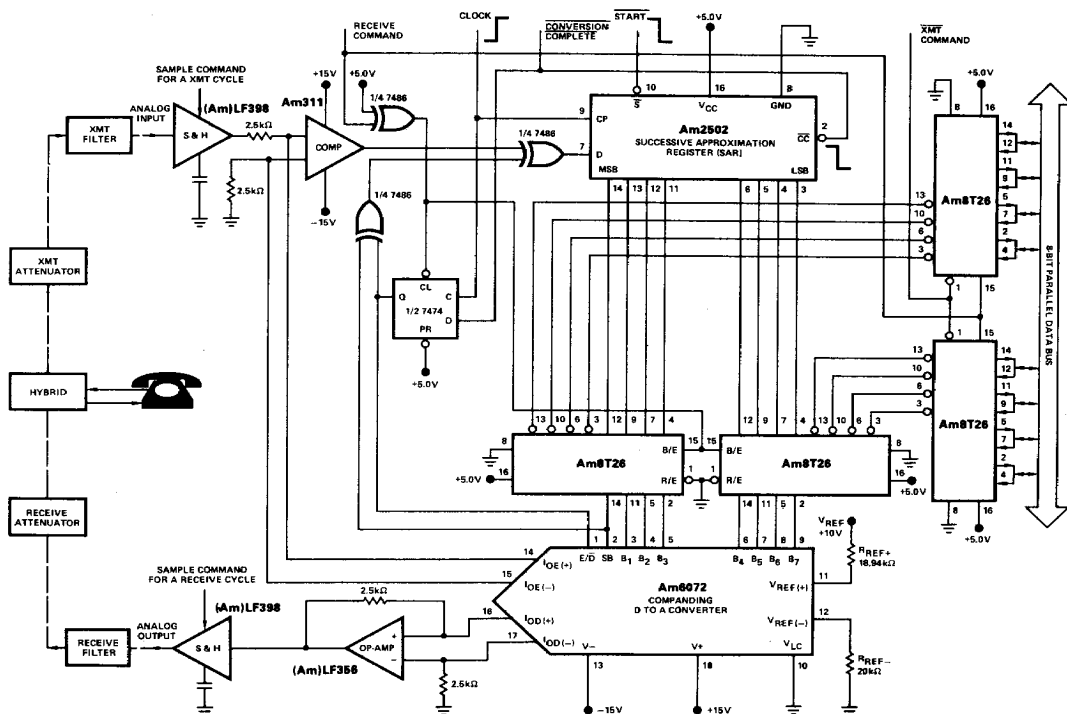
LIC-288

Notes: 4. Low distortion outputs are provided over a 72dB range.

5. Up to 4 channels of output may be selected by E/D and SB logic inputs.

TIME SHARED CONVERTER CONNECTIONS

SINGLE CHANNEL PCM CODEC – PARALLEL DATA I/O



LIC-290

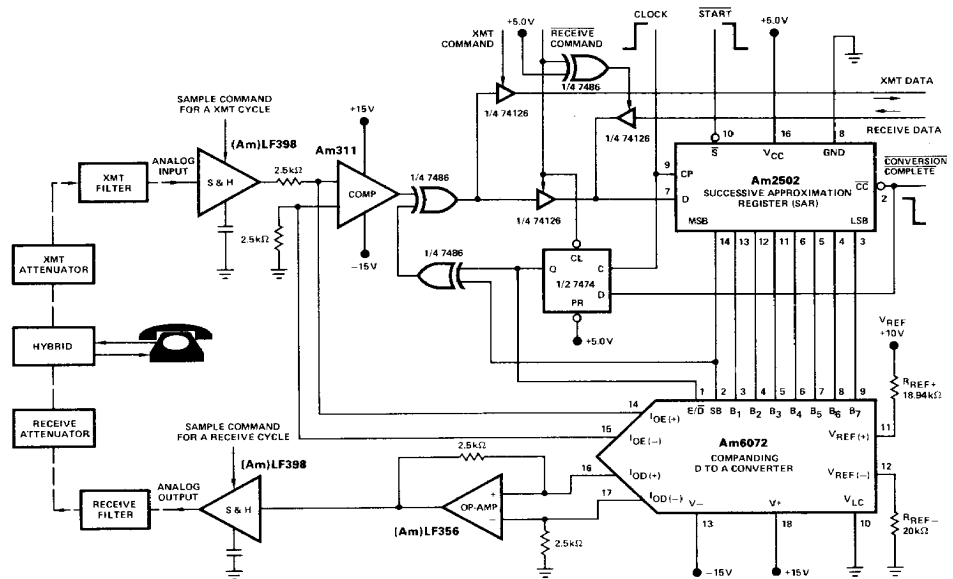
APPLICATION INFORMATION

1. To perform a transmit operation cycle the START pulse must be held low for one clock cycle; the receive operation is performed without the successive approximation register, SAR.
2. XMT and RECEIVE command signals are mutually exclusive.
3. Duration of the RECEIVE command signal must accommodate the Am6072 settling time plus the sampling time required by the sample and hold, (S & H), circuit used at the CODEC's analog output. The receiving data must not change during this time.
4. A XMT command signal must be issued after a high-to-low transition of the CONVERSION COMPLETE, CC, signal. Its duration depends on the time required by the digital time division switch circuitry to sample the 8-bit parallel transmit data bus.

5. Data conversion for a transmit operation is completed in 9 clock cycles because the SAR must be initialized before every new conversion. Data conversion for a receive operation corresponds to the Am6072 settling time; the receiving and transmit data transfers can be done simultaneously by employing separate transmit and receive data buses and utilizing data storage devices for the receive data.
6. A sample command pulse for a transmit operation can coincide with the START pulse; its duration depends on the sample and hold circuit used at the CODEC's analog input.
7. A sample command pulse for a receive operation must be delayed from a low-to-high transition of the RECEIVE command signal by an amount equal to the Am6072 settling time. Its termination can coincide with a high-to-low transition of the RECEIVE command signal.

TIME SHARED CONVERTER CONNECTIONS (Cont.)

SINGLE CHANNEL PCM CODEC — SERIAL DATA I/O



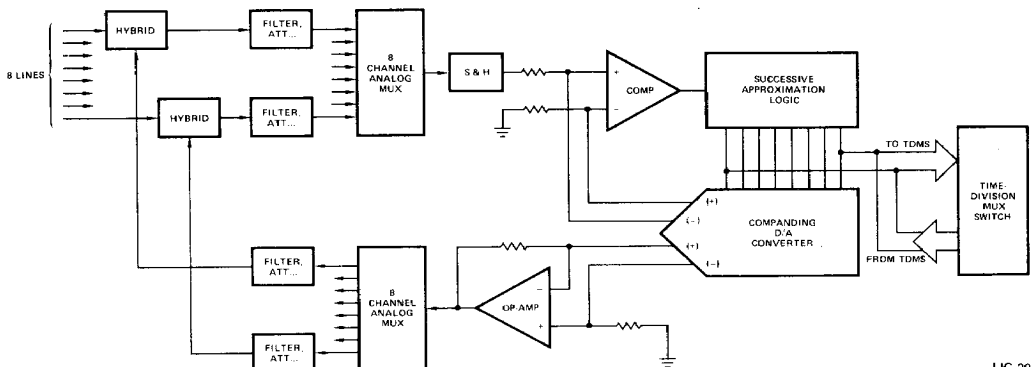
LIC-291

APPLICATION INFORMATION

1. Before beginning either a transmit or a receive operation, the START signal must be held low for one complete clock cycle.
2. XMT and RECEIVE command signals are mutually exclusive. Their durations must accommodate the time required for conversion of an outgoing or an incoming series of 8 digital bits, respectively.
3. Data conversion for either operation, transmit or receive, is completed in 9 clock cycles.

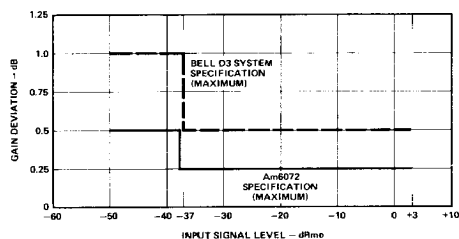
4. During the receive cycle the successive approximation register, SAR, is acting as a serial-in to parallel-out shift register, with data supplied from data storage devices.
5. A sample command pulse for a transmit cycle must be issued before a XMT command signal; its duration depends on the sample and hold, S & H, circuit used.
6. A sample command pulse for a receive cycle must be delayed by a time equal to the Am6072 settling time after a high-to-low transition of the CONVERSION COMPLETE, CC, signal occurs.

8 LINE CODEC TDM PCM/PABX SYSTEM — BLOCK DIAGRAM



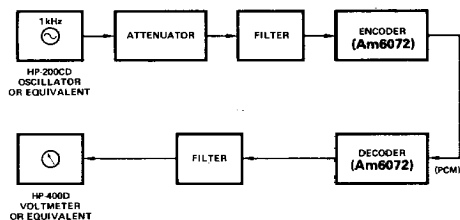
LIC-292

COMPANDOR TRACKING SPECIFICATION



LIC-293

COMPANDOR TRACKING TEST BLOCK DIAGRAM



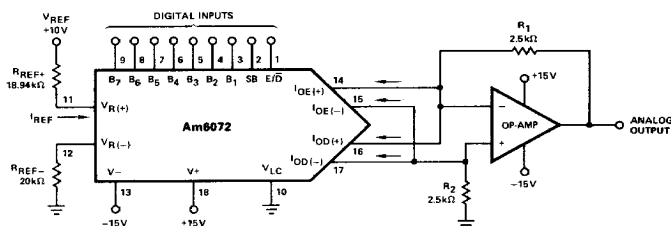
LIC-294

D3 NOISE AND DISTORTION SPECIFICATION

The Am6072 has a negligible idle channel noise contribution. Signal-to-quantizing-distortion ratio, (S/D), is guaranteed to exceed the minimum values specified for D3 channels as follows:

Input Level 1020 Hz Sinewave	S/D, C-Message Weighting
0 to -30 dBmo	33 dB
At -40 dBmo	27 dB
At -45 dBmo	22 dB

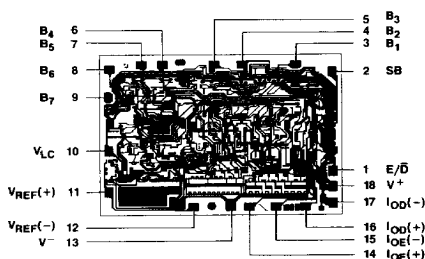
DECODER OPERATION DURING SIGNALLING FRAME



LIC-295

The Am6072 can perform the decoding function in a D3 channel bank system. During signalling frames the least significant bit, B7, of each 8-bit word is used for signalling messages and only seven bits are used for sample coding. In order to minimize the quantizing error during these signalling frames, the Am6072 output is increased by a half step from its corresponding decode output value by switching the E/D input from a logic level 0 to a logic 1.

Metallization and Pad Layout



DIE SIZE: 0.080" X 0.114"