

Section 17. Electrical Characteristics

17.1 Absolute Maximum Rating

Item	Symbol	Value	Unit
Supply voltage	V _{cc}	−0.3 to +7.0	V
Input voltage	V _{in}	−0.3 to V _{cc} + 0.3	V
Operating temperature	T _{opr}	−20 to +75	°C
Storage temperature	T _{stg}	−55 to +150	°C

Note: DC and AC characteristics for 10 MHz version are preliminary values.

17.2 DC Characteristics (V_{CC} = 5 V ± 5%, V_{SS} = 0 V, T_a = -20°C to +75°C)

Item	Symbol	Min	Type	Max	Unit	Condition
Input high voltage (EXTAL, RES, NMI, IRQ0, IRQ1)	V _{IHI}	V _{CC} - 0.6	-	V _{CC} + 0.3	V	-
Input high voltage (All inputs other than EXTAL, RES, NMI, IRQ0, IRQ1)	V _{IHZ}	2.1	-	V _{CC} + 0.3	V	-
Input low voltage (EXTAL)	V _{ILO}	-0.3	-	0.6	V	-
Input low voltage (RES, NMI, IRQ0, IRQ1)	V _{ILI}	-0.3	-	0.6	V	-
Input low voltage (All inputs other than EXTAL, RES, NMI, IRQ0, IRQ1)	V _{IL2}	-0.3	-	0.8	V	-
Output high voltage (All outputs)	V _{OH}	2.4	-	-	V	I _{OH} = -200 μA
		V _{CC} - 1.2	-	-		I _{OH} = -20 μA
Output low voltage (DONE)	V _{OLI}	-	-	0.45	V	I _{OL} = 6.4 mA
Output low voltage (All outputs other than DONE)	V _{OL2}	-	-	2.0	V	I _{OL} = 3.2 mA
Input leakage current (All inputs other than XTAL and EXTAL)	I _{IL}	-	-	2.0	μA	V _{in} = 0.7 to V _{CC} - 0.7V
Three-state leakage current	I _{TL}	-	-	2.0	μA	V _{in} = 0.7 to V _{CC} - 0.7V
Open-drain input current (off)	I _{OD}	-	-	1.0	μA	-
Current dissipation (Normal operation)	I _{CC}	-	60	90	mA	f = 8 MHz
		-	70	110		f = 10 MHz

DC Characteristics ($V_{CC} = 5\text{ V} \pm 5\%$, $V_{SS} = 0\text{ V}$, $T_a = -20^\circ\text{C}$ to $+75^\circ\text{C}$) (cont.)

Item	Symbol	Min	Type	Max	Unit	Condition
Current dissipation (Sleep mode)	I_{CC}	—	40	65	mA	$f = 8\text{ MHz}$
		—	45	80		$f = 10\text{ MHz}$
Current dissipation (System stop mode)		—	20	45	mA	$f = 8\text{ MHz}$
		—	25	55		$f = 10\text{ MHz}$
Pin capacity	C_P	—	—	15	pF	$V_{in} = 0\text{ V}$ $f = 1\text{ MHz}$ $T_a = 25^\circ\text{C}$
Oscillation limit resistance	R_S	—	—	500	Ω	$f = 1\text{ MHz}$
		—	—	60		$f = 4\text{ MHz}$
		—	—	20		$f = 8\text{ MHz}$
		—	—	15		$f = 10\text{ MHz}$

17.3 AC Characteristics (V_{CC} = 5 V ±5%, V_{SS} = 0 V, T_a = −20°C to +75°C)

Item	Symbol	8 MHz		10 MHz		Unit	Reference Timing Chart	
		Min	Max	Min	Max			
Clock	Clock cycle time	t _{cyc}	125	1000	100	1000	ns	Figure 17-1
	Clock width low	t _{CL}	50	-	40	-	ns	
	Clock width high	t _{CH}	50	-	40	-	ns	
	Clock rise time	t _{Cr}	-	15	-	12	ns	
	Clock fall time	t _{Cf}	-	15	-	12	ns	
	E clock delay time	t _{ED}	-	15	-	13	ns	Figure 17-2
	Input clock rise time	t _{EXr}	-	25	-	10	ns	Figure 17-3
	Input clock fall time	t _{EXf}	-	25	-	10	ns	
CPU Bus Cycle	Address delay time 1	t _{AD1}	-	60	-	60	ns	Figure 17-4
	Address delay time 2	t _{AD2}	30	-	20	-	ns	
	Address delay time to high impedance 1	t _{ADZ1}	-	50	-	50	ns	
	Address delay time to high impedance 2	t _{ADZ2}	-5	-	-5	-	ns	
	Read data setup time	t _{RDS}	40	-	35	-	ns	
	Read data hold time	t _{RDH}	5	-	5	-	ns	
	Write data setup time	t _{WDS}	5	-	5	-	ns	Figure 17-5
	Write data hold time	t _{WDH}	10	-	10	-	ns	
	Write data delay time	t _{WDD}	-	60	-	55	ns	
	Setup time from $\overline{AS}$	t _{ASS}	10	-	7	-	ns	Figure 17-4
	Hold time from $\overline{AS}$ 1	t _{ASH1}	30	-	25	-	ns	
	Hold time from $\overline{AS}$ 2	t _{ASH2}	10	-	10	-	ns	
	$\overline{AS}$ delay time	t _{ASD}	-	45	-	45	ns	
	R/ $\overline{W}$ delay time	t _{AD1}	-	60	-	60	ns	
	PF delay time	t _{AD1}	-	60	-	60	ns	

AC Characteristics ($V_{CC} = 5\text{ V} \pm 5\%$, $V_{SS} = 0\text{ V}$, $T_a = -20^\circ\text{C}$ to $+75^\circ\text{C}$) (cont.)

Item	Symbol	8 MHz		10 MHz		Unit	Reference Timing Chart	
		Min	Max	Min	Max			
CPU Bus Cycle (cont.)	$\overline{S}/\overline{U}$ delay time	t_{AD1}	-	60	-	60	ns	Figure 17-4
	ST2, ST1, ST0 delay time	t_{AD1}	-	60	-	60	ns	
	PCS1, PCS0 delay time 1	t_{PCSD1}	-	60	-	60	ns	
	$\overline{HDS}$, $\overline{LDS}$ delay time 1	t_{DSD1}	-	45	-	45	ns	
	$\overline{HDS}$, $\overline{LDS}$ delay time 2	t_{DSD2}	-	45	-	45	ns	Figure 17-5
	$\overline{HDS}$, $\overline{LDS}$ delay time 3	t_{DSD3}	-	45	-	45	ns	Figure 17-4
	$\overline{AS}$ width high 1	t_{ASW1}	95	-	60	-	ns	Figure 17-5
	$\overline{AS}$ width high 2	t_{ASW2}	120	-	105	-	ns	Figure 17-6
	$\overline{HDS}$, $\overline{LDS}$ width low	t_{DSW}	90	-	65	-	ns	Figure 17-10
	$\overline{WAIT}$ setup time	t_{WTS}	35	-	35	-	ns	Figure 17-16
	$\overline{WAIT}$ hold time	t_{WTH}	10	-	7	-	ns	
	$\overline{BRTRY}$ setup time	t_{BRS}	40	-	40	-	ns	Figure 17-17
$\overline{BRTRY}$ hold time	t_{BRH}	20	-	0	-	ns		
Refresh	Refresh address delay time	t_{RAD}	-	60	-	60	ns	Figure 17-18
	Refresh address delay time to high impedance	t_{RADZ}	-	50	-	50	ns	
	Refresh address setup time from $\overline{AS}$	t_{RASS}	10	-	7	-	ns	
	Refresh address hold time from $\overline{AS}$	t_{RASH}	30	-	25	-	ns	
Interrupt	$\overline{NMI}$ pulse width	t_{NMIW}	2.0	-	2.0	-	tcyc	Figure 17-19
	$\overline{IRQ0}$, $\overline{IRQ1}$ pulse width	t_{IRQW}	2.0	-	2.0	-	tcyc	Figure 17-20
	$\overline{IRQ0}$, $\overline{IRQ1}$ setup time	t_{IRQS}	50	-	50	-	ns	
	$\overline{IACK}$ delay time	t_{IACKD}	-	40	-	40	ns	Figure 17-21

AC Characteristics (Vcc = 5 V $\pm$ 5%, Vss = 0 V, Ta = -20°C to +75°C) (cont.)

Item		Symbol	8 MHz		10 MHz		Unit	Reference Timing Chart
			Min	Max	Min	Max		
Bus Release	$\overline{\text{BREQ}}$ setup time	t ^{BRQS}	40	-	35	-	ns	Figure 17-22
	$\overline{\text{BREQ}}$ hold time	t ^{BRQH}	10	-	10	-	ns	
	PCS1, PCS0 delay time 2	t ^{PCSD2}	-	85	-	85	ns	
	Address delay time to high impedance 3	t ^{ADZ3}	-	50	-	45	ns	
	$\overline{\text{BACK}}$ delay time	t ^{BACKD}	-	45	-	40	ns	
	$\overline{\text{AS}}$ input setup time	t ^{ASIS}	40	-	40	-	ns	Figure 17-23
	Address setup time	t ^{ADS}	40	-	35	-	ns	
	Address hold time	t ^{ADH}	40	-	35	-	ns	
		$\overline{\text{WAIT}}$ output delay time	t ^{WTOD}	-	40	-	40	ns
DMAC	$\overline{\text{DREQ}}$ setup time	t ^{DRQS}	40	-	35	-	ns	Figure 17-25
	$\overline{\text{DREQ}}$ hold time	t ^{DRQH}	10	-	10	-	ns	
	$\overline{\text{DREQ}}$ width low	t ^{DRQW}	2.0	-	2.0	-	t _{cy}	
	$\overline{\text{DACK}}$ delay time 1	t ^{DACD1}	-	50	-	45	ns	
	$\overline{\text{DACK}}$ delay time 2	t ^{DACD2}	-	50	-	45	ns	
	$\overline{\text{DACK}}$ delay time 3	t ^{DACD3}	-	50	-	45	ns	
	$\overline{\text{DONE}}$ delay time 1	t ^{DOND1}	-	50	-	45	ns	
	$\overline{\text{DONE}}$ delay time 2	t ^{DOND2}	-	50	-	45	ns	
	$\overline{\text{DONE}}$ setup time	t ^{DONS}	40	-	35	-	ns	
		$\overline{\text{DONE}}$ hold time	t ^{DONH}	10	-	5	-	ns

AC Characteristics ($V_{CC} = 5\text{ V} \pm 5\%$, $V_{SS} = 0\text{ V}$, $T_a = -20^\circ\text{C}$ to $+75^\circ\text{C}$) (cont.)

Item	Symbol	8 MHz		10 MHz		Unit	Reference Timing Chart
		Min	Max	Min	Max		
Timer	Timer clock width	t_{TMC1}	2.0	—	2.0	—	t_{cyc} Figure 17-26
		t_{TMC2}	2.0	—	2.0	—	t_{cyc}
		t_{TMCKW}	8.0	—	8.0	—	t_{cyc}
	Timer clock setup time	t_{TMCKS}	30	—	25	—	ns
	Timer trigger pulse width	t_{TMIWL}	2.0	—	2.0	—	t_{cyc}
		t_{TMIWH}	2.0	—	2.0	—	t_{cyc}
	Timer trigger setup time	t_{TMIS}	35	—	30	—	ns
	Timer output delay time	t_{TMOD}	—	60	—	60	ns
ASCII	Transmit clock cycle time	t_{Tcyc}	2.5	—	2.5	—	t_{cyc} Figure 17-27
	Transmit clock width low	t_{TCLW}	1.0	—	1.0	—	t_{cyc}
	Transmit clock width high	t_{TCHW}	1.0	—	1.0	—	t_{cyc}
	Transmit clock fall time	t_{TCf}	—	50	—	50	ns
	Transmit clock rise time	t_{TCr}	—	50	—	50	ns
	Transmit clock delay time	t_{TCD}	—	60	—	50	ns
	Transmit data delay time 1	t_{TDD1}	—	60	—	50	ns
	Transmit data delay time 2	t_{TDD2}	1.5	2.5	1.5	2.5	t_{cyc}
	Receive clock cycle time	t_{Rcyc}	2.5	—	2.5	—	t_{cyc}
	Receive clock width low	t_{RCLW}	1.0	—	1.0	—	t_{cyc}
	Receive clock width high	t_{RCHW}	1.0	—	1.0	—	t_{cyc}
	Receive clock fall time	t_{RCf}	—	50	—	50	ns
	Receive clock rise time	t_{RCr}	—	50	—	50	ns
	Receive clock delay time	t_{RCD}	—	60	—	50	ns
	Receive data setup time 1	t_{RDS1}	40	—	35	—	ns
	Receive data hold time 1	t_{RDH1}	10	—	10	—	ns

AC Characteristics ($V_{cc} = 5\text{ V} \pm 5\%$, $V_{ss} = 0\text{ V}$, $T_a = -20^\circ\text{C}$ to $+75^\circ\text{C}$) (cont.)

Item	Symbol	8 MHz		10 MHz		Unit	Reference Timing Chart	
		Min	Max	Min	Max			
ASCI (cont.)	Receive data setup time 2	t _{RDS2}	40	-	40	-	ns	Figure 17-27
	Receive data hold time 2	t _{RDH2}	10	-	10	-	ns	
	RTS delay time	t _{RTSD}	-	60	-	55	ns	
	CTS width low	t _{CTSLW}	2.0	-	2.0	-	t _{cyc}	
	CTS width high	t _{CTSHW}	2.0	-	2.0	-	t _{cyc}	
	DCD width low	t _{DCDLW}	2.0	-	2.0	-	t _{cyc}	
	DCD width high	t _{DCDHW}	2.0	-	2.0	-	t _{cyc}	
Reset	RES setup time	t _{RESS}	30	-	30	-	ns	Figure 17-28
	RES hold time	t _{RESH}	0	-	0	-	ns	
	RES rise time	t _{Rr}	-	50 (Note)	-	50 (Note)	ms	
	RES fall time	t _{Rf}	-	50 (Note)	-	50 (Note)	ms	
	RES width low	t _{RESW}	12	-	12	-	t _{cyc}	

Note: $\overline{\text{RES}}$ rise and fall times are specified as 50 ns (max). However, if reset does not satisfy all other AC characteristics, its fall and rise time must be changed to satisfy these.

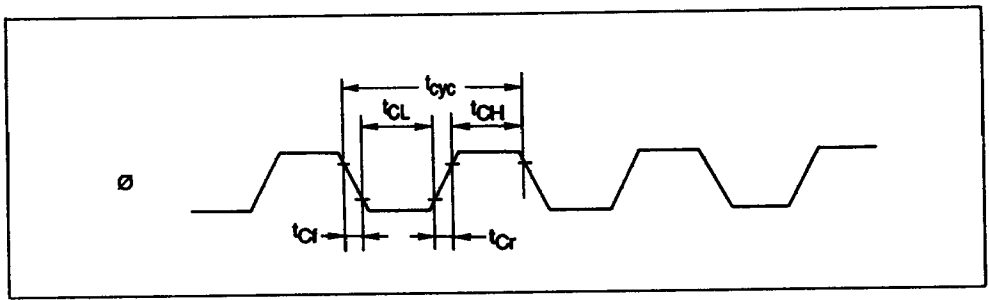


Figure 17-1. $\emptyset$ Clock Timing

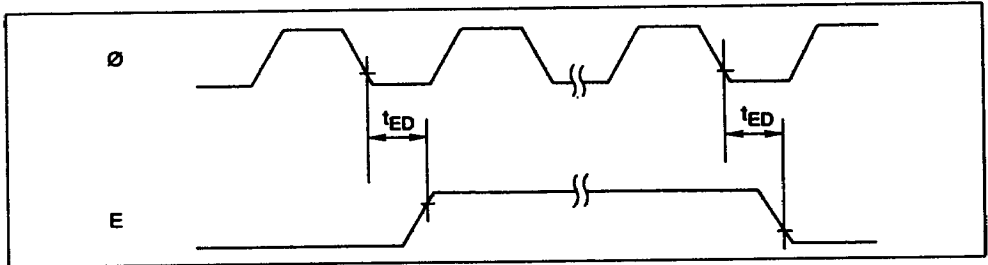


Figure 17-2. E Clock Timing

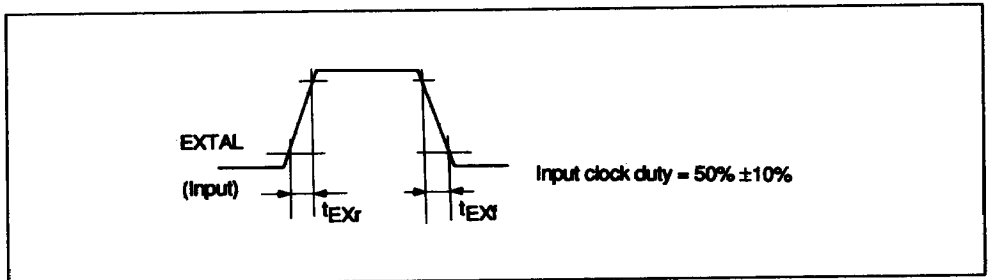


Figure 17-3. Input Clock Timing

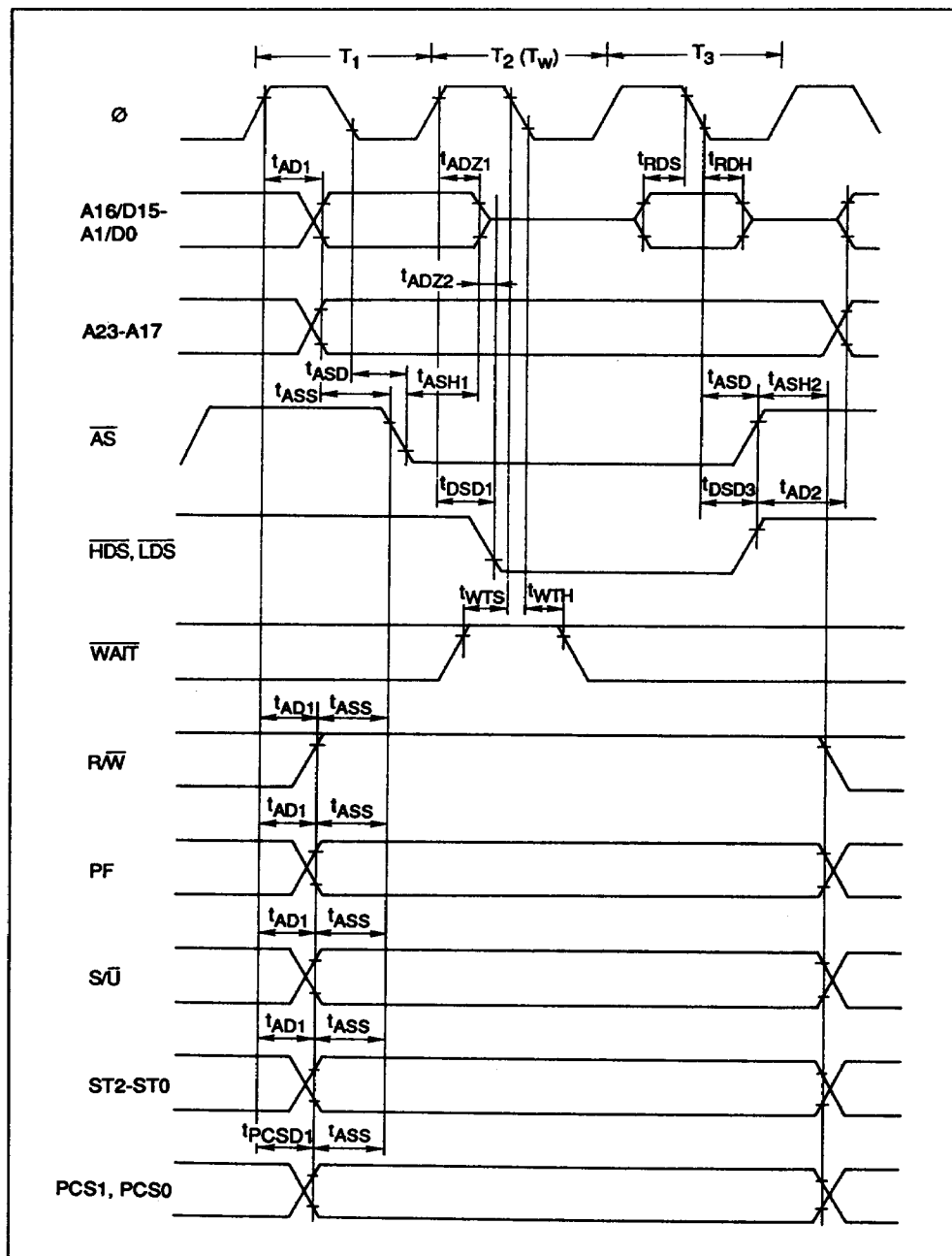


Figure 17-4. Read Cycle Timing (without T_p)

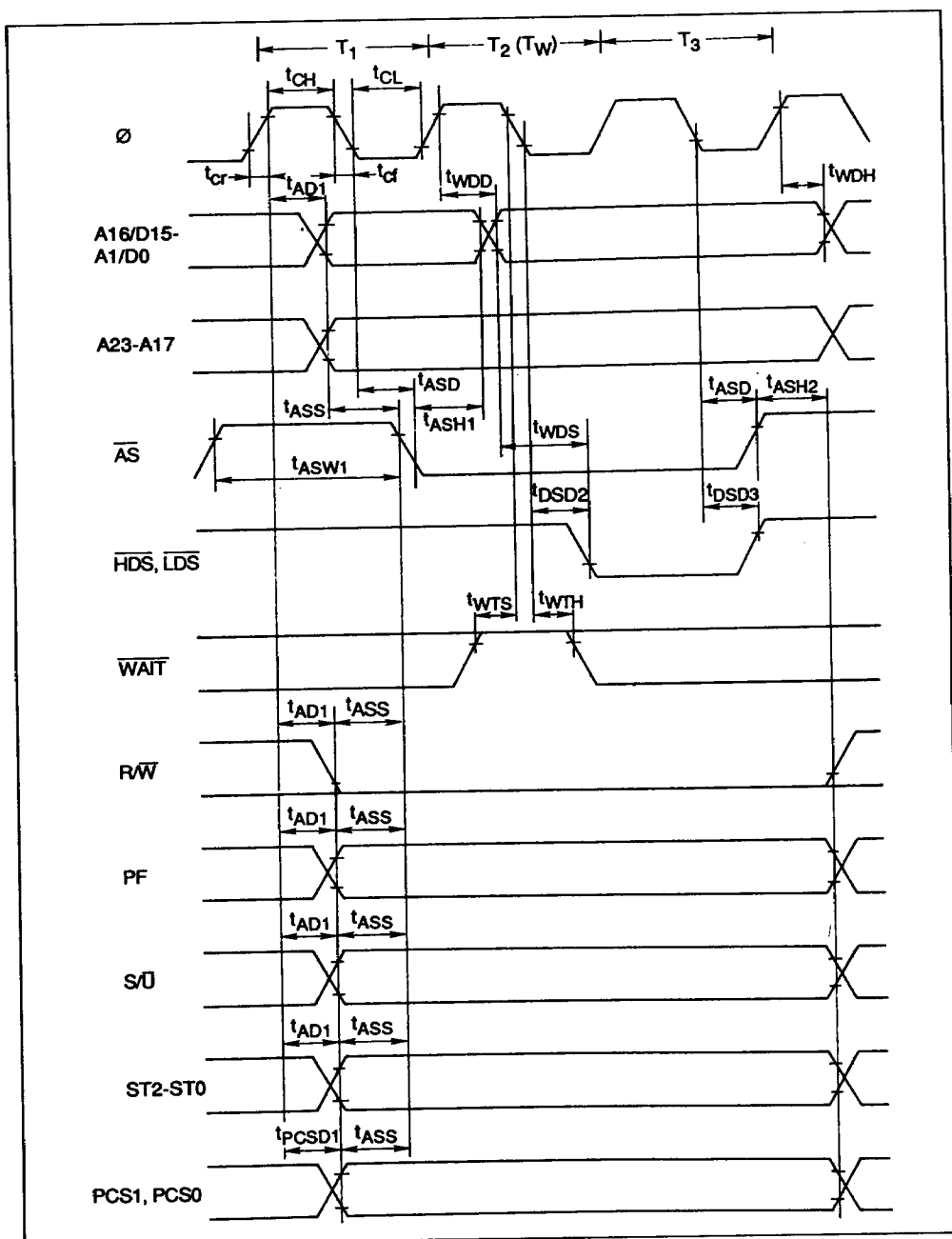


Figure 17-5. Write Cycle Timing (without T_p)

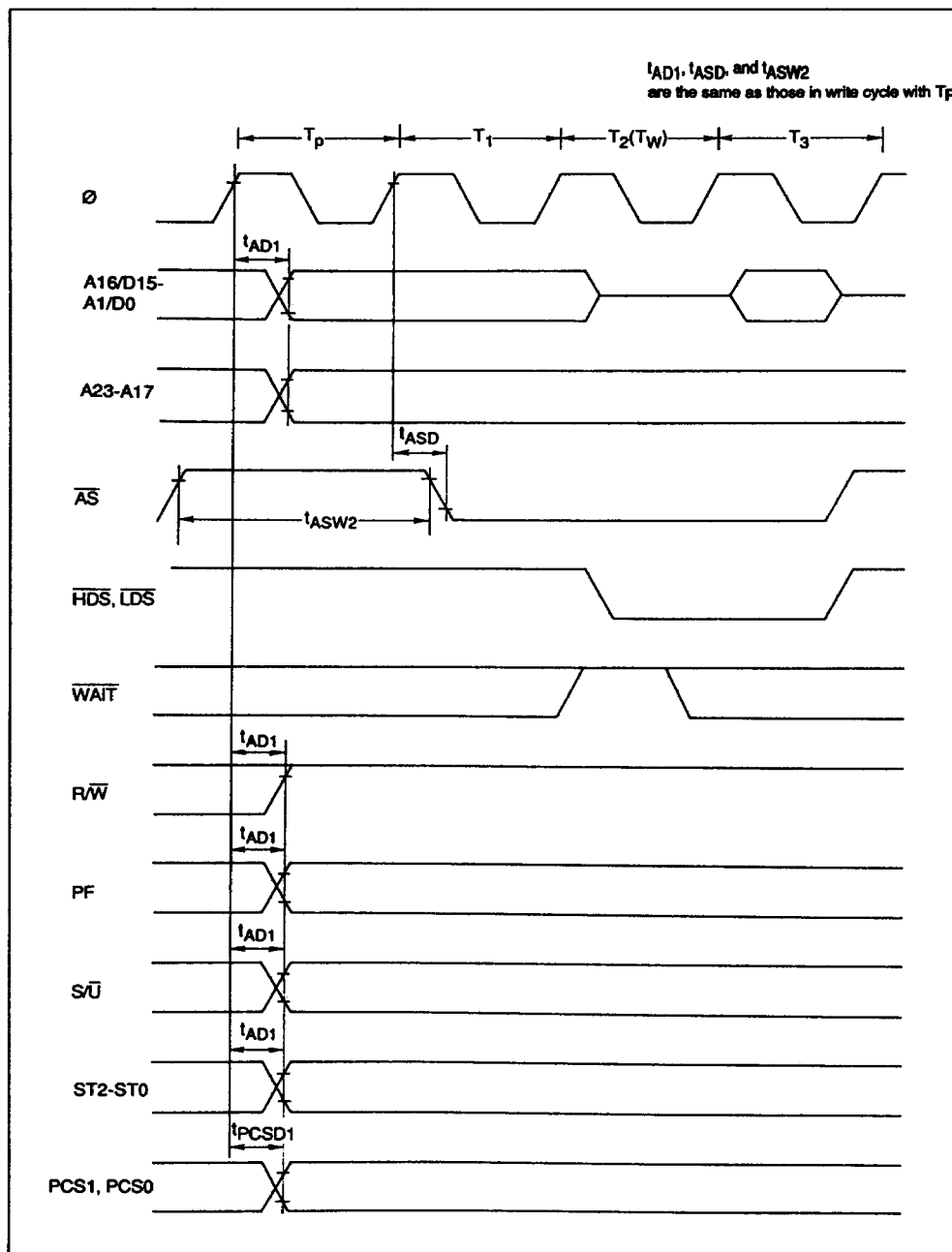


Figure 17-6. Read Cycle Timing (with T_p)

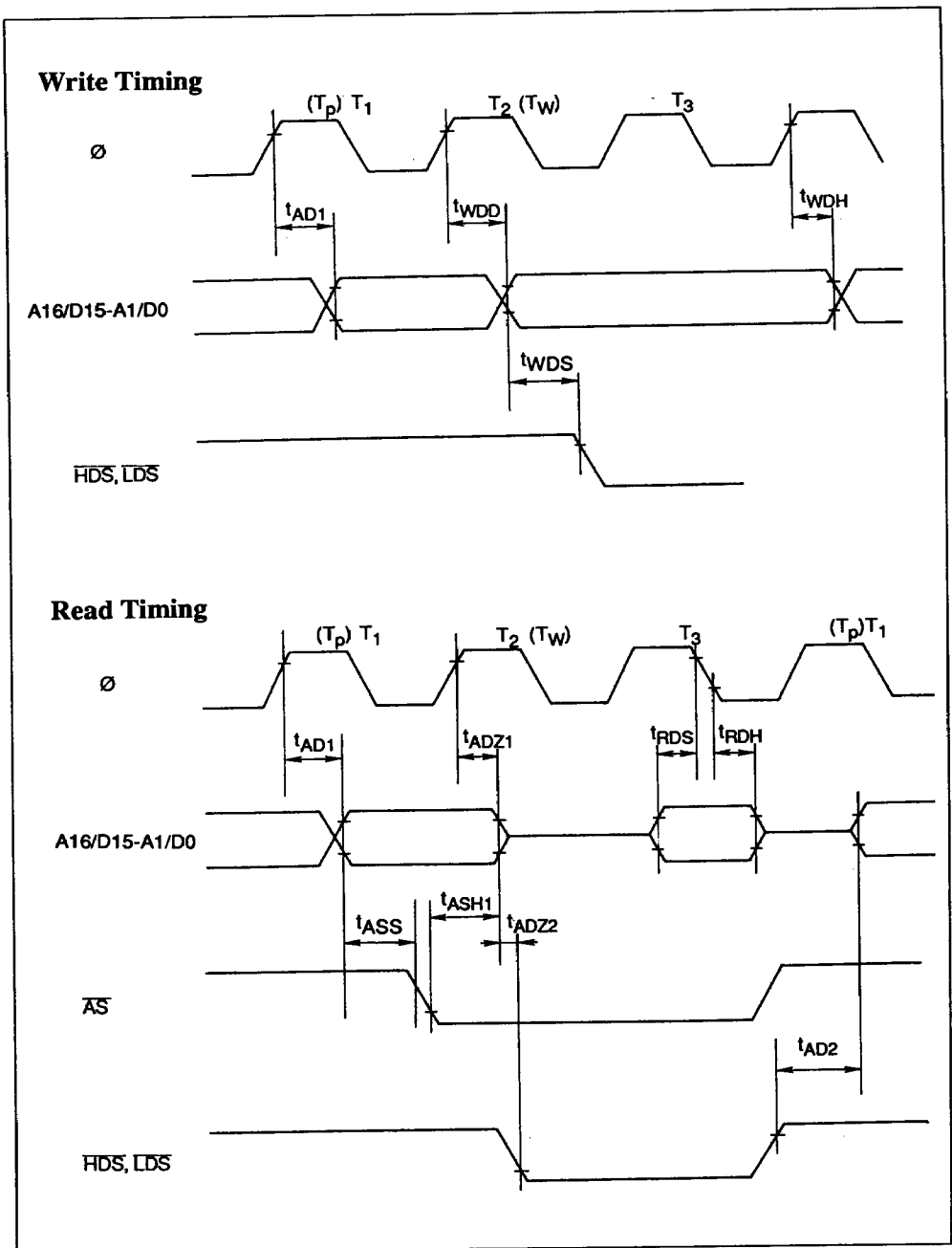


Figure 17-7. Address/Data Timing

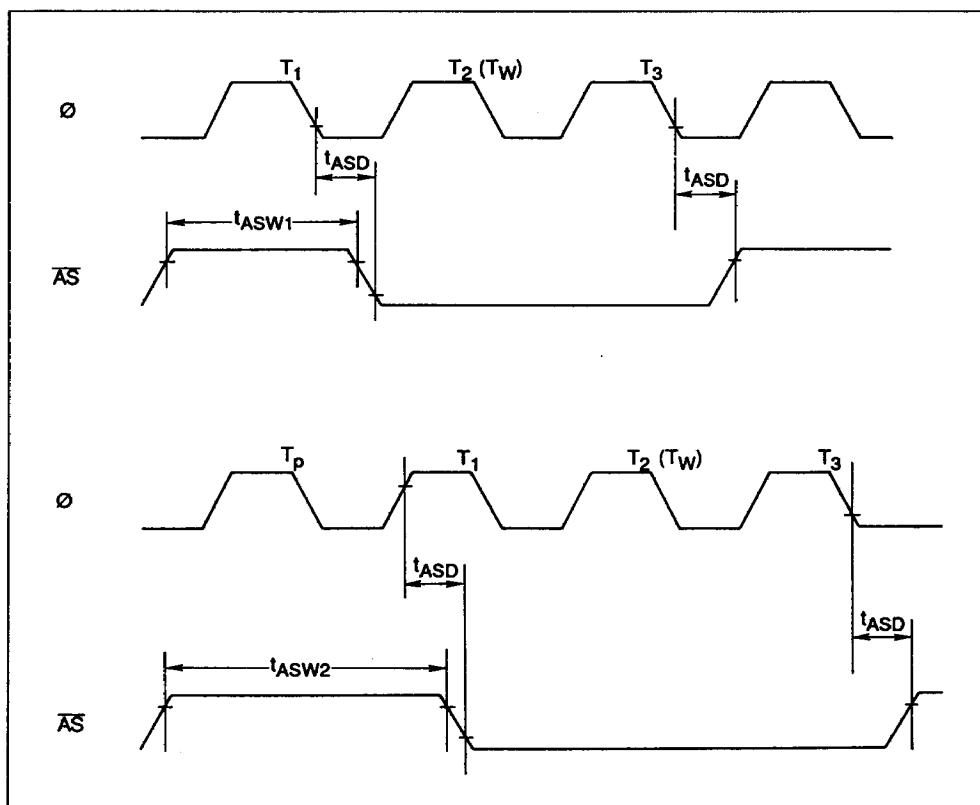


Figure 17-8. $\overline{AS}$ Timing

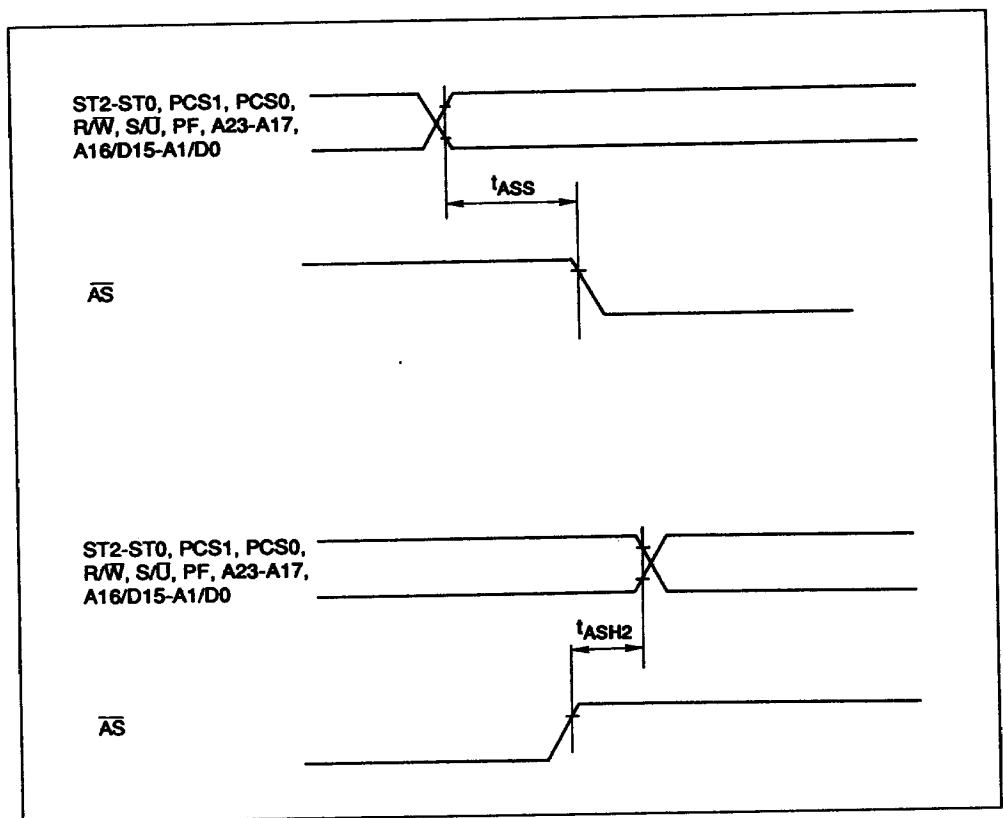


Figure 17-9. Control Signal Timing

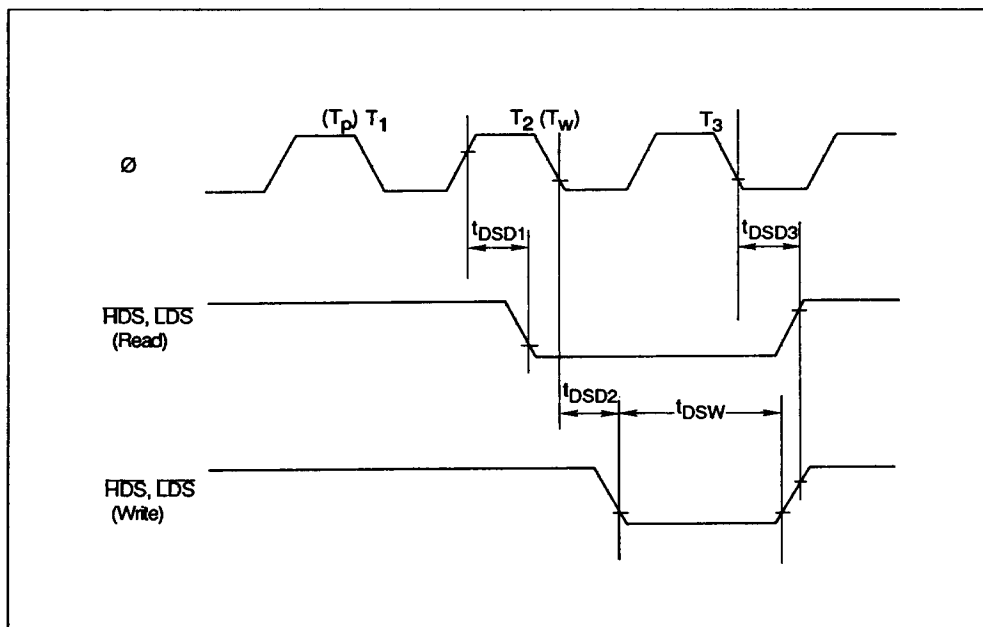


Figure 17-10. HDS, LDS Timing

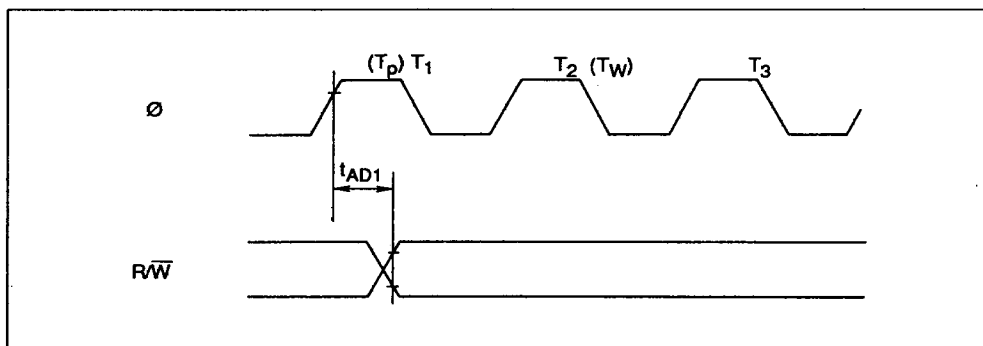


Figure 17-11. R/W Timing

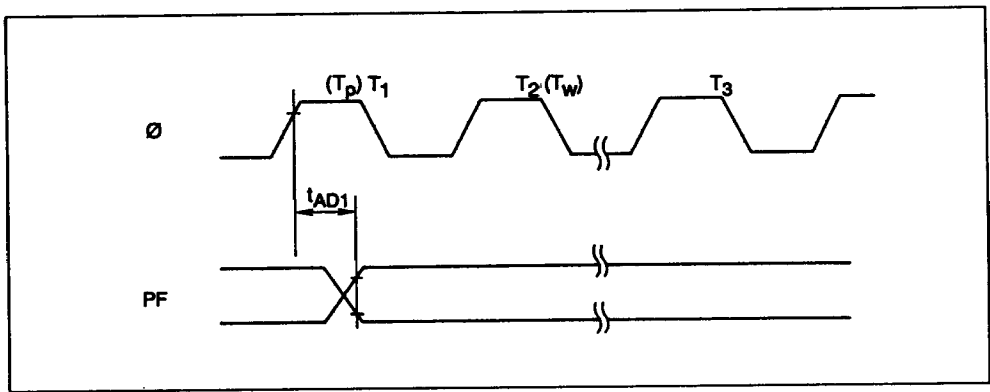


Figure 17-12. PF Timing

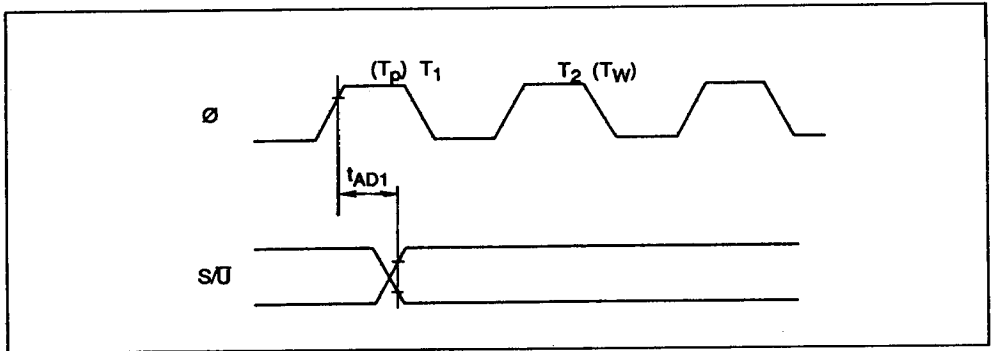


Figure 17-13. S/U Timing

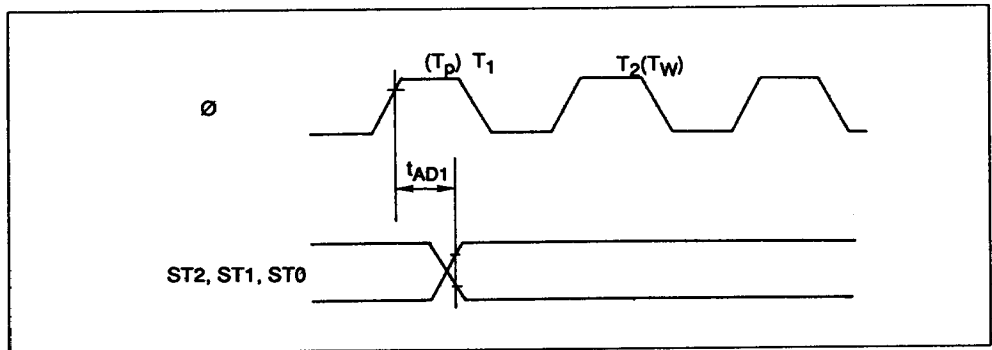


Figure 17-14. ST2, ST1, ST0 Timing

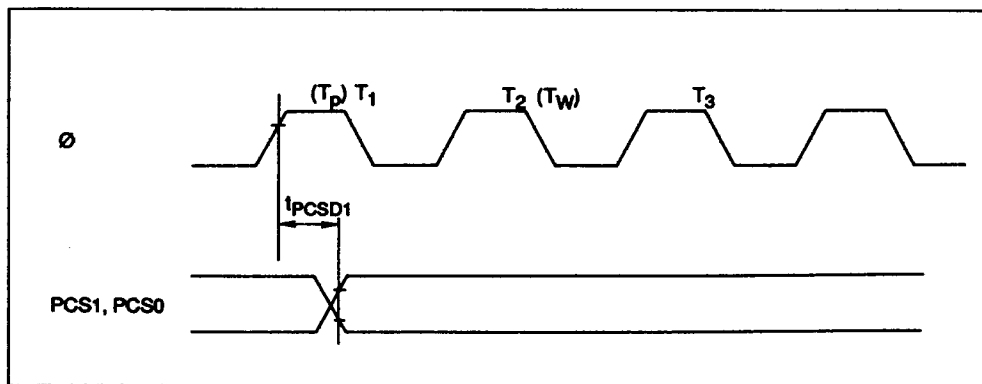


Figure 17-15. PCS1-PCS0 Timing

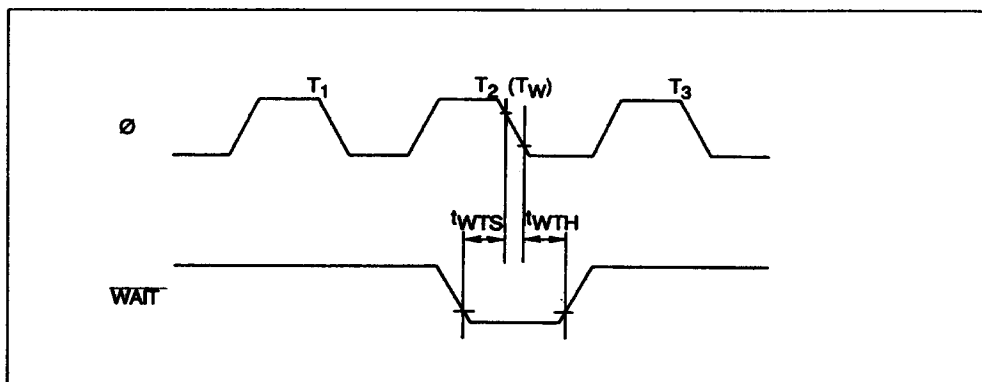


Figure 17-16. $\overline{\text{WAIT}}$ Input Timing

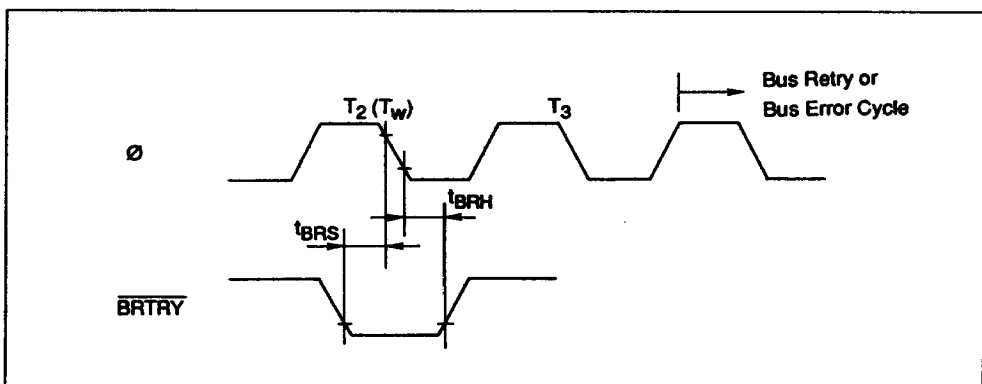


Figure 17-17. $\overline{\text{BRTRY}}$ Timing

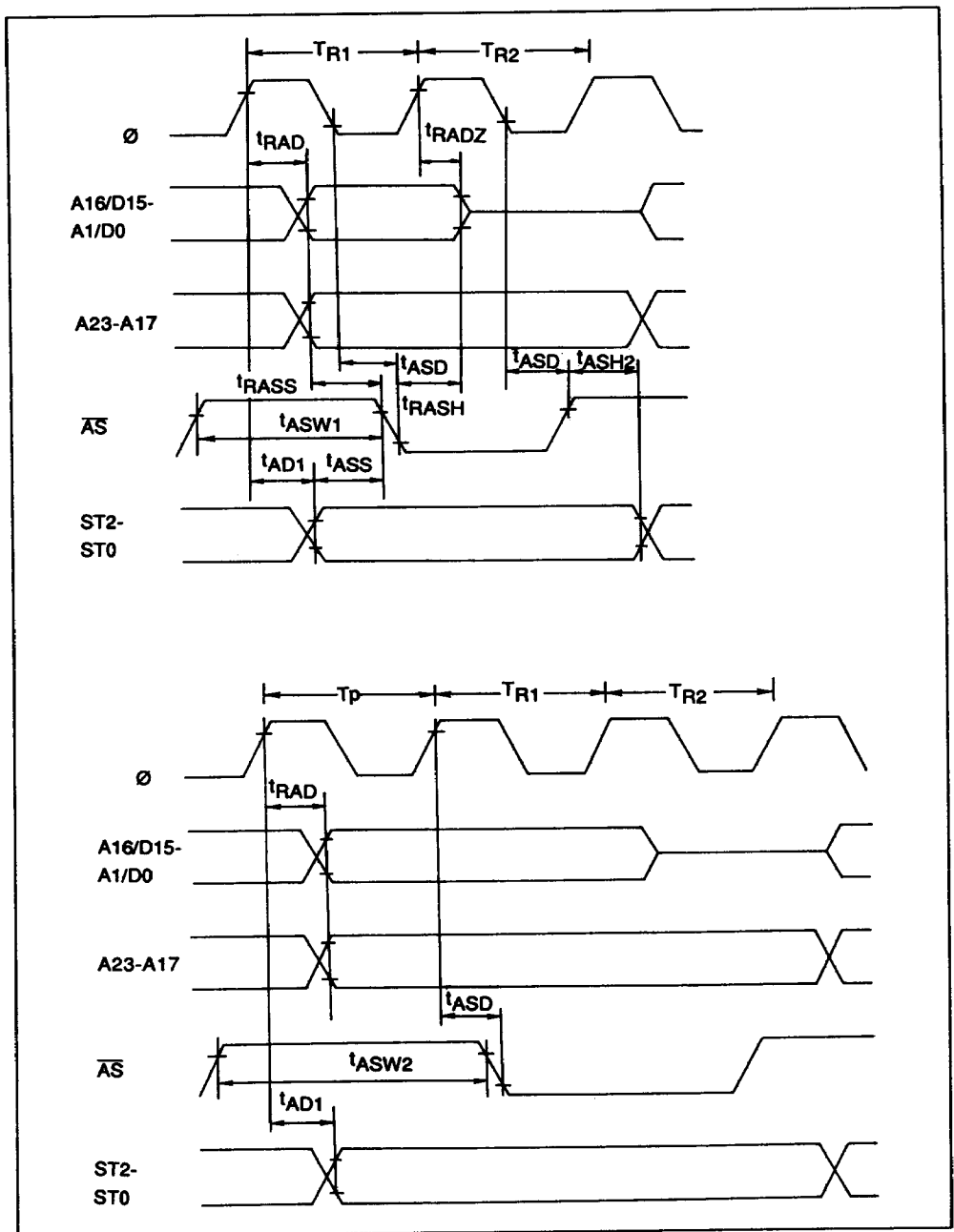


Figure 17-18. Refresh Timing (with or without T_w state)

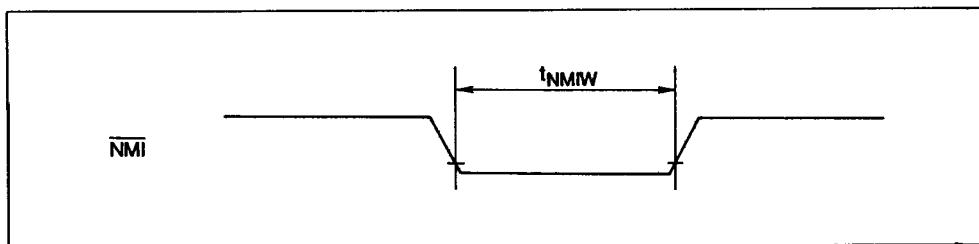


Figure 17-19. $\overline{\text{NMI}}$ Timing

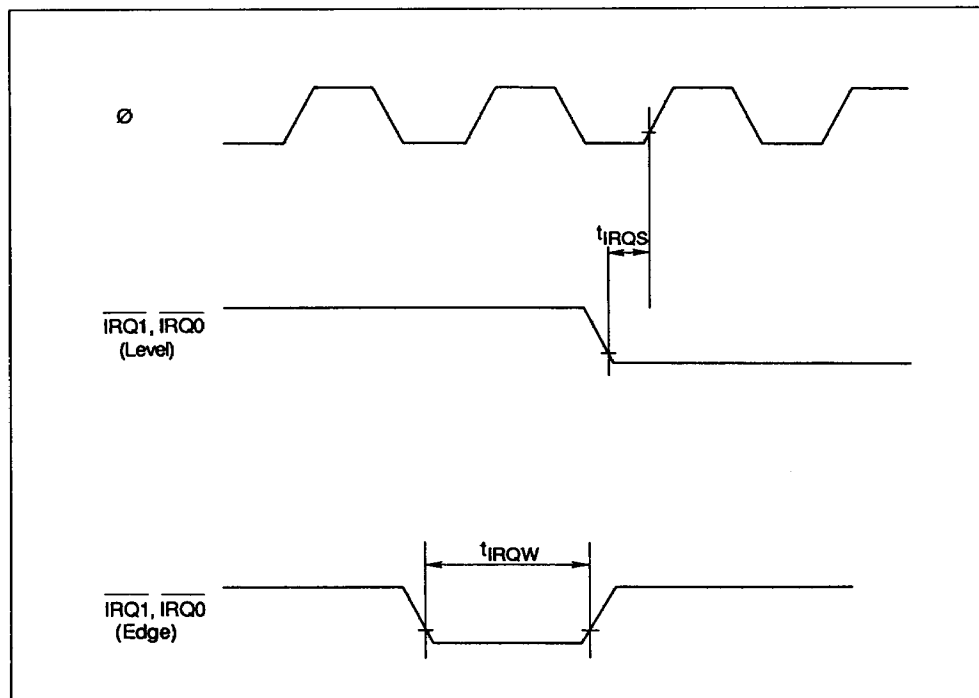


Figure 17-20. $\overline{\text{IRQ0}}, \overline{\text{IRQ1}}$ Timing

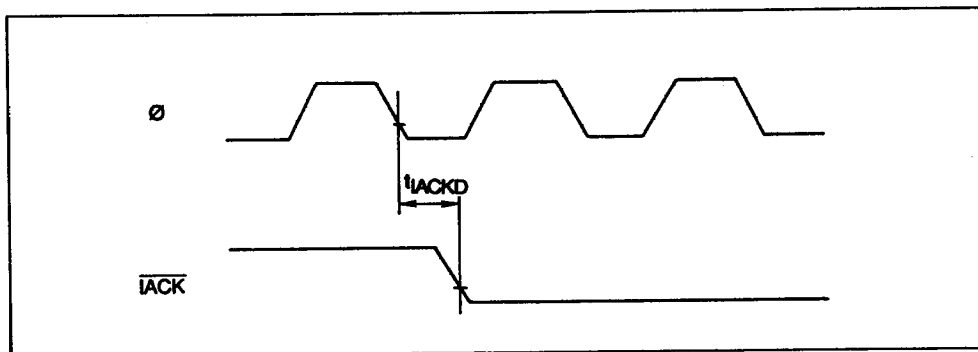


Figure 17-21. $\overline{IACK}$ Timing

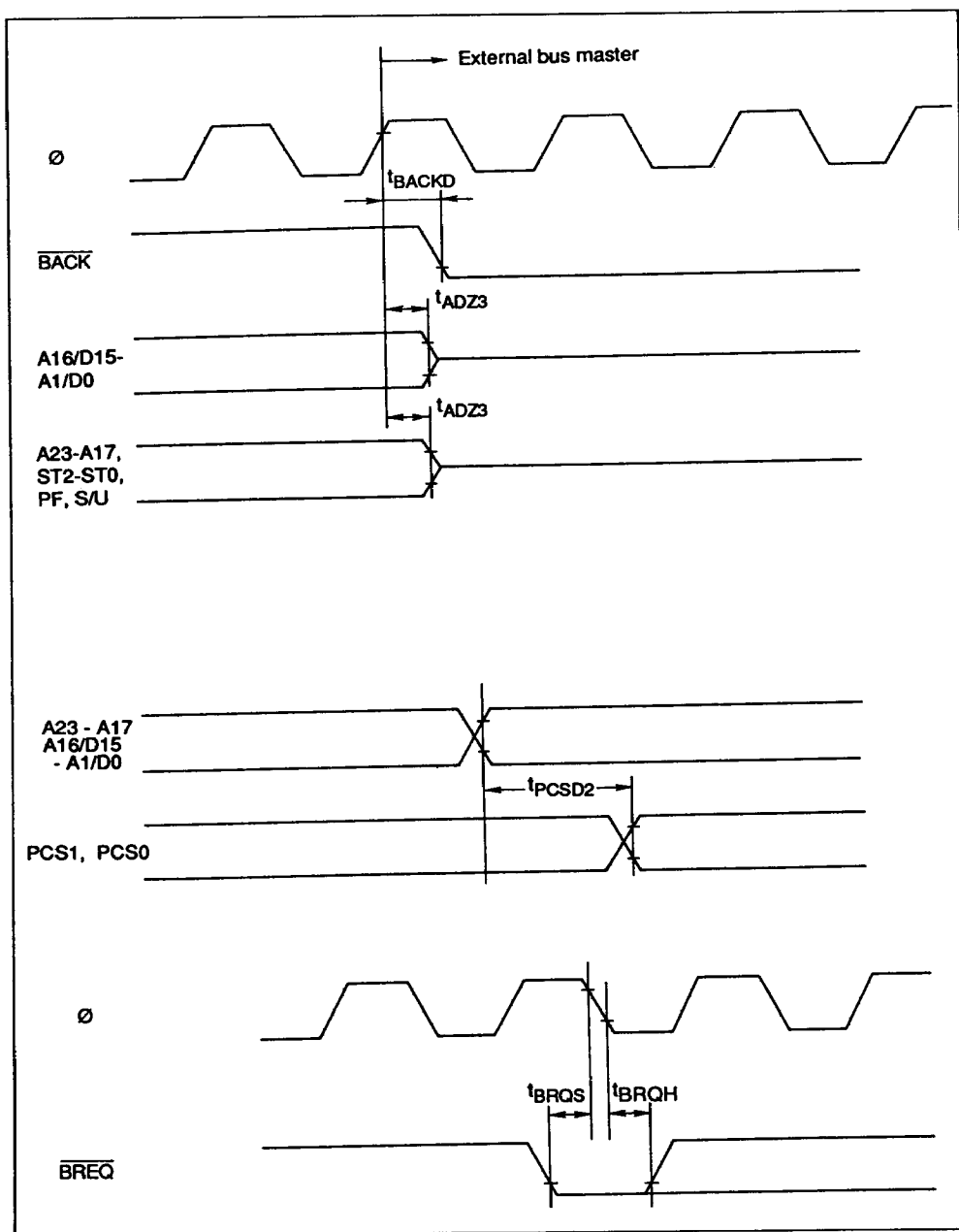


Figure 17-22. External Bus Master Bus Timing

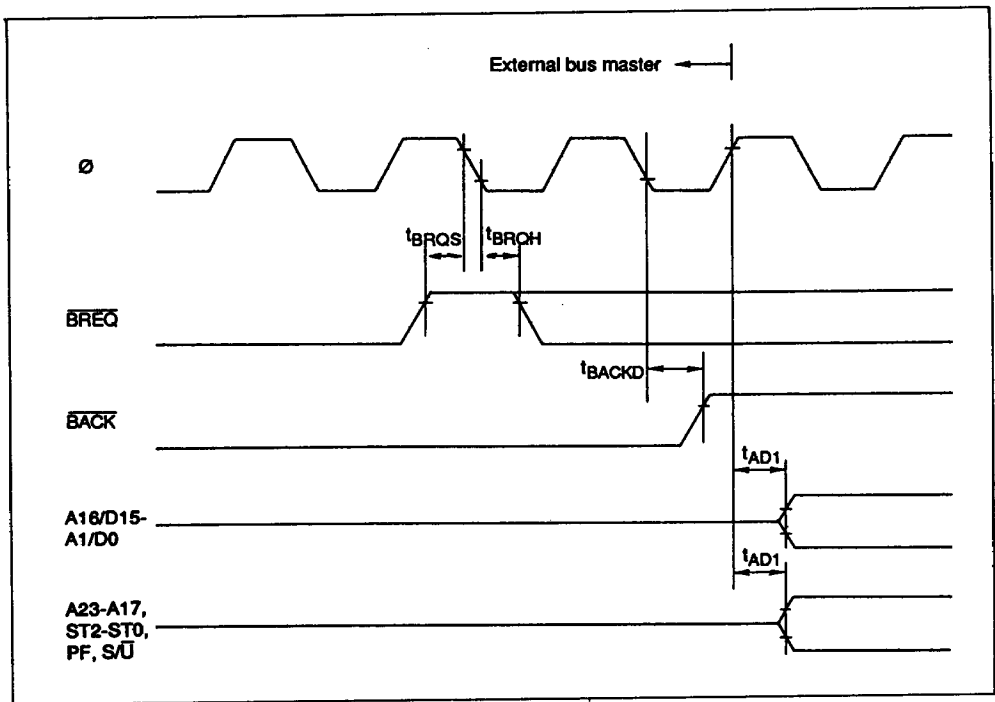


Figure 17-22. External Bus Master Bus Timing (cont.)

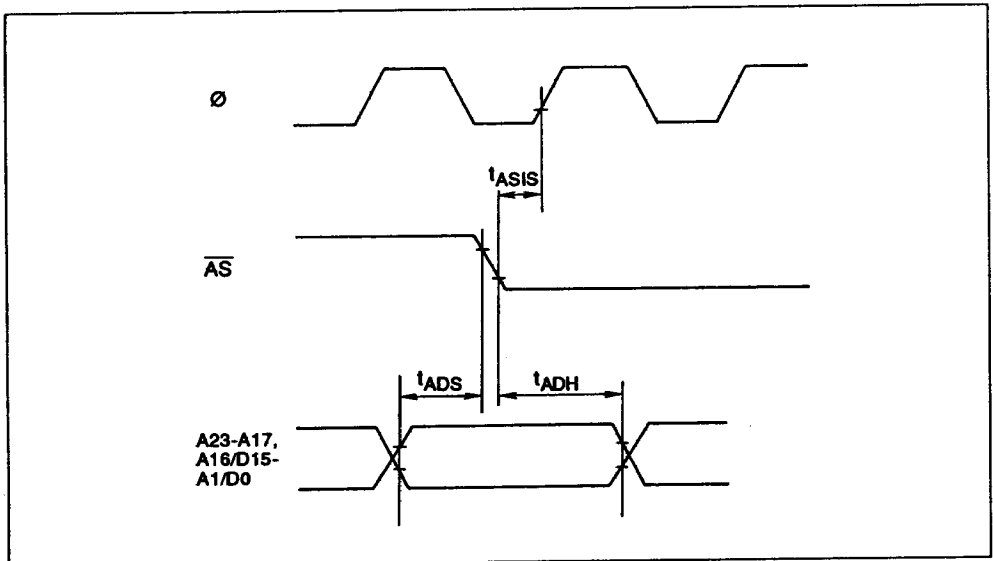


Figure 17-23. $\overline{AS}$, Address Input Timing (bus release)

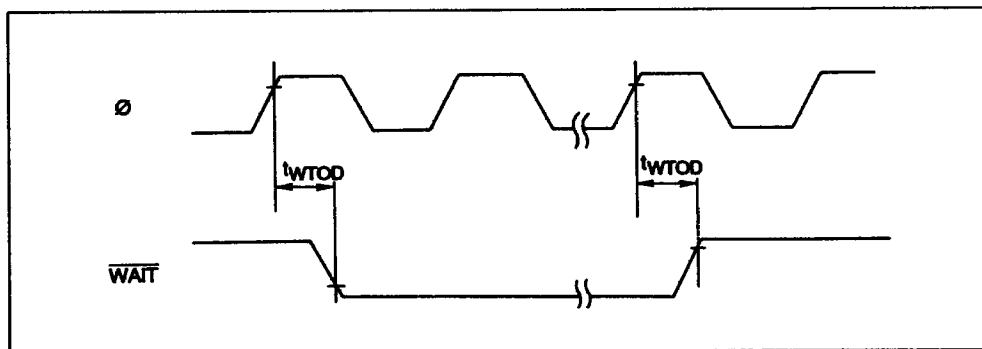


Figure 17-24. $\overline{\text{WAIT}}$ Output Timing

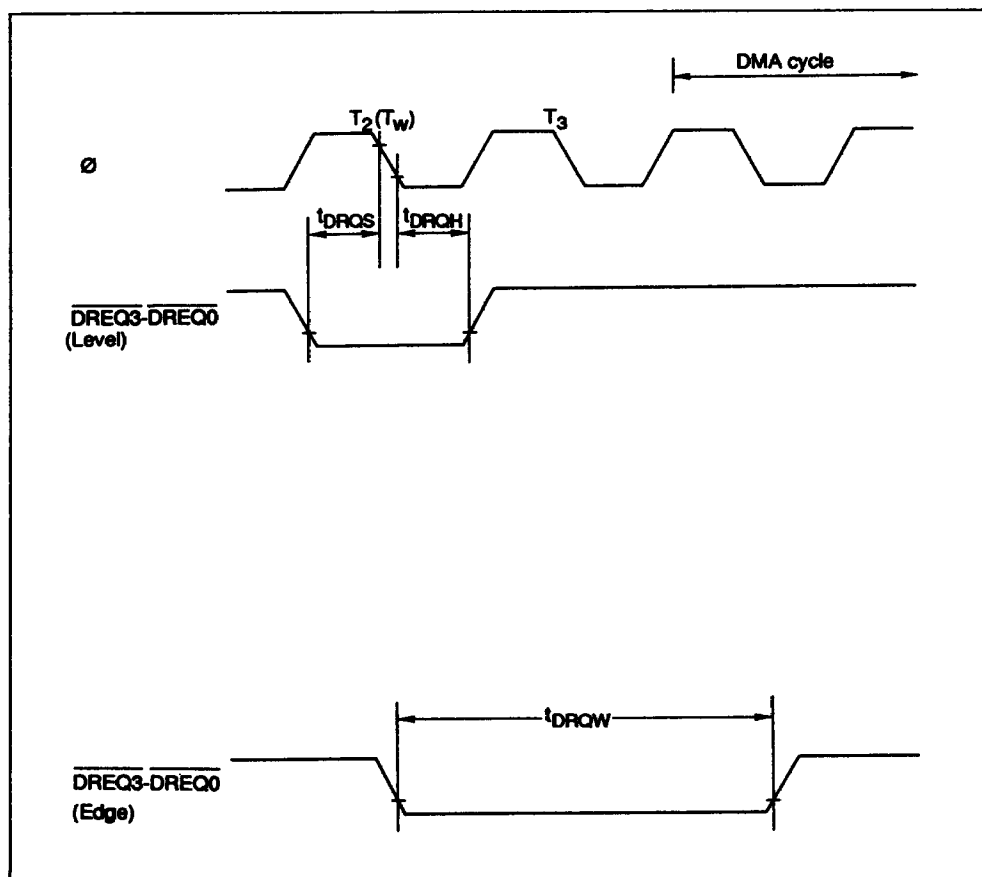


Figure 17-25. DMAC Timing

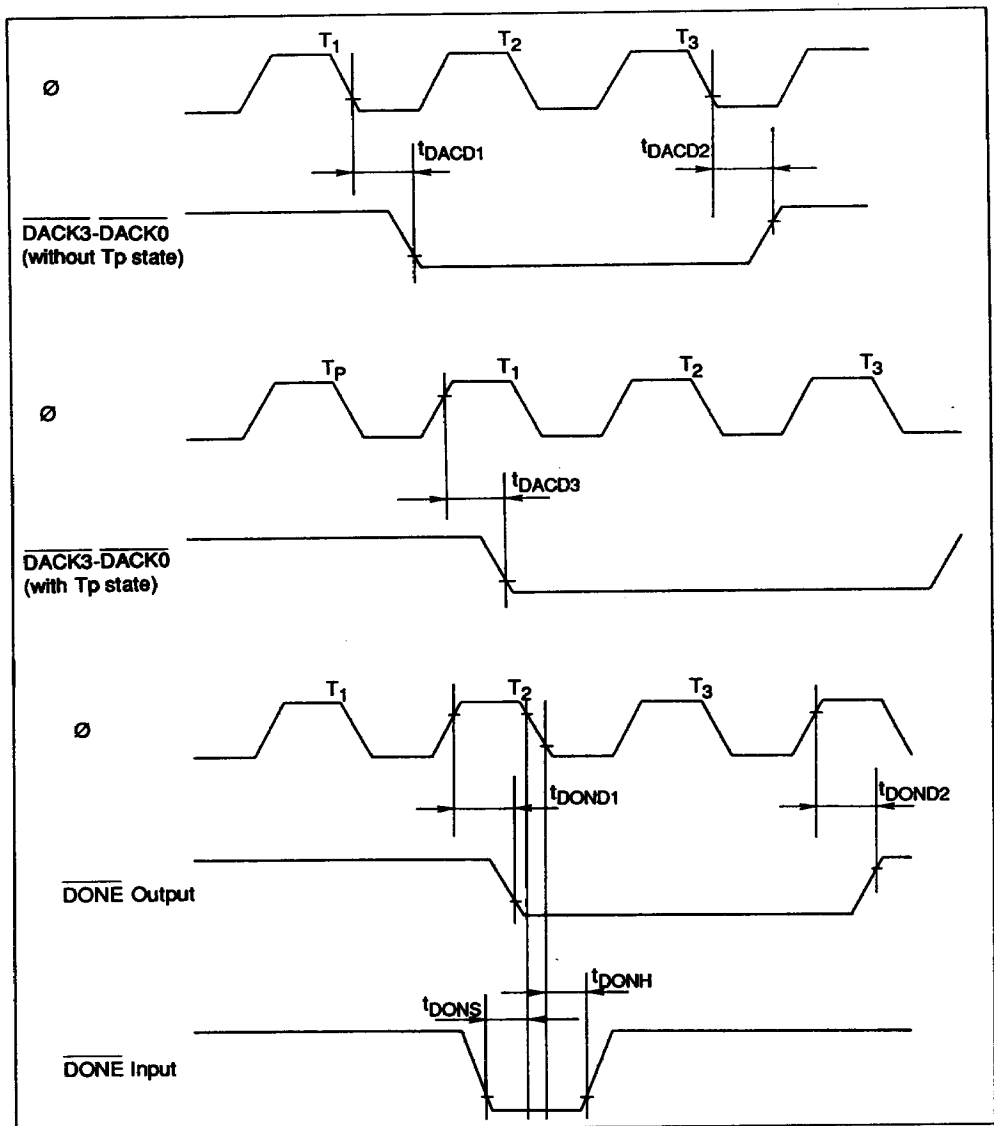
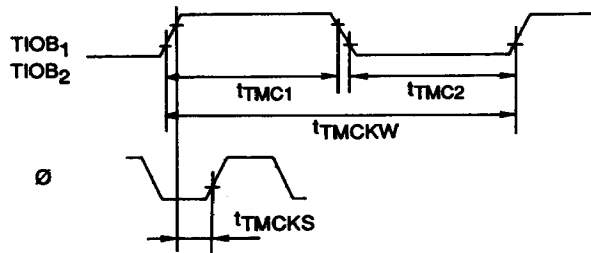
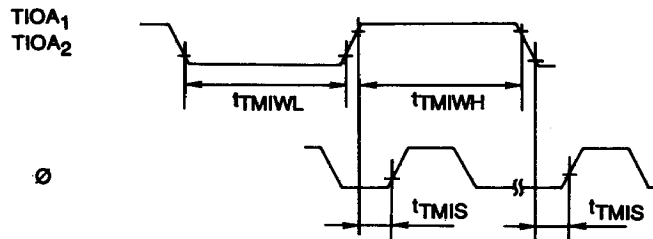


Figure 17-25. DMAC Timing (cont.)

Clock Input



Trigger Input



Timer Output

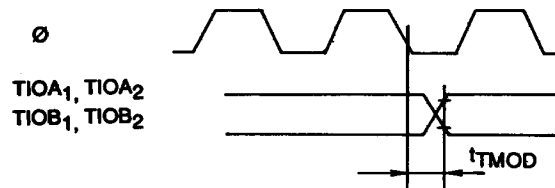
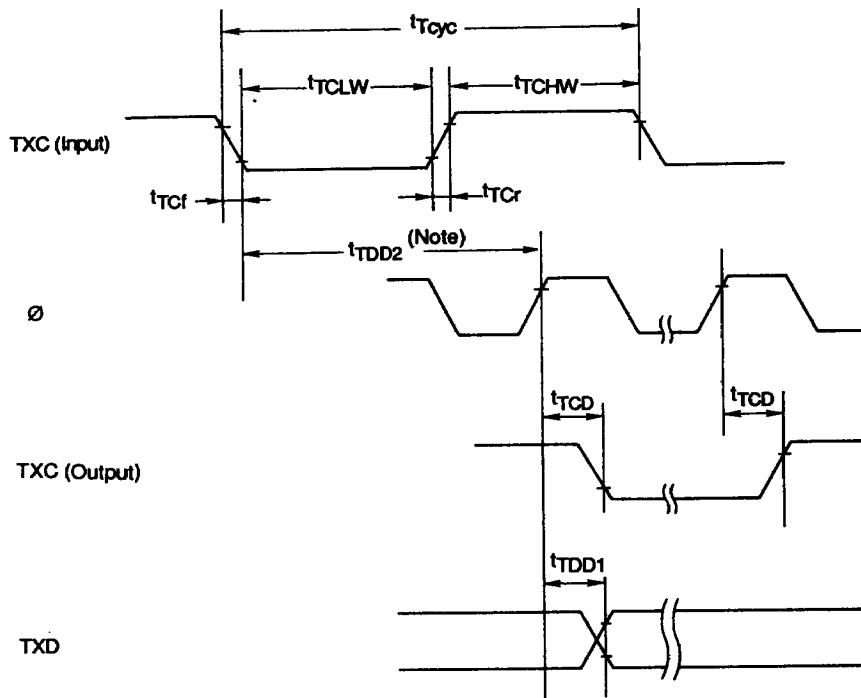


Figure 17-26. Timer Timing

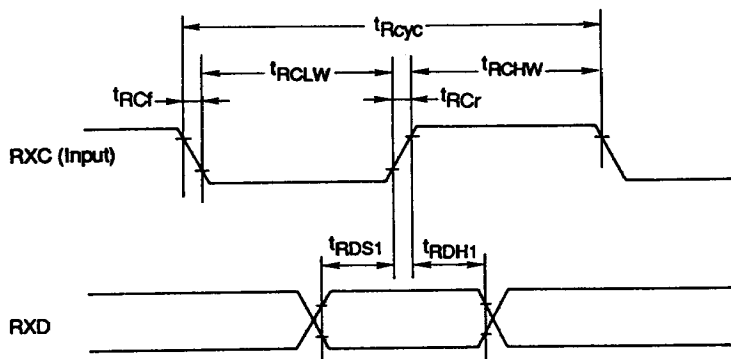
Transmission (TxC, TXD)



Note: TXD delay time in TxC input mode

Figure 17-27. ASCII Timing

Reception (RXC Input, RXD)



Reception (RXC Output, RXD)

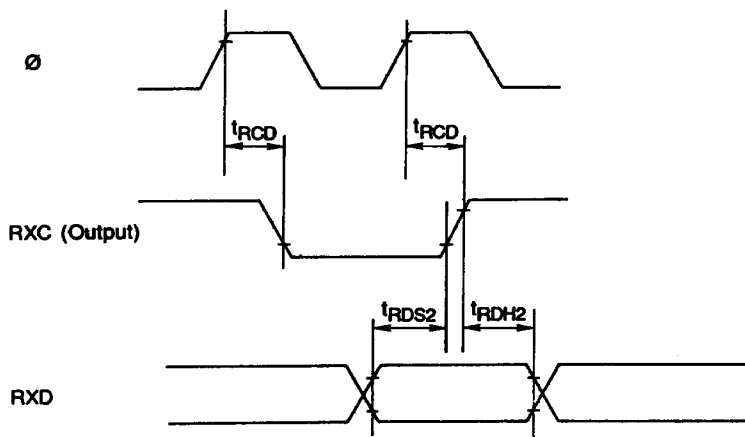
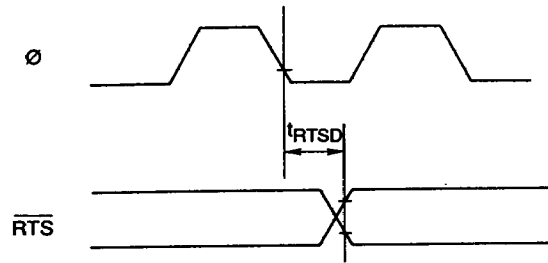


Figure 17-27. ASCII Timing (cont.)

$\overline{\text{RTS}}$



$\overline{\text{CTS}}, \overline{\text{DCD}}$

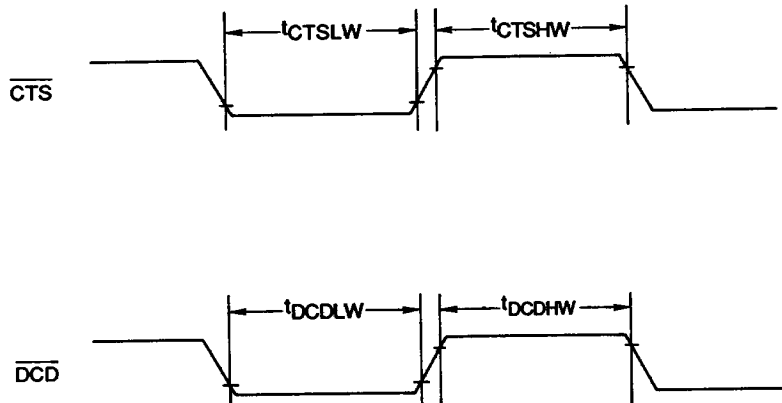


Figure 17-27. ASCII Timing (cont.)

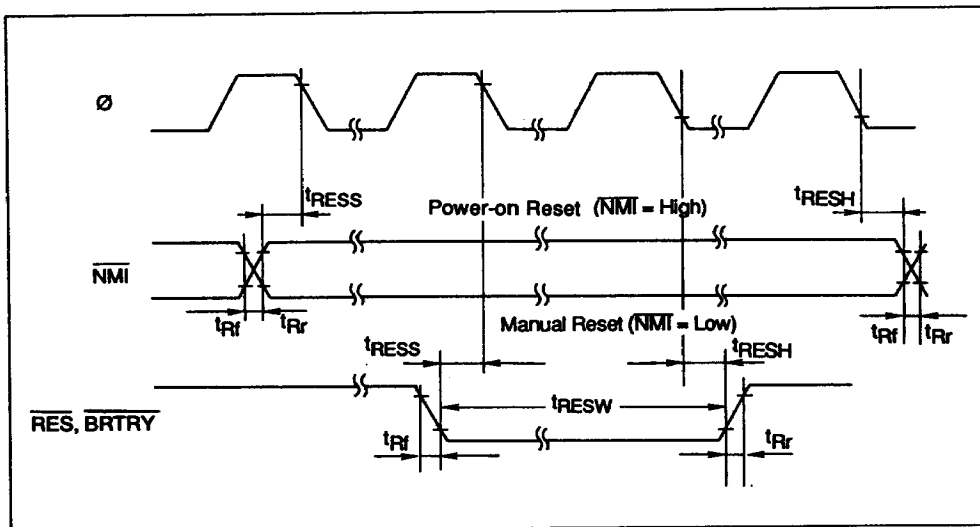


Figure 17-28. $\overline{\text{RES}}$ Timing

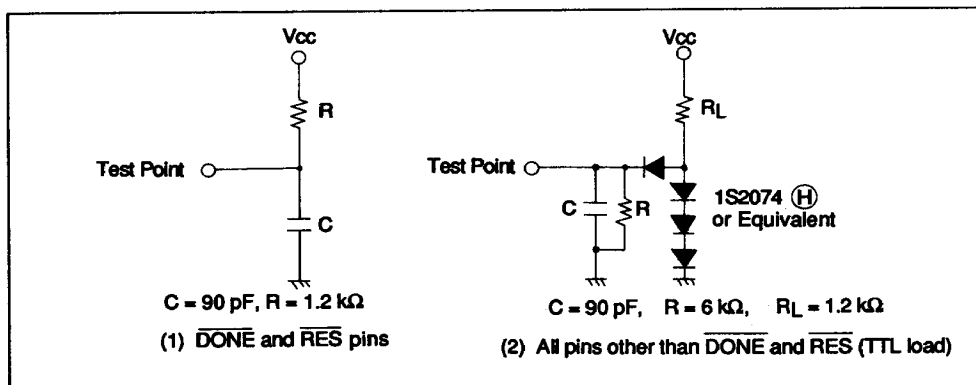


Figure 17-29. Bus Timing Test Loads

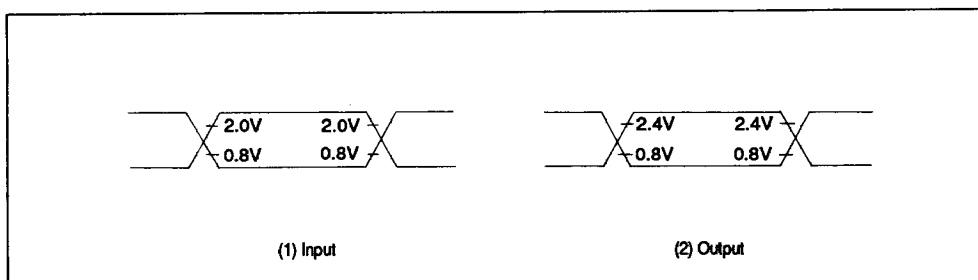


Figure 17-30. Reference Levels