National Semiconductor

ADVANCE INFORMATION
June 1992

NATL SEMICOND (MEMORY)

T-46-13-25

NM27LV210
1,048,576-Bit (64K x 16) Low Voltage EPROM

General Description

The NM27LV210 is a high performance Low Voltage Electrical Programmable read only memory. It is manufactured using National's latest 1.2μ CMOS split gate SVG EPROM technology. This technology allows the part to operate at speeds as fast as 200 ns over commercial temperature (0°C to +70°C) and 250 ns over industrial temperatures (−40°C to +85°C).

This Low Voltage and Low Power EPROM is designed with power sensitive hand held and portable battery products in mind. This allows for code storage of firmware for applications like notebook computers, palm top computers, cellular phones, and HDD.

National still maintains its commitment to High Quality and Reliability with EPI processing on the NM27LV210. Latch up immunity is guaranteed for stresses up to 200 mA on address and data pins from −1V to V_{CC} + 0.3V. ESD protection is also guaranteed up to 2000V.

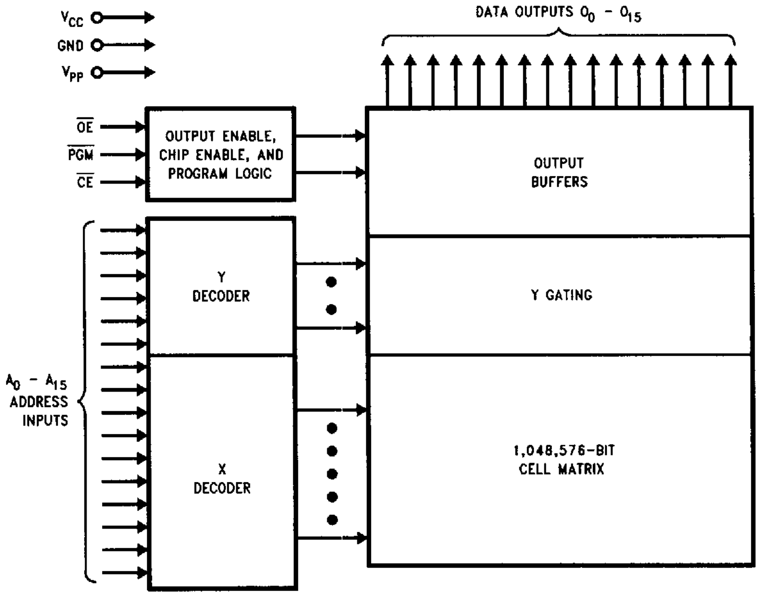
Small outline packages are just as critical to portable applications as Low Voltage and Low Power. National Semiconductor has foreseen this need and provides windowed LCC for prototyping and software development, PLCC for production runs, and TSOP for PC board sensitive users.

The NM27LV010 is one member of National's growing Low Voltage product family.

Features

- 3.0V to 5.5V operation
- 200 ns maximum access time
- Low current operation
  - — 15 mA I_{CC} active current @ 5 MHz
  - — 20 μA I_{CC} standby current @ 5 MHz
- Ultra low power operation
  - — 60 μA standby power @ 3.3V
  - — 50 mW active power @ 3.3V
- High reliability EPI processing
  - — Latch up immunity up to 200 mA
  - — 2000V ESD protection
- Surface mount package options
  - — TSOP package
  - — 44-Pin PLCC

Block Diagram



TL/D/11376-1

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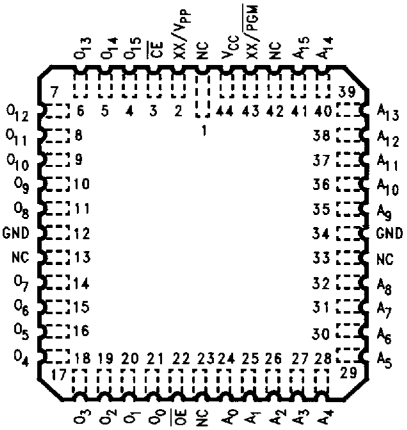
RRD-B20M62/Printed in U. S. A.

9000-3946

TSOP Pin Configuration

T-46-13-25

PLCC Pin Configuration



TL/D/11376-3

Top View

Commercial Temperature Range (0°C to +70°C)
V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NM27LV210 V, T	200
NM27LV210 V, T	250
NM27LV210 V, T	300

Extended Temperature Range (−40°C to +85°C)
V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NM27LV210 VE, TE	250
NM27LV210 VE, TE	300

Note: Surface mount PLCC package available for commercial and extended temperature ranges only.

Package Types: NM27LV210 V, TXXX
T = TSOP Type 1
V = PLCC package

- All packages conform to JEDEC standard.
- All versions are guaranteed to function in slower applications.

Pin Names

A0–A15	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O0–O15	Outputs
$\overline{PGM}$	Program
XX	Don't Care (During Read)
NC	No Connect
V_{PP}	Programming Voltage

T-46-13-25

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
All Input Voltages except A9 with Respect to Ground (Note 10)	−0.6V to +7V
V_{PP} and A9 with Respect to Ground	−0.6V to +14V
V_{CC} Supply Voltage with Respect to Ground	−0.6V to +7V
ESD Protection	>2000V
All Output Voltages with Respect to Ground (Note 10)	V_{CC} + 1.0V to GND − 0.6V

Operating Range

Range	Temperature	V_{CC}	Tolerance
Commercial	0°C to +70°C	3.3	±0.3
Industrial	−40°C to +85°C	3.3	±0.3

DC Read Characteristics Over Operating Range with $V_{PP} = V_{CC}$

Symbol	Parameter	Test Conditions	Min	Max	Units
V_{IL}	Input Low Level		−0.3	0.8	V
V_{IH}	Input High Level		2.0	V_{CC} ±0.3	V
V_{OL1}	Output Low Voltage (TTL)			0.4	V
V_{OH1}	Output High Voltage (TTL)		2.4		V
V_{OL2}	Output Low Voltage (CMOS)			0.2	V
V_{OH2}	Output High Voltage (CMOS)		V_A −0.3		V
I_{SB1}	V_{CC} Standby Current (TTL)	$\overline{CE} = V_{IH}$		50	µA
I_{SB2}	V_{CC} Standby Current (CMOS)	$\overline{CE} = V_{CC}$ ±0.3V		20	µA
I_{CC}	V_{CC} Active Current	$\overline{CE} = \overline{OE} = V_{IL}$, I/O = 0 µA f = 5 MHz		20	mA
I_{PP}	V_{PP} Supply Current	$V_{PP} = V_{CC}$		10	µA
I_{LI}	Input Load Current	V_{IN} = 3.3 or GND	−1	1	µA
I_{LO}	Output Leakage Current	V_{OUT} = 3.3V or GND	−1	1	µA

AC Read Characteristics Over Operating Range with $V_{PP} = V_{CC}$

Symbol	Parameter	200		250		300		Units
		Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		200		250		300	ns
t_{CE}	$\overline{CE}$ to Output Delay		200		250		300	
t_{OE}	$\overline{OE}$ to Output Delay		70		70		75	
t_{DF} (Note 2)	Output Disable to Output Float	0	50	0	50	0	60	
t_{OH} (Note 2)	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	0		0		0		

Capacitance $T_A = +25°C$, f = 1 MHz (Note 2)

T-46-13-25

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	$V_{IN} = 0V$	12	20	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	13	20	pF

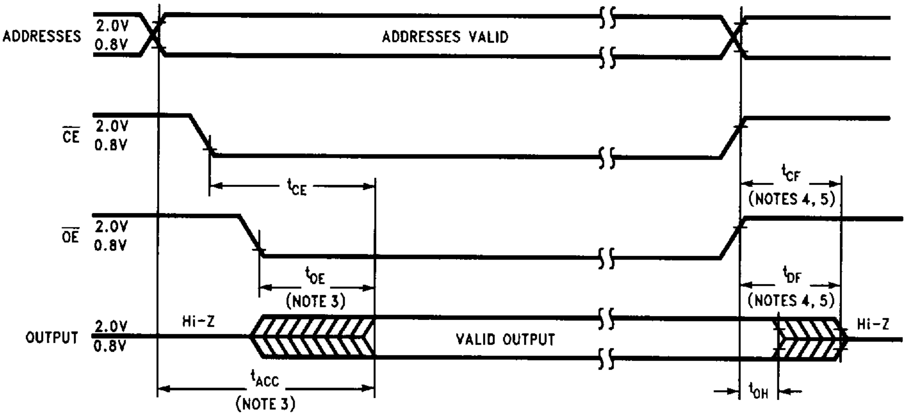
AC Test Conditions

Output Load	1 TTL Gate and $C_L = 100$ pF (Note 8)
Input Rise and Fall Times	≤5 ns
Input Pulse Levels	0.45V to 2.4V

Timing Measurement Reference Level

Inputs	0.8V and 2V
Outputs	0.8V and 2V

AC Waveforms (Notes 6, 7, & 9)



TL/D/11376-4

Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: This parameter is only sampled and is not 100% tested.

Note 3: $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impacting t_{ACC}.

Note 4: The t_{DF} and t_{CF} compare level is determined as follows:
High to TRI-STATE®, the measured V_{OH1} (DC) − 0.10V;
Low to TRI-STATE, the measured V_{OL1} (DC) + 0.10V.

Note 5: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 6: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND.

Note 7: The outputs must be restricted to V_{CC} + 1.0V to avoid latch-up and device damage.

Note 8: 1 TTL Gate: $I_{OL} = 1.6$ mA, $I_{OH} = -400$ μA.
C_L: 100 pF includes fixture capacitance.

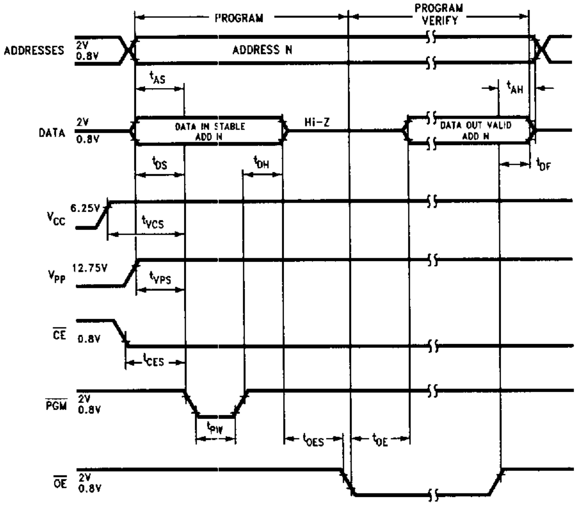
Note 9: V_{PP} may be connected to V_{CC} except during programming.

Note 10: Inputs and outputs can undershoot to −2.0V for 20 ns Max.

Programming Characteristics (Notes 1, 2, 3, 4 & 5)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{AS}	Address Setup Time		1			µs
t_{OES}	$\overline{OE}$ Setup Time		1			µs
t_{CES}	$\overline{CE}$ Setup Time	$\overline{OE} = V_{IH}$	1			µs
t_{DS}	Data Setup Time		1			µs
t_{VPS}	V_{PP} Setup Time		1			µs
t_{VCS}	V_{CC} Setup Time		1			µs
t_{AH}	Address Hold Time		0			µs
t_{DH}	Data Hold Time		1			µs
t_{DF}	Output Enable to Output Float Delay	$\overline{CE} = V_{IL}$	0		60	ns
t_{PW}	Program Pulse Width		95	100	105	µs
t_{OE}	Data Valid from $\overline{OE}$	$\overline{CE} = V_{IL}$			100	ns
I_{PP}	V_{PP} Supply Current during Programming Pulse	$\overline{CE} = V_{IL}$ $\overline{PGM} = V_{IL}$			40	mA
I_{CC}	V_{CC} Supply Current				50	mA
T_A	Temperature Ambient		20	25	30	°C
V_{CC}	Power Supply Voltage		6.0	6.25	6.5	V
V_{PP}	Programming Supply Voltage		12.5	12.75	13.0	V
t_{FR}	Input Rise, Fall Time		5			ns
V_{IL}	Input Low Voltage			0.0	0.45	V
V_{IH}	Input High Voltage		2.4	4.0		V
t_{IN}	Input Timing Reference Voltage		0.8		2.0	V
t_{OUT}	Output Timing Reference Voltage		0.8		2.0	V

Programming Waveforms (Note 3)



TL/D/11376-5

Note 1: National's standard product warranty applies only to devices programmed to specifications described herein.

Note 2: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The EPROM must not be inserted into or removed from a board with voltage applied to V_{PP} or V_{CC}.

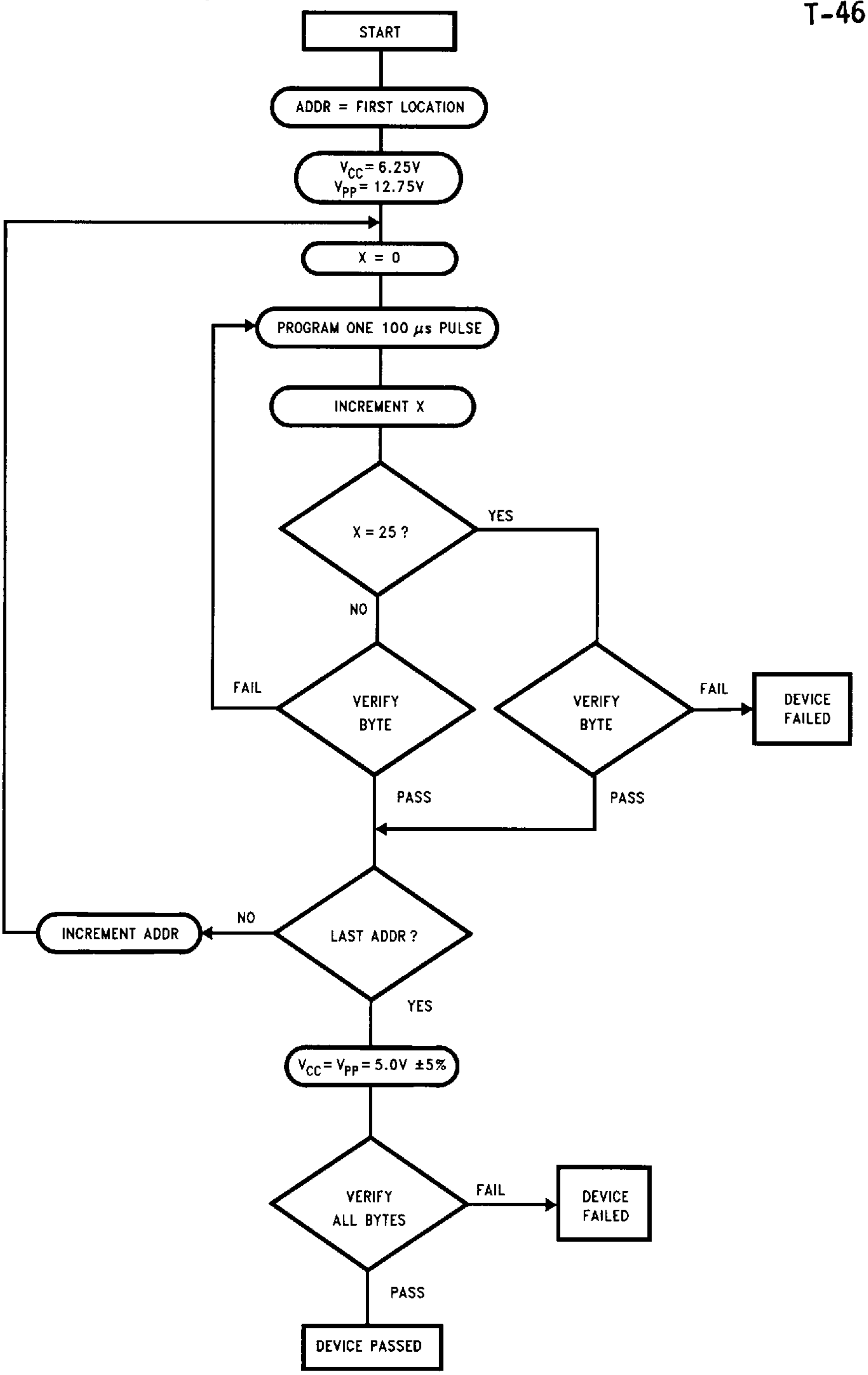
Note 3: The maximum absolute allowable voltage which may be applied to the V_{PP} pin during programming is 14V. Care must be taken when switching the V_{PP} supply to prevent any overshoot from exceeding this 14V maximum specification. At least a 0.1 µF capacitor is required across V_{PP}, V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Note 4: Programming and program verify are tested with the fast Program Algorithm, at typical power supply voltages and timings.

Note 5: During power up the $\overline{PGM}$ pin must be brought high ($\geq V_{IH}$) either coincident with or before power is applied to V_{PP}.

Fast Programming Algorithm Flow Chart

T-46-13-25



TL/D/11376-6

FIGURE 1

Functional Description

DEVICE OPERATION

The six modes of operation of the EPROM are listed in Table I. It should be noted that all inputs for the six modes are at TTL levels. The power supplies required are V_{CC} and V_{PP}. The V_{PP} power supply must be at 12.75V during the three programming modes, and must be at 3.3V in the other three modes. The V_{CC} power supply must be at 6.25V during the three programming modes, and at 3.3V in the other three modes.

Read Mode

The EPROM has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that the addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC}-t_{OE}$.

Standby Mode

The EPROM has a standby mode which reduces the active power dissipation by over 99%, from 66 mW to 0.66 μW. The EPROM is placed in the standby mode by applying a CMOS high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Output Disable

The EPROM is placed in output disable by applying a TTL high signal to the $\overline{OE}$ input. When in output disable all circuitry is enabled, except the outputs are in a high impedance state (TRI-STATE).

Output OR-Tying

Because the EPROM is usually used in larger memory arrays, National has provided a 2-line control function that accommodates this use of multiple memory connections. The 2-line control function allows for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that CE be decoded and used as the primary device selecting function, while OE be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 14V on the V_{PP} or A9 pin will damage the EPROM.

Initially, and after each erasure, all bits of the EPROM are in the "1's" state. Data is introduced by selectively programming "0's" into the desired bit locations. Although only "0's" will be programmed, both "1's" and "0's" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The EPROM is in the programming mode when the V_{PP} power supply is at 12.75V and $\overline{OE}$ is at V_{IH}. It is required that at least a 0.1 μF capacitor be placed across V_{PP}, V_{CC} to ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 16 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, an active low, TTL program pulse is applied to the $\overline{PGM}$ input. A program pulse must be applied at each address location to be programmed. The EPROM is programmed with the Fast Programming Algorithm shown in *Figure 1.* Each Address is programmed with a series of 100 μs pulses until it verifies good, up to a maximum of 25 pulses. Most memory cells will program with a single 100 μs pulse.

The EPROM must not be programmed with a DC signal applied to the $\overline{PGM}$ input.

Programming multiple EPROM in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the parallel EPROM may be connected together when they are programmed with the same data. A low level TTL pulse applied to the PGM input programs the paralleled EPROM.

Functional Description (Continued)

Program Inhibit

Programming multiple EPROM's in parallel with different data is also easily accomplished. Except for $\overline{CE}$ all like inputs (including $\overline{OE}$ and $\overline{PGM}$) of the parallel EPROM may be common. A TTL low level program pulse applied to an EPROM's $\overline{PGM}$ input with $\overline{CE}$ at V_{IL} and V_{PP} at 12.75V will program that EPROM. A TTL high level $\overline{CE}$ input inhibits the other EPROM's from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify may be performed with V_{PP} at 12.75V. V_{PP} must be at V_{CC}, except during programming and program verify.

AFTER PROGRAMMING

Opaque labels should be placed over the EPROM window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

MANUFACTURER'S IDENTIFICATION CODE

The EPROM has a manufacturer's identification code to aid in programming. When the device is inserted in an EPROM programmer socket, the programmer reads the code and then automatically calls up the specific programming algorithm for the part. This automatic programming control is only possible with programmers which have the capability of reading the code.

The Manufacturer's Identification code, shown in Table II, specifically identifies the manufacturer and device type. The code for the NM27LV210 is "8FD6", where "8F" designates that it is made by National Semiconductor, and "D6" designates a 1 Megabit (64K x 16) part.

The code is accessed by applying 12V ±0.5V to address pin A_9. Addresses A_1–A_8, A_{10}–A_{15}, and all control pins are held at V_{IL}. Address pin A0 is held at V_{IL} for the manufacturer's code, and held at V_{IH} for the device code. The code is read on the lower eight data pins, O_0–O_7. Proper code access is only guaranteed at 25°C ± 5°C.

ERASURE CHARACTERISTICS

The erasure characteristics of the device are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000Å–4000Å range.

The recommended erasure procedure for the EPROM is exposure to short wave ultraviolet light which has a wavelength of 2537Å. The integrated dose (i.e., UV intensity × exposure time) for erasure should be a minimum of 15W-sec/cm^2.

The EPROM should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure.

An erasure system should be calibrated periodically. The distance from lamp to device should be maintained at one inch. The erasure time increases as the square of the distance from the lamp (if distance is doubled the erasure time increases by factor of 4). Lamps lose intensity as they age. When a lamp is changed, the distance has changed, or the lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer: the standby current level, the active current level, and the transient current peaks that are produced by voltage transitions on input pins. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. The associated V_{CC} transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

MODE SELECTION

The modes of operation of the NM27LV210 are listed in Table I. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and A9 for device signature.

T-46-13-25

TABLE I. Modes Selection

Pins Mode	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{PP}	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	X (Note 1)	X	3.3V	D_{OUT}
Output Disable	X	V_{IH}	X	X	3.3V	High Z
Standby	V_{IH}	X	X	X	3.3V	High Z
Programming	V_{IL}	V_{IH}	V_{IL}	12.75V	6.25V	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	12.75V	6.25V	D_{OUT}
Program Inhibit	V_{IH}	X	X	12.75V	6.25V	High Z

Note 1: X can be V_{IL} or V_{IH}.

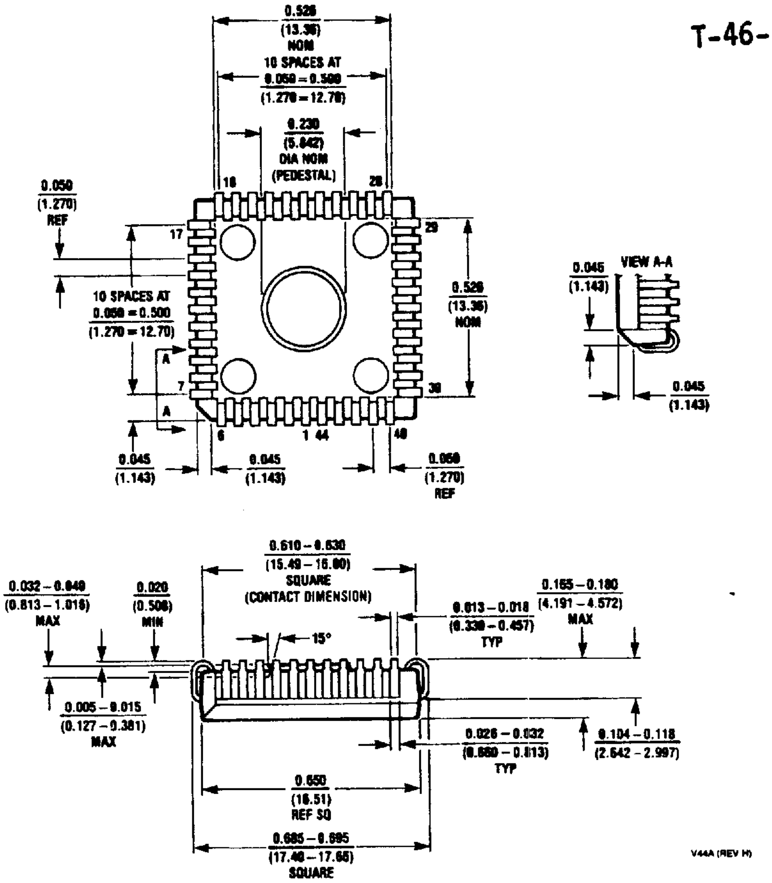
TABLE II. Manufacturer's Identification Code

Pins	A0 (21)	A9 (31)	O_7 (12)	O_6 (13)	O_5 (14)	O_4 (15)	O_3 (16)	O_2 (17)	O_1 (18)	O_0 (19)	Hex Data
Manufacturer Code	V_{IL}	12V	1	0	0	0	1	1	1	1	8F
Device Code	V_{IH}	12V	1	1	0	1	0	1	1	0	D6

Physical Dimensions inches (millimeters)

Lit. # 112264

T-46-13-25



44-Lead Plastic Chip Carrier (V)
Order Number NM27LV210XXX
NS Package Number V44A

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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