

MOS INTEGRATED CIRCUIT

μ PD23C64040JL, 23C64080JL

64M-BIT MASK-PROGRAMMABLE ROM

8M-WORD BY 8-BIT (BYTE MODE) / 4M-WORD BY 16-BIT (WORD MODE)

PAGE ACCESS MODE

Description

The μ PD23C64040JL, 23C64080JL are a 67,108,864 bits mask-programmable ROM. The word organization is selectable (BYTE mode : 8,388,608 words by 8 bits, WORD mode : 4,194,304 words by 16 bits).

The active levels of OE (Output Enable Input) can be selected with mask-option.

The μ PD23C64040JL, 23C64080JL are packed in 48-pin PLASTIC TSOP (I) and 44-pin PLASTIC SOP.

Features

- Word organization
 - 8,388,608 words by 8 bits (BYTE mode)
 - 4,194,304 words by 16 bits (WORD mode)
- Page access mode
 - BYTE mode : 8 byte random page access (μ PD23C64040JL)
 - : 16 byte random page access (μ PD23C64080JL)
 - WORD mode : 4 word random page access (μ PD23C64040JL)
 - : 8 word random page access (μ PD23C64080JL)
- Operating supply voltage : $V_{CC} = 2.7$ to 3.6 V

Operating supply voltage V_{CC}	Package	Access time / Page access time ns (MAX.)	Power supply current (Active mode) mA (MAX.)		Standby current (CMOS level input) μ A (MAX.)
			μ PD23C64040JL	μ PD23C64080JL	
$3.0\text{ V} \pm 0.3\text{ V}$	TSOP (I)	100 / 25	40	60	30
	SOP	120 / 25	35	50	
$3.3\text{ V} \pm 0.3\text{ V}$	TSOP (I)	90 / 25	55	75	
	SOP	100 / 25	50	65	

Remark The access time and power supply current vary depending on the package type.

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Not all products and/or types are available in every country. Please check with an NEC Electronics sales representative for availability and additional information.

Ordering Information

Part number	Package
μ PD23C64040JLGY-xxx-MJH	48-pin PLASTIC TSOP (I) (12 × 18) (Normal bent)
μ PD23C64040JLGY-xxx-MKH	48-pin PLASTIC TSOP (I) (12 × 18) (Reverse bent)
μ PD23C64040JLGX-xxx	44-pin PLASTIC SOP (15.24 mm (600))
μ PD23C64080JLGY-xxx-MJH	48-pin PLASTIC TSOP (I) (12 × 18) (Normal bent)
μ PD23C64080JLGY-xxx-MKH	48-pin PLASTIC TSOP (I) (12 × 18) (Reverse bent)
μ PD23C64080JLGX-xxx	44-pin PLASTIC SOP (15.24 mm (600))

(xxx : ROM code suffix No.)

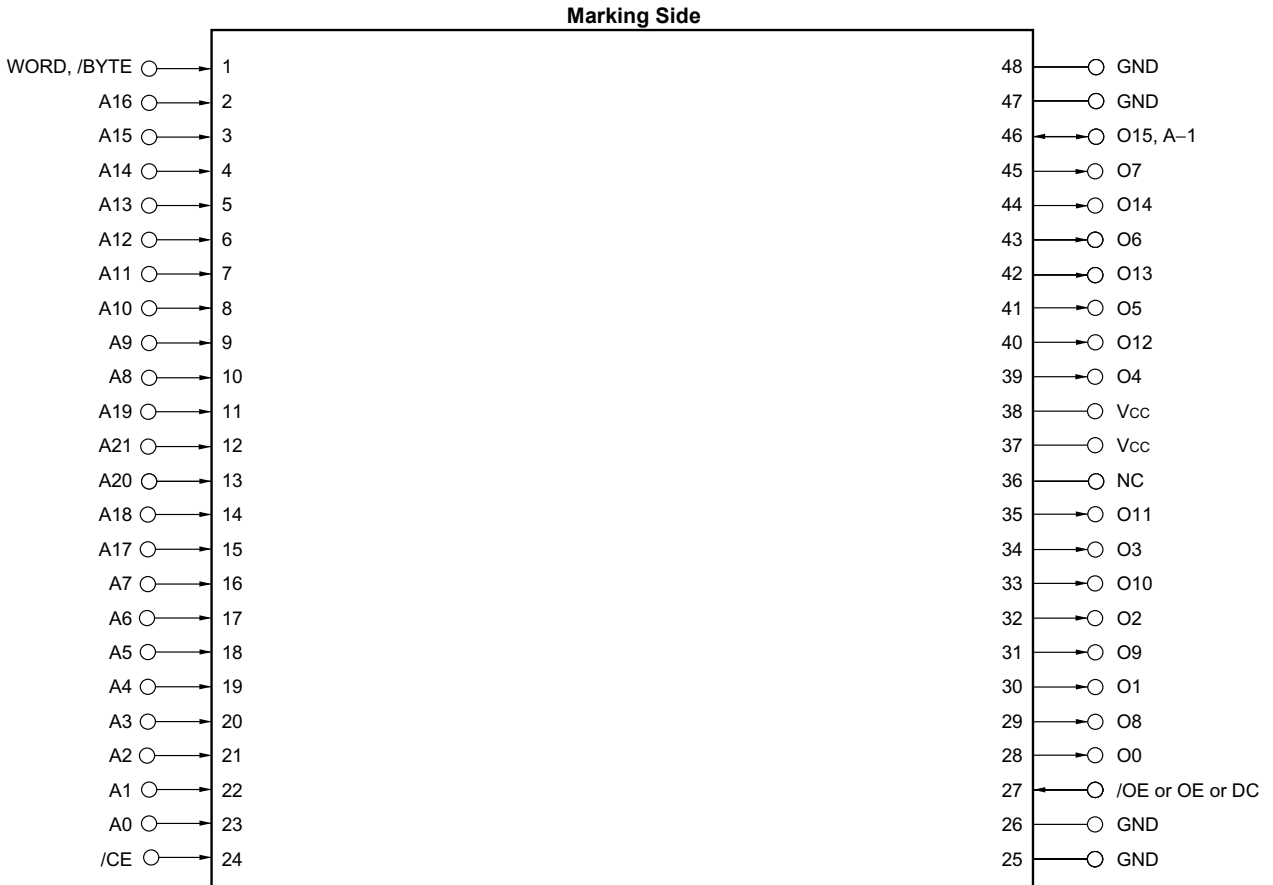
Pin Configurations

/xxx indicates active low signal.

48-pin PLASTIC TSOP (I) (12 × 18) (Normal bent)

[μPD23C64040JLGY-xxx-MJH]

[μPD23C64080JLGY-xxx-MJH]



- | | |
|---------------------|--|
| A0 to A21 | : Address inputs |
| O0 to O7, O8 to O14 | : Data outputs |
| O15, A-1 | : Data output 15 (WORD mode),
LSB Address input (BYTE mode) |
| WORD, /BYTE | : Mode select input |
| /CE | : Chip Enable input |
| /OE or OE | : Output Enable input |
| Vcc | : Supply voltage |
| GND | : Ground |
| NC ^{Note} | : No Connection |
| DC | : Don't Care |

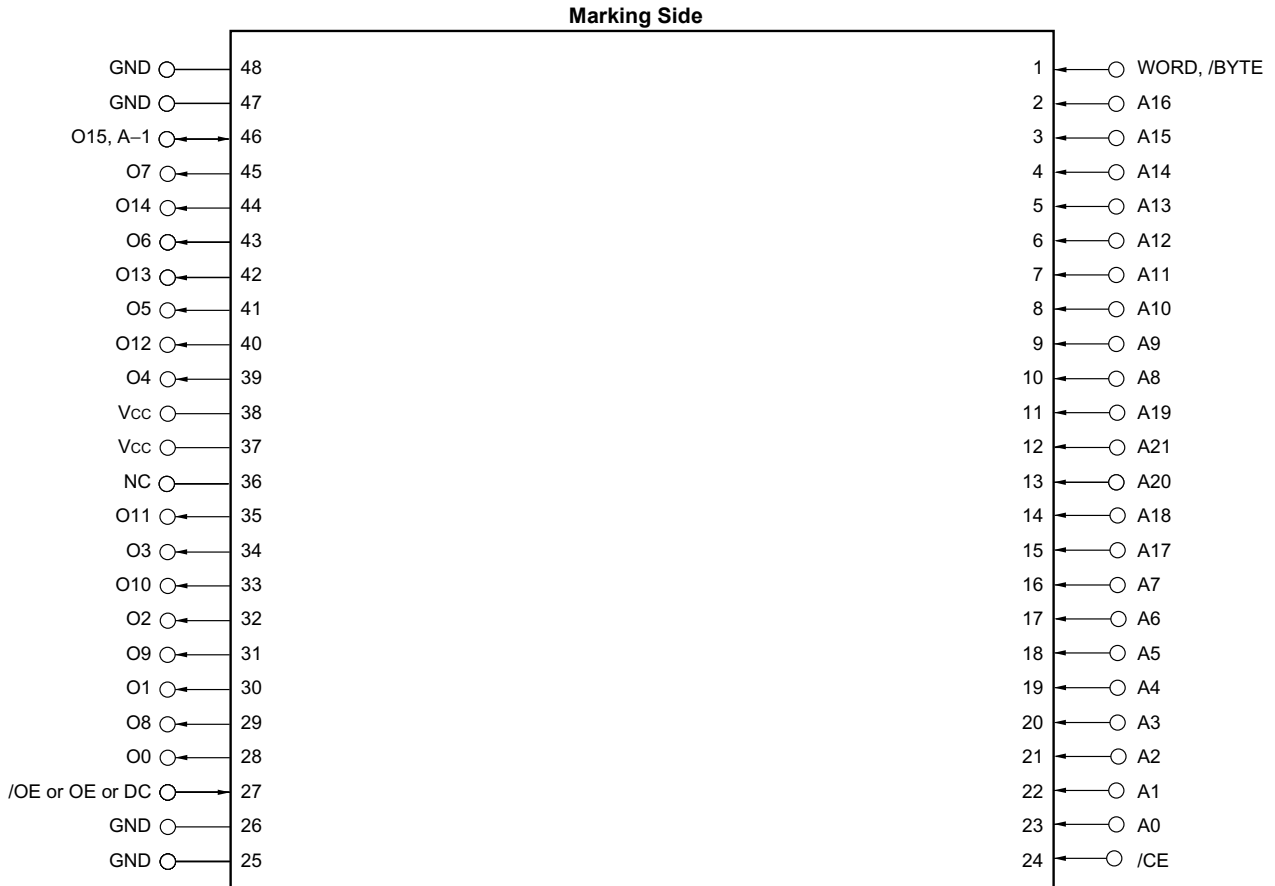
Note Some signals can be applied because this pin is not connected to the inside of the chip.

Remark Refer to **Package Drawings** for the 1-pin index mark.

48-pin PLASTIC TSOP (I) (12 × 18) (Reverse bent)

[μPD23C64040JLGY-xxx-MKH]

[μPD23C64080JLGY-xxx-MKH]



- A0 to A21 : Address inputs
- O0 to O7, O8 to O14 : Data outputs
- O15, A-1 : Data output 15 (WORD mode),
LSB Address input (BYTE mode)
- WORD, /BYTE : Mode select input
- /CE : Chip Enable input
- /OE or OE : Output Enable input
- Vcc : Supply voltage
- GND : Ground
- NC^{Note} : No Connection
- DC : Don't Care

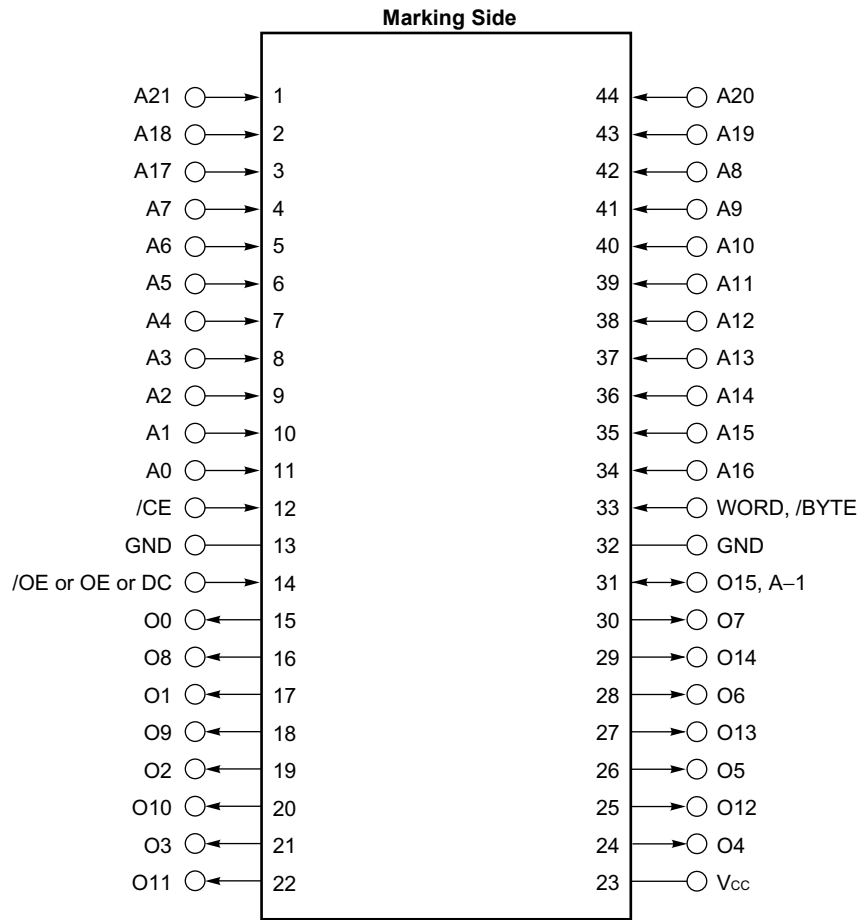
Note Some signals can be applied because this pin is not connected to the inside of the chip.

Remark Refer to **Package Drawings** for the 1-pin index mark.

44-pin PLASTIC SOP (15.24 mm (600))

[μPD23C64040JLGX-xxx]

[μPD23C64080JLGX-xxx]



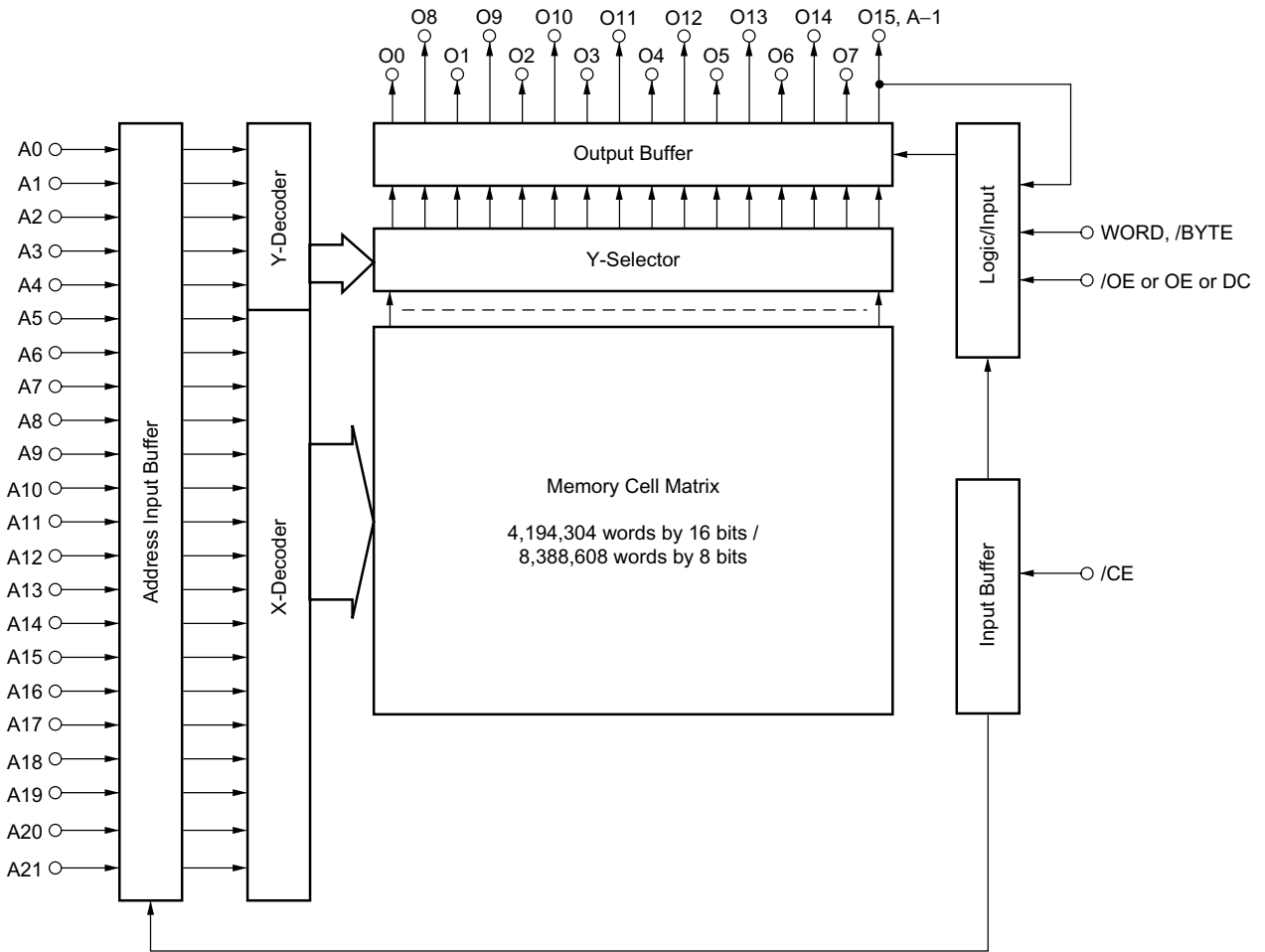
- A0 to A21 : Address inputs
- O0 to O7, O8 to O14 : Data outputs
- O15, A-1 : Data output 15 (WORD mode),
LSB Address input (BYTE mode)
- WORD, /BYTE : Mode select input
- /CE : Chip Enable input
- /OE or OE : Output Enable input
- V_{CC} : Supply voltage
- GND : Ground
- DC : Don't Care

Remark Refer to **Package Drawings** for the 1-pin index mark.

Input / Output Pin Functions

Pin name	Input / Output	Function
WORD, /BYTE	Input	The pin for switching WORD mode and BYTE mode. High level : WORD mode (4M-word by 16-bit) Low level : BYTE mode (8M-word by 8-bit)
A0 to A21 (Address inputs)	Input	Address input pins. A0 to A21 are used differently in the WORD mode and the BYTE mode. WORD mode (4M-word by 16-bit) A0 to A21 are used as 22 bits address signals. BYTE mode (8M-word by 8-bit) A0 to A21 are used as the upper 22 bits of total 23 bits of address signal. (The least significant bit (A-1) is combined to O15.)
O0 to O7, O8 to O14 (Data outputs)	Output	Data output pins. O0 to O7, O8 to O14 are used differently in the WORD mode and the BYTE mode. WORD mode (4M-word by 16-bit) The lower 15 bits of 16 bits data outputs to O0 to O14. (The most significant bit (O15) combined to A-1.) BYTE mode (8M-word by 8-bit) 8 bits data outputs to O0 to O7 and also O8 to O14 are high impedance.
O15, A-1 (Data output 15, LSB Address input)	Output, Input	O15, A-1 are used differently in the WORD mode and the BYTE mode. WORD mode (4M-word by 16-bit) The most significant output data bus (O15). BYTE mode (8M-word by 8-bit) The least significant address bus (A-1).
/CE (Chip Enable)	Input	Chip activating signal. When the OE is active, output states are following. High level : High-Z Low level : Data out
/OE or OE or DC (Output Enable, Don't Care)	Input	Output enable signal. The active level of OE is mask option. The active level of OE can be selected from high active, low active and Don't care at order.
V _{cc}	–	Supply voltage
GND	–	Ground
NC	–	Not internally connected (The signal can be connected).

Block Diagram



Mask Option

The active levels of output enable pin (/OE or OE or DC) are mask programmable and optional, and can be selected from among "0" "1" "x" shown in the table below.

Option	/OE or OE or DC	OE active level
0	/OE	L
1	OE	H
x	DC	Don't care

Operation modes for each option are shown in the tables below.

Operation mode (Option : 0)

/CE	/OE	Mode	Output state
L	L	Active	Data out
	H		High-Z
H	H or L	Standby	High-Z

Operation mode (Option : 1)

/CE	OE	Mode	Output state
L	L	Active	High-Z
	H		Data out
H	H or L	Standby	High-Z

Operation mode (Option : x)

/CE	DC	Mode	Output state
L	H or L	Active	Data out
H	H or L	Standby	High-Z

Remark L : Low level input
 H : High level input

Electrical Specifications

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Supply voltage	V _{CC}		-0.3 to +4.6	V
Input voltage	V _I		-0.3 to V _{CC} + 0.3	V
Output voltage	V _O		-0.3 to V _{CC} + 0.3	V
Operating ambient temperature	T _A		-10 to +70	°C
Storage temperature	T _{stg}		-65 to +150	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Capacitance (T_A = 25 °C)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C _I	f = 1 MHz			10	pF
Output capacitance	C _O				12	pF

DC Characteristics (T_A = -10 to +70 °C, V_{CC} = 2.7 to 3.6 V)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit	
High level input voltage	V _{IH}		2.0		V _{CC} + 0.3	V	
Low level input voltage	V _{IL}	V _{CC} = 3.0 V ± 0.3 V	-0.3		+0.5	V	
		V _{CC} = 3.3 V ± 0.3 V	-0.3		+0.8		
High level output voltage	V _{OH}	I _{OH} = -100 μA	2.4			V	
Low level output voltage	V _{OL}	I _{OL} = 2.1 mA			0.4	V	
Input leakage current	I _{LI}	V _I = 0 V to V _{CC}	-10		+10	μA	
Output leakage current	I _{LO}	V _O = 0 V to V _{CC} , Chip deselected	-10		+10	μA	
Power supply current	I _{CC1}	/CE = V _{IL} (Active mode), I _O = 0 mA	μPD23C64040JL				mA
			V _{CC} = 3.0 V ± 0.3 V	TSOP (I)			
		SOP				35	
		V _{CC} = 3.3 V ± 0.3 V	TSOP (I)			55	
			SOP			50	
		μPD23C64080JL				mA	
		V _{CC} = 3.0 V ± 0.3 V	TSOP (I)				60
			SOP				50
		V _{CC} = 3.3 V ± 0.3 V	TSOP (I)				75
			SOP			65	
Standby current	I _{CC3}	/CE = V _{CC} - 0.2 V (Standby mode)			30	μA	

AC Characteristics (TA = -10 to +70 °C, VCC = 2.7 to 3.6 V)

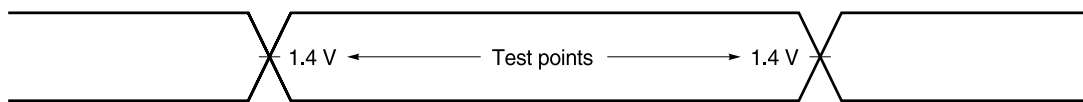
Parameter	Symbol	Test condition	VCC = 3.0 V ± 0.3 V			VCC = 3.3 V ± 0.3 V			Unit
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Address access time	tACC	TSOP (I)			100			90	ns
		SOP			120			100	
Page access time	tPAC				25			25	ns
Address skew time	tSKEW	Note			10			10	ns
Chip enable access time	tCE	TSOP (I)			100			90	ns
		SOP			120			100	
Output enable access time	tOE				25			25	ns
Output hold time	tOH		0			0			ns
Output disable time	tDF		0		25	0		25	ns
WORD, /BYTE access time	twB	TSOP (I)			100			90	ns
		SOP			120			100	

- ★ **Note** tSKEW indicates the following three types of time depending on the condition.
- 1) When switching /CE from high level to low level, tSKEW is the time from the /CE low level input point until the next address is determined.
 - 2) When switching /CE from low level to high level, tSKEW is the time from the address change start point to the /CE high level input point.
 - 3) When /CE is fixed to low level, tSKEW is the time from the address change start point until the next address is determined.
- Since specs are defined for tSKEW only when /CE is active, tSKEW is not subject to limitations when /CE is switched from high level to low level following address determination, or when the address is changed after /CE is switched from low level to high level.

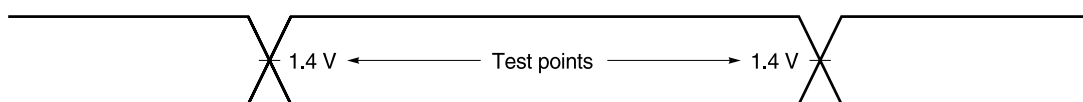
Remark tDF is the time from inactivation of Chip Enable input (/CE) or Output Enable input (/OE or OE) to high impedance state output.

AC Test Conditions

Input waveform (Rise / Fall Time ≤ 5 ns)



Output waveform



Output load

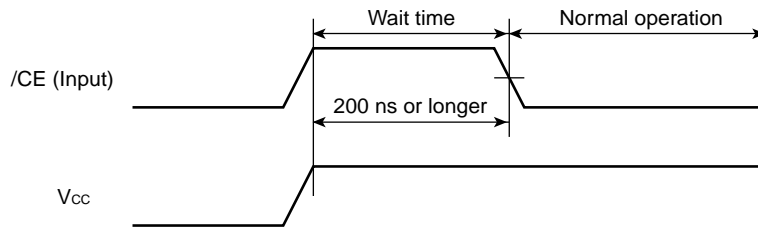
1 TTL + 100 pF

★ **Cautions on power application**

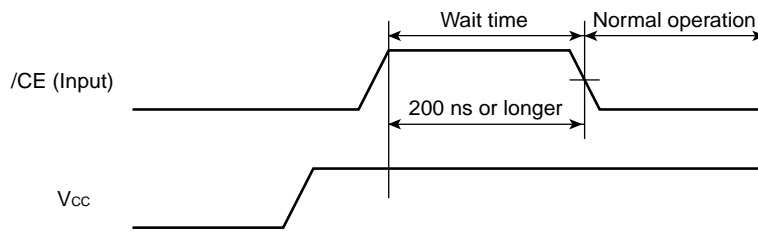
To ensure normal operation, always apply power using /CE following the procedure shown below.

- 1) Input a high level to /CE during and after power application.
- 2) Hold the high level input to /CE for 200 ns or longer (wait time).
- 3) Start normal operation after the wait time has elapsed.

Power Application Timing Chart 1 (When /CE is made high at power application)

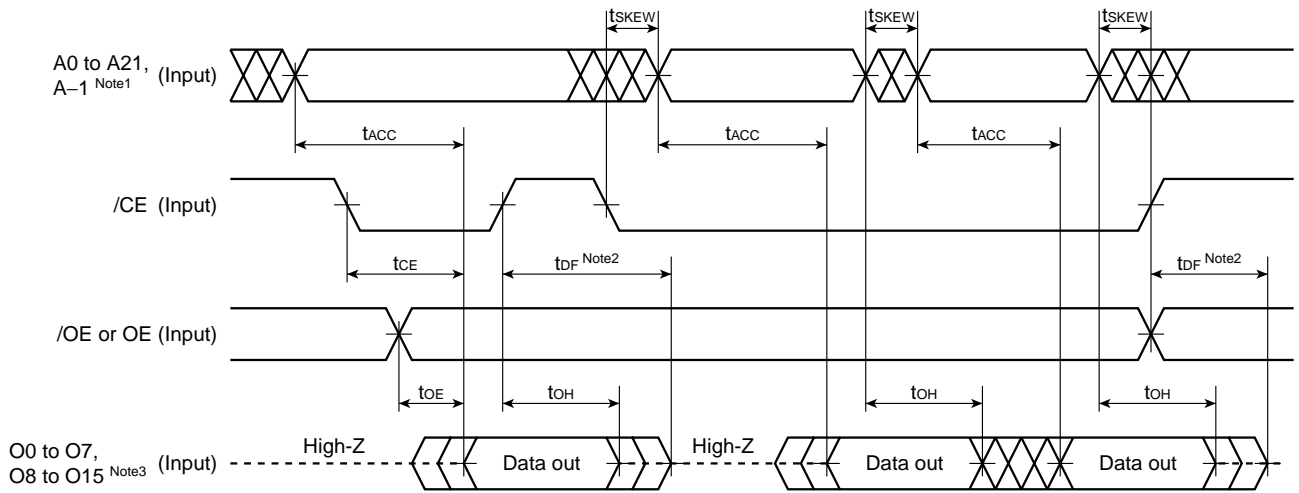


Power Application Timing Chart 2 (When /CE is made high after power application)



Caution Other signals can be either high or low during the wait time.

★ Read Cycle Timing Chart 1

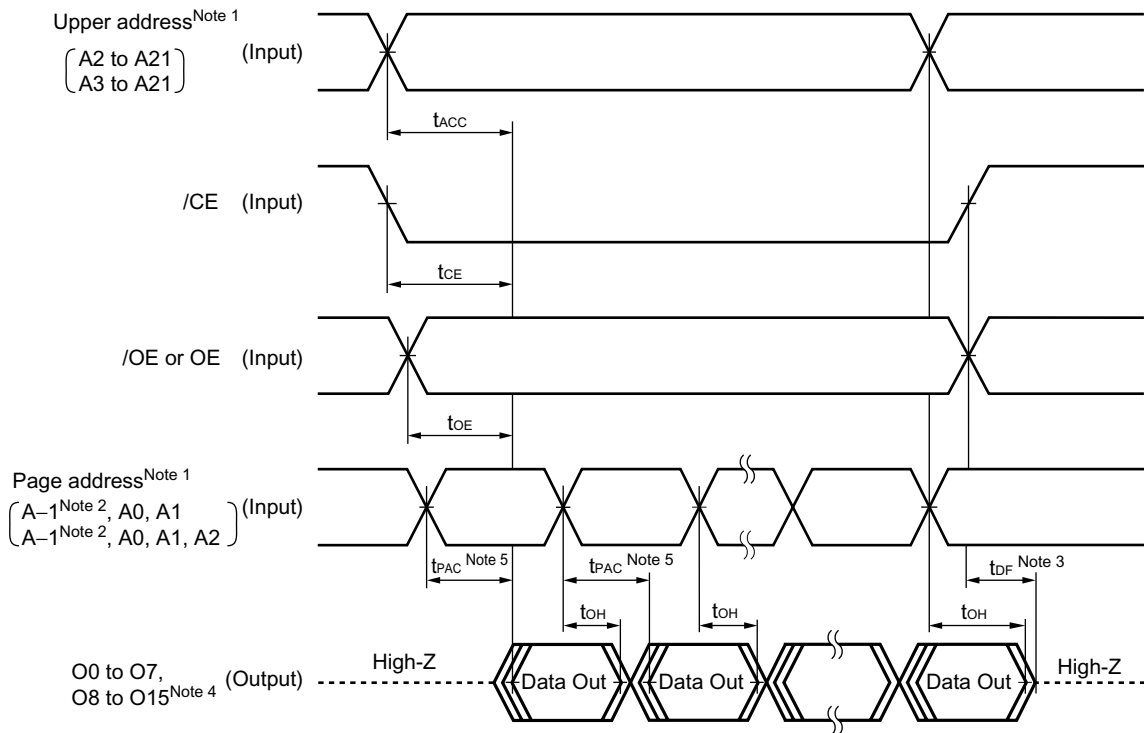


Notes 1. During WORD mode, A-1 is O15.

2. t_{DF} is the time from inactivation of Chip Enable input (/CE) or Output Enable input (/OE or OE) to high impedance state output.

3. During BYTE mode, O8 to O14 are high impedance and O15 is A-1.

Read Cycle Timing Chart 2 (Page Access Mode)



Notes 1. The address differs depending on the product as follows.

Part Number	Upper address	Page address
μPD23C64040JL	A2 to A21	A-1, A0, A1
μPD23C64080JL	A3 to A21	A-1, A0, A1, A2

2. During WORD mode, A-1 is O15.

3. t_{DF} is the time from inactivation of Chip Enable input (/CE) or Output Enable input (/OE or OE) to high impedance state output.

4. During BYTE mode, O8 to O14 are high impedance and O15 is A-1.

5. The definition of page access time is as follows.

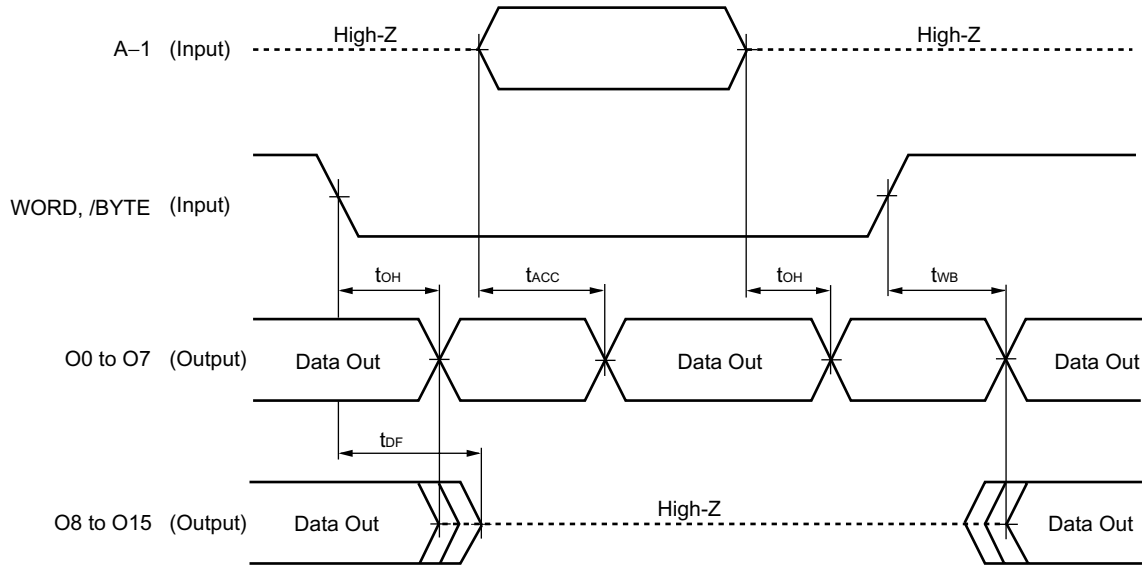
[μPD23C64040JL]

Page access time	Upper address (A2 to A21) inputs condition	/CE input condition	/OE or OE input condition
t_{PAC}	Before $t_{ACC} - t_{PAC}$	Before $t_{CE} - t_{PAC}$	Before stabilizing of page address (A-1, A0, A1)

[μPD23C64080JL]

Page access time	Upper address (A3 to A21) inputs condition	/CE input condition	/OE or OE input condition
t_{PAC}	Before $t_{ACC} - t_{PAC}$	Before $t_{CE} - t_{PAC}$	Before stabilizing of page address (A-1, A0, A1, A2)

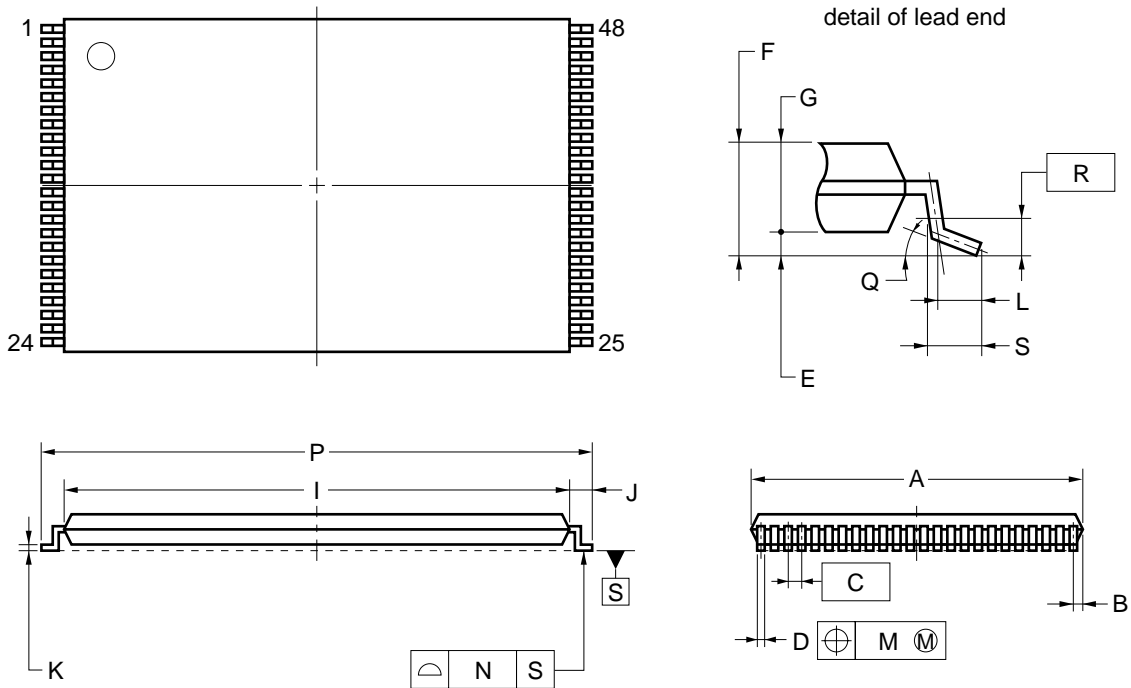
WORD, /BYTE Switch Timing Chart



Remark Chip Enable (/CE) and Output Enable (/OE or OE) : Active.

Package Drawings

48-PIN PLASTIC TSOP(I) (12x18)



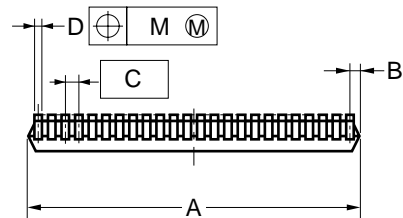
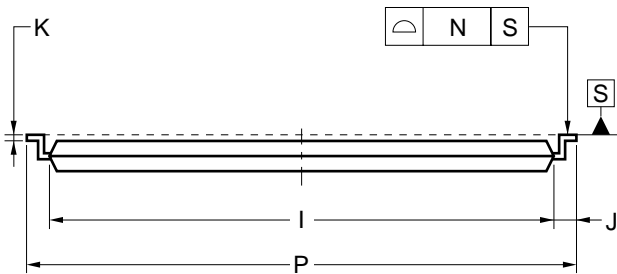
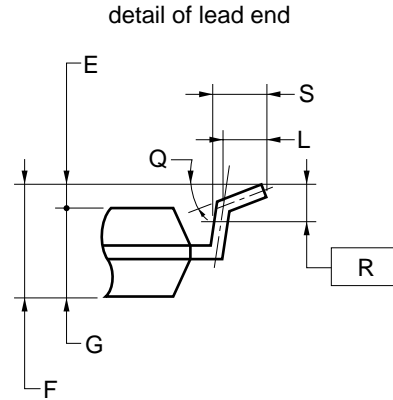
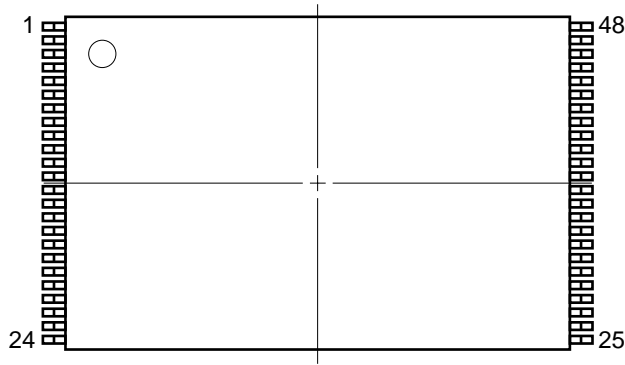
NOTES

1. Each lead centerline is located within 0.10 mm of its true position (T.P.) at maximum material condition.
2. "A" excludes mold flash. (Includes mold flash : 12.4 mm MAX.)

ITEM	MILLIMETERS
A	12.0±0.1
B	0.45 MAX.
C	0.5 (T.P.)
D	0.22±0.05
E	0.1±0.05
F	1.2 MAX.
G	1.0±0.05
I	16.4±0.1
J	0.8±0.2
K	0.145±0.05
L	0.5
M	0.10
N	0.10
P	18.0±0.2
Q	3°+5° -3°
R	0.25
S	0.60±0.15

S48GY-50-MJH1-1

48-PIN PLASTIC TSOP(I) (12x18)



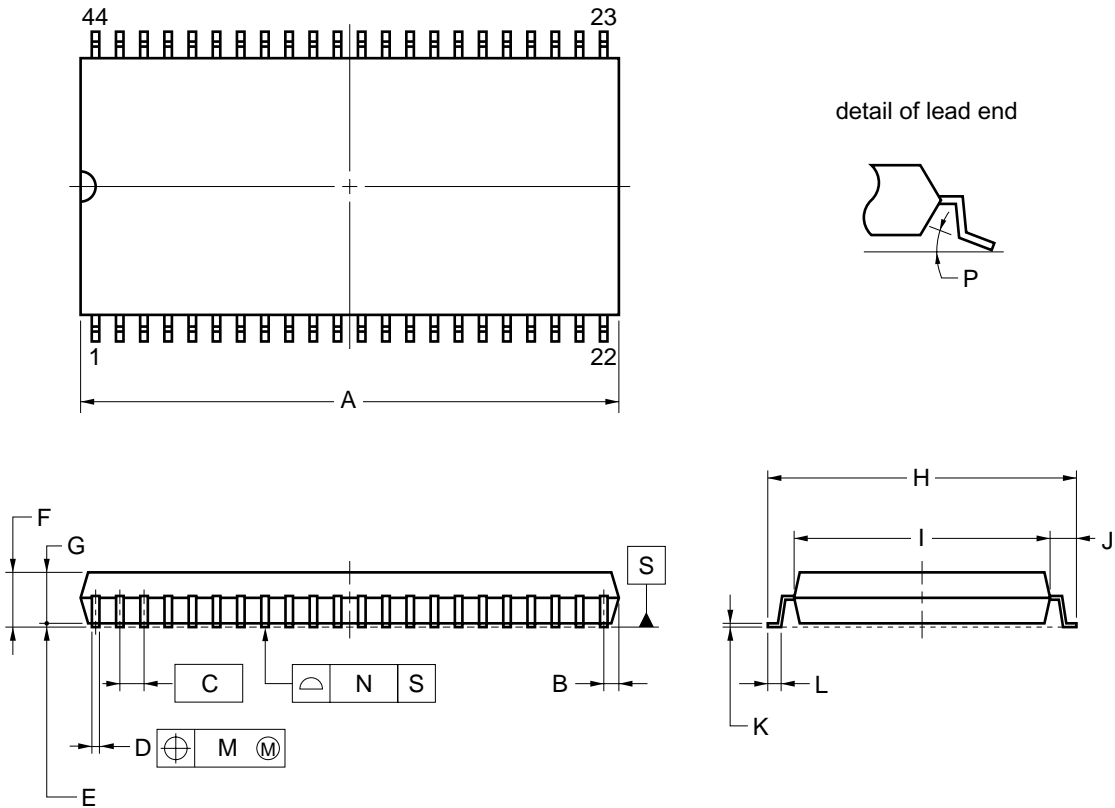
NOTES

1. Each lead centerline is located within 0.10 mm of its true position (T.P.) at maximum material condition.
2. "A" excludes mold flash. (Includes mold flash : 12.4 mm MAX.)

ITEM	MILLIMETERS
A	12.0±0.1
B	0.45 MAX.
C	0.5 (T.P.)
D	0.22±0.05
E	0.1±0.05
F	1.2 MAX.
G	1.0±0.05
I	16.4±0.1
J	0.8±0.2
K	0.145±0.05
L	0.5
M	0.10
N	0.10
P	18.0±0.2
Q	3° ^{+5°} -3°
R	0.25
S	0.60±0.15

S48GY-50-MKH1-1

44-PIN PLASTIC SOP (15.24 mm (600))



NOTE

Each lead centerline is located within 0.12 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	27.83 ^{+0.4} _{-0.05}
B	0.78 MAX.
C	1.27 (T.P.)
D	0.42 ^{+0.08} _{-0.07}
E	0.15±0.1
F	3.0 MAX.
G	2.7±0.05
H	16.04±0.3
I	13.24±0.1
J	1.4±0.2
K	0.22 ^{+0.08} _{-0.07}
L	0.8±0.2
M	0.12
N	0.10
P	3° ^{+7°} _{-3°}

P44GX-50-600A-4

Recommended Soldering Conditions

Please consult with our sales offices for soldering conditions of the μ PD23C64040JL, 23C64080JL.

Types of Surface Mount Device

μ PD23C64040JLGY-xxx-MJH	: 48-pin PLASTIC TSOP (I) (12 × 18) (Normal bent)
μ PD23C64040JLGY-xxx-MKH	: 48-pin PLASTIC TSOP (I) (12 × 18) (Reverse bent)
μ PD23C64040JLGX-xxx	: 44-pin PLASTIC SOP (15.24 mm (600))
μ PD23C64080JLGY-xxx-MJH	: 48-pin PLASTIC TSOP (I) (12 × 18) (Normal bent)
μ PD23C64080JLGY-xxx-MKH	: 48-pin PLASTIC TSOP (I) (12 × 18) (Reverse bent)
μ PD23C64080JLGX-xxx	: 44-pin PLASTIC SOP (15.24 mm (600))

Revision History

Edition/ Date	Page		Type of revision	Location	Description (Previous edition → This edition)
	This edition	Previous edition			
3rd edition/ Feb. 2003	p.10	p.10	Addition	AC Characteristics	Address skew time (t_{SKEW}) Note
	p.11	–	Addition		Cautions on power application
	p.12	p.11	Modification		Read Cycle Timing Chart 1

[MEMO]

[MEMO]

[MEMO]

NOTES FOR CMOS DEVICES**① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS**

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF THE APPLIED WAVEFORM OF INPUT PINS AND THE UNUSED INPUT PINS FOR CMOS

Note:

Input levels of CMOS devices must be fixed. CMOS devices behave differently than Bipolar or NMOS devices. If the input of a CMOS device stays in an area that is between V_{IL} (MAX.) and V_{IH} (MIN.) due to the effects of noise or some other irregularity, malfunction may result. Therefore, not only the input waveform is fixed, but also the waveform changes, it is important to use the CMOS device under AC test conditions. For unused input pins in particular, CMOS devices should not be operated in a state where nothing is connected, so input levels of CMOS devices must be fixed to high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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(Note)

- (1) "NEC Electronics" as used in this statement means NEC Electronics Corporation and also includes its majority-owned subsidiaries.
- (2) "NEC Electronics products" means any product developed or manufactured by or for NEC Electronics (as defined above).