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MJ2812HS

32 WORDS x 8 BIT FIFO MEMORY

The MJ2812HS is a high speed version of the MJ2812 32-word by 8-bit first-in first-out memory. The device has completely independent read and write controls and three state outputs controlled by an output enable pin (OE). Data on the data inputs (D_0 - D_7) is written into the memory by a pulse on load (PL). The data word automatically ripples through the memory until it reaches the output or another data word.

Data is read from the memory by applying a shift out pulse on PD. This dumps the word on the outputs (Q_0 - Q_7) and the next word in the buffer moves to the output. An output ready signal (OR) indicates that data is available at the output and also provides a memory empty signal. An input ready signal ($\overline{IR}$) indicates that the device is ready to accept data and also provides a memory full signal.

The MJ2812HS has master reset inputs which initialise the FIFO control logic and clear all data from the device (reset to all lows). A FLAG signal goes high when the memory is approximately half full.

The MJ2812HS can perform input and output data transfer on a bit-serial basis as well as on 8-bit parallel words. The input buffer is an 8-bit shift register which can be loaded in parallel by the PL command or can be loaded serially through the D_0 input by using the SL clock. When 8 bits have been shifted into the input buffer serially, the 8-bit word automatically moves in parallel through the memory. The output includes a built in parallel-to-serial converter, so that data can be shifted out of the Q_7 output by using the SD clock. After 8 clock pulses a new 8-bit word appears at the outputs.

The timing and function of the four control signals PL, $\overline{IR}$, PD and OR are designed so that two FIFOs can be placed end-to-end, with OR of the first driving PL of the second and $\overline{IR}$ of the second driving PD of the first. With this simple interconnection, strings of FIFOs can control each other reliably to make a FIFO array any number of words deep. Cascadability is only guaranteed up to 3MHz data rate.

FEATURES

- Serial or Parallel Inputs and Outputs
- 32 Words x 8 Bits
- Stand Alone
- Easily Stacked Sideways
- Data Rates up to 5.0MHz
- Independent Reading and Writing
- Half-Full FLAG
- Last Word Retention
- TTL — Compatible Tri-state Outputs
- Input and Output Ready Signals
- Master Reset
- Single +5V Supply

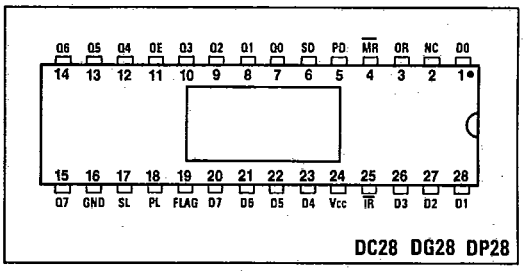

Fig.1 MJ2812HS (32 x 8) pin connections

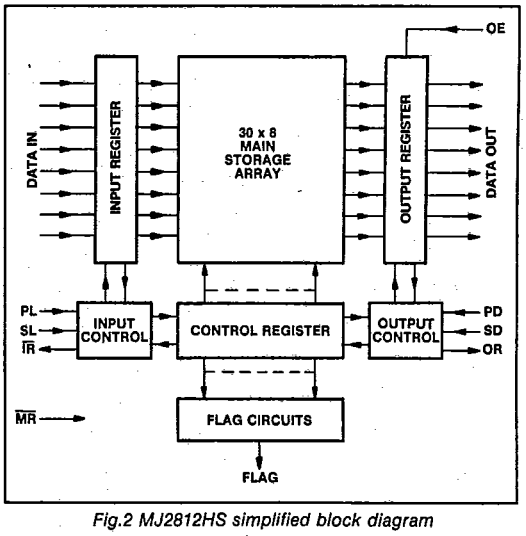

Fig.2 MJ2812HS simplified block diagram

APPLICATIONS

- Smoothing Data Rates from Keyboards
- Buffer Between Differently-Clocked Systems (Short Fast Bursts into Steady Data Stream, and Vice Versa)
- Temporary Storage in Error Removing Systems which use Repeated Transmission
- Buffer Store in Interrupt-Orientated Systems
- Computer-to-Line Printer Buffer

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OPERATING RANGE

Type number	Ambient temperature	Vcc	Ground
MJ2812HS	0°C to +70°C	5.0V ± 5%	0V

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
As specified in Operating Range table (above)

Static Characteristics

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Output high voltage	V_{OH}	2.4			V	I_{OH} = -0.3mA
Output low voltage	V_{OL}			0.4	V	I_{OL} = 1.6mA
Input high voltage	V_{IH}	2.5			V	
Input low voltage	V_{IL}			0.8	V	
Input leakage current	V_{IL}			10	μA	V_{IN} = 0V
Input high current	V_{IH}			10	μA	V_{IN} = 5.25V
Vcc current	I_{CC}		70	114	mA	T_{amb} = 0°C to +70°C
			70	120	mA	T_{amb} = -55°C to +125°C

Switching Characteristics

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Maximum parallel load or dump frequency	f_P	4.1†	5		MHz	
Delay, PL or SL high to $\overline{IR}$ inactive	t_{IR+}		180	200	ns	
Delay, PL or SL low to $\overline{IR}$ active	t_{IR}		200	350	ns	
Minimum PL or PD high time	$t_{pwH(P)}$			80	ns	
Minimum PL or PD low time	$t_{pwL(P)}$			100	ns	
Minimum SL or SD high time	$t_{pwH(S)}$			80	ns	
Minimum SL or SD low time	$t_{pwl(S)}$			80	ns	
Data hold time	$t_{h(D)}$			200	ns	
Data set-up time	$t_{s(D)}$			0	ns	to PL
				0	ns	to SL
Delay, PD or SD high to OR low	t_{OR+}		125	240	ns	OE high
Delay, PD or SD low to OR high	t_{OR-}		200	400	ns	DE high
Ripple through time	t_{PT}		1.0	2.5	μs	FIFO empty
Delay, PD low to data out changing	t_{DH}			240	ns	
Delay, data out to OR high	t_{DA}	0			ns	PD = high
Minimum reset pulse width	t_{MRW}			290	ns	
Delay, OE low to output off	t_{DO}			250	ns	
Delay, OE high to output active	t_{EO}			250	ns	
Delay from PL or SL low to FLAG high or PD or SD low to FLAG low	t_{DF}		700	1.0	ns	
Input capacitance	C_I			7	pF	

NOTES
1. $\overline{IR}$ is active low.
2. Minimum and maximum delays generally occur at opposite temperature extremes. Devices at approximately the same temperature will have compatible switching characteristics and will drive each other.

+ Cascadability is only guaranteed up to 3MHz.

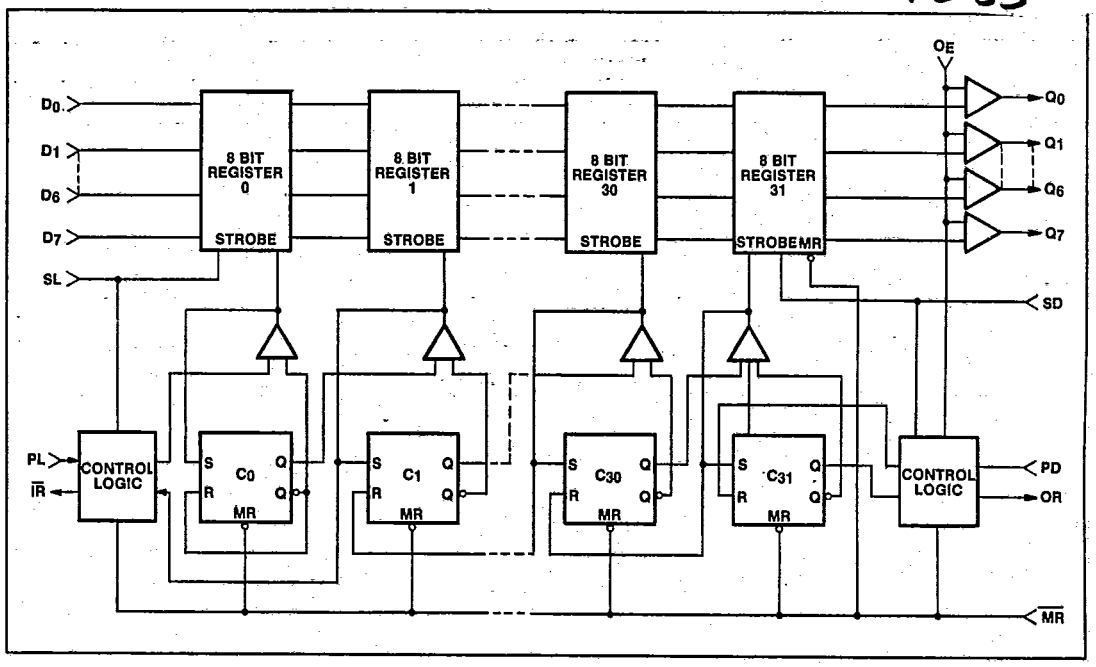

Fig.3 Logic block diagram

MJ2812HS FIFO OPERATION

The MJ2812HS FIFO consists internally of 32 data registers and one 32-bit control register, as shown in the logic block diagram. A '1' in a bit of the control register indicates that a data word is stored in the corresponding data register. A '0' in a bit of the control register indicates that the corresponding data register does not contain valid data. The control register directs the movement of data through the data registers. Whenever the (n)th bit of the control register contains a '1' and the (n + 1)th bit contains a '0', then a strobe is generated causing the (n + 1)th data register to read the contents of the (n)th data register, simultaneously setting the (n + 1)th control register bit and clearing the (n)th control register bit, so that the control strobe moves with the data. In this fashion data in the data register moves down the stack of data registers toward the output as long as there are 'empty' locations ahead of it. The fall through opertion stops when the data reaches a register n with a '1' in the (n + 1)th control register bit, or the end of the register.

Data is initially loaded from the data inputs by applying a low-to-high transition on the parallel load (PL) input. A '1' is placed in the first control register bit simultaneously. The first control register bit is returned buffered, to the input ready ($\overline{IR}$) output, and this pin goes inactive indicating that data has been entered into the first data register and the input is now 'busy', unable to accept more data. When PL next goes low, the fall through process begins (assuming that at least the second location is empty). The data in the first register is copied into the second, and the first control register bit is cleared. This caused $\overline{IR}$ to go active, indicating the inputs are available for another data word.

Note: The device will malfunction if a data load is attempted when the inputs are not ready (as indicated by the $\overline{IR}$ output signals).

The data falling through the register stacks up at the output end. At the output the last control register bit is buffered and brought out as Output Ready (OR). A high on OR indicates there is a '1' in the last control register bit and therefore there is valid data on the data outputs. A parallel dump command is used to shift the data word out of the FIFO. A low-to-high transition on PD clears the last register bit, causing OR to go LOW, indicating that the data on the outputs may no longer be valid. When PD goes low, the '0' which is now present at the last control register bit allows the data in the next to the last register to move into the last register position and on to the outputs. The '0' in the control register then 'bubbles' back toward the input as the data shifts towards the output.

If the memory is emptied by reading out all the data, then when the last word is being read out and PD goes high, OR will go low as before, but when PD next goes low, there is no data to move into the last location, so OR remains low until more data arrives at the output. The last data word will be retained at the output. Similarly, when the memory is full data written into the first location will not shift into the second when PL goes low, and $\overline{IR}$ will remain inactive instead of returning to an active state.

The pairs of input and output control signals are designed so that the PD input of one FIFO can be driven by the $\overline{IR}$ output of another, and the OR output of the first FIFO can drive the PL input of the second, allowing simple expansion of the FIFO to any depth. Wider buffers are formed by allowing parallel rows of FIFO's to operate together.

ABSOLUTE MAXIMUM RATINGS

Storage temperature	-65°C to +150°C
Temperature (ambient) under bias	-55°C to +125°C
Voltage on any pin w.r.t. ground (0V)	-0.3V to +9V
DC input voltage	-0.3V to +6V

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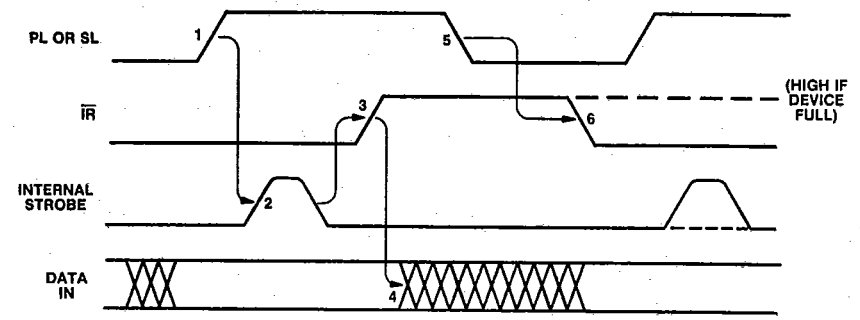
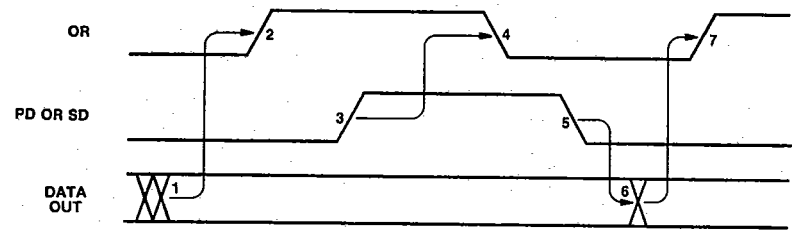


MJ2812HS INPUT TIMING

When data is steady PL is brought high (1) causing internal data strobe to be generated (2). When data has been loaded, $\overline{IR}$ goes high (3) and data may be changed (4). $\overline{IR}$ remains high until PL is brought low (5); then $\overline{IR}$ goes low (6) indicating new data may be entered.



MJ2812HS OUTPUT TIMING

When data out is steady (1), OR goes high (2). When PD goes high (3), OR goes low (4). When PD goes low again (5), the output data changes (6) and OR returns high (7).

The input and output timing diagram above illustrate the sequence of control on the MJ2812HS. Note that PL matches OR and IR matches PD in time, as though the signals were driving each other.

Fig.4 MJ2812HS timing diagram

Because the input ready signal is active low on the MJ2812HS a peculiarity occurs when several devices are placed end-to-end. When the second unit of two MJ2812HSs fills up, the data out of the first is not dumped immediately. That is, no shift out command occurs, so that the data last written into the second device remains on the output of the first until an empty location bubbles up from the output. The net effect is that n MJ2812HSs connected end-to-end store $31n + 1$ words (instead of 32n).

Flag Output

A flag output is available on the MJ2812HS to indicate when the FIFO is approximately half full. Assuming the memory is empty, the flag output will go high within 1μs of the 13th word being loaded into the memory (14 high-low transitions on PL or 112 transitions on SL). Assuming a full memory the flag output will go low within 1μs of the 20th PD or 160th SD high-low transition, i.e. when 13 words remain in the memory.

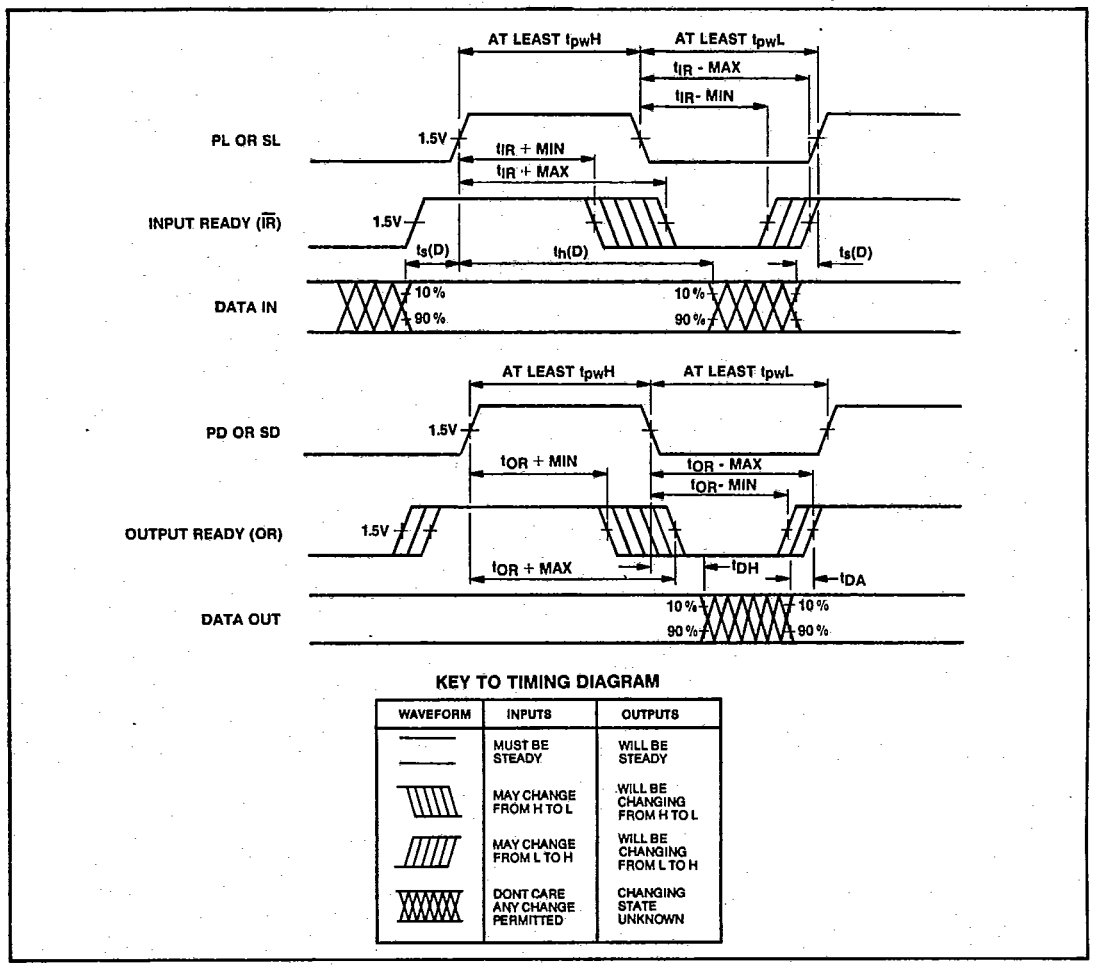
Serial Input and Output

The MJ2812HS also has the ability to read or write serial bit streams, rather than 8-bit words. The device then works like a 256 by 1-bit FIFO. A serial data stream can be loaded into the device by using the serial load input and applying data to D_0 input.

The SL signal operates just like the PL input, causing $\overline{IR}$ to go high and low as the bits are entered. The data is simply shifted across the 8-bit input register until 8 bits have been entered; the 8 bits then fall through the register as though they have been loaded in parallel. Following the 8th SL pulse, $\overline{IR}$ will remain inactive if the FIFO is full.

A corresponding operation occurs on the output, with clock pulses on SD causing successive bits of data to appear on the Q_7 output. OR moves high and low with SD exactly as it does with PD. When 8 bits have been shifted out, the next word appears at the output. If a PD command is applied after the 8 bits on the outputs have been partially shifted out, the remainder of the word is dumped and the new 8-bit word is brought to the output. OR will stay low if the FIFO is empty.

When the serial input or output clock is used, the corresponding parallel control line should be grounded and when the PD or PL controls are used the corresponding serial clocks should be grounded.



KEY TO TIMING DIAGRAM

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DONT CARE ANY CHANGE PERMITTED	CHANGING STATE UNKNOWN

Fig.5 Timing diagram

OPERATING NOTES

1. When the memory is empty the last word read will remain on the outputs until the master reset is strobed or a new data word falls through to the output. However, OR will remain low, indicating data at the output is not valid.
2. When the output data changes as a result of a pulse on PD, the OR signal always goes low before there is any change in output data and always stays low until after the new data has appeared on the outputs, so any time OR is high, there is good, stable data on the outputs.
3. If PD is held high while the memory is emptied and a word is written into the input, then that word will fall through the memory to the output. OR will go high for one internal cycle (at least t_{OR+}) and then will go back low again. The stored word will remain on the outputs. If more words are written into the FIFO, they will line up behind the first word and will not appear on the outputs until PD has been brought low.
4. When the master reset is brought low, the control register and the outputs are cleared and the control logic is initialised. $\overline{IR}$ and OR go low. If PL is high when the master reset goes high then $\overline{IR}$ will remain in the high state until PL is brought low. If PL is low when the master reset is ended, then $\overline{IR}$ will be low until PL goes high.
5. The output enable pin OE inhibits dump commands while it is low and forces the Q outputs to a high impedance state.
6. The serial load and dump lines should not be used for interconnecting two FIFOs. Use the parallel interconnection instead.
7. If less than eight bits have been shifted in using the serial load command, a parallel load pulse will destroy the data in the partially filled input register.
8. The $\overline{IR}$ and OR signals are provided to ensure that data is written into, or read out of, the FIFO correctly. If the specified minimum pulse widths, for PL, SL, PD or SD are not provided *after* an $\overline{IR}$ or OR transition the memory may corrupt and lock out any further data input. The memory should be cleared to restore normal operation.