TV CAMERA SYNC GENERATOR

GENERAL DESCRIPTION

The MMC 371 camera sync generator is a metal-gate CMOS integrated circuit designed to supply the basic output functions for the monochrome 625 line/50 Hz and 525 line/60 Hz interlaced camera for closed TV system. The output signals are supplied for both OIRT and CCIR standards.
The MMC 371 can operate from any of two frequency sources: an internal oscillator with an externa crystal or an externally applied clock signal (4 MHz for the 625 line/50 Hz camera and 4.032 MHz for the 525 line/60 Hz camera).

FEATURES

- Output functions for the monochrome 625 line/50 Hz and 525 line/60 Hz interlaced cameras.
- Output signals to control multiple camera installations
- Internal oscillator or external frequency source.

ABSOLUTE MAXIMUM RATINGS

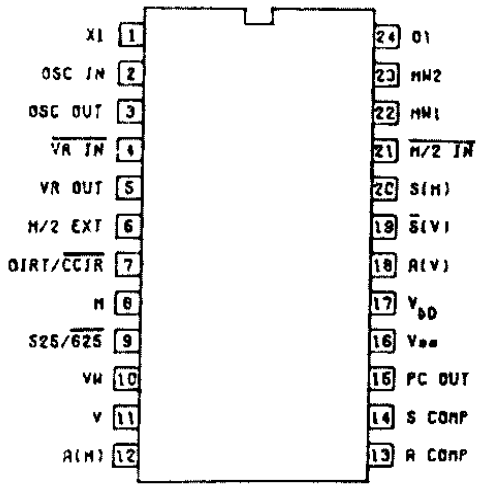
V_{DD}*	Supply voltage:			
V_i	Input voltage	-0.5 to	18	V
I_i	DC input current (any one input)	-0.5 to	V_{DD}+0.5	V
P_{tot}	Total power dissipation (per package)		±10	mA
	Dissipation per output transistor		200	mW
	for T_A = full package-temperature range		100	mW
T_A	Operating			
	temperature :			
	E and F types	-40 to	85	°C
T_{stg}	Storage temperature	-65 to	150	°C

* All voltage values are referred to V_{SS} pin voltage

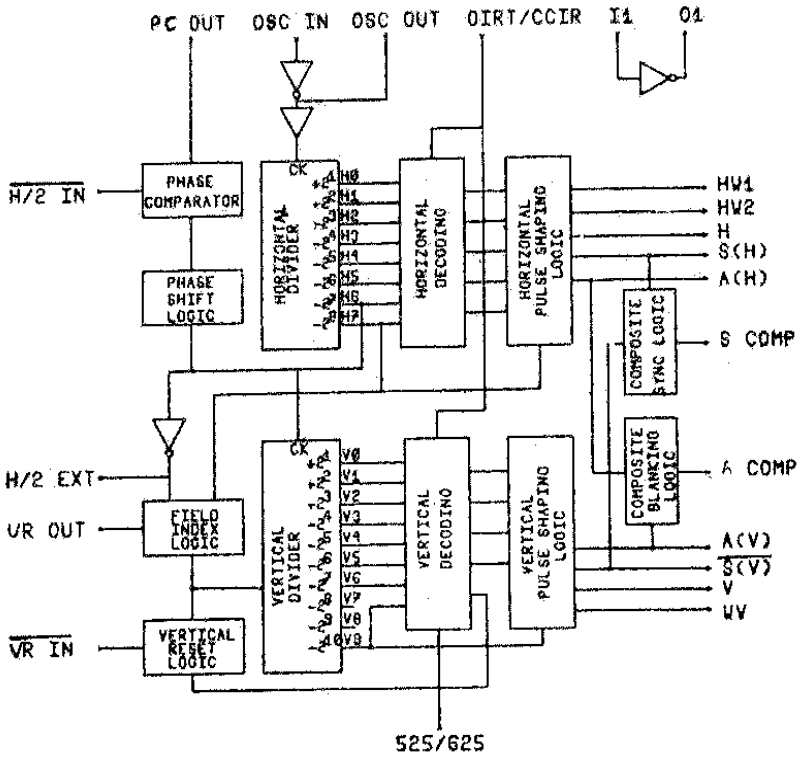
RECOMMENDED OPERATING CONDITIONS

V_{DD}*	Supply voltage:	5 to	15	V
V_i	Input voltage	0 to	V_{DD}	V
T_A	Operating			
	temperature :	-55 to	125	°C
	E and F types	-40 to	85	°C

CONNECTION DIAGRAM



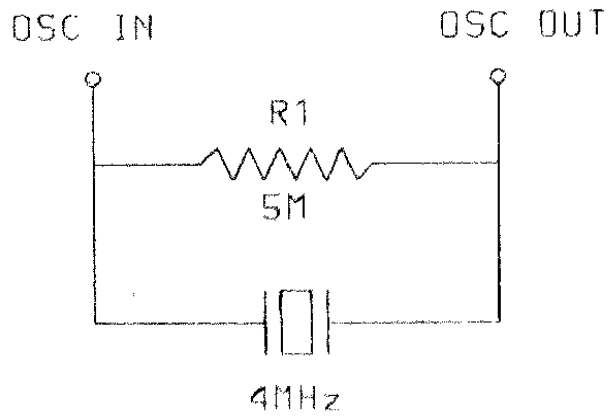
BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The MMC 371 sync generator operates with a 4 MHz clock frequency for the 625 line/50Hz camera, and with 4.032 MHz clock frequency for the 525 line/60 Hz camera. When using an external frequency source to operate the MMC 371, that signal should be applied at OSC IN pin.

For the operation in the crystal oscillator mode, a crystal and a resistor R must be connected to the on-chip CMOS inverter/amplifier between OSC IN and OSC OUT pins, as shown in figure bellow. The output of the oscillator is cleaned up by next two internal inverters and applied on the input of a 2^8 by divider to obtain the frequency of horizontal signals. The horizontal divider is operated on the falling edge of the signal from the OSC OUT pin. The input clock signal divided by 2^7 is applied on the input of the vertical 2^{10} by divider that is reseted after the necessary number of lines 262,5 lines for the 525 line/60Hz camera and 312, 5 lines for the 625 line/50 Hzcamera) to obtain the TV fields.



For the external synchronization of the MMC 371 sync generator circuit two external signals must be applied on the H/2 IN and VR IN simultaneonly.

H/2 IN is the input of a digital phase comparator based on a $\overline{SR}$ latch. The result of the phase comparation between the external H/2 IN signal and the internal signal of same frequency is used to control the local oscillator.

The external signal applied on $\overline{VR\ IN}$ resets the vertical dividers at the beginning of the fields.

The MMC 371 sync generator provides the output signals: H/2 EXT and VR OUT for synchronizing other MMC 371 sync generators.

A functional description of the circuit pins is given bellow:

I1, Pin 1

Independent inverter input. (See block diagram)

OSC IN, Pin 2

Osculator input or external frequency source input

OSC OUT, Pin 3

Oscilator output or inverted OSC IN signal output

$\overline{VR\ IN}$, Pin 4

Vertical reset input. A low level voltage applied on this input resets the vertical dividers at the beginning of the fields.

The external vertical reset signal must be a negative pulse that occurs once at two fields within the H/2 IN signal positive semiperiod.

When unused, this input must be connected to V_{DD}.

VR OUT, Pin 5

Vertical reset output. This signal is a pulse that occurs once each even field, at the leading edge of A(V) in that field (see fig. 6).

It can be used for external synchronization of other MMC 371 circuits.

H/2 EXT, Pin 6
Horizontal external sunchronization output signal (fig. 6). The frequency of this signal is twice the frequency of the horizontal signals.

OIRT/$\overline{\text{CCIR}}$, Pin 7
A logic „1" level on OIRT/$\overline{\text{CCIR}}$ selects the OIRT output functions.
A logic „0" level on OIRT/$\overline{\text{CCIR}}$ selects the CCIR output functions.

H, Pin 8
Horizontal drive output signal (see fig. 5)

525/$\overline{\text{625}}$, Pin 9
A logic „1" level on 525/625 selects the internal vertical reset for the 525 line/60 Hz camera.
A logic „0" level on 525/625 selects the internal vertical reset for the 625 line/50 Hz camera.

VW, Pin 10
Vertical write output signal, for the 625 line/50 Hz. camera.
It is a pulse that begins after 26 lines from the leading edge of A(V) and ends after 240 lines (see fig. 6).

V, Pin 11
Vertical drive output signal (see fig. 6)

A(H), Pin 12
Horizontal blanking output signal (see fig. 5)

A COMP, Pin 13
Composite blanking output signal (see fig. 4)

S COMP, Pin 14
Composite sync output signal (see fig. 4)

PC OUT, Pin 15
Digital phase comparator output. It is the Q output of a $\overline{\text{SR}}$ latch.
The signal from this output is the results of the comparation between the external $\overline{\text{H/2 IN}}$ signal and the internal signal of same frequency and can be used to command the local oscillator.

V_{SS}, Pin 16
Ground

V_{DD}, Pin 17
Positive supply voltage

A(V), Pin 18
Vertical blanking output signal (see fig. 6)

S(V), Pin 19
Vertical sync output signal (see fig. 6)

S(H), Pin 20
Horizontal sync output signal (see fig. 5)

H/2 IN, Pin 21
Horizontal external synchronization input signal. This signal is applied on the $\overline{\text{S}}$ input of a $\overline{\text{SR}}$ latch for digital phase comparation (see also PC out, Pin 15). The frequency of the external H/2 IN signal is twice the frequency of horizontal signals.
When unused, H/2 IN will be connected to V_{SS}

HW1, Pin 22
„Horizontal Write 1" output signal, for the 625 line/50 Hz camera.
It consists of 80 pulses of 0,5 μs each on a line, (see fig. 5).

HW2, Pin 23
„Horizontal Write 2" output signal, for the 625 line/50 Hz camera.
It consists of 40 pulses of 1 μs each on a line, (see fig. 5).

O1, Pin 24
Inverter output. (See block diagram)

TIMING DIAGRAMS

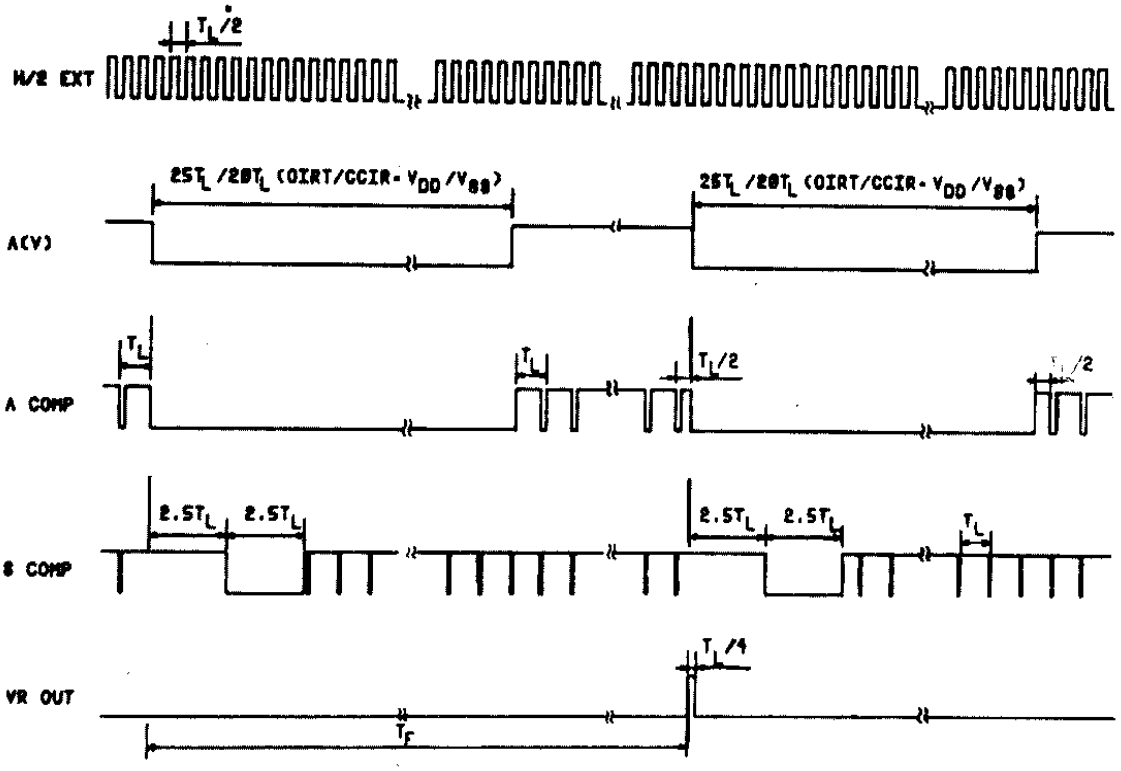


Figure 4

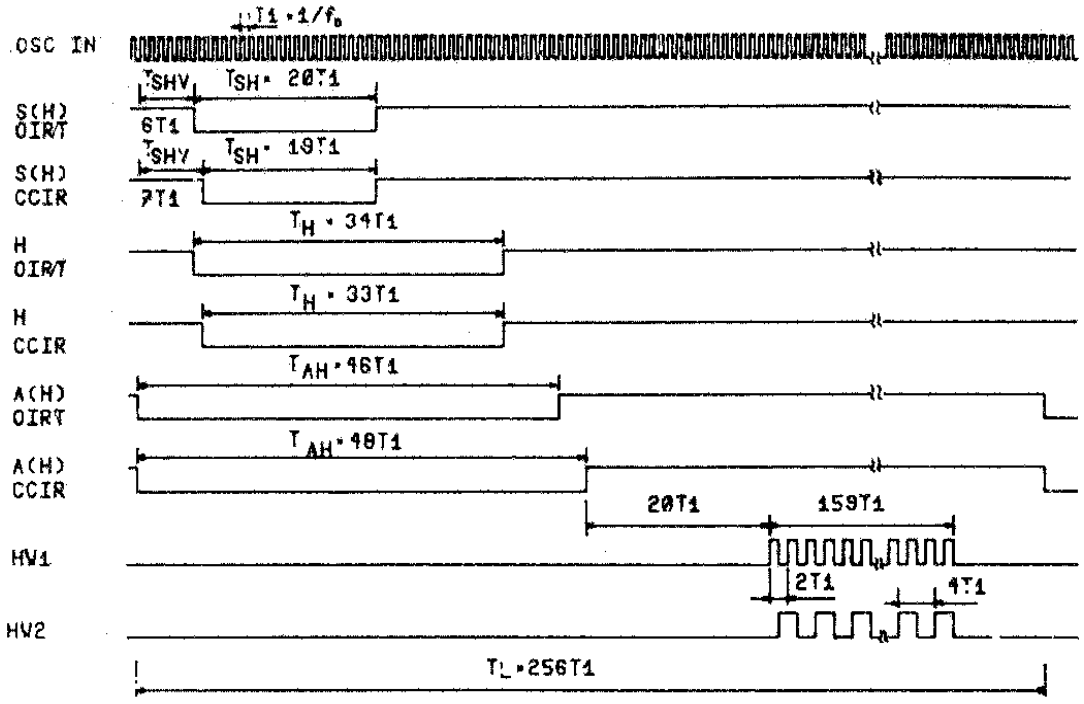


Fig. 5 Horizontal timing fo is the clock frequency

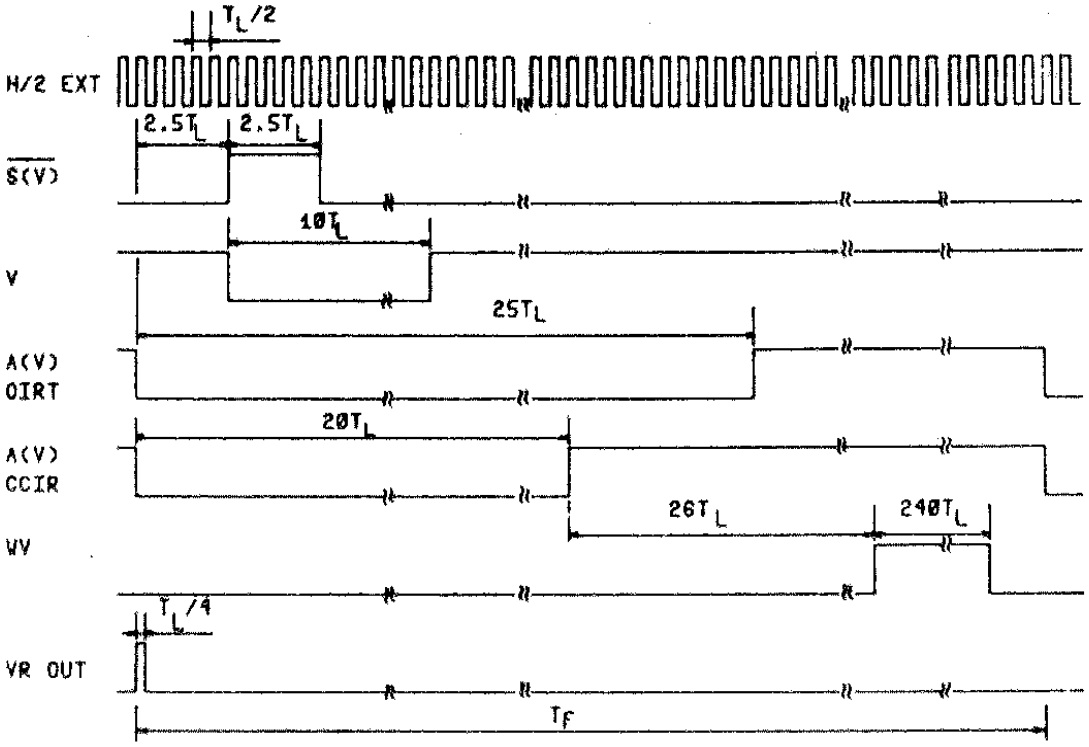


Fig.6 Vertical timing

$T_F = 262.5T_L$ for 525/625 V_{DD} ; $T_F = 312.5T_L$ for 525/625 V_{SS} .

only for 525/625 V_{SS} .

STATIC ELECTRICAL CHARACTERISTICS

(T_A = 25 C)

PARAMETER		TEST CONDITIONS				VALUES		UNIT
		V_I (V)	V_O (V)	I_O (uA)	V_{DD} (V)	Min.	Max.	
I_I	Quiescent current	0/5 0/10 0/15			5 10 15		200 400 800	µA
V_{IH}	Input high voltage		0.5/4.5 1/9 1.5/13.5	<1 <1 <1	5 10 15	3.5 7 11		V
V_{IL}	Input low voltage		4.5/0.5 9/1 13.5/1.5	<1 <1 <1	5 10 15		1.5 3 4	V
V_{OH}	Output high voltage	0/5 0/10 0/15		<1 <1 <1	5 10 15	4.9 9.9 14.9		V
V_{OL}	Output low voltage	5/0 10/0 15/0		<1 <1 <1	5 10 15		0.1 0.1 0.1	V
I_{OH}	Output drive current	0/5 0/5 0/10 0/15	2.5 4.6 9.5 13.5		5 5 10 15	0.8 0.3 0.6 1.5		mA
I_{OL}	Output sink current	5/0 10/0 15/0	0.4 0.5 1.5		5 10 15	0.3 0.6 1.5		mA
I_{IL}, I_{IH}	Input leakage current	0/15	Any input		15		±0.3	µA

The Noise Margin for both "1" and "0" level is:

1 V min. with V_{DD} = 5 V
2 V min. with V_{DD} = 10 V
2.5 V min. with V_{DD} = 15 V

DYNAMIC ELECTRICAL CHARACTERISTICS

(T_A = 25°C, C_L = 15 pF, R_L = 200 k, typical temperature coefficient for all V_{DD} values is 0.3%/°C, all input rise and fall time = 20 ns)

	PARAMETER	TEST CONDITIONS	VALUES			UNIT
		V_{DD} (V)	min.	typ.	max.	
t_W	Clock pulse width (external frequency source)	5 10 15	115		135	ns
t_{TLH} t_{THL}	Transition time	5 10 15			200 100 80	ns
t_{PLH}	Propagation delay from OSC IN to A(H)	5 10 15		450 200 130	650 300 200	ns
t_{PHL}	Propagation delay from OSC IN to A(H)	5 10 15		650 300 180	850 500 350	ns
t_{PLH}, t_{PHL}	Propagation delay from OSC IN to H, S(H), H/2 EXT, HW1, HW2	5 10 15		450 200 130	650 300 200	ns