400 MSPS 14-Bit, 1.8V CMOS Direct Digital Synthesizer

Preliminary Technical Data AD9954

FEATURES

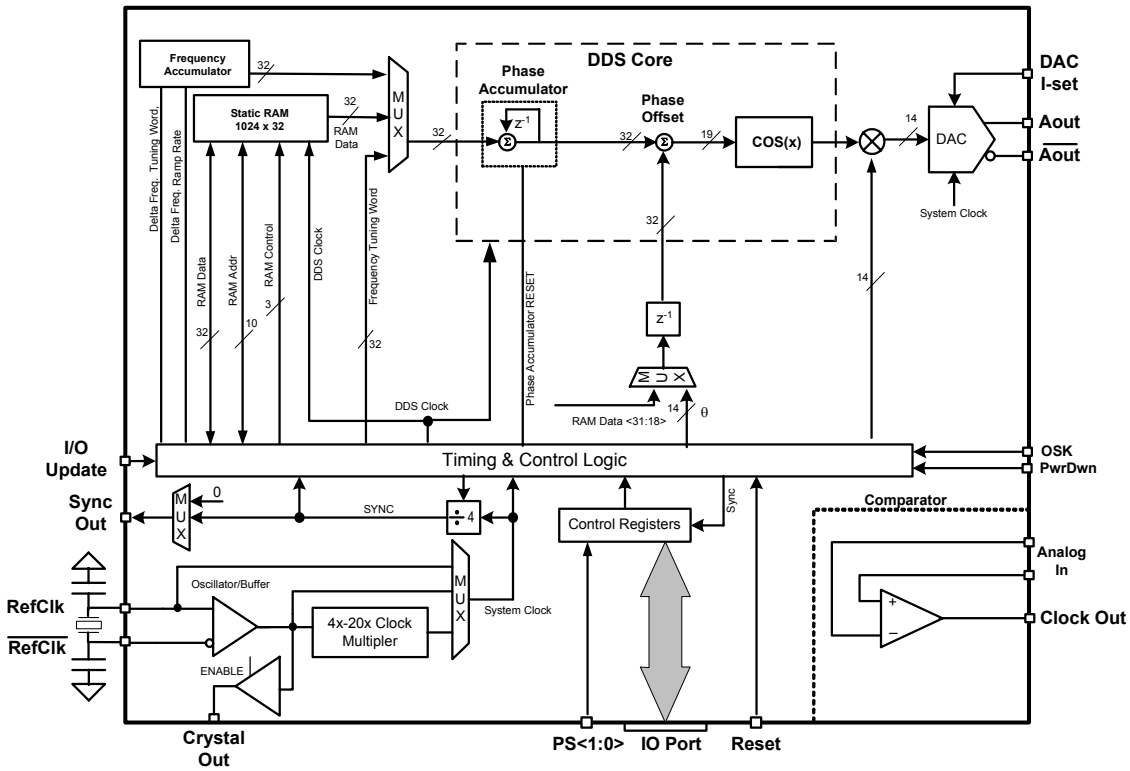
400 MSPS Internal Clock Speed
Integrated 14-bit D/A Converter
Programmable phase/amplitude dithering
32-bit Tuning Word
Phase Noise <=-125 dBc/Hz @ 1KHz offset (DAC output)
Excellent Dynamic Performance
80dB SFDR @ 130MHz (+/- 100KHz Offset) Ao ut
Serial I/O Control
Ultra-high speed analog comparator, <1psRMS jitter
Automatic linear and non-linear frequency Sweeping capability
4 Frequency/Phase Offset Profiles
1.8V Power Supply
Software and Hardware controlled power down
48-lead EPAD-TQFP package

Linear and non-linear frequency sweeping capability
Integrated 1024x32 word RAM
Support for 5v input levels on most digital inputs
PLL REFCLK multiplier (4X to 20X)
Internal oscillator, can be driven by a single crystal
Phase modulation capability
Multi-Chip Synchronization

APPLICATIONS

Agile L.O. Frequency Synthesis
Programmable Clock Generator
FM Chirp Source for Radar and Scanning Systems
Automotive Radar
Test and Measurement Equipment
Acousto-Optic Device Driver

Functional Block Diagram



REV. PrB

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GENERAL DESCRIPTION

The AD9954 is a Direct Digital Synthesizer (DDS) featuring a 14-bit DAC operating up to 400MSPS. The AD9954 uses advanced DDS technology, coupled with an internal high-speed, high performance D/A converter to form a digitally-programmable, complete high-frequency synthesizer capable of generating a frequency-agile analog output sinusoidal waveform at up to 200 MHz. The AD9954 is designed to provide fast frequency hopping and fine tuning resolution (32-bit frequency tuning word). The frequency tuning and control words are loaded into the AD9954 via a serial I/O port. The AD9954 includes an integrated 1024x32 Static RAM to support flexible frequency sweep capability in several modes. The AD9954 also supports a user defined linear sweep mode of operation. The device includes an on-chip high speed comparator for applications requiring a square wave output.

The AD9954 is specified to operate over the extended industrial temperature range of -40° to +85°C.

ABSOLUTE MAXIMUM RATINGS[1]

Maximum Junction Temp. ..... +150 °C
Vs ..... +4 V
Digital Input Voltage..... -0.7 V to +Vs
Digital Output Current ..... 5 mA
Storage Temperature ..... -65 °C to +150 °C
Operating Temp. ..... -40 °C to +85 °C
Lead Temp. (10 sec. soldering) ..... +300 °C
θ_{JA} ..... 38°C/W
θ_{JC} 15 °C/W

***** Absolute maximum ratings are limiting values, to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied. Exposure of absolute maximum rating conditions for extended periods of time may affect device reliability.

CONTENTS

AD9954 PRELIMINARY ELECTRICAL SPECIFICATIONS

(Unless otherwise noted: (V_S=+1.8 V ±5%, R_{SET}=1.96 kΩ, External reference clock frequency = 20 MHz with REFCLK Multiplier enabled at 20×)

Parameter	Temp	Test Level	AD9954 Min	AD9954 Typ	AD9954 Max	Units
REF CLOCK INPUT CHARACTERISTICS						
Frequency Range						
REFCLK Multiplier Disabled	FULL	VI	1		400	MHz
REFCLK Multiplier Enabled at 4X	FULL	VI	20		100	MHz
REFCLK Multiplier Enabled at 20X	FULL	VI	4		20	MHz
Input Capacitance	+25°C	V		3		pF
Input Impedance	+25°C	V		100		MΩ
Duty Cycle	+25°C	V		50		%
Duty Cycle with REFCLK Multiplier Enabled	+25°C	V	35		65	%
DAC OUTPUT CHARACTERISTICS						
Resolution				14		Bits
Full Scale Output Current	+25°C		5	10	15	mA
Gain Error	+25°C	I	-10		+10	%FS
Output Offset	+25°C	I			0.6	µA
Differential Nonlinearity	+25°C	V		1		LSB
Integral Nonlinearity	+25°C	V		2		LSB
Output Capacitance	+25°C	V		5		pF
Residual Phase Noise @ 1 kHz Offset, 40 MHz A_{out}						
REFCLK Multiplier Enabled @ 20×	+25°C	V		-89		dBc/Hz
REFCLK Multiplier Enabled @ 4×	+25°C	V		-105		dBc/Hz
REFCLK Multiplier Disabled	+25°C	V		-116		dBc/Hz
Voltage Compliance Range	+25°C	I	AVDD-0.375		AVDD + 0.25V	V
Wideband SFDR:						
1 – 20 MHz Analog Out	+25°C	V				dBc
20 – 40 MHz Analog Out	+25°C	V				dBc
40 – 60 MHz Analog Out	+25°C	V				dBc
60 – 80 MHz Analog Out	+25°C	V				dBc
80 – 100 MHz Analog Out	+25°C	V				dBc
100 – 120 MHz Analog Out	+25°C	V				dBc
120 – 140 MHz Analog Out	+25°C	V				dBc
140 – 160 MHz Analog Out	+25°C	V				dBc
Narrow Band SFDR						
10 MHz Analog Out (±1 MHz)	+25°C	V				dBc
10 MHz Analog Out (±250 kHz)	+25°C	V				dBc
10 MHz Analog Out (± 50 kHz)	+25°C	V				dBc
10 MHz Analog Out (± 10 kHz)	+25°C	V				dBc
65 MHz Analog Out (± 1 MHz)	+25°C	V				dBc
65 MHz Analog Out (± 250 kHz)	+25°C	V				dBc
65 MHz Analog Out (± 50 kHz)	+25°C	V				dBc
65 MHz Analog Out (± 10 kHz)	+25°C	V				dBc
80 MHz Analog Out (± 1 MHz)	+25°C	V				dBc
80 MHz Analog Out (± 250 kHz)	+25°C	V				dBc
80 MHz Analog Out (± 50 kHz)	+25°C	V				dBc
80 MHz Analog Out (± 10 kHz)	+25°C	V				dBc
100 MHz Analog Out (± 1 MHz)	+25°C	V				dBc
100 MHz Analog Out (± 250 kHz)	+25°C	V				dBc
100 MHz Analog Out (± 50 kHz)	+25°C	V				dBc
100 MHz Analog Out (± 10 kHz)	+25°C	V				dBc
120 MHz Analog Out (± 1 MHz)	+25°C	V				dBc
120 MHz Analog Out (± 250 kHz)	+25°C	V				dBc
120 MHz Analog Out (± 50 kHz)	+25°C	V				dBc
120 MHz Analog Out (± 10 kHz)	+25°C	V				dBc
140 MHz Analog Out (± 1 MHz)	+25°C	V				dBc
140 MHz Analog Out (± 250 kHz)	+25°C	V				dBc
140 MHz Analog Out (± 50 kHz)	+25°C	V				dBc
140 MHz Analog Out (± 10 kHz)	+25°C	V				dBc
160 MHz Analog Out (± 1 MHz)	+25°C	V				dBc
160 MHz Analog Out (± 250 kHz)	+25°C	V				dBc

Parameter	Temp	Test Level	Min	Typ	Max	Units
160 MHz Analog Out (± 50 kHz)	+25°C	V				dBc
160MHz Analog Out (± 10 kHz)	+25°C	V				dBc
COMPARATOR INPUT CHARACTERISTICS						
Input Capacitance	+25°C	V		3		pF
Input Resistance	+25°C	IV		500		kΩ
Input Current	+25°C	I		±12		µA
Hysteresis	+25°C	IV	30		45	mV
COMPARATOR OUTPUT CHARACTERISTICS						
Logic "1" voltage, high Z load	FULL	VI	+1.6			V
Logic "0" voltage, high Z load	FULL	VI			+0.4	V
Propagation Delay	+25°C	IV		3		ns
Output Duty Cycle Error[3]	+25°C	IV		±5		%
Rise/Fall Time, 5pF load	+25°C	IV			1	Ns
Toggle Rate, high Z load	+25°C	IV				MHz
Output Jitter[4]	+25°C	IV			1	ps RMS
COMPARATOR NARROWBAND SFDR[2]						
10MHz (1MHz)	+25°C	V		80		dBc
10MHz (250KHz)	+25°C	V		85		dBc
10MHz (50KHz)	+25°C	V		90		dBc
10MHz (10KHz)	+25°C	V		95		dBc
70MHz (1MHz)	+25°C	V		80		dBc
70MHz (250KHz)	+25°C	V		85		dBc
70MHz (50KHz)	+25°C	V		90		dBc
70MHz (10KHz)	+25°C	V		95		dBc
110MHz (1MHz)	+25°C	V		80		dBc
110MHz (250KHz)	+25°C	V		85		dBc
110MHz (50KHz)	+25°C	V		90		dBc
110MHz (10KHz)	+25°C	V		95		dBc
140MHz (1MHz)	+25°C	V		80		dBc
140MHz (250KHz)	+25°C	V		85		dBc
140MHz (50KHz)	+25°C	V		90		dBc
140MHz (10KHz)	+25°C	V		95		dBc
160MHz (1MHz)	+25°C	V		80		dBc
160MHz (250KHz)	+25°C	V		85		dBc
160MHz (50KHz)	+25°C	V		90		dBc
160MHz (10KHz)	+25°C	V		95		dBc
CLOCK GENERATOR OUTPUT JITTER[3]						
5 MHz A_{OUT}	+25°C	V		20		ps RMS
10 MHz A_{OUT}	+25°C	V		20		ps RMS
40 MHz A_{OUT}	+25°C	V		20		ps RMS
80 MHz A_{OUT}	+25°C	V		20		ps RMS
120 MHz A_{OUT}	+25°C	V		20		ps RMS
140 MHz A_{OUT}	+25°C	V		20		ps RMS
160 MHz A_{OUT}	+25°C	V		20		ps RMS
TIMING CHARACTERISTICS						
Serial Control Bus	FULL	IV				
Maximum Frequency	FULL	IV			25	MHz
Minimum Clock Pulse Width Low (t_{PWL})	FULL	IV	7			ns
Minimum Clock Pulse Width High (t_{PWH})	FULL	IV	7			ns
Maximum Clock Rise/Fall Time	FULL	IV		5		ns
Minimum Data Setup Time (t_{DS})	FULL	IV	10			ns
Minimum Data Hold Time (t_{DH})	FULL	IV	0			ns
Maximum Data Valid Time (t_{DV})	FULL	IV	25			ns
Wake-Up Time[4]	FULL	IV		1		ms
Minimum Reset Pulsewidth High (t_{RH})	FULL	IV	5			SYSCLK cycles[5]
CMOS LOGIC INPUTS						
Logic "1" Voltage @ DVDD = 1.8V	+25°C	I	1.25			V
Logic "0" Voltage @ DVDD = 1.8V	+25°C	I			0.6	V
Logic "1" Voltage @ DVDD = 3.3V	+25°C	I	2.2			V
Logic "0" Voltage @ DVDD = 3.3V	+25°C	I			0.8	V
Logic "1" Current	+25°C	V		3	12	µA
Logic "0" Current	+25°C				12	µA
Input Capacitance	+25°C					pF
CMOS LOGIC OUTPUTS (1mA load) DVDD=1.8V						
Logic "1" Voltage	+25°C	I	1.35			V
Logic "0" Voltage	+25°C	I			0.4	V

Parameter	Temp	Test Level	Min	Typ	Max	Units
POWER SUPPLY						
+VS Current	+25°C	I			30	mA
Full Operating Conditions	+25°C	I			TBD	mA
400 MHz Clock	+25°C	I			TBD	mA
120 MHz Clock	+25°C	I			TBD	mA
Power-Down Mode	+25°C	I			TBD	mA
Full-Sleep Mode	+25°C	I			TBD	mA

NOTES

[1]Absolute maximum ratings are limiting values to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied. Exposure of absolute maximum rating conditions for extended periods of time affect device reliability.

[2]Comparator input originates from DDS section via external 7-pole elliptic LPF. Single-ended input, .5V p-p. Comparator output terminated in 50 Ohms.

[3]Represents comparator's inherent cycle-to-cycle jitter contribution.

[4]Wake-Up Time refers to recovery from analog power down modes (see Power Down Modes of Operation). The longest time required is for the Reference Clock Multiplier PLL to lock up (if it is being used). The Wake-Up Time assumes that there is no capacitor on DAC_BP, and that the recommended PLL loop filter values are used.

[5]SYSCLK refers to the actual clock frequency used on-chip by the AD9954. If the Reference Clock Multiplier is used to multiply the external reference frequency, then the SYSCLK frequency is the external frequency multiplied by the Reference Clock Multiplier multiplication factor. If the Reference Clock Multiplier is not used, then the SYSCLK frequency is the same as the external REFCLK frequency.

EXPLANATION OF TEST LEVELS

I – 100% Production Tested.
II – 100% Production Tested at +25°C and sample tested at specified temperatures.
III – Sample Tested Only.
IV – Parameter is guaranteed by design and characterization testing.
V – Parameter is a typical value only.
VI – Devices are 100% production tested at +25°C and guaranteed by design and characterization testing for industrial operating temperature range.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD9954ASV	-40°C to +85°C	48-lead QFP EPAD	SV-48
AD9954PCB	+25°C	Evaluation Board	

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD9954 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

AD9954 Pinmap

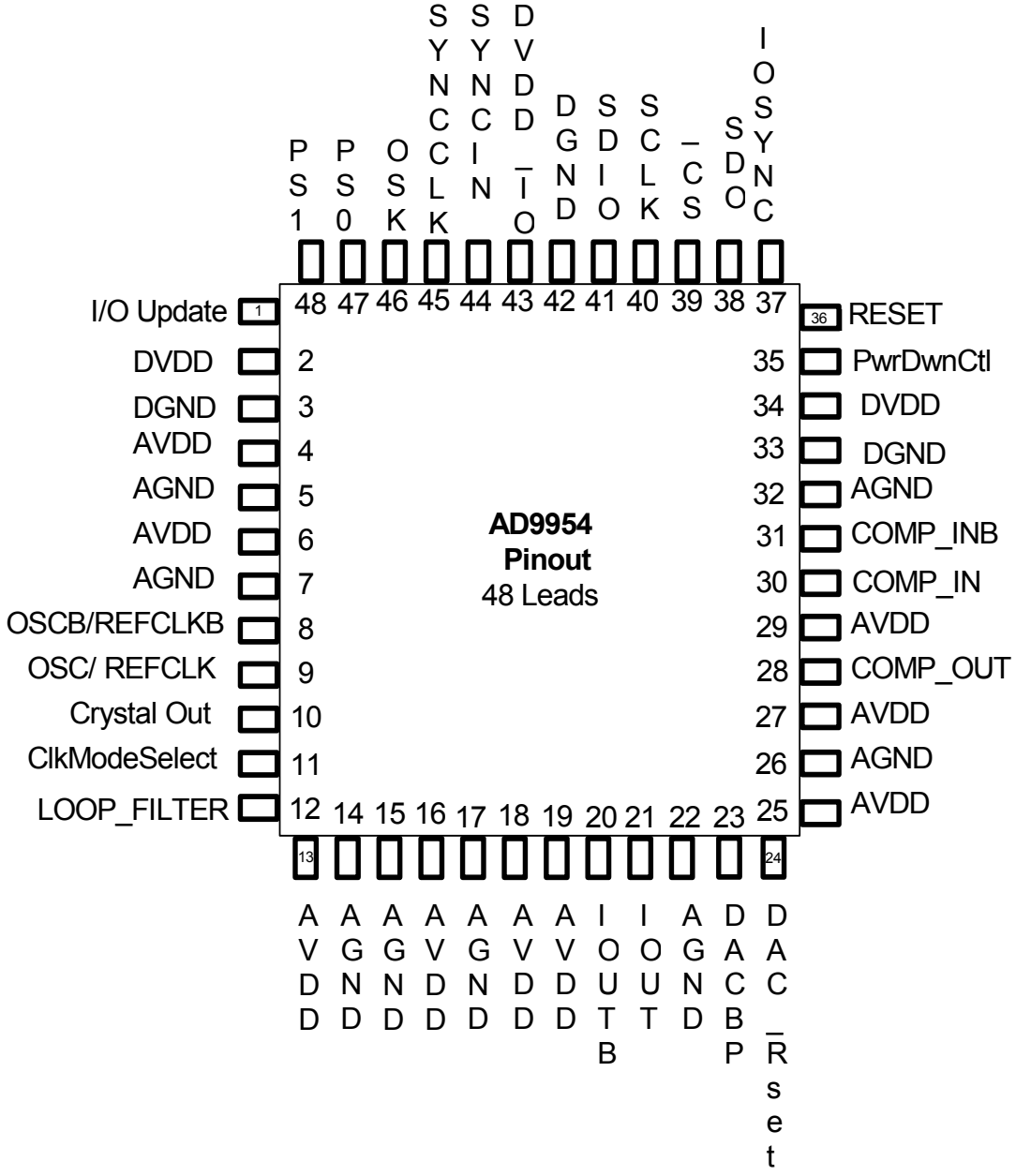

Figure 1 AD9954 Pinmap

Hardware Pin Descriptions

Pin #	Pin Name	I/O	Description
1	I/O UPDATE	I	The rising edge transfers the contents of the internal buffer memory to the IO Registers.
2,34	DVDD	I	Digital power supply pins.
3,33, 42	DGND	I	Digital power ground pins.
4,6, 13,16, 18,19, 25,27, 29	AVDD	I	Analog power supply pins.
5,7, 14,15, 17,22, 26,32	AGND	I	Analog power ground pins.
8	OSCB/REFCLKB	I	Complementary reference clock/oscillator input (400MHz max.). NOTE: When the REFCLK port is operated in single-ended mode, then REFCLKB should be decoupled to AVDD with a 0.1μF capacitor.
9	OSC/REFCLK	I	Reference clock/oscillator input (400 MHz max.). See Clock Input section of datasheet for details on the REFCLK/OSCILLATOR operation.
10	Crystal Out	O	Output of the oscillator section.
11	ClkModeSelect	I	Control pin for the oscillator section. When high, the oscillator section is enabled. When low, the oscillator section is bypassed.
12	LOOP_FILTER	I	This Pin provides the connection for the external zero compensation network of the REFCLK Multiplier's PLL loop filter. The network consists of a 1K ohm resistor in series with a 0.1 μF capacitor tied to AVDD.
20	IOUTB	O	Complementary DAC output.
21	IOUT	O	DAC output.
23	DACBP	I	DAC "biasline" decoupling pin.
24	DAC_Rset	I	A resistor (3.85KΩ nominal) connected from AGND to DAC_Rset establishes the reference current for the DAC.
28	COMP_OUT	O	Comparator Output
30	COMP_IN	I	Comparator input
31	COMP_INB	I	Comparator complementary input
35	PwrDwnCtl	I	Input pin used as an external power down control. See the External Power Down Control section of this document for details.

36	RESET	I	Active high hardware reset pin. Assertion of the RESET pin forces the AD9954 to the initial state, as described in the IO Port Register map.
37	IOSYNC	I	Asynchronous active high reset of the serial port controller. When high, the current IO operation is immediately terminated enabling a new IO operation to commence once IOSYNC is returned low
38	SDO	O	When operating the I/O port as a 3-wire serial port this pin serves as the serial data output. When operated as a 2-wire serial port this pin is the unused and can be left unconnected.
39	CS-BAR	I	This pin functions as an active low chip select that allows multiple devices to share the IO bus.
40	SCLK	I	This pin functions as the serial data clock for IO operations
41	SDIO	I/O	When operating the I/O port as a *3-wire* serial port this pin serves as the serial *data input*, only. When operated as a *2-wire* serial port this pin is the *bi-directional serial data* pin.
43	DVDD_I/O	I	Digital power supply (for IO cells only, 3.3v optional)
44	SYNC_IN	I	Input signal used to synchronize multiple AD9954s. This input is connected to the SYNC_CLK output of a different AD9954.
45	SYNC_CLK	O	Clock output pin, which serves as a synchronizer for external hardware.
46	OSK	I	Input pin used to control the direction of the Shaped On-Off Keying function when programmed for operation. OSK is synchronous to the SYNC_CLK pin. When OSK is not programmed, this pin should be tied to DGND.
47,48	PS0, PS1	I	Input pins used to select one of the four internal profiles. Profile<1:0>are synchronous to the SYNC_CLK pin. Any change in these inputs transfers the contents of the internal buffer memory to the IO Registers (sends an internal I/O UPDATE).

Table 1 Hardware Pin Descriptions

Component Blocks

DDS Core

The output frequency (f_o) of the DDS is a function of the frequency of system clock (**SYSCLK**), the value of the frequency tuning word (FTW), and the capacity of the accumulator (2^{32}, in this case). The exact relationship is given below with f_s defined as the frequency of SYSCLK.

$f_o = (FTW)(f_s) / 2^{32}$ $\{ 0 \le FTW \le 2^{31}$

$f_o = f_{s*} (1 - (FTW / 2^{32}))$ $\{ 2^{31} < FTW < 2^{32} -1$

The AD9954 frequency tuning word(s) are unsigned numbers, where 80000000(hex) represents the highest output frequency possible, commonly referred to as the Nyquist frequency. Values ranging from than 80000001(hex) to FFFFFFFF (hex) will be expressed as aliased frequencies less than Nyquist. An example using a 3-bit phase accumulator will illustrate this principle. For a tuning word of 001, the phase accumulator output (PAO) increments from all zeros to all ones and repeats when the accumulator overflows after clock cycle number 8. For the tuning word of 111, the phase accumulator output (PAO) decrements from all ones to all zeros and repeats when the accumulator overflows after clock cycle number 8. While the phase accumulator outputs are "reversed" with respect to clock cycles, the outputs provide identical inputs to the phase to amplitude converter, which means the DDS output frequencies are identical.

Mathematically, for a 3-bit accumulator, the following equations apply:

$f_o = f_{s*} (FTW / 2^3)$ $\{ 0 \le FTW \le 2^2$

$f_o = f_{s*} (1 - (FTW / 2^3))$ $\{ 2^2 < FTW < 2^3 -1$

For the 001 frequency tuning word:

$Fout = Fs * 1/2^3 = 1/8*Fs$

And for the 111 frequency tuning word:

$Fout = Fs * (1 - 7/8) = 1/8*Fs$

The value at the output of the Phase Accumulator is translated to an amplitude value via the COS(x) functional block and routed to the DAC.

In certain applications it is desirable to force the output signal to ZERO phase. Simply setting the FTW to 0 does not accomplish this. It only results in the DDS core holding its current phase value. Thus, a control bit is required to force the Phase Accumulator output to zero.

At power up the Clear Phase Accumulator bit is set to logic one but the buffer memory for this bit is cleared (logic zero). Therefore, upon power up, the phase accumulator will remain clear until the first I/O UPDATE is issued.

Phase Truncation

The 32-bit phase values generated by the Phase Accumulator are truncated to 19 bits prior to the COS(x) block. That is, the 19 most significant bits of phase are retained for subsequent processing. This is typical of standard DDS architecture and is a trade off between hardware complexity and spurious performance. It can be shown that 19-bit phase resolution is sufficient to yield 14-bit amplitude resolution with an error of less than ½ LSB. The decision to truncate at 19 bits of phase guarantees the phase error of the COS(x) block to be less than the phase error associated with the amplitude resolution of the 14-bit DAC.

Clock Input

The AD9954 supports various clock methodologies. Support for differential or single-ended input clocks, enabling of an on-chip oscillator and/or phase-locked loop (PLL) multiplier are all controlled via user programmable bits. The AD9954 may be configured in one of six operating modes to generate the system clock. The modes are configured using the ClkModeSelect pin, CFR2<0>, and CFR2<7:3>. Connecting the external pin ClkModeSelect to logic HIGH enables the on-chip crystal oscillator circuit. With the on-chip oscillator enabled, users of the AD9954 connect an external crystal to the REFCLK and REFCLKB inputs to produce a low frequency reference clock in the range of 20-30MHz. The signal generated by the oscillator is buffered before it is delivered to the rest of the chip. This buffered signal is available via the crystal out pin. Bit CFR2<0> can be used to enable or disable the buffer, turning on or off the system clock. The oscillator itself is not powered down in order to avoid long start-up times associated with turning on a crystal oscillator. Writing bit CFR2<1> to logic HIGH enables the crystal oscillator output buffer. Logic LOW at CFR2<1> disables the oscillator output buffer.

Connecting ClkModeSelect to logic LOW disables the on-chip oscillator and the oscillator output buffer. With the oscillator disabled an external oscillator must provide the REFCLK and/or REFCLKB signals. For differential operation these pins are driven with complementary signals. For single-ended operation a 0.1uF capacitor should be connected between the unused pin and the positive power supply. With the capacitor in place the clock input pin bias voltage is 1.35V. In addition, the PLL may be used to multiply the reference frequency by an integer value in the range of the 4 to 20.

The modes of operation are summarized in the table below. Please note the PLL multiplier is controlled via the CFR2<7:3> bits, independently of the CFR2<0> bit.

ClkModeSelect	CFR2<0>	CFR2<7:3>	SYSTEM CLOCK	Frequency Range (MHz)
HIGH	LOW	3 < M < 21	$F_{clk} = F_{osc}$ x M	$80 < F_{clk} < 400$
HIGH	LOW	M < 4 or M > 20	$F_{clk} = F_{osc}$	$20 < F_{clk} < 30$
HIGH	HIGH	X	$F_{clk} = 0$	$F_{clk} = 0$
LOW	X	3 < M < 21	$F_{clk} = F_{ref}$ x M	$80 < F_{clk} < 400$
LOW	X	M < 4 or M > 20	$F_{clk} = F_{ref}$	$5 < F_{clk} < 400$

Table 2 Clock Input Modes of Operation

Phase Locked Loop (PLL)

The PLL is required to facilitate multiplication of the REFCLK frequency. Control of the PLL is accomplished by programming the 5-bit REFCLK Multiplier portion of Control Function Register #2, bits <7:3>.

When programmed for values ranging from 04h – 14h (4-20 decimal), the PLL multiplies the REFCLK input frequency by the corresponding decimal value. The maximum output frequency of the PLL is restricted to 400MHz, however. Whenever the PLL value is changed, the user should be aware that time must be allocated to allow the PLL to lock (approximately 1ms).

The PLL is bypassed by programming a value outside the range of 4-20 (decimal). When bypassed, the PLL is shut down to conserve power.

DAC Output

The AD9954 incorporates an integrated 14-bit current output DAC. Two complementary outputs provide a combined full-scale output current (I_{out}). Differential outputs reduce the amount of common-mode noise that might be present at the DAC output, offering the advantage of an increased signal-to-noise ratio. The full-scale current is controlled by means of an external resistor (R_{set}) connected between the DAC_Rset pin and the DAC ground (AGND_DAC). The full-scale current is proportional to the resistor value as follows:

$$R_{set} = 39.19/I_{out}$$

The maximum full-scale output current of the combined DAC outputs is 15mA, but limiting the output to 10mA provides the best spurious-free-dynamic-range (SFDR) performance. The DAC output compliance range is AVDD+0.25V to AVDD-0.375V. Voltages developed beyond this range will cause excessive DAC distortion and could potentially damage the DAC output circuitry. Proper attention should be paid to the load termination to keep the output voltage within this compliance range.

Comparator

Many applications require a square wave signal rather than a sine wave. For example, in most clocking applications a high slew rate helps to reduce phase noise and jitter. To support these applications, the AD9954 includes an on-chip comparator. The comparator has a bandwidth greater than 200MHz and a common mode input range of 1.3V to 1.8V. By setting the comparator power-down bit, CFR1<6>, the comparator can be turned off to save on power consumption.

Serial IO Port

The AD9954 serial port is a flexible, synchronous serial communications port allowing easy interface to many industry standard micro-controllers and microprocessors. The serial I/O port is compatible with most synchronous transfer formats, including both the Motorola 6905/11 SPI and Intel 8051 SSR protocols.

The interface allows read/write access to all registers that configure the AD9954. MSB first or LSB first transfer formats are supported. In addition, the AD9954's serial interface port can be configured as a single pin I/O (SDIO), which allows a two-wire interface or two unidirectional pins for in/out (SDIO/SDO), which enables a three wire interface. Two optional pins (IOSYNC and CSB) enable greater flexibility for system design-in of the AD9954.

Register Maps and Descriptions

The Register Maps are listed in the following tables. **The appropriate register map depends on the state of the Linear Sweep Enable bit because certain registers are re-mapped depending on which mode the part is operating in**. Specifically, registers h'07, h'08, h'09 and h'0A act as the RAM segment control words for each of the RAM profile slices when the Linear Sweep Enable bit is false. When the Linear Sweep Enable Bit is true, h'07 becomes the negative linear sweep control word and h'08 becomes the positive linear sweep control word. The h'09 and h'0A registers are not used in Linear Sweep mode. Because the Linear Sweep operation takes precedence over RAM operations, ADI recommends that the RAM enable bit CFR1<31> be set to zero when the Linear Sweep Enable Bit CFR1<21> is true to conserve power. The serial address numbers associated with each of the registers are shown in hexadecimal format. Angle brackets <> are used to reference specific bits or ranges of bits. For example, <3> designates bit 3 while <7:3> designates the range of bits from 7 down to 3, inclusive.

Linear Sweep Enable Bit	Register Map
False (CFR1<21>=0)	RAM Segment Control Words Active
True (CFR1<21> = 1)	Linear Sweep Control Words Active

Table 3 Register Mapping Based On Linear Sweep Enable Bit

AD9954 Register Map – when Linear Sweep Enable Bit is False (CFR1<21>=0)

(NOTE: RAM Enable Bit CFR1<31> only activates the RAM itself, not the RAM Segment Control Words)

Register Name (Serial address)	Bit Range	(MSB) Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	(LSB) Bit 0	Default Value OR Profile
Control Function Register #1 (**CFR1**) **(00h)**	<7:0>	Digital Power Down	Comp Power Down	DAC Power Down	Clock Input Power Dwn	External Power Down Mode	Linear Sweep No Dwell	Sync CLK Out Disable	Not Used	00h
	<15:8>	Load SRR @I/O UD	AutoClr Freq. Accum	AutoClr Phase Accum	Enable SINE Output	Clear Freq Accum.	Clear Phase Accum.	SDIO Input Only	LSB First	00h
	<23:16>	Automatic Sync Enable	Software Manual Sync	Linear Sweep Enable	Amplitude Dither Enable	Phase Dither En<3>	Phase Dither En<2>	Phase Dither En<1>	Phase Dither En<0>	00h
	<31:24>	RAM Enable	RAM Dest. Is Phase Word	Internal Profile Control <2:0>			Load ARR @I/O UD	OSK Enable	Auto OSK Keying	00h
Control Function Register #2 **(CFR2) (01h)**	<7:0>	REFCLK Multiplier 00h or 01h or 02h or 03h: Bypass Multiplier 04h –14h: 4x – 20x multiplication					VCO Gain	Charge Pump Control <1:0>		00h
	<15:8>	**not used**				High Speed Sync Enable	Hardware Manual Sync Enable	Crystal Out Pin Active	DAC Prime Data Disable	00h
	<23:16>	**not used**								00h
Amplitude Scale Factor (**ASF**) **(02h)**	<7:0>	Amplitude Scale Factor Register <7:0>								00h
	<15:8>	Auto Ramp Rate Speed Control <1:0>		Amplitude Scale Factor Register <13:8>						00h
Amplitude Ramp Rate **(ARR) (03h)**	<7:0>	Amplitude Ramp Rate Register <7:0>								00h
Frequency Tuning Word (**FTW0**) **(04h)**	<7:0>	Frequency Tuning Word #0 <7:0>								00h
	<15:8>	Frequency Tuning Word #0 <15:8>								00h
	<23:16>	Frequency Tuning Word #0 <23:16>								00h
	<31:24>	Frequency Tuning Word #0 <31:24>								00h
Phase Offset Word (**POW0**) **(05h)**	<7:0>	Phase Offset Word #0 <7:0>								00h
	<15:8>	Not used<1:0>		Phase Offset Word #0 <13:8>						00h

Frequency Tuning Word (**FTW1**) **(06h)**	<7:0>	Frequency Tuning Word #1 <7:0>				00h
	<15:8>	Frequency Tuning Word #1 <15:8>				00h
	<23:16>	Frequency Tuning Word #1 <23:16>				00h
	<31:24>	Frequency Tuning Word #1 <31:24>				00h
RAM Segment Control Word #0 (**RSCW0**) **(07h)**	<7:0>	RAM Segment 0 Mode Control <2:0>	No Dwell Active	RAM Segment 0 Beginning Address <9:6>		PS0=0 PS1=0
	<15:8>	RAM Segment 0 Beginning Address <5:0>			RAM Segment 0 Final Address <9:8>	PS0=0 PS1=0
	<23:16>	RAM Segment 0 Final Address <7:0>				PS0=0 PS1=0
	<31:24>	RAM Segment 0 Address Ramp Rate <15:8>				PS0=0 PS1=0
	<39:32>	RAM Segment 0 Address Ramp Rate <7:0>				PS0=0 PS1=0
RAM Segment Control Word #1 (**RSCW1**) **(08h)**	<7:0>	RAM Segment 1 Mode Control <2:0>	No Dwell Active	RAM Segment 1 Beginning Address <9:6>		PS0=1 PS1=0
	<15:8>	RAM Segment 1 Beginning Address <5:0>			RAM Segment 1 Final Address <9:8>	PS0=1 PS1=0
	<23:16>	RAM Segment 1 Final Address <7:0>				PS0=1 PS1=0
	<31:24>	RAM Segment 1Address Ramp Rate <15:8>				PS0=1 PS1=0
	<39:32>	RAM Segment 1 Address Ramp Rate <7:0>				PS0=1 PS1=0
RAM Segment Control Word #2 (**RSCW2**) **(09h)**	<7:0>	RAM Segment 2 Mode Control <2:0>	No Dwell Active	RAM Segment 2 Beginning Address <9:6>		PS0=0 PS1=1
	<15:8>	RAM Segment 2 Beginning Address <5:0>			RAM Segment 2 Final Address <9:8>	PS0=0 PS1=1
	<23:16>	RAM Segment 2 Final Address <7:0>				PS0=0 PS1=1
	<31:24>	RAM Segment 2 Address Ramp Rate <15:8>				PS0=0 PS1=1
	<39:32>	RAM Segment 2 Address Ramp Rate <7:0>				PS0=0 PS1=1
RAM Segment Control Word #3 (**RSCW3**) **(0Ah)**	<7:0>	RAM Segment 3 Mode Control <2:0>	No Dwell Active	RAM Segment 3 Beginning Address <9:6>		PS0=1 PS1=1
	<15:8>	RAM Segment 3 Beginning Address <5:0>			RAM Segment 3 Final Address <9:8>	PS0=1 PS1=1
	<23:16>	RAM Segment 3 Final Address <7:0>				PS0=1 PS1=1
	<31:24>	RAM Segment 3 Address Ramp Rate <15:8>				PS0=1 PS1=1
	<39:32>	RAM Segment 3 Address Ramp Rate <7:0>				PS0=1 PS1=1
RAM **(0Bh)**	<31:0>	RAM [1023:0] <31:0> (Read Instructions write out RAM Signature Register data)				-

AD9954 Register Map – when Linear Sweep enable bit is true (CFR1<21> = 1)

(NOTE: RAM Enable Bit CFR1<31> only activates the RAM itself, not the RAM Segment Control Words)

Register Name (Serial address)	Bit Range (Internal address)	(MSB) Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	(LSB) Bit 0	Default Value OR Profile
Control Function Register #1 (**CFR1**) **(00h)**	<7:0> **(00h)**	Digital Power Down	Comp power Down	DAC Power Down	Clock Input Power Dwn	External Power Down Mode	Crystal Out Pin Active	Sync CLK Out Disable	Not Used	00h
	<15:8> **(01h)**	Load SRR @I/O UD	AutoClr Freq. Accum	AutoClr Phase Accum	Enable SINE Output	Clear Freq Accum.	Clear Phase Accum.	SDIO Input Only	LSB First	00h
	<23:16> **(02h)**	Automatic Sync Enable	Software Manual Sync	Linear Sweep Enable	Amplitude Dither Enable	Phase Dither En<3>	Phase Dither En<2>	Phase Dither En<1>	Phase Dither En<0>	00h
	<31:24> **(03h)**	RAM Enable	RAM Dest. Is Phase Word	Internal Profile Control <2:0>			Load ARR @I/O UD	Output Shaped Keying Enable	Auto Output Shaped Keying	00h
Control Function Register #2 **(CFR2) (01h)**	<7:0> **(04h)**	REFCLK Multiplier 00h or 01h or 02h or 03h: Bypass Multiplier 04h –14h: 4x – 20x multiplication					VCO Gain	Charge Pump Control <1:0>		00h
	<15:8> **(05h)**	currently **not used**				High Speed Sync Enable	Hardware Manual Sync Enable	Crystal Out Pin Active	DAC Prime Data Disable	00h
	<23:16> **(06h)**	currently **not used**								00h
Amplitude Scale Factor (**ASF**) **(02h)**	<7:0> **(07h)**	Amplitude Scale Factor Register <7:0>								-
	<15:8> **(08h)**	Auto Ramp Rate Speed Control <1:0>	Amplitude Scale Factor Register <13:8>							-
Amplitude Ramp Rate **(ARR) (03h)**	<7:0> **(09h)**	Amplitude Ramp Rate Register <7:0>								-
Frequency Tuning Word (**FTW0**) **(04h)**	<7:0> **(0Ah)**	Frequency Tuning Word #0 <7:0>								00h
	<15:8> **(0Bh)**	Frequency Tuning Word #0 <15:8>								00h
	<23:16> **(0Ch)**	Frequency Tuning Word #0 <23:16>								00h
	<31:24> **(0Dh)**	Frequency Tuning Word #0 <31:24>								00h
Phase Offset Word (**POW0**) **(05h)**	<7:0> **(0Eh)**	Phase Offset Word #0 <7:0>								00h
	<15:8> **(0Fh)**	Open<1:0>	Phase Offset Word #0 <13:8>							00h

Frequency Tuning Word (**FTW1**) **(06h)**	<7:0> **(10h)**	Frequency Tuning Word #1 <7:0>	-
	<15:8> **(11h)**	Frequency Tuning Word #1 <15:8>	-
	<23:16> **(12h)**	Frequency Tuning Word #1 <23:16>	-
	<31:24> **(13h)**	Frequency Tuning Word #1 <31:24>	-
Negative Linear Sweep Control Word (**NLSCW**) **(07h)**	<7:0> **(14h)**	Falling Delta Frequency Tuning Word <7:0>	Profile0
	<15:8> **(15h)**	Falling Delta Frequency Tuning Word <15:8>	Profile0
	<23:16> **(16h)**	Falling Delta Frequency Tuning Word <23:16>	Profile0
	<31:24> **(17h)**	Falling Delta Frequency Tuning Word <31:24>	Profile0
	<39:32> **(18h)**	Falling Sweep Ramp Rate Word <7:0>	Profile0
Positive Linear Sweep Control Word (**PLSCW**) **(08h)**	<7:0> **(19h)**	Rising Delta Frequency Tuning Word <7:0>	Profile1
	<15:8> **(1Ah)**	Rising Delta Frequency Tuning Word <15:8>	Profile1
	<23:16> **(1Bh)**	Rising Delta Frequency Tuning Word <23:16>	Profile1
	<31:24> **(1Ch)**	Rising Delta Frequency Tuning Word <31:24>	Profile1
	<39:32> **(1Dh)**	Rising Sweep Ramp Rate Word <7:0>	Profile1

Control Register Bit Descriptions

Control Function Register #1 (CFR1)

The CFR1 is used to control the various functions, features, and modes of the AD9954. The functionality of each bit is detailed below.

CFR1<31>: RAM Enable bit.

When CFR1<31> = 0 *(default)*. When CFR1<31> is inactive, the RAM is disabled for operation. Either Single tone mode of operation or linear sweep mode of operations is enabled.

When CFR1<31> = 1, if CFR1<31> is active, the RAM is enabled for operation. Access control for normal operation is controlled via the mode control bits of the RSCW for the current profile.

CFR1<30>: RAM Destination bit.

CFR1<30> = 0 *(default)* If CFR1<31> is active, a logic 0 on the RAM Destination bit (CFR1<30>=0) configures the AD9954 such that RAM output drives the phase accumulator (i.e. is the frequency tuning word). If CFR1<31> is inactive, CFR1<30> is a don't care.

CFR1<30> = 1 If CFR1<31> is active, a logic 1 on the RAM Destination bit (CFR1<30>=1) configures the AD9954 such that RAM output drives the phase-offset adder (i.e. sets the phase offset of the DDS core).

CFR1<29:27>: Internal Profile Control bits. These bits cause the Profile Bits to be ignored and put the AD9954 into an automatic "profile loop sequence" that allows the user to implement a frequency/phase composite sweep that runs without external inputs. See the **Internal Profile Control** section of this document for details.

CFR1<26>: Amplitude ramp rate load control bit.

When CFR1<26> = 0 *(default)*, the amplitude ramp rate timer is loaded only upon timeout (timer ==1) and is NOT loaded due to an I/O UPDATE input signal.

When CFR1<26> = 1, the amplitude ramp rate timer is loaded upon timeout (timer ==1) or at the time of an I/O UPDATE input signal.

CFR1<25>: Shaped On-Off Keying enable bit.

When CFR1<25> = 0 *(default,)* Shaped On-Off Keying is bypassed.

When CFR1<25> = 1, Shaped On-Off Keying is enabled. When enabled, CFR1<24> controls the mode of operation for this function.

CFR1<24>: AUTO Shaped On-Off Keying enable bit (only valid when CFR1<25> is active high).

When CFR1<24> = 0 *(default)*. When CFR1<25> is active, a logic 0 on CFR1<24> enables the MANUAL Shaped On-Off Keying operation. See the **Shaped On-Off Keying** section of this document for details.

When CFR1<24> = 1, if CFR1<25> is active, a logic 1 on CFR1<24> enables the AUTO Shaped On-Off Keying operation. See the **Shaped On-Off Keying** section of this document for details.

CFR1<23>: Automatic Synchronization Enable Bit.

When CFR1<23> = 0 *(default),* the automatic synchronization of multiple AD9954s feature is inactive.

When CFR1<23> = 1, the automatic synchronization of multiple AD9954s feature is active. See the **Synchronizing Multiple AD9954s** section of this document for details.

CFR1<22>: Software Manual Synchronization of Multiple AD9954.

When CFR1<22> = 0 *(default),* the manual synchronization of multiple AD9954s feature is inactive.

When CFR1<22> = 1, the software controlled manual synchronization of multiple AD9954s feature is executed. The SYNC_CLK rising edge is advanced by one SYSCLK cycle and this bit is cleared. To advance the rising edge multiple times, this bit needs to be set for each advance. See the **Synchronizing Multiple AD9954s** section of this document for details.

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CFR1<21>: Linear Frequency Sweep Enable.

When CFR1<21> = 0 *(default)*, the linear frequency sweep capability of the AD9954 is inactive.

When CFR1<21> = 1, the linear frequency sweep capability of the AD9954 is enabled. When enabled, either the Rising or Falling Delta Frequency Tuning Word is applied to the Frequency accumulator at the programmed ramp rate causing the output frequency to ramp up or ramp down, controlled by the Profile 0 input. See the **Linear Sweep Capability** section of this document for details.

CFR1<20>: Amplitude dither enable bit.

When CFR1<20> = 0 *(default)*, amplitude dithering is disabled.

When CFR1<20> = 1, amplitude dithering is enabled.

CFR1<19>: Phase bit <16> dither enable bit.

When CFR1<19> = 0 *(default)*, phase dithering for truncated phase words, bit 16 of <31:13>, is disabled.

When CFR1<19> = 1, phase dithering for truncated phase words, bit 16 of <31:13>, is enabled.

CFR1<18>: Phase bit <15> dither enable bit.

When CFR1<18> = 0 *(default)*, phase dithering for truncated phase words, bit 15 of <31:13>, is disabled.

When CFR1<18> = 1, phase dithering for truncated phase words, bit 15 of <31:13>, is enabled.

CFR1<17>: Phase bit <14> dither enable bit.

When CFR1<17> = 0 *(default)*, phase dithering for truncated phase words, bit 14 of <31:13>, is disabled.

When CFR1<17> = 1, phase dithering for truncated phase words, bit 14 of <31:13>, is enabled.

CFR1<16>: Phase bit <13> dither enable bit.

When CFR1<16> = 0 *(default)*, phase dithering for truncated phase words, bit 13 of <31:13>, is disabled.

When CFR1<16> = 1, phase dithering for truncated phase words, bit 13 of <31:13>, is enabled.

CFR1<15>: Linear Sweep ramp rate load control bit.

When CFR1<15> = 0 *(default)*, the linear sweep ramp rate timer is loaded only upon timeout (timer ==1) and is NOT loaded due to an I/O UPDATE input signal.

When CFR1<15> = 1, the linear sweep ramp rate timer is loaded upon timeout (timer ==1) or at the time of an I/O UPDATE input signal.

CFR1<14>: Auto Clear Frequency Accumulator bit.

When CFR1<14> = 0 (*default*), a new delta frequency word is applied to the input, as in normal operation, but not loaded into the accumulator.

When CFR1<14> = 1, this bit automatically synchronously clears (loads zeros into) the frequency accumulator for one cycle upon reception of the I/O UPDATE sequence indicator.

CFR1<13>: AutoClear Phase Accumulator bit.

When CFR1<13> = 0 *(default)*, a new frequency tuning word is applied to the inputs of the phase accumulator, but not loaded into the accumulator.

When CFR1<13> = 1, this bit automatically synchronously clears (loads zeros into) the phase accumulator for one cycle upon reception of the I/O UPDATE sequence indicator.

CFR1<12>: Sine/Cosine select bit.

When CFR1<12> = 0 *(default)*, the angle-to-amplitude conversion logic employs a COSINE function.

When CFR1<12> = 1, the angle-to-amplitude conversion logic employs a SINE function.

CFR1<11>: Clear Frequency Accumulator.

When CFR1<11> = 0 *(default)*, the frequency accumulator functions as normal.

When CFR1<11> = 1, the frequency accumulator memory elements are asynchronously cleared.

CFR1<10>: Clear Phase Accumulator.

When CFR1<10> = 0 *(default)*, the phase accumulator functions as normal.

When CFR1<10> = 1, the phase accumulator memory elements are asynchronously cleared.

CFR1<9>: SDIO Input Only.

When CFR1<9> = 0 (*default*), the SDIO pin has bi-directional operation (2-wire serial programming mode).

When CFR1<9> = 1, the serial data I/O pin (SDIO) is configured as an input only pin (3-wire serial programming mode).

CFR1<8>: LSB First.

When CFR1<8> = 0 (*default*), MSB first format is active.

When CFR1<8> = 1, the serial interface accepts serial data in LSB first format.

CFR1<7>: Digital Power Down bit.

When CFR1<7> = 0 (*default*), all digital functions and clocks are active.

When CFR1<7> = 1, all non-IO digital functionality is suspended and all heavily loaded clocks are stopped. This bit is intended to lower the digital power to nearly zero, without shutting down the PLL clock multiplier function or the DAC.

CFR1<6>: Comparator Power Down bit.

When CFR1<6> = 0 (*default*), the comparator is enabled for operation.

When CFR1<6> = 1, the comparator is disabled and is in its lowest power dissipation state.

CFR1<5>: DAC Power Down bit.

When CFR1<5> = 0 (*default*), the DAC is enabled for operation.

When CFR1<5> = 1, the DAC is disabled and is in its lowest power dissipation state.

CFR1<4>: Clock Input Power Down bit.

When CFR1<4> = 0 (*default*), the clock input circuitry is enabled for operation.

When CFR1<4> = 1, the clock input circuitry is disabled and the device is in its lowest power dissipation state.

CFR1<3>: External Power Down Mode.

When CFR1<3> = 0 *(default)* the external power down mode selected is the "fast recovery power down" mode. In this mode, when the PwrDwnCtl input pin is high, the digital logic and the DAC digital logic are powered down. The DAC bias circuitry, comparator, PLL, oscillator, and clock input circuitry is NOT powered down.

When CFR1<3> = 1, the external power down mode selected is the "full power down" mode. In this mode, when the PwrDwnCtl input pin is high, all functions are powered down. This includes the DAC and PLL, which take a significant amount of time to power up.

CFR1<2>: Linear Sweep No Dwell bit.

When CFR1<2> = 0 *(default)* the Linear Sweep no dwell function is inactive.

When CFR1<2> = 1, the Linear Sweep no dwell function is active. If CFR1<21>, the Linear Sweep Enable bit, is active and CFR1<2> is active, the Linear Sweep no dwell function is activated. See the Linear Sweep section of this document for details. If CFR1<21> is clear, this bit is a don't care.

CFR1<1>: SyncClk Disable bit.

When CFR1<1> = 0 *(default)*, the SyncClk pin is active.

When CFR1<1> = 1, the SyncClk pin assumes a static logic 0 state (disabled). In this state the pin drive logic is shut down to keep noise generated by the digital circuitry at a minimum. However, the synchronization circuitry remains active (internally) to maintain normal device timing.

CFR1<0>: Not used. Leave at 0.

NOTE: Assertion of this bit may cause the SyncClk pin to momentarily stop generating a Sync Clock signal. The device will not be operational during the re-synchronization period.

Control Function Register #2 (CFR2)

The CFR2 is comprised of three bytes located in parallel addresses 06h-04h. The CFR2 is used to control the various functions, features, and modes of the AD9954, primarily related to the analog sections of the chip. All bits of the CFR2 will be routed directly to the Analog section of the AD9954 as a single 24-bit bus labeled CFR2<23:0>.

CFR2<15:12>: Not Used.

CFR2<11>: High Speed Sync Enable bit.

When CFR2<11> = 0 *(default)* the High Speed Sync enhancement is off.

When CFR2<11> = 1, the High Speed Sync enhancement is on. See the **Synchronizing Multiple AD9954s** section of this document for details.

CFR2<10>: Hardware Manual Sync Enable bit.

When CFR2<10> = 0 *(default)* the Hardware Manual Sync function is off.

When CFR2<11> = 1, the Hardware Manual Sync function is enabled. While this bit is set, a rising edge on the SYNC_IN pin will cause the device to advance the SYNC_CLK rising edge by one REFCLK cycle. Unlike the software manual sync enable bit, this bit does not self-clear. Once the hardware manual sync mode is enabled, it will stay enabled until this bit is cleared. See the **Synchronizing Multiple AD9954s** section of this document for details.

CFR2<9>: Crystal Out Enable bit.

When CFR2<9> = 0 *(default)* the Crystal Out pin is inactive.

When CFR2<9> = 1, the Crystal Out pin is active. When active, the crystal oscillator circuitry output drives the Crystal Out pin, which can be connected to other devices to produce a reference frequency.

CFR2<8>: DAC prime data disable bit.

When CFR2<8> = 0 (*default*), the DAC prime data is enabled for operation.

When CFR2<8> = 1, the DAC prime data is not generated and these outputs remain logic zeros.

CFR2<7:3>: Reference clock multiplier control bits. See the **Phase Locked Loop (PLL)** section of this document for details.

CFR2<2>: VCO gain control bit. This bit is used to control the gain setting on the VCO.

CFR<1:0>: Charge Pump gain control bits. These bits are used to control the gain setting on the charge pump.

Other Register Descriptions

Amplitude Scale Factor (ASF)

The ASF Register stores the 2-bit Auto Ramp Rate Speed value ASF<15:14> and the 14-bit Amplitude Scale Factor ASF<13:0> used in the Output Shaped Keying (OSK) operation. In auto OSK operation, that is CFR1<24> = 1, ASF <15:14> tells the OSK block how many amplitude steps to take for each increment or decrement. ASF<13:0> sets the maximum value achievable by the OSK internal multiplier. In manual OSK mode, that is CFR1<24>=0, ASF<15:14> have no affect. ASF <13:0> provide the output scale factor directly. If the OSK enable bit is cleared, CFR1<25>=0, this register has no affect on device operation.

Amplitude Ramp Rate (ARR)

The ARR register stores the 8-bit Amplitude Ramp Rate used in the Auto OSK mode, that is CFR1<25>=1, CFR<24>=1. This register programs the rate the amplitude scale factor counter increments or decrements. In the OSK is set to manual mode, CFR1<25>=1 CFR<24>=0, or if OSK enable is cleared CFR1<25>=0, this register has no affect on device operation.

Frequency Tuning Word 0 (FTW0)

The Frequency Tuning Word is a 32-bit register that controls the rate of accumulation in the phase accumulator of the DDS core. Its specific role is dependent on the device mode of operation.

Phase Offset Word (POW)

The Phase Offset Word is a 14-bit register that stores a phase offset value. This offset value is added to the output of the phase accumulator to offset the current phase of the output signal. The exact value of phase offset is given by the following formula: $\Phi = \left(\frac{POW}{2^{14}}\right) * 360°$

When the RAM enable bit is set, CFR1<31> = 1, and the RAM destination is cleared, CFR1<30>=0, the RAM supplies the phase offset word and this register has no affect on device operation.

Frequency Tuning Word 1 (FTW1)

The Frequency Tuning Word is a 32-bit register that controls the rate of accumulation in the phase accumulator of the DDS core. Its specific role is dependent on the device mode of operation.

Negative & Positive Linear Sweep Control Word (NLSCW), (PLSCW)

Registers h'07 and h'08 are multifunctional registers. When the linear sweep bit CFR1<21> is enabled, register h'07 acts as the Negative Linear Sweep Control Word (NLSCW) and register 'h08 acts as the Positive Linear Sweep Control Word (PLSCW). Each of the linear sweep control words contains a 32-bit Delta Frequency Tuning Word (FDFTW, RDFTW) and an 8-bit Sweep Ramp Rate Word (FSRRW, RSRRW). The delta frequency tuning words determine the amount the frequency accumulator will increment or decrement the resultant tuning word. The sweep ramp rate words determine the rate at which the accumulator will increment or decrement, in number of clock cycles.

RAM Segment Control Words 0,1,2,3 (RSCW0) (RSCW1) (RSCW2), (RSCW3)

When the Linear Sweep Enable Bit is cleared, CFR1<21> =0, registers h'07, h'08, h'09 and h'0A act as the RAM segment Control words, RSCW0, RSCW1, RCSW2 and RCSW3 respectively. Each of the RAM Segment Control Words contains a 3-bit Mode Control value, a 'No Dwell' bit, a 10-bit Beginning Address, a 10-bit Final Address and a 16-bit Address Ramp Rate. Please see the section on RAM modes of operation for details on how each of these values works in the various RAM modes of operation.

RAM

The AD9954 incorporates a 1024x32 block of SRAM. The RAM is bi-directional single-port. That is to say, both READ and WRITE operations from and to the RAM are valid, but they cannot occur simultaneously. WRITE operations from the serial I/O port have precedence, and if an attempt to WRITE to RAM is made during a READ operation, the READ operation will be halted. The RAM is controlled in multiple ways, dictated by modes of operation described in the RAM Segment Control Word <7:5> as well as data in the Control Function Register. Read/write control for the RAM will be described for each mode supported.

When the RAM Enable bit (CFR1<31>) is set, the RAM output optionally drives the input to the phase accumulator OR the phase offset adder, depending upon the state of the "RAM Destination" bit (CFR1<30>). If CFR1<30> is a logic one, the RAM output is connected to the Phase Offset adder and supplies the phase offset control word(s) for the device. When CFR1<30> is logic zero (default condition), the RAM output is connected to the input of the phase accumulator and supplies the frequency tuning word(s) for the device. When the RAM output drives the phase accumulator, the Phase Offset Word (POW, hex address 05h) drives the phase-offset adder. Similarly, when the RAM output drives the phase offset adder the Frequency Tuning Word (FTW, hex address 04h) drives the phase accumulator. When CFR1<31> is logic zero, the RAM is inactive unless being written to via the serial port. The power up state of the AD9954 is single

tone mode, in which the RAM Enable bit is inactive. The RAM is segmented into four unique slices controlled by the Profile<1:0> input pins.

All RAM writes/reads, unless otherwise specified, are controlled by the Profile<1:0> input pins and the respective RAM Segment Control Word. The RAM can be written to during normal operation BUT any IO operation that commands the RAM to be written immediately suspends read operation from the RAM, causing the current mode of operation to be non-functional. This excludes single tone mode, as the RAM is not read in this mode.

Linear Sweep Block

Linear sweep is a mode of operation whereby changes from a start frequency (F0) to a terminal frequency (F1) are not instantaneous but instead are accomplished in a sweep or "ramped" fashion. Frequency ramping, whether linear or non-linear necessitates that many intermediate frequencies between F0 and F1 will be output in addition to the primary F0 and F1 frequencies.
The linear sweep block is comprised of the falling and rising delta frequency tuning words, the falling and rising delta frequency ramp rates and the frequency accumulator. The Linear Sweep Enable bit CFR1 <21> enables the Linear Sweep block. In addition, the Linear Sweep No-Dwell bit controls the Linear Sweep Block's behavior upon reaching the terminal frequency in a sweep. The actual method for programming a frequency sweep is covered in the 'Modes of Operation' section of this datasheet.

Modes of Operation

Single Tone Mode

In single tone mode, the DDS core uses a single tuning word. Whatever value is stored in FTW0 is supplied to the phase accumulator. This value can only be changed statically, which is done by writing a new value to FTW0 and issuing an I/O UPDATE. Phase adjustment is possible through the phase offset register.

RAM Controlled Modes of Operation

Direct Switch Mode

Direct Switch Mode enables FSK or PSK modulation. The AD9954 is programmed for Direct Switch Mode by writing the RAM Enable bit true and programming the RAM Segment Mode Control bits of each desired profile to logic 000(b). This mode simply reads the RAM contents at the RAM Segment Beginning Address for the current profile. No address ramping is enabled in Direct Switch mode.

To perform 4-tone FSK, the user programs each RAM Segment Control Word for Direct Switch Mode and a unique beginning address value. In addition, the RAM Enable bit is written true which enables the RAM and the RAM destination bit is written false, setting the RAM output to be the frequency tuning word. The Profile<1:0> inputs are the 4-tone FSK data inputs. When the profile

is changed, the frequency tuning word stored in the new profile is loaded into the phase accumulator and used to increment the currently stored value in a phase continuous fashion. The Phase Offset Word drives the phase-offset adder. 2-tone FSK is accomplished by using only one Profile pin for data.

Programming the AD9954 for PSK modulation is similar to FSK except the RAM destination bit is set to a logic 1, enabling the RAM output to drive the phase offset adder. The FTW drives the input to the phase accumulator. Toggling the profile pins changes (modulates) the current phase value. The upper 14-bits of the RAM drive the phase adder (bits <31:18>). Bits <17:0> of the RAM output are unused when the RAM destination bit is set. The "No Dwell" bit is a don't care in Direct Switch Mode.

Ramp-Up Mode

Ramp-Up mode, in conjunction with the segmented RAM capability, allows up to four different "sweep profiles" to be programmed into the AD9954. The AD9954 is programmed for Ramp-Up mode by writing the RAM Enable bit true and programming the RAM Mode Control bits of each profile to be used to logic 001(b). As in all modes that enable the memory, the RAM destination bit controls whether the RAM output drives the phase accumulator or the phase offset adder.

Upon starting a sweep (vian I/O UPDATE or change in Profile bits), the RAM address generator loads the RAM Segment Beginning Address bits of the current RSCW, driving the RAM output from this address and the Ramp Rate Timer loads the RAM Segment Address Ramp Rate bits. When the ramp rate timer finishes a cycle, the RAM address generator increments to the next address, the timer reloads the ramp rate bits and begins a new countdown cycle. This sequence continues until the RAM address generator has incremented to an address equal to the RAM Segment Final Address bits of the current RSCW.

If the "No Dwell" bit is clear, when the RAM address generator equals the final address, the generator stops incrementing as the terminal frequency has been reached. The sweep is complete and does not re-start until an I/O UPDATE or change in Profile is detected to enable another sweep from the beginning to the final RAM address as described above.

If the "No Dwell" bit is set, when the RAM address generator equals the final address, after the next ramp rate timer cycle the phase accumulator is cleared. The phase accumulator remains cleared until another sweep is initiated via an I/O UPDATE input or change in profile.

Notes to the Ramp-Up mode:

1) The user must insure that the beginning address is lower than the final address.
2) Changing profiles automatically terminates the current sweep and starts the next sweep.
3) The AD9954 offers no output signal indicating when a terminal frequency has been reached.

4) Setting the RAM destination bit true such that the RAM output drives the phase-offset adder is valid. While the above discussion describes a frequency sweep, a phase sweep operation is also available.

Another application for Ramp-Up mode is non-symmetrical FSK modulation. With the RAM configured for two segments, using the Profile<0> bit as the data input allows non-symmetrical ramped FSK.

Bi-directional Ramp Mode

Bi-directional Ramp mode allows the AD9954 to offer a symmetrical sweep between two frequencies using the Profile<0> signal as the control input. The AD9954 is programmed for Bi-directional Ramp mode by writing the RAM Enable bit true and the RAM Mode Control bits of RSCW0 to logic 010(b). In Bi-directional Ramp mode, the Profile<1> input is ignored and the Profile<0> input is the ramp direction indicator. In this mode, the memory is not segmented and uses only a single beginning and final address. The address registers that affect the control of the RAM are located in the RSCW associated with profile 0.

Upon entering this mode (via an I/O UPDATE or changing Profile<0>), the RAM address generator loads the RAM Segment Beginning Address bits of RSCW0 and the Ramp Rate Timer loads the RAM Segment Address Ramp Rate bits. The RAM drives data from the beginning address and the ramp rate timer begins to count down to 1. While operating in this mode, toggling the Profile<0> pin does not cause the device to generate an internal I/O UPDATE. That is to say, when the Profile<0> pin is acting as the ramp direction indicator, any transfer of data from the I/O buffers to the internal registers can only be initiated by a rising edge on the I/O UPDATE pin.

RAM address control now is a function of the Profile<0> input. When the Profile<0> bit is a logic one, the RAM address generator increments to the next address when the ramp rate timer completes a cycle (and reloads to start the timer again). As in the Ramp-Up mode, this sequence continues until the RAM address generator has incremented to an address equal to the final address as long as the Profile<0> input remains high**.** If the Profile<0> input goes low, the RAM address generator immediately decrements and the ramp rate timer is reloaded. The RAM address generator will continue to decrement at the ramp rate period until the RAM address is equal to the beginning address as long as the Profile<0> input remains low**.**

The sequence of ramping up and down is controlled via the Profile<0> input signal for as long as the part is programmed into this mode. The no dwell bit is a “don’t care” in this mode as is all data in the RAM Segment Control Words associated with profiles 1,2,3. Only the information in the RAM Segment Control Word for profile 0 is used to control the RAM in the Bi-Directional Ramp Mode.

Notes to the Bi-directional Ramp mode:

1) The user must insure that the beginning address is lower than the final address.
2) Issuing an I/O UPDATE automatically terminates the current sweep causing the starting address to be reloaded and the ramp rate timer to initialize.
3) Setting the RAM destination bit true such that the RAM output drives the phase-offset adder is valid. While the above discussion describes a frequency sweep, a phase sweep operation is also available.

Continuous Bi-directional Ramp Mode

Continuous Bi-directional Ramp mode allows the AD9954 to offer an automatic symmetrical sweep between two frequencies. The AD9954 is programmed for Continuous Bi-directional Ramp mode by writing the RAM Enable bit true and the RAM Mode Control bits of each profile to be used to logic 011(b).

Upon entering this mode (via an I/O_update or changing Profile<1:0>), the RAM address generator loads the RAM Segment Beginning Address bits of the current RSCW and the Ramp Rate Timer loads the RAM Segment Address Ramp Rate bits. The RAM drives data from the beginning address and the ramp rate timer begins to count down to 1. When the ramp rate timer completes a cycle, the RAM address generator increments to the next address, the timer reloads the ramp rate bits and continues counting down. This sequence continues until the RAM address generator has incremented to an address equal to the RAM Segment Final Address bits of the current RSCW. Upon reaching this terminal address, the RAM address generator will decrement in value at the ramp rate until it reaches the RAM Segment Beginning address. Upon reaching the beginning address, the entire sequence repeats.

The entire sequence repeats for as long as the part is programmed for this mode. The No Dwell bit is a “don’t care” in this mode. In general, this mode is identical in control to the Bi-directional Ramp Mode except the ramp up and down is automatic (no external control via the Profile<0> input) and switching profiles is valid. Once in this mode, the address generator ramps from beginning address to final address back to beginning address at the rate programmed into the ramp rate register. This mode enables generation of an automatic saw tooth sweep characteristic.

Notes to the Continuous Bi-directional Ramp mode:

1) The user must insure that the beginning address is lower than the final address.
2) Changing profiles or issuing an I/O UPDATE automatically terminates the current sweep and starts the next sweep.
3) Setting the RAM destination bit true such that the RAM output drives the phase-offset adder is valid. While the above discussion describes a frequency sweep, a phase sweep operation is also available.

Continuous Re-circulate Mode

Continuous Re-circulate mode allows the AD9954 to offer an automatic, continuous unidirectional sweep between two frequencies. The AD9954 is programmed for Continuous Re-circulate mode by writing the RAM Enable bit true and the RAM Mode Control bits of each profile to be used to logic 100(b).

Upon entering this mode (vian I/O UPDATE or changing Profile<1:0>), the RAM address generator loads the RAM Segment Beginning Address bits of the current RSCW and the Ramp Rate Timer loads the RAM Segment Address Ramp Rate bits. The RAM drives data from the beginning address and the ramp rate timer begins to count down to 1. When the ramp rate timer completes a cycle, the RAM address generator increments to the next address, the timer reloads the ramp rate bits and continues counting down. This sequence continues until the RAM address generator has incremented to an address equal to the RAM Segment Final Address bits of the current RSCW. Upon reaching this terminal address, the RAM address generator reloads the RAM Segment Beginning Address bits and the sequence repeats.

The sequence of circulating through the specified RAM addresses repeats for as long as the part is programmed for this mode. The No Dwell bit is a don't care in this mode.

Notes to the Continuous Re-circulate mode:

1) The user must insure that the beginning address is lower than the final address.
2) Changing profiles or issuing an I/O UPDATE automatically terminates the current sweep and starts the next sweep.
3) Setting the RAM destination bit true such that the RAM output drives the phase-offset adder is valid. While the above discussion describes a frequency sweep, a phase sweep operation is also available.

RAM Controlled Modes of Operation Summary

The AD9954 offers 5 modes of RAM controlled operation, as shown in table 3 below.

RSCW<7:5> (binary)	Mode	Notes
000	Direct Switch Mode	No sweeping, Profiles valid, No Dwell invalid
001	Ramp Up	Sweeping, Profiles valid, No Dwell valid
010	Bi-directional Ramp	Sweeping, Profile<0> is a direction control bit, No Dwell invalid
011	Continuous Bi-directional Ramp	Sweeping, Profiles valid, No Dwell invalid
100	Continuous Re-circulate	Sweeping, Profiles valid, No Dwell invalid

101,110,111	OPEN	Invalid mode – default to Direct Switch

Table 4 RAM Modes of Operation

Internal Profile Control

The AD9954 offers a mode in which a composite frequency sweep can be built, for which the timing control is software programmable. The "internal profile control" capability disengages the Profile<1:0> pins and enables the AD9954 to take control of switching between profiles. Modes are defined that allow continuous or single burst profile switches for three combinations of profile selection bits. These are listed in the table below. When the any of the CFR1<29:27> bits are active, the internal profile control mode is engaged. Internal profile control is only valid when the device is operating in RAM mode. There is no internal profile control for linear sweeping operations.

When the internal profile control mode is engaged, the RAM Segment Mode Control bits are "Don't care" and the device operates all profiles as if these mode control bits were programmed for Ramp-Up mode. Switching between profiles occurs when the RAM address generator has exhausted the memory contents for the current profile.

CFR1<29:27> (binary)	Mode Description
000	Internal Control Inactive
001	Internal Control Active, Single Burst, activate profile 0, then 1, then stop
010	Internal Control Active, Single Burst, activate profile 0, then 1, then 2, then stop
011	Internal Control Active, Single Burst, activate profile 0, then 1, then 2, then 3, then stop
100	Internal Control Active, Continuous, activate profile 0, then 1, then loop starting at 0.
101	Internal Control Active, Continuous, activate profile 0, then 1, then 2, then loop starting at 0.
110	Internal Control Active, Continuous, activate profile 0, then 1, then 2, then 3, then loop starting at 0
111	Invalid

Table 5 Internal Profile Control

A single burst mode is one in which the composite sweep is executed once. For example, assume the device is programmed for Ramp-Up mode and the CFR1<29:27> bits are written to 010(b).

Upon receiving an I/O UPDATE, the internal control logic signals the device to begin executing the Ramp-Up mode sequence for profile 0. Upon reaching the RAM Segment Final Address value for profile 0, the device automatically switches to profile 1 and begins executing that Ramp-Up sequence. Upon reaching the RAM Segment Final Address value for profile 1, the device automatically switches to profile 2 and begins executing that Ramp-Up sequence. When the RAM Segment Final Address value for profile 2 is reached, the sequence is over and the composite sweep has completed. Issuing another I/O UPDATE re-starts the burst process.

A continuous internal profile control mode is one in which the composite sweep is continuously executed for as long as the device is programmed into that mode. Using the example above, except programming the CFR1<29:27> bits to 101(b), the operation would be identical until the RAM Segment Final Address value for profile 2 is reached. At this point, instead of stopping the sequence, it repeats starting with profile 0.

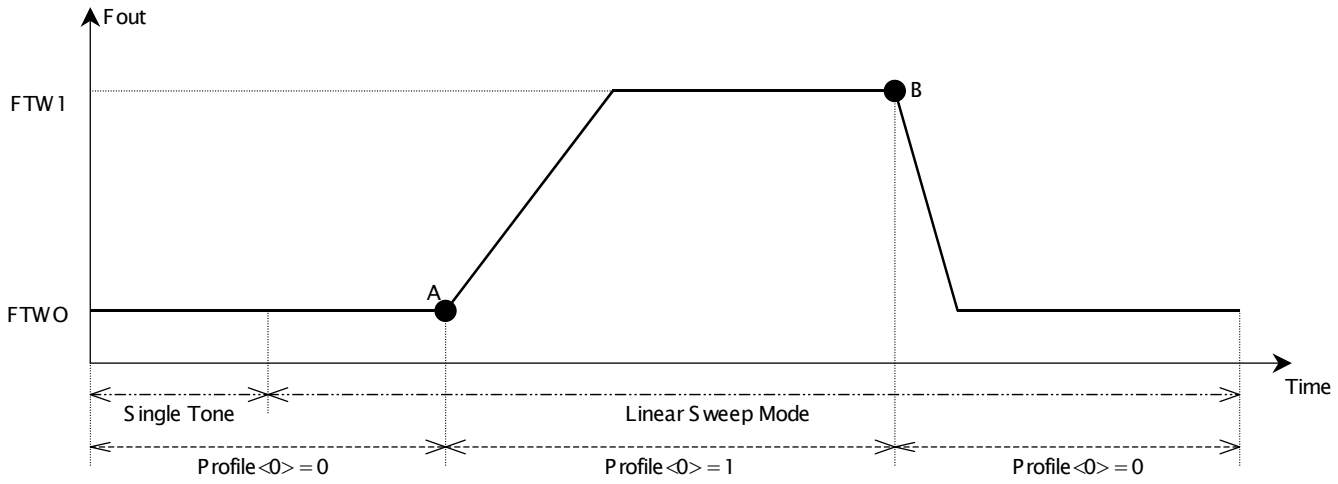
Linear Sweep Mode

The AD9954 is placed in linear sweep mode by setting the linear sweep enable bit CR1<21>. When in Linear Sweep mode, the AD9954 output frequency will ramp up from a starting frequency, programmed by FTW0 to a finishing frequency FTW1, or down from FTW1 to FTW0. The delta frequency tuning words and the ramp rate word determine the rate at which this ramping takes place. The Linear Sweep No-Dwell bit CFR1<2> controls the behavior of the device upon reaching the terminal frequency. The 32-bit rising delta frequency tuning word (RDFTW) increments the frequency accumulator is when ramping up from FTW0 to FTW1. The 8-bit rising sweep ramp rate word (RSRRW) controls the rate at which the frequency accumulator is incremented. The 32-bit falling delta frequency tuning word (FDFTW) decrements the accumulator when ramping down from FTW1 to FTW0. The 8-bit falling sweep ramp rate word (FSRRW) determines the rate at which the accumulator is decremented. In linear sweep mode, the different RAM profiles are not valid. The Profile <0> pin controls the direction of the sweep, rising to FTW1 or falling to FTW0. Upon reaching the destination frequency, the AD9954 linear sweep function will either hold at the destination frequency until the state on the Profile <0> pin is changed or immediately return to the initial frequency, FTW0, depending on the state of the Linear Sweep No-Dwell bit CFR1<02>. While operating in Linear Sweep mode, toggling the Profile<0> pin does not cause the device to generate an internal I/O UPDATE. That is to say, when the Profile<0> pin is acting as the sweep direction indicator, any transfer of data from the I/O buffers to the internal registers can only be initiated by a rising edge on the I/O UPDATE pin.

The linear sweep function of the AD9954 requires the lowest frequency to be loaded into FTW0 register and the highest frequency into FTW1 register. For piece-wise, non-linear frequency transitions, it is necessary to reprogram the registers *while* the frequency transition is in progress to affect the desired response. Figure A demonstrates a typical frequency ramping operation. After a reset or a power-up, the device will initially be in single tone mode. The programming steps to operate in linear sweep mode are:

0) Profile inputs at 00

1) Set the Linear Sweep Enable bit (CFR1<21>=1) and set or clear the Linear Sweep No-Dwell bit (CFR1<2>={0,1}) as desired.
2) Program the rising and falling delta frequency tuning words and ramp rate values
3) Program the lower and higher output frequencies into the FTW0 and FTW1 register, respectively.
4) Apply an I/O UPDATE to move this data into the registers (the output frequency will be FTW0)
5) Change the profile 0 input as desired to sweep between the lower to higher frequency and back.



- At point A: load rising ramp rate register, apply rising DFTW;
- At point B: load falling ramp rate register, apply falling DFTW.

Figure A – Linear Sweep Frequency Plan

Regarding Figure A it can be seen that the device initially powers up in Single Tone Mode. The profile inputs are low which places the FTW0 input to the phase accumulator. The user then configures the device as desired by writing the rising and falling delta frequency tuning words and ramp rates, as well as the Linear Sweep Enable bit, via the serial port (Point A in the figure above). In this example, the Linear Sweep No-Dwell bit is cleared (CFR1<2>=0).

Linear Sweep No Dwell Feature

The Linear Sweep function can be operated with a "no dwell" feature. If the Linear Sweep No Dwell bit is set, CFR1<2>=1, the rising sweep is started in an identical manner to the non-no dwell linear sweep mode. That is, upon detecting a rising edge on the profile<0> input pin the rising sweep action is initiated. The frequency continues to sweep up at the rate set by the rising sweep ramp rate at the resolution set by the rising delta frequency tuning word until it reaches the terminal frequency. Upon reaching the terminal frequency, the output frequency immediately returns to the

starting frequency and remains at the starting frequency until the device detects a subsequent rising edge on the Profile<0> pin. Figure B below is an example of the linear sweep mode operation when the Linear Sweep No Dwell bit is set. The points labeled A indicate where a rising edge on PS0 is detected and the points labeled B indicate where the AD9954 has determined Fout has reached the terminal frequency and automatically returns to the starting frequency. Please note that in this mode each sweep will require a separate rising edge on the Profile <0> pin. Linear sweeps using the No-Dwell bit can only be swept from FTW0 to FTW1 using the Positive Linear Sweep Control Word. Toggling the Profile <0> from 1 to 0 will not initiate a falling sweep when the No Dwell bit is set.

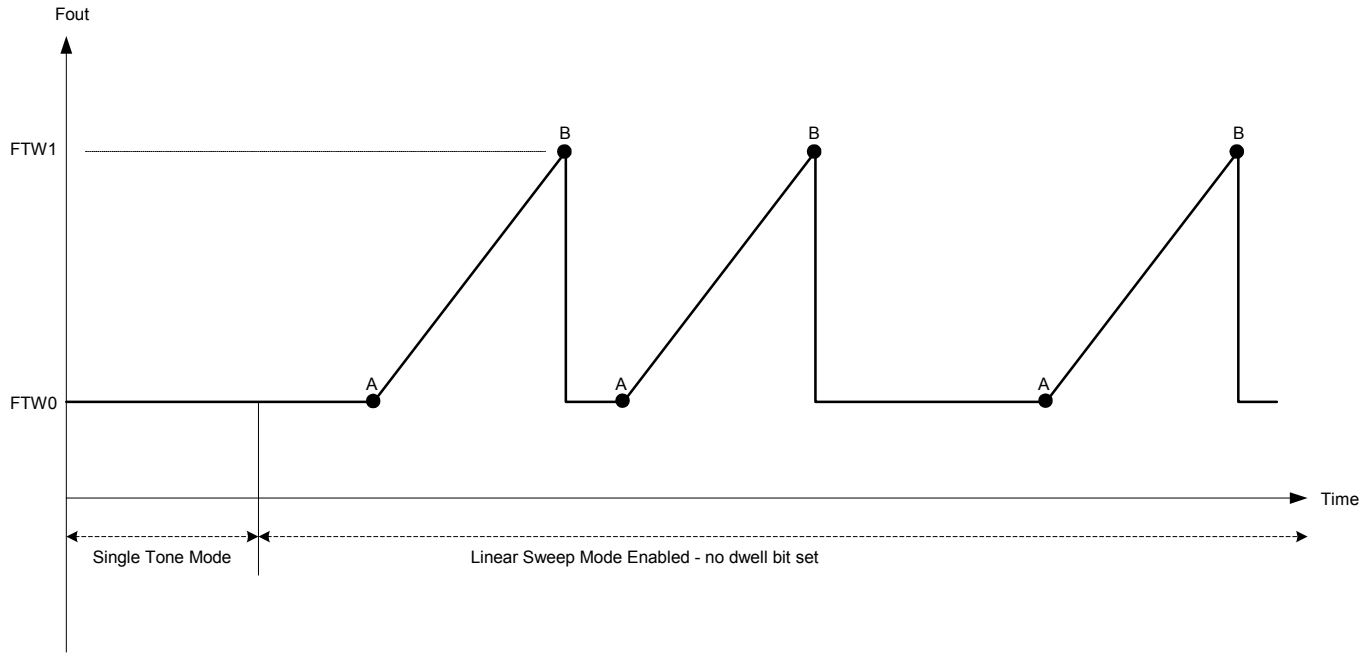


Figure B – Linear Sweep Using No-Dwell Frequency Plan

General Operation of Linear Sweep Capability:

In Linear Sweep mode the profile 1 pin must be tied to logic 0. With linear sweep mode active, when the profile 0 pin transitions from a low to high, the RDFTW is applied to the input of the frequency accumulator and the RSRR register is loaded into the sweep rate timer. The sweep rate timer counts down from an initial value to one, at which point the frequency accumulator is allowed to "accumulate" the input. This accumulation of the RDFTW at the rate given by the ramp rate (RSRR) continues until the output of the frequency adder is equal to the FTW1 register value. At this time, the accumulation is stopped causing the AD9954 to output the frequency given by the FTW1. The output remains at FTW1 for as long as the profile 0 pin remain logic 1.

When the profile 0 pin transitions from a high to low, the negated FDFTW is applied to the input of the frequency accumulator and the FSRR register is loaded into the sweep rate timer. Each time the timer counts down to one, the frequency accumulator is allowed to "accumulate" the input. This accumulation of the negated FDFTW at the rate given by the ramp rate (FSRR) continues until the output of the frequency adder is equal to the FTW0 register value. At this time, the accumulation is stopped causing the AD9954 to output the frequency given by the FTW0. The output remains at FTW0 for as long as the profile 0 pin remain logic 0.

Programming the ramp rate timer

The linear sweep ramp rate timer is a loadable down counter that, when enabled, continuously counts down from the loaded value to a count of 1. When in a rising transition the loaded value is the RSRRW, when in a falling transition this value is the FSRRW. When the ramp rate timer equals 1, the proper RFDTW or FDFTW is loaded and the counter begins counting down to one again. This load and count down operation continues for as long as the timer is enabled unless the timer is forced to load before reaching a count of 1.

The ramp timer can be loaded before reaching a count of 1 by three methods.

Method one is by changing the profile<0> input pin. When the profile<0> input pin changes from a logic zero to a logic 1, the RSRRW value is loaded into the ramp rate timer, which then proceeds to count down as normal. When the profile<0> input pin changes from a logic one to a logic zero, the FSRR value is loaded into the ramp rate timer, which then proceeds to count down as normal.

The second method in which the sweep ramp rate timer can be loaded before reaching a count of 1 is if the CFR1<15> bit is set and an I/O UPDATE is issued. If sweep is enabled and CFR1<15> is set, the ramp rate timer loads the value determined by the profile<0> pin every time an I/O UPDATE is issued. If the profile<0> pin is low (high), the ramp rate timer loads the FSRRW (RSRRW).

The last method in which the sweep ramp rate timer can be loaded before reaching a count of 1 is when going from the inactive linear sweep mode to the active linear sweep mode. That is, when the sweep enable bit is being set. The ramp rate that is loaded is a function of the profile<0> input pin.

Continuous and "Clear and Release" Frequency and Phase Accumulator Clear Functions

The AD9954 allows for a programmable continuous zeroing of the frequency sweep logic and the phase accumulator as well as a "clear and release", or automatic zeroing function. Each feature is individually controlled via bits the CFR1. CFR1<14> is the Automatic Clear Frequency Accumulator bit and CFR1<13> is the Automatic Clear Phase Accumulator bit. The continuous clear bits are located in CFR1<11:10>, where CFR1<11> clears the Frequency accumulator and CFR1<10> clears the Phase Accumulator.

Continuous Clear bits

The continuous clear bits are simply static control signals that, when active high, hold the respective accumulator at zero for the entire time the bit is active. When the bit goes low, inactive, the respective accumulator is allowed to operate.

The Auto Clear Frequency Accumulator bit, when set, clears and releases the frequency accumulator upon receiving an I/O update signal or change in one of the PROFILE pins. The Auto Clear Phase Accumulator, when set, clears and releases the phase accumulator upon receiving an I/O update or change on one of the PROFILE pins. The automatic clearing function is repeated for every subsequent I/O update or change on one of the PROFILE pins until the appropriate auto-clear control bit is cleared.

Note: These bits are programmed independently and do not have to be active at the same time. For example, one accumulator may be using the clear and release function while the other is continuously cleared.

Programming AD9954 Features

Phase Offset Control

A 14-bit phase-offset (θ) may be added to the output of the Phase Accumulator by means of the Control Registers. This feature provides the user with three different methods of phase control.

The first method is a static phase adjustment, where a fixed phase-offset is loaded into the appropriate phase-offset register and left unchanged. The result is that the output signal is offset by a constant angle relative to the nominal signal. This allows the user to phase align the DDS output with some external signal, if necessary.

The second method of phase control is where the user regularly UPDATEs the phase-offset register via the I/O Port. By properly modifying the phase-offset as a function of time, the user can implement a phase modulated output signal. However, both the speed of the I/O Port and the frequency of sysclk limit the rate at which phase modulation can be performed.

The third method of phase control involves the RAM and the profile input pins. The AD9954 can be configured such that the RAM drives the phase adjust circuitry. The user can control the phase offset via the RAM in an identical manner allowed for frequency sweeping. See the RAM Control and the Sweep Modes of Operation sections for details.

Phase/Amplitude Dithering

The AD9954 DDS core includes optional phase and/or amplitude dithering controlled via the CFR1<20:16> bits.

Phase dithering is the randomization of the state of the least significant bits of each phase word. Phase dithering reduces spurious signal strength caused by phase truncation by spreading the spurious energy over the entire spectrum. The downside to dithering is a rise in the noise floor. Amplitude dithering is similar, except it affects the output signal routed to the DAC.

The AD9954 uses a 32-bit linear feedback shift register (LFSR), shown in Figure 7 below, to generate the pseudo random binary sequence that is used for both phase and amplitude dither data. The LFSR will generate, at the sync_clk rate, the pseudo random sequence only if dithering is enabled. The enable signal is the 4-input OR of the dithering control bits (CFR1<20:16>).

Phase dithering is independently controlled on the four least significant bits of the phase word routed to the angle rotation function. That is, any or all of the phase word four least significant bits may be dithered or not dithered, controlled by the user via the serial port. Specifically, the CFR1<19> bit controls the phase dithering enable function of the phase word <16> bit. The CFR1<18> bit controls the phase dithering enable function of the phase word <15> bit. The CFR1<17> bit controls the phase dithering enable function of the phase word <14> bit. The CFR1<16> bit controls the phase dithering enable function of the phase word <13> bit. This enable function is such that if the bit is high, dithering is enabled. If the bit is low, dithering is not enabled.

Amplitude dithering uses one control bit to enable or disable dithering. If the amplitude dither enable bit (CFR1<20>) is logic 0, no amplitude dithering is enabled and the data from the DDS core is passed unchanged. When high, amplitude dithering is enabled.

Shaped On-Off Keying

General Description: The Shaped On-Off keying function of the AD9954 allows the user to control the ramp-up and ramp-down time of an "on-off" emission from the DAC. This function is used in "burst transmissions" of digital data to reduce the adverse spectral impact of short, abrupt bursts of data.

AUTO and MANUAL Shaped On-Off Keying modes are supported. The AUTO mode generates a linear scale factor at a rate determined by the Amplitude Ramp Rate (ARR) Register controlled by an external pin (OSK). MANUAL mode allows the user to directly control the output amplitude by writing the scale factor value into the Amplitude Scale Factor (ASF) Register (ASF).

The Shaped On-Off keying function may be bypassed (disabled) by clearing the OSK Enable bit (CFR1<25>=0).

The modes are controlled by two bits located in the most significant byte of the Control Function Register (CFR). CFR1<25> is the Shaped On-Off Keying enable bit. When CFR1<25> is set, the

output scaling function is enabled; CFR1<25> bypasses the function. CFR1<24> is the internal Shaped On-Off Keying active bit. When CFR1<24> is set, internal Shaped On-Off Keying mode is active; CFR1<24> cleared is external Shaped On-Off Keying mode active. CFR1<24> is a "Don't care" if the Shaped On-Off Keying enable bit (CFR1<25>) is cleared. The power up condition is Shaped On-Off Keying disabled (CFR1<25> = 0). Figure C below shows the block diagram of the OSK circuitry.

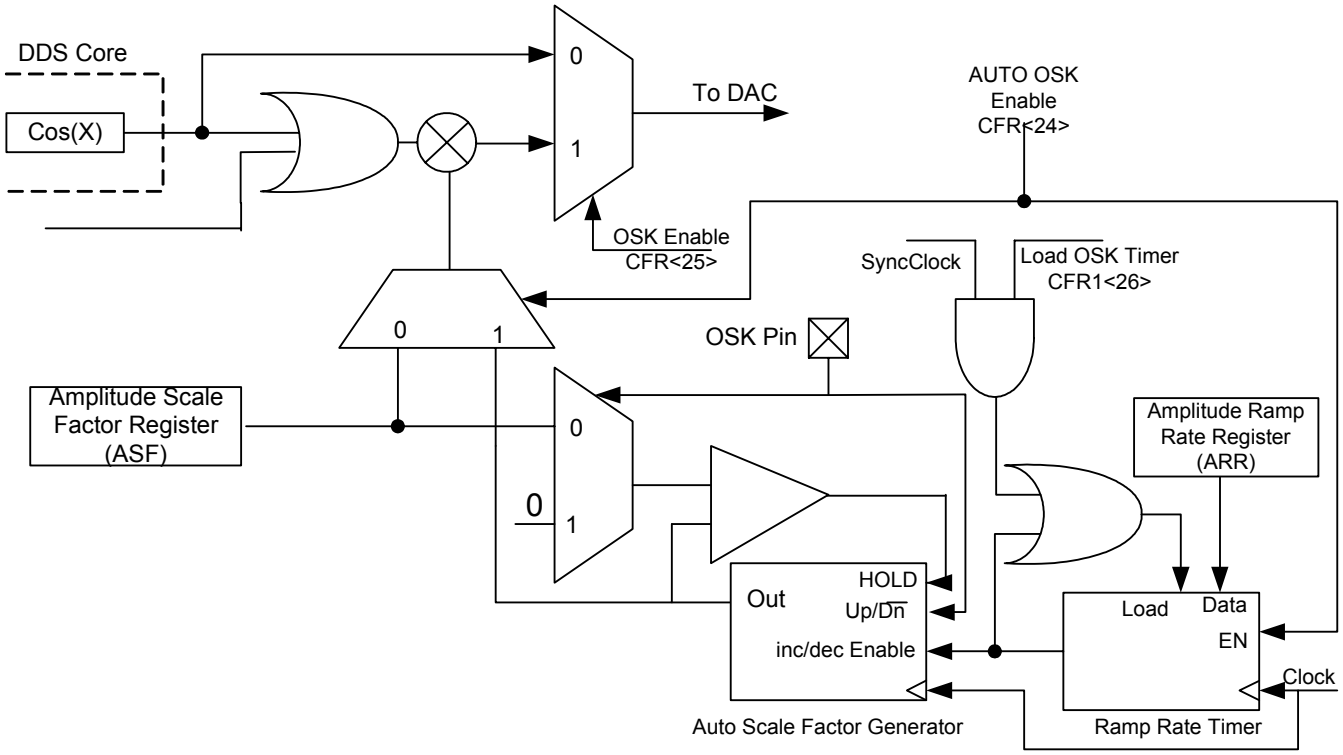


Figure C. On-Off Shaped Keying, Block Diagram

AUTO Shaped On-Off Keying mode operation:

The AUTO Shaped On-Off Keying mode is active when CFR1<25> and CFR1<24> are set. When AUTO Shaped On-Off Keying mode is enabled, a single scale factor is internally generated and applied to the multiplier input for scaling the output of the DDS core block (See Figure 9 above). The scale factor is the output of a 14-bit counter which increments/decrements at a rate determined by the contents of the 8-bit output ramp rate register. The scale factor increases if the OSK pin is high, decreases if the pin is low. The scale factor is an unsigned value such that all zeros multiplies the DDS core output by 0 (decimal) and 3FFFh multiplies the DDS core output by 16383 decimal.

For those users who use the full amplitude (14-bits) but need fast ramp rates, the internally generated scale factor step size is controlled via the ASF<15:14> bits. The table below describes the increment/decrement step size of the internally generated scale factor per the ASF<15:14> bits.

ASF<15:14> (binary)	Increment/decrement size
00	1
01	2
10	4
11	8

Table 6 Auto-Scale Factor Internal Step Size

A special feature of this mode is that the maximum output amplitude allowed is limited by the contents of the Amplitude Scale Factor Register. This allows the user to ramp to a value less than full scale.

OSK Ramp Rate Timer

The OSK ramp rate timer is a loadable down counter, which generates the clock signal to the 14-bit counter that generates the internal scale factor. The ramp rate timer is loaded with the value of the ASFR every time the counter reaches 1 (decimal). This load and count down operation continues for as long as the timer is enabled unless the timer is forced to load before reaching a count of 1.

If the Load OSK Timer bit (CFR1<26>) is set, the ramp rate timer is loaded upon an I/O UPDATE, change in profile input or upon reaching a value of 1. The ramp timer can be loaded before reaching a count of 1 by three methods.

Method one is by changing the OSK input pin. When the OSK input pin changes state the ASFR value is loaded into the ramp rate timer, which then proceeds to count down as normal.

The second method in which the sweep ramp rate timer can be loaded before reaching a count of 1 is if the Load OSK Timer bit (CFR1<26>) bit is set and an I/O UPDATE (or change in profile) is issued.

The last method in which the sweep ramp rate timer can be loaded before reaching a count of 1 is when going from the inactive AUTO Shaped On-Off Keying mode to the active AUTO Shaped On-Off Keying mode. That is, when the sweep enable bit is being set.

External Shaped On-Off Keying mode operation:

The external Shaped On-Off Keying mode is enabled by writing CFR1<25> to a logic 1 AND writing CFR1<24> to a logic 0. When configured for external Shaped On-Off Keying, the content of the ASFR becomes the scale factor for the data path. The scale factors are synchronized to sync_clk via the I/O UPDATE functionality.

Synchronization; Register Updates (I/O UPDATE)

Functionality of the SyncClk and I/O UPDATE

Data into the AD9954 is synchronous to the sync_clk signal (supplied externally to the user on the SYNC_CLK pin). The I/O UPDATE pin is sampled on the rising edge of the sync_clk.

Internally, sysclk is fed to a divide-by-4 frequency divider to produce the sync_clk signal. The sync_clk signal is provided to the user on the SYNC_CLK pin. This enables synchronization of external hardware with the device's internal clocks. This is accomplished by forcing any external hardware to obtain its timing from sync_clk. The I/O UPDATE signal coupled with sync_clk is used to transfer internal buffer contents into the Control Registers of the device. The combination of the sync_clk and I/O UPDATE pins provides the user with constant latency relative to sysclk and also ensures phase continuity of the analog output signal when a new tuning word or phase offset value is asserted. Figure E demonstrates an I/O Update timing cycle and synchronization.

Notes to synchronization logic:

1) The I/O UPDATE signal is edge detected to generate a single rising edge clock signal that drives the register bank flops. The I/O UPDATE signal has no constraints on duty cycle. The minimum low time on I/O UPDATE is one sync_clk clock cycle.
2) The I/O UPDATE pin is setup and held around the rising edge of sync_clk and has zero hold time and 10ns setup time.

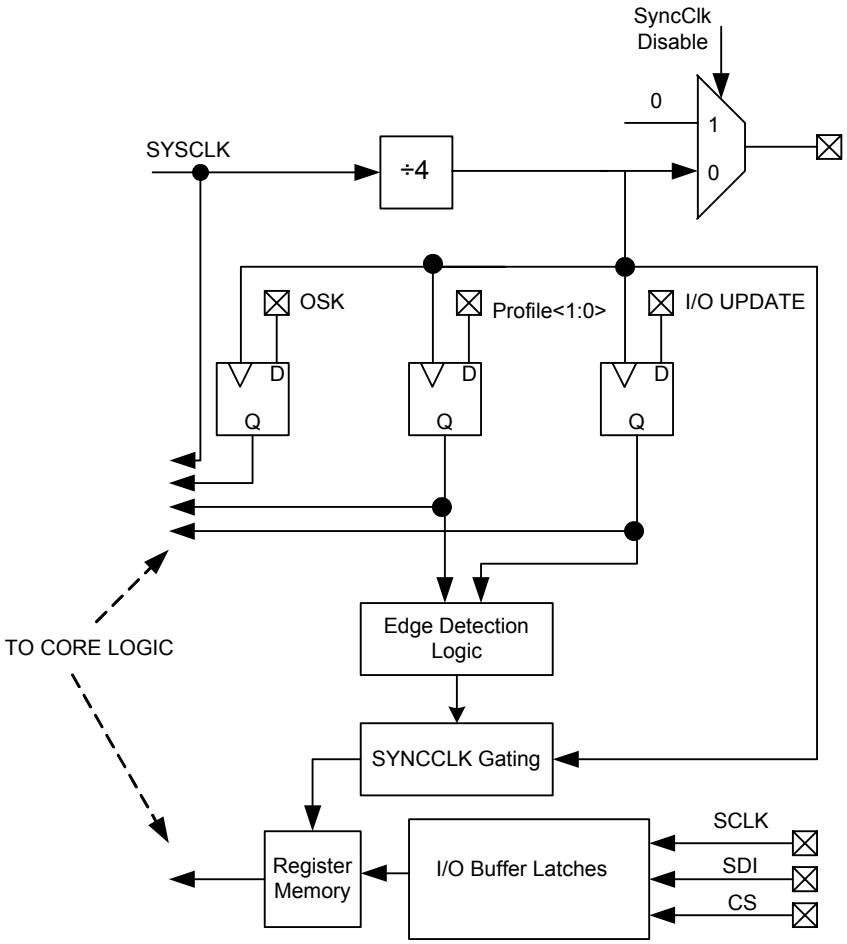
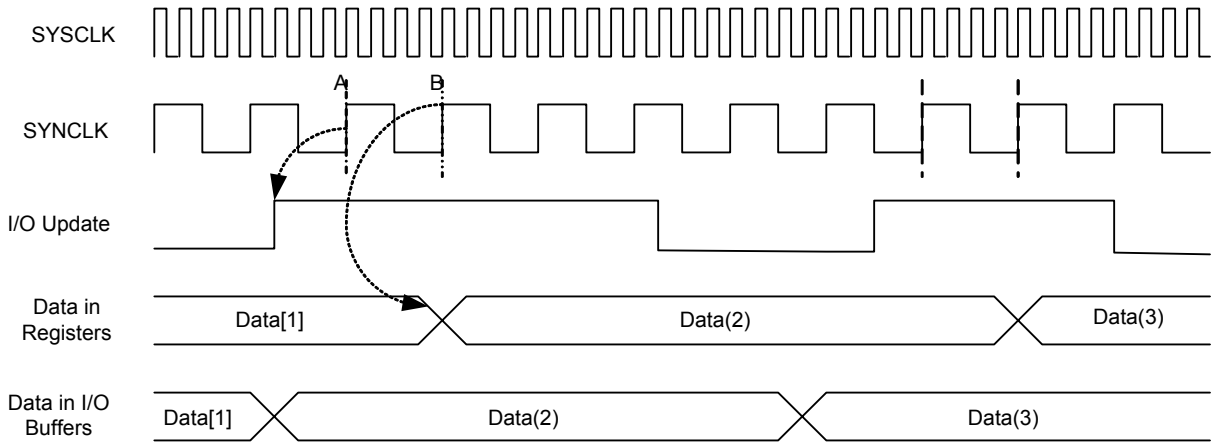


Figure D- I/O Synchronization Block Diagram



The device registers an I/O Update at point A. The data is tranferred from the asynchronously loaded I/O buffers at point B.

Figure E - I/O Synchronization Timing Diagram

Synchronizing Multiple AD9954s

The AD9954 product allows easy synchronization of multiple AD9954s. There are three modes of synchronization available to the user: an automatic synchronization mode; a software controlled manual synchronization mode; and a hardware controlled manual synchronization mode. In all cases, when a user wants to synchronize two or more devices, the following considerations must be observed. First, all units must share a common clock source. Trace lengths and path impedance of the clock tree must be designed to keep the phase delay of the different clock branches as closely matched as possible. Second, the I/O update signal's rising edge must be provided synchronously to all devices in the system. Finally, regardless of the internal synchronization method used, the DVDD_I/O supply should be set to 3.3V for all devices that are to be synchronized. AVDD and DVDD should be left at 1.8V.

In automatic synchronization mode, one device is chosen as a master, the other device(s) will be slaved to this master. When configured in this mode, all the slaves will automatically synchronize their internal clocks to the sync_clk output signal of the master device. To enter automatic synchronization mode, set the slave device's automatic synchronization bit (CFR1<23>=1). Connect the SYNC_IN input(s) to the master SYNC_CLK output. The slave device will continuously update the phase relationship of its sync_clk until it is in phase with the SYNC_IN input, which is the sync_clk of the master device. When attempting to synchronize devices running at sysclk speeds beyond 250MSPS, the high-speed sync enhancement enable bit should be set (CFR2<11>=1).

In software manual synchronization mode, the user forces the device to advance the sync_clk rising edge one sysclk cycle (1/4 sync_clk period). To activate the manual synchronization mode, set the slave device's software manual synchronization bit (CFR1<22> =1). The bit (CFR1<22>) will be immediately cleared. To advance the rising edge of the sync_clk multiple times, this bit will need to be set multiple times.

In hardware manual synchronization mode, the SYNC_IN input pin is configured such that it will now advance the rising edge of the sync_clk signal each time the device detects a rising edge on the SYNC_IN pin. To put the device into hardware manual synchronization mode, set the hardware manual synchronization bit (CFR2<10>=1). Unlike the software manual synchronization bit, this bit does not self-clear. Once the hardware manual synchronization mode is enabled, all rising edges detected on the SYNC_IN input will cause the device to advance the rising edge of the sync_clk by one sysclk cycle until this enable bit is cleared (CFR2<10=0).

Using a Single Crystal To Drive Multiple AD9954 Clock Inputs

The AD9954 crystal oscillator output signal is available on the CrystalOut pin, enabling one crystal to drive multiple AD9954s. In order to drive multiple AD9954s with one crystal, the CrystalOut pin of the AD9954 using the external crystal should be connected to the REFCLK input of the other AD9954.

The CrystalOut pin is static until the CFR2<1> bit is set, enabling the output. The drive strength of the CrystalOut pin is typically very low, so this signal should be buffered prior to using it to drive any loads.

Serial Port Operation

With the AD9954, the Instruction Byte specifies read/write operation and register address. Serial operations on the AD9954 occur only at the register level, not the byte level. For the AD9954, the serial port controller recognizes the Instruction Byte register address and automatically generates the proper register byte address. In addition, the controller expects that all bytes of that register will be accessed. **It is a requirement that all bytes of a register be accessed during serial I/O operations,** with one exception. The SYNCIO function can be used to abort an IO operation thereby allowing less than all bytes to be accessed.

There are two phases to a communication cycle with the AD9954. Phase 1 is the instruction cycle, which is the writing of an instruction byte into the AD9954, coincident with the first eight SCLK rising edges. The instruction byte provides the AD9954 serial port controller with information regarding the data transfer cycle, which is Phase 2 of the communication cycle. The Phase 1 instruction byte defines whether the upcoming data transfer is read or write and the serial address of the register being accessed. [Note – the serial address of the register being accessed is NOT the same address as the bytes to be written. See the Example Operation section below for details].

The first eight SCLK rising edges of each communication cycle are used to write the instruction byte into the AD9954. The remaining SCLK edges are for Phase 2 of the communication cycle. Phase 2 is the actual data transfer between the AD9954 and the system controller. The number of bytes transferred during Phase 2 of the communication cycle is a function of the register being accessed. For example, when accessing the Control Function Register 2, which is three bytes wide, Phase 2 requires that three bytes be transferred. If accessing the Frequency Tuning Word, which is four bytes wide, Phase 2 requires that four bytes be transferred. After transferring all data bytes per the instruction, the communication cycle is completed.

At the completion of any communication cycle, the AD9954 serial port controller expects the next 8 rising SCLK edges to be the instruction byte of the next communication cycle. All data input to the AD9954 is registered on the rising edge of SCLK. All data is driven out of the AD9954 on the falling edge of SCLK. Figures 34 - 37 are useful in understanding the general operation of the AD9954 Serial Port.

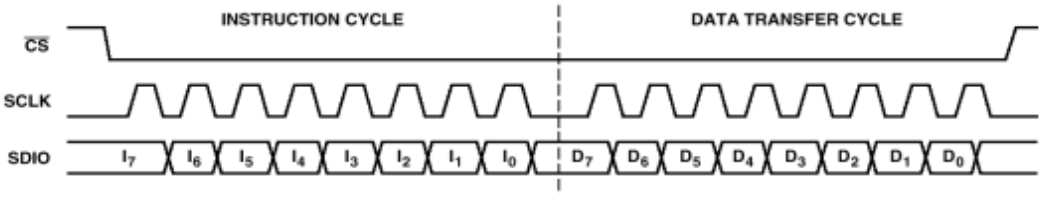


Figure 34. Serial Port Writing Timing—Clock Stall Low

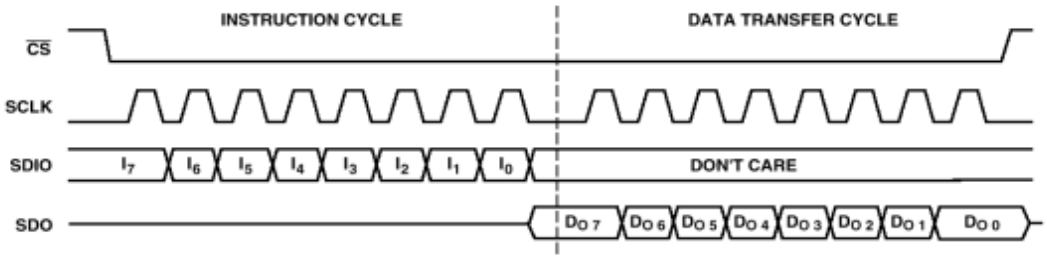


Figure 35. Three-Wire Serial Port Read Timing—Clock Stall Low

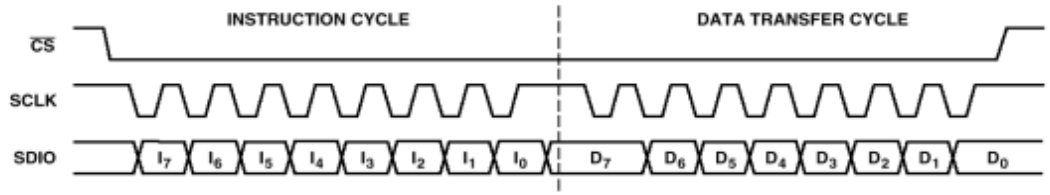


Figure 36. Serial Port Write Timing—Clock Stall High

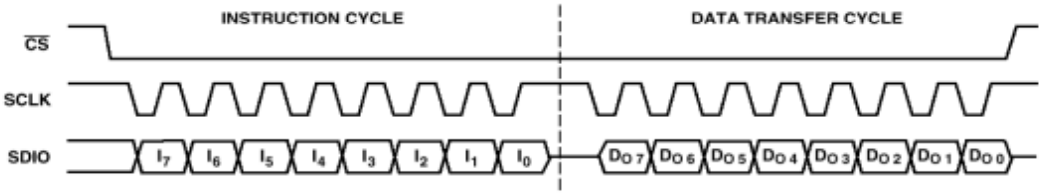


Figure 37. Two-Wire Serial Port Read Timing—Clock Stall High

Instruction Byte

The instruction byte contains the following information as shown in the table below:

Instruction Byte Information

MSB	D6	D5	D4	D3	D2	D1	LSB
R/Wb	X	x	A4	A3	A2	A1	A0

Table 7 Instruction Byte

R/-Wb—Bit 7 of the instruction byte determines whether a read or write data transfer will occur after the instruction byte write. Logic high indicates read operation. Logic zero indicates a write operation.

X, X—Bits 6 and 5 of the instruction byte are don't care.

A4, A3, A2, A1, A0—Bits 4, 3, 2, 1, 0 of the instruction byte determine which register is accessed during the data transfer portion of the communications cycle.

Serial Interface Port Pin Description

SCLK — Serial Clock. The serial clock pin is used to synchronize data to and from the AD9954 and to run the internal state machines. SCLK maximum frequency is 25 MHz.

CSB — Chip Select Bar. Active low input that allows more than one device on the same serial communications line. The SDO and SDIO pins will go to a high impedance state when this input is high. If driven high during any communications cycle, that cycle is suspended until CS is reactivated low. Chip Select can be tied low in systems that maintain control of SCLK.

SDIO — Serial Data I/O. Data is always written into the AD9954 on this pin. However, this pin can be used as a bi-directional data line. Bit 7 of register address 0h controls the configuration of this pin. The default is logic zero, which configures the SDIO pin as bi-directional.

SDO — Serial Data Out. Data is read from this pin for protocols that use separate lines for transmitting and receiving data. In the case where the AD9954 operates in a single bi-directional I/O mode, this pin does not output data and is set to a high impedance state.

SYNCIO — Synchronizes the I/O port state machines without affecting the addressable registers contents. An active high input on the SYNC I/O pin causes the current communication cycle to abort. After SYNC I/O returns low (Logic 0) another communication cycle may begin, starting with the instruction byte write.

MSB/LSB Transqfers

The AD9954 serial port can support both most significant bit (MSB) first or least significant bit (LSB) first data formats. This functionality is controlled by the Control Register 00h<8> bit. The default value of Control Register 00h<8> is low (MSB first). When Control Register 00h<8> is set high, the AD9954 serial port is in LSB first format. The instruction byte must be written in the format indicated by Control Register 00h<8>. That is, if the AD9954 is in LSB first mode, the instruction byte must be written from least significant bit to most significant bit.

For MSB first operation, the serial port controller will generate the most significant byte (of the specified register) address first followed by the next lesser significant byte addresses until the IO

operation is complete. All data written to (read from) the AD9954 must be (will be) in MSB first order. If the LSB mode is active, the serial port controller will generate the least significant byte address first followed by the next greater significant byte addresses until the IO operation is complete. All data written to (read from) the AD9954 must be (will be) in LSB first order.

Example Operation

To write the Amplitude Scale Factor register in MSB first format apply an instruction byte of 02h (serial address is 00010(b)). From this instruction, the internal controller will generate an internal byte address of 07h (see the register map) for the first data byte written and an internal address of 08h for the next byte written. Since the Amplitude Scale Factor register is two bytes wide, this ends the communication cycle.

To write the Amplitude Scale Factor register in LSB first format apply an instruction byte of 40h. From this instruction, the internal controller will generate an internal byte address of 07h (see the register map) for the first data byte written and an internal address of 08h for the next byte written. Since the Amplitude Scale Factor register is two bytes wide, this ends the communication cycle.

RAM I/O Via Serial Port

Accessing the RAM via the serial port is identical to any other serial IO operation except that the number of bytes transferred is determined by the address space between the beginning address and the final address as specified in the current RAM Segment Control Word (RSCW). The final address describes the most significant word address for all IO transfers and the beginning address specifies the least significant address.

RAM I/O supports MSB/LSB first operation. When in MSB first mode, the first data byte will be for the most significant byte of the memory address described by the final address with the remaining three bytes making up the lesser significant bytes of that address. The remaining bytes come in most significant to least significant, destined for RAM addresses generated in descending order until the final four bytes are written into the address specified as the beginning address. When in LSB first mode, the first data byte will be for the least significant byte of the memory (specified by the beginning address) with the remaining three bytes making up the greater significant bytes of that address. The remaining bytes come in least significant to most significant, destined for RAM addresses generated in ascending order until the final four bytes are written into the memory address described by the final address. Of course, the bit order for all bytes is least significant to most significant first when in the LSB first bit is set. When the LSB first bit is cleared (default) the bit order for all bytes is most significant to least significant.

The RAM uses serial address 01011(b), so the instruction byte to write the RAM is 0Bh, in MSB first notation. As mentioned above, the RAM addresses generated are specified by the beginning and final address of the RSCW currently selected by the Profile<1:0> pins.

Notes on Serial Port Operation

1) The AD9954 serial port configuration bits reside in bits 8 and 9 of CFR1 (address 00h). The configuration changes immediately upon writing to this register. For multi-byte transfers, writing to this register may occur during the middle of a communication cycle. Care must be taken to compensate for this new configuration for the remainder of the current communication cycle.
2) The system must maintain synchronization with the AD9954 or the internal control logic will not be able to recognize further instructions. For example, if the system sends an instruction byte that describes writing a 2-byte register, then pulses the SCLK pin for a 3-byte write (24 additional SCLK rising edges), communication synchronization is lost. In this case, the first 16 SCLK rising edges after the instruction cycle will properly write the first two data bytes into the AD9954, but the next eight rising SCLK edges are interpreted as the next instruction byte, not the final byte of the previous communication cycle. In the case where synchronization is lost between the system and the AD9954, the SYNC I/O pin provides a means to re-establish synchronization without re-initializing the entire chip. The SYNC I/O pin enables the user to reset the AD9954 state machine to accept the next eight SCLK rising edges to be coincident with the instruction phase of a new communication cycle. By applying and removing a "high" signal to the SYNC I/O pin, the AD9954 is set to once again begin performing the communication cycle in synchronization with the system. Any information that had been written to the AD9954 registers during a valid communication cycle prior to loss of synchronization will remain intact.
3) Reading profile registers requires that the profile select pins (Profile<1:0>) be configured to select the desired register bank. When reading a register that resides in one of the profiles, the register address acts as an offset to select one of the registers among the group of registers defined by the profile. While the profile select pins select the appropriate register group.

Power Down Functions of the AD9954

The AD9954 supports an externally controlled, or hardware, power down feature as well as the more common software programmable power down bits found in previous ADI DDS products.

The software control power down allows the DAC, Comparator, PLL, Input Clock circuitry and the digital logic to be individually power down via unique control bits (CFR1<7:4>). With the exception of CFR1<6>, these bits are not active when the externally controlled power down pin (PwrDwnCtl) is high. External Power Down Control is supported on the AD9954 via the PwrDwnCtl input pin. When the PwrDwnCtl input pin is high, the AD9954 will enter a power down mode based on the CFR1<3> bit. When the PwrDwnCtl input pin is low, the external power down control is inactive.

When the CFR1<3> bit is zero, and the PwrDwnCtl input pin is high, the AD9954 is put into a "fast recovery power down" mode. In this mode, the digital logic and the DAC digital logic are powered down. The DAC bias circuitry, comparator, PLL, oscillator, and clock input circuitry is NOT powered down. The comparator can be powered down by setting the Comparator Power Down Bit, CFR1<6> =1.

When the CFR1<3> bit is high, and the PwrDwnCtl input pin is high, the AD9954 is put into the "full power down" mode. In this mode, all functions are powered down. This includes the DAC and PLL, which take a significant amount of time to power up.

When the PwrDwnCtl input pin is high, the individual power down bits (CFR1<7>, <5:4>) are invalid (don't care) and are unused; however the Comparator Power Down bit, CFR1<6>, will continue to control the power-down of the comparator. When the PwrDwnCtl input pin is low, the individual power down bits control the power down modes of operation.

NOTE – The power down signals are all designed such that a logic 1 indicates the low power mode and a logic zero indicates the active, or powered up mode.

The table below indicates the logic level for each power down bit that drives out of the AD9954 core logic to the analog section and the digital clock generation section of the chip for the External Power Down operation.

Control	Mode active	Description
PwrDwnCtl = 0 CFR1<3> don't care	Software Control	Digital power down = CFR1<7> Comparator power down = CFR1<6> DAC power down = CFR1<5> Input Clock power down = CFR1<4>
PwrDwnCtl = 1 CFR1<3> = 0	External Control, Fast recovery power down mode	Digital power down = 1'b1; Comparator power down = 1'b0 OR CFR1<6>; DAC power down = 1'b0; Input Clock power down = 1'b0;
PwrDwnCtl = 1 CFR1<3> = 1	External Control, Full power down mode	Digital power down = 1'b1; Comparator power down = 1'b1; DAC power down = 1'b1; Input Clock power down = 1'b1;

Table 8 Power Down Control Functions

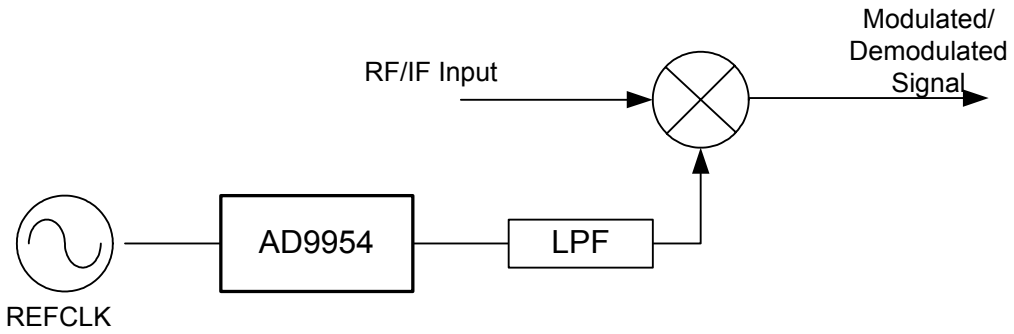


Figure F Synthesized L.O For Upconversion/DownConversion

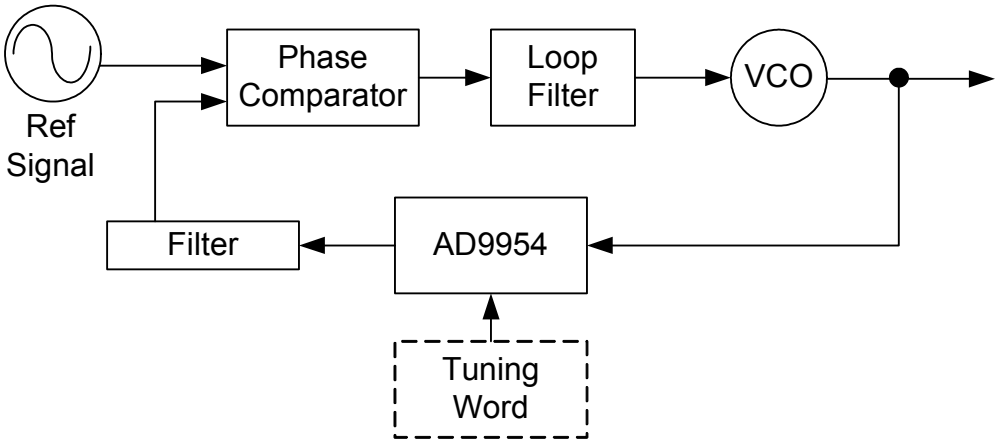


Figure G Digitally Programmable “Divide-by-N” Function in PLL

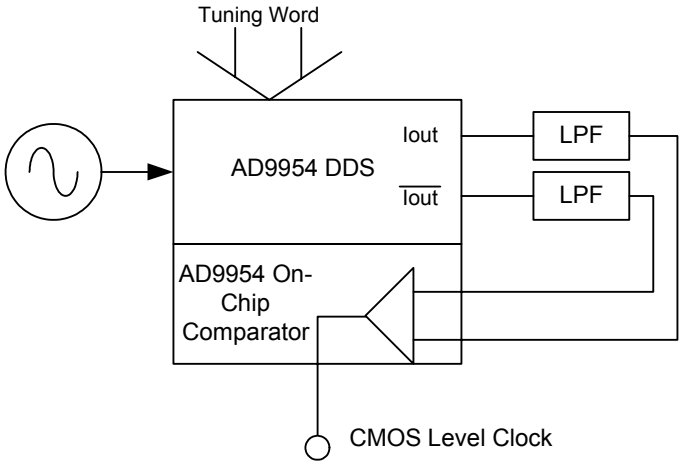


Figure H Frequency Agile Clock Generator

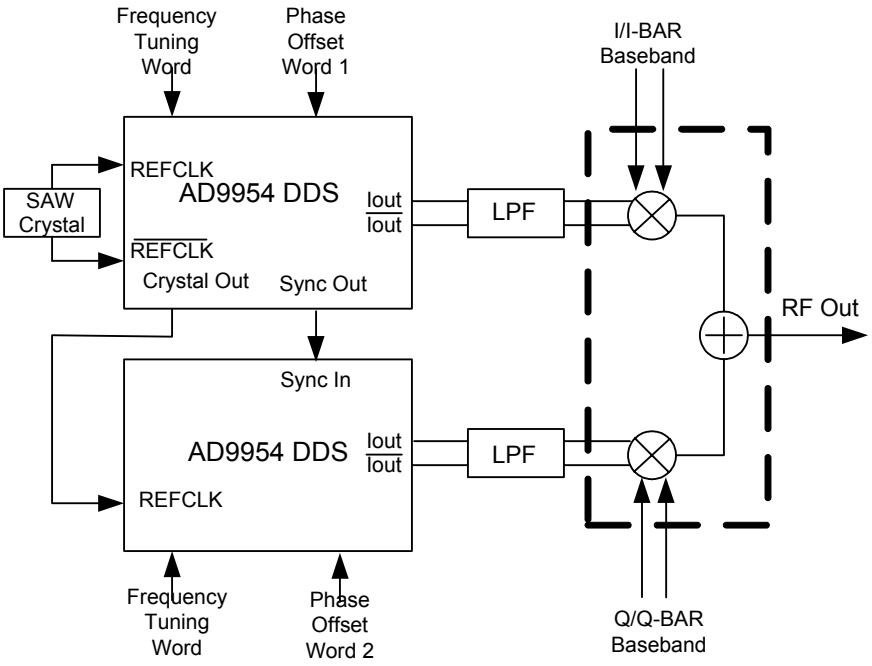


Figure I Two AD9954s Synchronized to Provide I & Q Carriers with Independent Phase Offsets for Nulling