Current-Mode PWM Controller

FEATURES

- Low Start-Up Current (300μA Typical)
- Internal Precision Reference.
- 500KHz Current-Mode Operation.
- Pulse-by-Pulse Current Limiting.
- Automatic Feed-Forward Compensation.
- Optimized for Off-line and DC/DC Converters.
- Under-voltage Lockout with Hysteresis.
- Double Pulse Suppression.
- High Current Totem Pole Output.

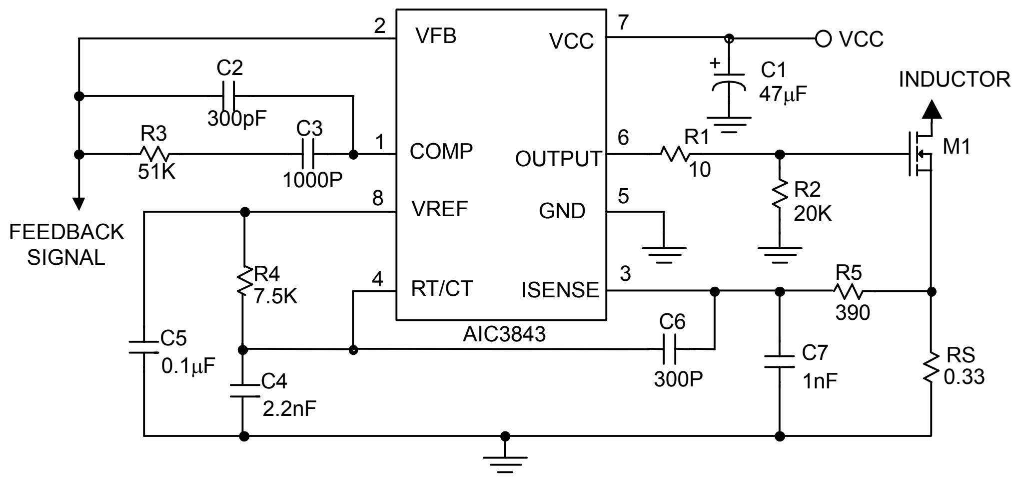
APPLICATIONS

- AC/DC Off-line Converter.
- DC/DC Off-line Converter.

DESCRIPTION

The AIC3843 control IC provides the features that are necessary to implement off-line or DC/DC Converter fixed-frequency current-mode schemes with a minimum number of external components. This integrated circuits features an under-voltage lockout (UVLO) with approximately 300μA start-up current, a precision reference trimmed for accuracy at the error amplifier input, high gain error amplifier, current sensing comparator, logic to insure latched operation, and a totem-pole output stage designed to source or sink high peak current. The output stage, suitable for driving the N-channel MOSFETs, is low in the off state.

TYPICAL APPLICATION CIRCUIT



Current Mode PWM Control Circuit

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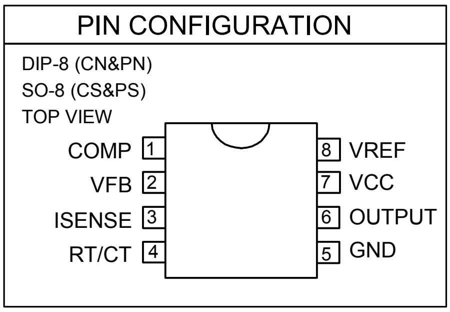
ORDERING INFORMATION

AIC3843XXXX

- PACKING TYPE
  TR: TAPE & REEL
  TB: TUBE
- PACKAGING TYPE
  N: PLASTIC DIP
  S: SMALL OUTLINE
- C: COMMERCIAL
  P: LEAD FREE COMMERCIAL



Example: AIC3843CSTR

→ in SO-8 Package & Taping & Reel Packing Type
(CN is not available in Tape & Reel packing type.)

AIC3843PSTR

→ in SO-8 Lead Free Package & Taping & Reel Packing Type

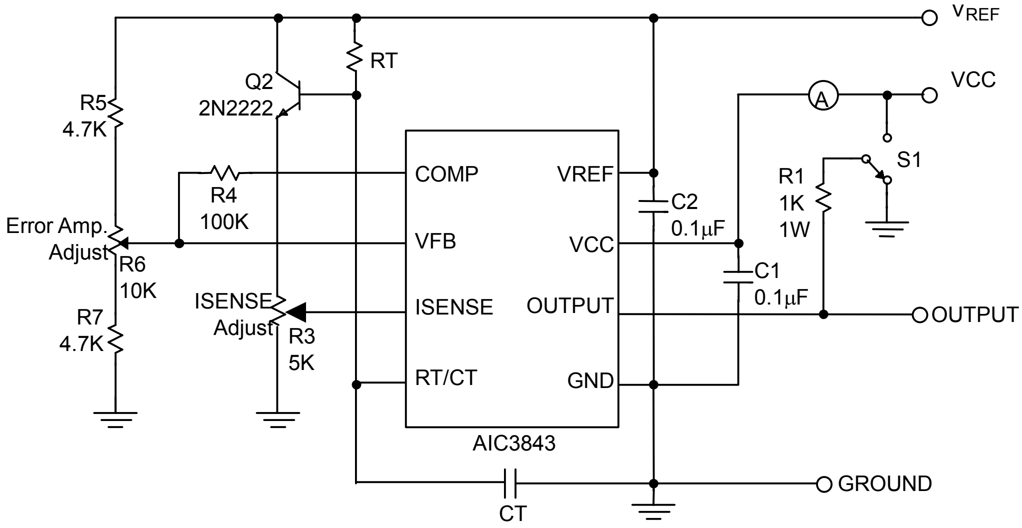
ABSOLUTE MAXIMUM RATINGS

Supply Voltage (Low Impedance Source)	30V
Supply Voltage (I_{CC}<30mA)	Self Limiting
Output Current	±1A
Output Energy (Capacitive Load)	5μJ
Analog Inputs (Pins 2, 3)	-0.3V ~ +6.3V
Error Amp Output Sink Current	10mA
Power Dissipation at TA≤25°C DIP Package	1W
SOIC Package	725mW
Operating Temperature Range	-40°C ~ 85°C
Junction Temperature Range	125°C
Storage Temperature Range	–65°C ~ 150°C
Lead Temperature (Soldering 10 Sec)	260°C

Note 1: All voltages are with respect to Pin 5.
All currents are positive into the specified terminal.

Note 2: Absolute Maximum Ratings are those values beyond which the life of a device may be Impaired.

■ TEST CIRCUIT



ELECTRICAL CHARACTERISTICS

{V_{CC}= 15V (see Note 3), -40°C ≦ T_A ≦85°C, unless otherwise specified.} (Note 6)

PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Reference Section					
Output Voltage	I_O=1mA	4.9	5	5.1	V
Line Regulation	V_{CC}=12V to 25V		5	20	mV
Load Regulation	I_O=1mA to 20mA		5	25	mV
Temperature Coefficient of Output Voltage			0.2	0.4	mV/°C
Output Noise Voltage	f =10Hz to 10KHz		50		μV
Output Voltage Long Term Drift	After 1000H at T_A=25°C		5	25	mV
Short Circuit Output Current		-30	-85	-180	mA
Oscillator Section					
Oscillator Frequency (see Note 4)		47	52	57	KHz
Frequency Change with Supply Voltage	VCC=12V to 25V		0.2	1	%
Frequency Change with Temperature	TA=TLOW to THIGH		5		%
Peak-to-Peak Amplitude at RT/CT			1.7		V
Error Amplifier Section					
Feedback Input Voltage	COMP at 2.5V	2.42	2.50	2.58	V
Input Bias Current			-0.3	-2	μA
Open-Loop Voltage Amplification	V_O=2V to 4V	65	90		dB
Gain-Bandwidth Product		0.7	1		MHz
Supply Voltage Rejection Ratio	V_{CC}=12V to 25V	60	70		dB
Output Sink Current	V_{FB} at 2.7V, COMP at 1.1V	2	10		mA
Output Source Current	V_{FB} at 2.3V, COMP at 5V	-0.5	-1		mA
High-Level Output Voltage	V_{FB} at 2.3V, R_L=15KΩ to GND	5	6.2		V
Low-Level Output Voltage	V_{FB} at 2.7V, R_L=15Ω to VREF		0.8	1.1	V

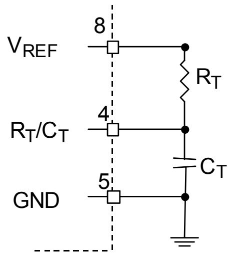
ELECTRICAL CHARACTERISTICS (Continued)

PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Current Sense Section					
Voltage Amplification	See Note 4 and 5	2.85	3	3.15	V/V
Current Sense Comparator Threshold	COMP at 5V, See Note 4	0.9	1	1.1	V
Supply Voltage Rejection Ratio	V_{CC}=12V to 25V, See Note 4		70		dB
Input Bias Current			-2	-10	μA
Delay Time to Output			150	300	nS
Output Section					
High-Level Output Voltage	I_{SOURCE}=20mA	13	13.5		V
	I_{SOURCE} =200mA	12	13.4		V
Low-Level Output Voltage	I_{SINK}=20mA		0.1	0.4	V
	I_{SINK}=200mA		1.5	2.2	V
Rise Time	C_L=1nF		50	150	nS
Fall Time	C_L=1nF		50	150	nS
Under voltage Lockout Section					
Start Threshold Voltage		7.8	8.4	9.0	V
Minimum Operating Voltage after Start-Up		7.0	7.6	8.2	V
Pulse-Width-Modulator Section					
Maximum Duty Cycle		95	96	100	%
Minimum Duty Cycle				0	%
Supply Voltage					
Start-Up Current			0.3	0.5	mA
Operating Supply Current	V_{FB} and I_{SENSE} at 0V		12	17	mA
Limiting Voltage	I_{CC}=25mA	30	34		V

Note: 3: Adjust VCC above the start threshold before setting it to 15V.
4. These parameters are measured at the trip point of the latch with VFB at 0V.
5. Voltage amplification is measured between ISENSE and COMP with the input changing from 0V to 0.8V.
6. Specifications are production tested at TA = 25°C. Specifications over the -40°C to 85°C operating Temperature range are assured by design, characterization and correlation with Statistical Quality Controls (SQC).

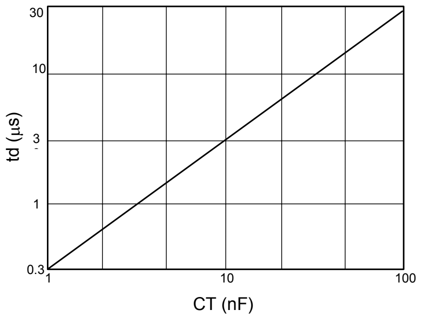
TYPICAL PERFORMANCE CHARACTERISTICS

Oscillator Section



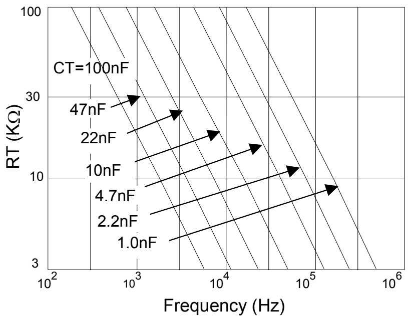
For RT>5k, f≈ $\frac{1.72}{R_T * C_T}$

Fig. 1-1



Deadtime vs CT (RT>5KΩ)

Fig. 1-2



Timing Resistance vs. Frequency

Fig. 1-3

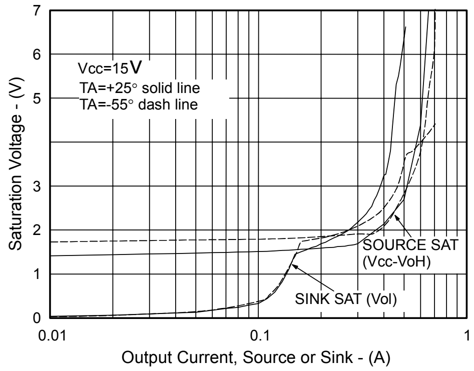


Fig. 1-4 Output saturation characteristics

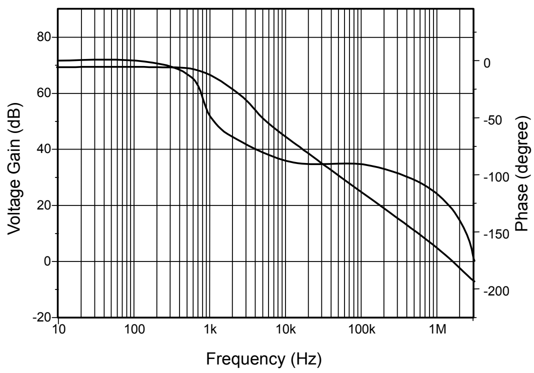
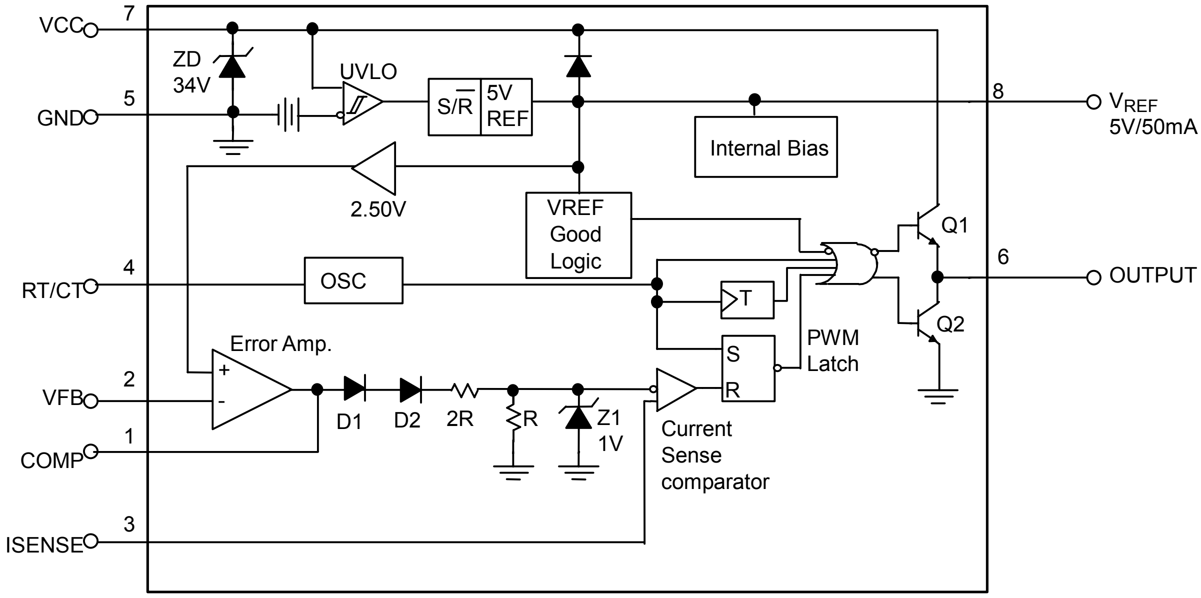


Fig. 1-5 Error Amplifier Open-Loop Frequency Response

BLOCK DIAGRAM



PIN DESCRIPTIONS

PIN 1: COMP - This pin is the error amplifier output and is made available for loop compensation.

PIN 2: VFB - This is the inverting input of the error amplifier. It is normally connected to the switching power supply output through a resistor divider.

PIN 3: ISENSE - A voltage proportional to inductor current is connected to this input. The PWM uses this information to terminate the output switch conduction.

PIN 4: RT/CT - The oscillator frequency and maximum output duty cycle are programmed by connecting resistor R_T to V_{REF} and capacitor C_T to ground. It is feasible to operate when f$\leqq$ 500KHz.

PIN 5: GND - This pin is the combined control circuitry and power ground.

PIN 6: OUTPUT- This output directly drives the gate of a power MOSFET. Peak currents up to 1A are sourced and sunk by this pin.

PIN 7: VCC - This pin is the positive supply of the control IC.

PIN 8: VREF - This is the reference output. It provides charging current for capacitor CT through resistor RT.

APPLICATION INFORMATION

Under voltage Lockout

There are two separate under voltage lockout comparators incorporated to make sure that the IC is fully functional before the output stage is enabled. One is for power supply voltage (VCC) and the other is for reference output voltage (VREF). Each has a built in hysteresis to prevent erratic output behavior when their respective thresholds are crossed. For VCC comparator the upper and lower thresholds are 8.4V and 7.6V, respectively. The large hysteresis and low start up current (0.3mA) of the AIC3843 make it ideally suited in off-line converter applications where efficient bootstrap startup techniques are required. A 34V zener is connected as a shunt regulator from VCC to ground. Its purpose is to protect the IC from excessive voltage that can occur during system start-up.

Reference Output

The 5.0V reference output is trimmed to ±2.0% tolerance at T_A=25°C. It supplies charging current to the oscillator timing capacitor and is capable of providing current in excess of 20mA for powering additional control system circuitry. In case of overload, the reference is short-circuit protected at about 85mA.

Error Amplifier

A fully compensated error amplifier is provided with inverting input and output externally accessible. The non-inverting input is internally biased at 2.5V. The converter output voltage is usually divided down and connected to the inverting input.

The output of the error amplifier is accessible for external loop compensation, with an offset at two diode drops (≅1.4V) and divided by three, before connected to the inverting input of the current sense comparator. This guarantees that no drive pulse appears at the output (pin 6).

Oscillator

The oscillator frequency can be programmed through the setting of timing components R_T and C_T. Capacitor C_T is charged from the 5.0V reference output through R_T to about 2.8V and discharged to about 1.2V by the internal discharge current. When C_T is discharged the output (pin 6) must be in the low state, thus producing a controlled amount of output deadtime. Note that many values of R_T and C_T can produce the same frequency but only one combination will yield a specific output deadtime at a given frequency.

Current Sense Comparator and PWM Latch

The output switch of AIC3843 is initiated by the oscillator and terminated when the peak inductor current reaches the threshold level established by the error amplifier output (pin 1). The AIC3843 is operated at a current mode since the inductor current is monitored cycle-by-cycle and decides the duty cycle.

The inductor current is converted to a voltage by inserting the ground referenced sense resistor R_S in series with the source of output switch M1. This voltage is monitored by the current sense input (pin 3) and is compared to a level derived from the error amplifier output. In the normal operating conditions the peak inductor current is controlled by the voltage at pin 1 where

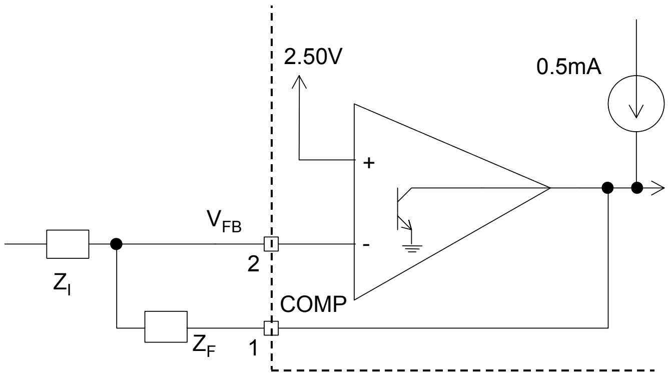
$$I_{PK} = \frac{V(\text{pin }1) - 1.4V}{3RS}$$

PWM Latch is used to ensure that only a single pulse appears at the output during any given oscillator cycle. However, a narrow spike on the leading edge of the current waveform can usually be observed and may cause the power supply to exhibit an instability when the output is tightly loaded.

Output Switch

The AIC3843 contains a single totem-pole output stage that was specifically designed for direct drive of power MOSFET. If any under voltage lockout is detected, internal circuitry will keep the output switch in a sinking current mode, no external pull down resistor is needed.

Error AMP Configuration



Error Amp can Source or Sink up to 0.5mA

Fig. 2

Under-Voltage Lockout

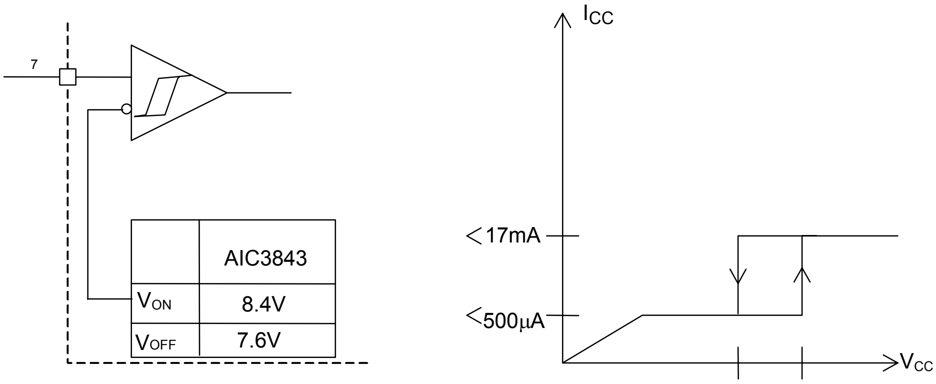
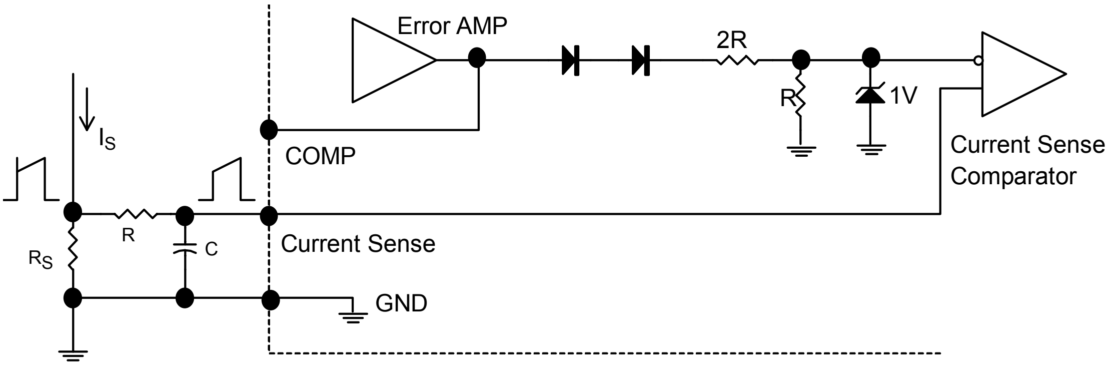


Fig. 3-1 Fig. 3-2

During under-voltage lockout, the output driver is biased to sink minor amounts of current. Pin 6 should be shunted to ground with a bleeder resistor to prevent activating the power switch with extraneous leakage currents.

Current Sense Circuit



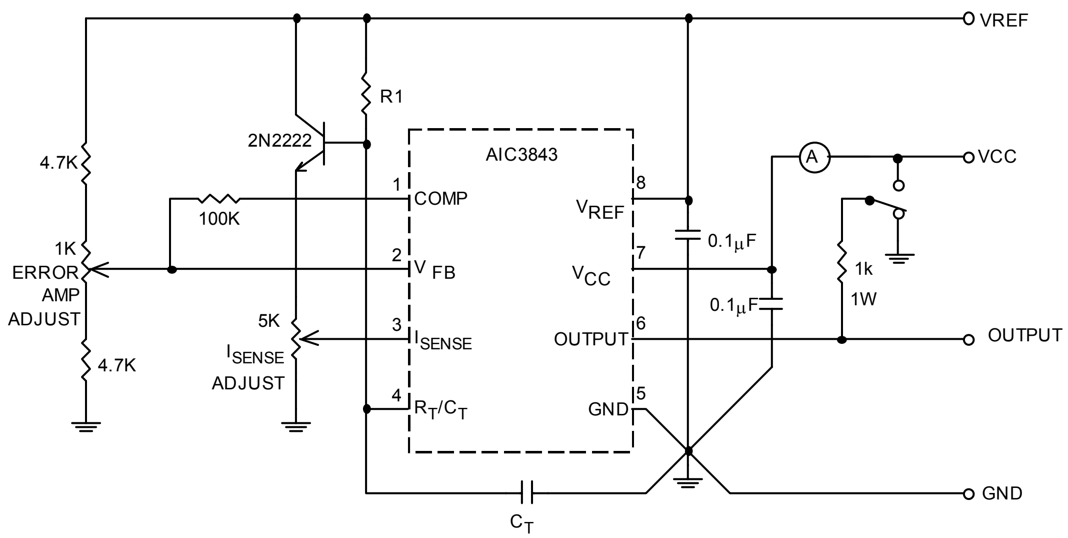
Peak Current (Is) is Determined By The Formula

$$I_{SMAX} \approx \frac{1.0V}{R_S}$$

A small RC filter may be required to suppress switch transients.

Fig. 4

Open-Loop Laboratory Fixture



High peak currents associated with capacitive loads necessitate careful grounding techniques. Timing and bypass capacitors should be connected close to pin 5 in a single point ground. The transistor and 5k potentiometer are used to sample the oscillator waveform and apply an adjustable ramp to pin 3.

Fig. 5

Open-Loop Laboratory Fixture

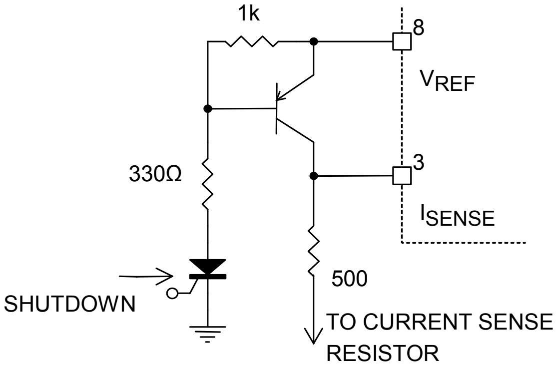


Fig. 6-1

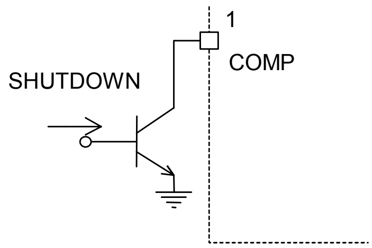
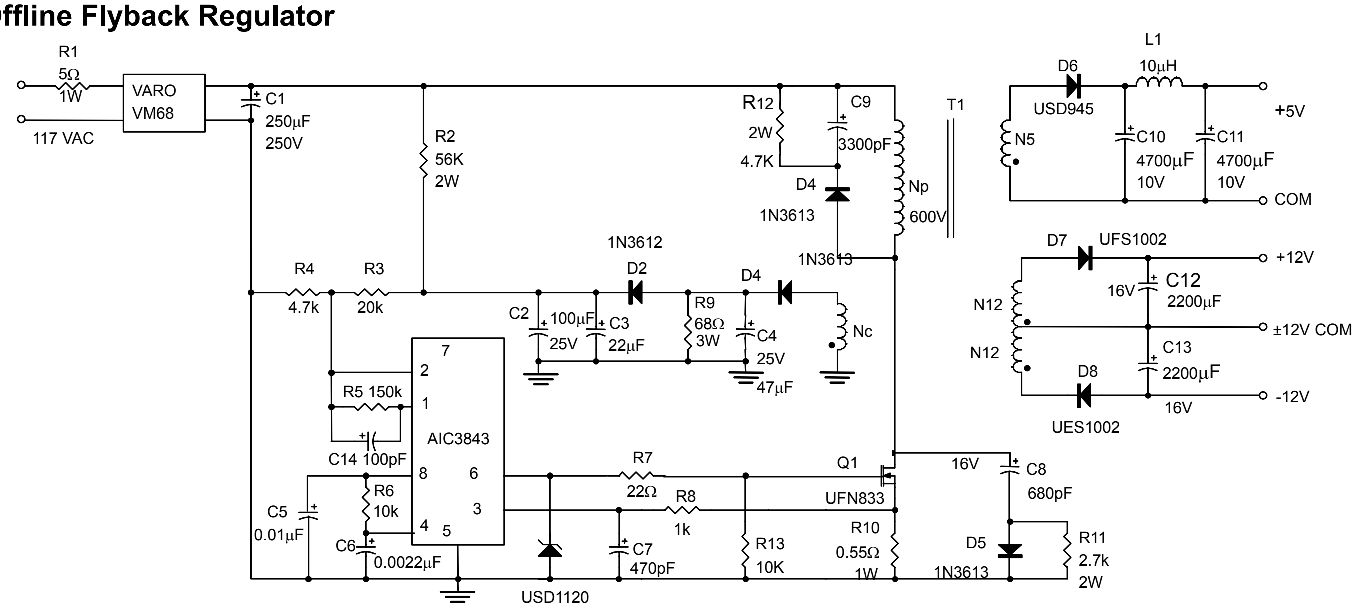


Fig. 6-2

Shutdown of the AIC3843 can be accomplished by two methods; either raise pin 3 above 1V or pull pin 1 below a voltage two-diode drops above ground. Either method causes the output of the PWM comparator to be high (refer to block diagram). The PWM latch is reset dominant so that the output will remain low until the next clock cycle after the shutdown condition at pin 1 and/or 3 is removed. In one example, an externally latched shutdown may be accomplished by adding an SCR, which will be reset by cycling Vcc below the lower UVLO threshold. At this point the reference turns off, allowing the SCR to reset.

Offline Flyback Regulator



Power Supply Specifications

1. Input Voltage 95VAC to 130VA (50Hz/60Hz)
2. Line Isolation 3750V
3. Switching Frequency 40kHz
4. Efficiency @ Full Load 70%
5. Output Voltage:
   A. +5V, ±5%; 1A to 4A load
      Ripple voltage: 50mV P-P Max
   B. +12V, ±3%; 0.1A to 0.3A load
      Ripple voltage: 100mV P-P Max
   C. -12V, ±3%; 0.1A to 0.3A load
      Ripple voltage: 100mV P-P Max

Fig. 7

Slope compensation

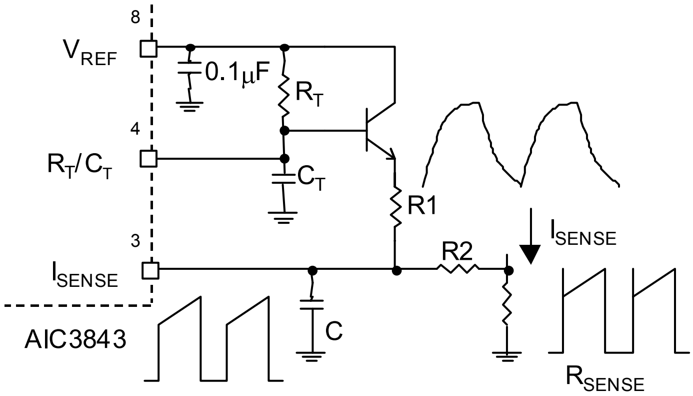
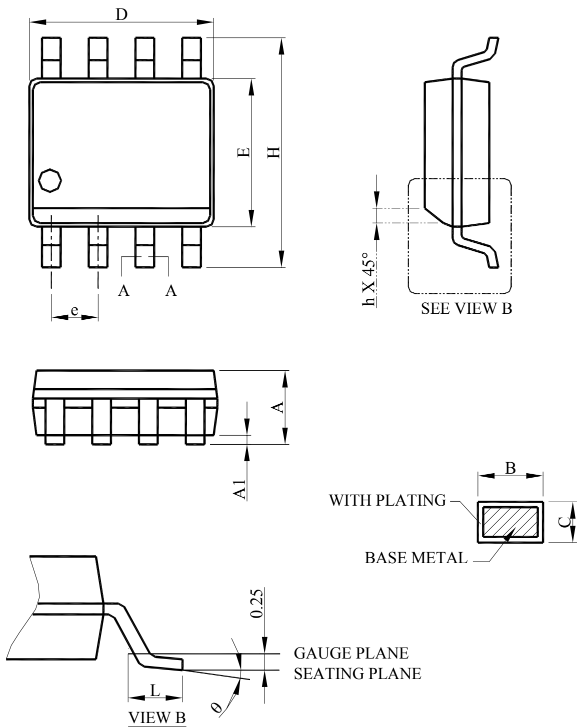


Fig. 8

A fraction of the oscillator ramp can be resistively summed with the current sense signal to proved slope compensation for converters requiring duty cycles over 50% Note that capacitor, C forms a filter with R2 to suppress the leading edge switch spikes.

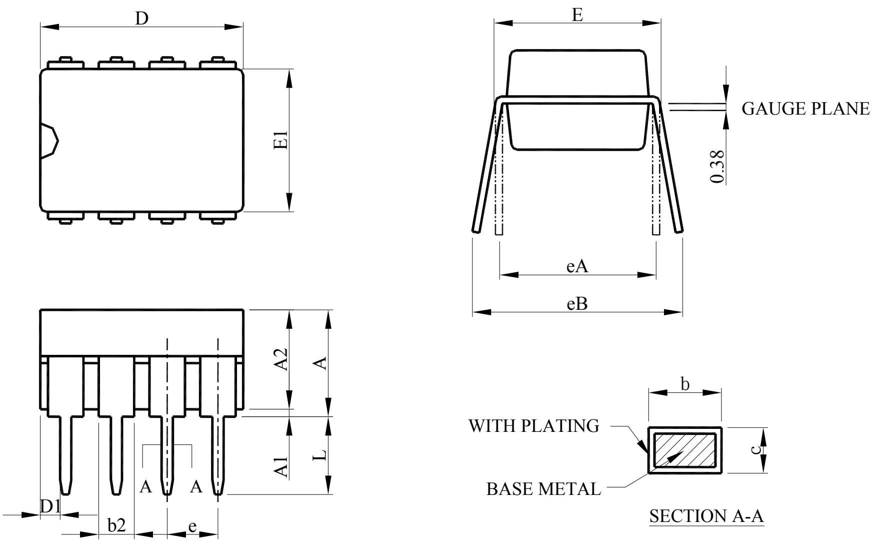
■ PHYSICAL DIMENSIONS

● 8 LEAD PLASTIC SO



SYMBOL	SOP-8	
	MILLIMETERS	
	MIN.	MAX.
A	1.35	1.75
A1	0.10	0.25
B	0.33	0.51
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.27
θ	0°	8°

- **8 LEAD PLASTIC DIP**



SYMBOL	DIP-8	
	MILLIMETERS	
	MIN.	MAX.
A		5.33
A1	0.38	
A2	2.92	4.95
b	0.36	0.56
b2	1.14	1.78
c	0.20	0.35
D	9.01	10.16
D1	0.13	
E	7.62	8.26
E1	6.10	7.11
e	2.54 BSC	
eA	7.62 BSC	
eB		10.92
L	2.92	3.81

Note:

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