Microprocessor Supervisory Circuit in 4-Lead SOT-143

ADM811/ADM812

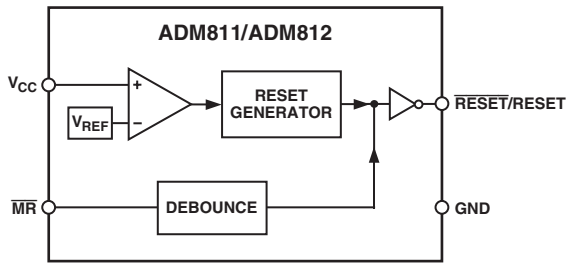
FEATURES

Superior Upgrade for MAX811/MAX812
Specified over Temperature
Low Power Consumption (5 μA Typ)
Precision Voltage Monitor: 2.5 V, 3 V, 3.3 V, 5 V Options
Reset Assertion Down to 1 V V_{CC}
140 ms Min Power-On Reset
Logic Low $\overline{RESET}$ Output (ADM811)
Logic High RESET Output (ADM812)
Built-In Manual Reset

APPLICATIONS

Microprocessor Systems
Controllers
Intelligent Instruments
Automotive Systems
Safety Systems
Portable Instruments

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The ADM811/ADM812 is a reliable voltage monitoring device suitable for use in most voltage monitoring applications. The ADM811/ADM812 is designed to monitor six different voltages, each allowing for a 5% or 10% degradation of standard PSU voltages before a reset occurs. These voltages have been selected for the effective monitoring of 2.5 V, 3 V, 3.3 V, and 5 V supply voltage levels.

Included in this circuit is a debounced manual reset input. Reset can be activated using an electrical switch (or an input from another digital device) or by a degradation of the supply voltage. The manual reset function is very useful, especially if the circuit in which the ADM811/ADM812 is operating enters into a state that can only be detected by the user. Allowing the user to reset a system manually can reduce the damage or danger that could otherwise be caused by an out-of-control or locked system.

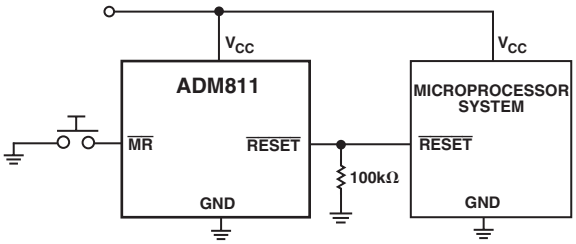


Figure 1. Typical ADM811 Operating Circuit

REV. C

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ADM811/ADM812–SPECIFICATIONS (V_{CC} = Full Operating Range; $T_A = T_{MIN}$ to T_{MAX}; V_{CC} typ = 5 V for L/M, 3.3 V for T/S, 3 V for R, 2.5 V for Z Models; unless otherwise noted.)

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY					
Voltage	1.0		5.5	V	T_A = 0°C to 70°C
	1.2			V	T_A = –40°C to +85°C
Current		8	15	µA	V_{CC} < 5.5 V, ADM81_L/M, I_{OUT} = 0 mA
		5	10	µA	V_{CC} < 3.6 V, ADM81_R/S/T/Z, I_{OUT} = 0 mA
RESET VOLTAGE THRESHOLD					
ADM81_L	4.54	4.63	4.72	V	T_A = 25°C
ADM81_L	4.50		4.75	V	T_A = –40°C to +85°C
ADM81_M	4.30	4.38	4.46	V	T_A = 25°C
ADM81_M	4.25		4.50	V	T_A = –40°C to +85°C
ADM81_T	3.03	3.08	3.14	V	T_A = 25°C
ADM81_T	3.00		3.15	V	T_A = –40°C to +85°C
ADM81_S	2.88	2.93	2.98	V	T_A = 25°C
ADM81_S	2.85		3.00	V	T_A = –40°C to +85°C
ADM81_R	2.58	2.63	2.68	V	T_A = 25°C
ADM81_R	2.55		2.70	V	T_A = –40°C to +85°C
ADM81_Z	2.28	2.32	2.35	V	T_A = 25°C
ADM81_Z	2.25		2.38	V	T_A = –40°C to +85°C
RESET THRESHOLD TEMPERATURE COEFFICIENT		30		ppm/°C	
V_{CC} TO RESET/$\overline{\text{RESET}}$ DELAY		40		µs	V_{OD} = 125 mV, ADM81_L/M
		20		µs	V_{OD} = 125 mV, ADM81_R/S/T/Z
RESET ACTIVE TIMEOUT PERIOD	140		560	ms	$V_{CC} = V_{TH(MAX)}$
	300		700	ms	(ADM811-3T Only)
MANUAL RESET					
Minimum Pulsewidth	10			µs	
Glitch Immunity		100		ns	
RESET/$\overline{\text{RESET}}$ Propagation Delay		0.5		µs	
Pull-Up Resistance	10	20	30	kΩ	
The Manual Reset Circuit Will Act On:					
An Input Rising Above	2.3			V	$V_{CC} > V_{TH(MAX)}$, ADM81_L/M
An Input Falling Below			0.8	V	$V_{CC} > V_{TH(MAX)}$, ADM81_L/M
An Input Rising Above	0.7 × V_{CC}			V	$V_{CC} > V_{TH(MAX)}$, ADM81_R/S/T/Z
An Input Falling Below			0.25 × V_{CC}	V	$V_{CC} > V_{TH(MAX)}$, ADM81_R/S/T/Z
RESET/$\overline{\text{RESET}}$ Output Voltage					
Low (ADM812R/S/T/Z)			0.3	V	$V_{CC} = V_{TH(MAX)}$, I_{SINK} = 1.2 mA
Low (ADM812L/M)			0.4	V	$V_{CC} = V_{TH(MAX)}$, I_{SINK} = 3.2 mA
High (ADM812R/S/T/Z/L/M)	0.8 × V_{CC}			V	1.8 V < V_{CC} < $V_{TH(MIN)}$, I_{SOURCE} = 150 µA
Low (ADM811R/S/T/Z)			0.3	V	$V_{CC} = V_{TH(MIN)}$, I_{SINK} = 1.2 mA
Low (ADM811L/M)			0.4	V	$V_{CC} = V_{TH(MIN)}$, I_{SINK} = 3.2 mA
Low (ADM811R/S/T/Z/L/M)			0.3	V	V_{CC} > 1.0 V, I_{SINK} = 50 µA
High (ADM811R/S/T/Z)	0.8 × V_{CC}			V	$V_{CC} > V_{TH(MAX)}$, I_{SOURCE} = 500 µA
High (ADM811L/M)	V_{CC} – 1.5			V	$V_{CC} > V_{TH(MAX)}$, I_{SOURCE} = 800 µA

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*
(Typical values are at T_A = 25°C, unless otherwise noted.)

Terminal Voltage (With Respect to Ground)
- V_{CC} . . . . . –0.3 V to +6 V
- All Other Inputs . . . . . –0.3 V to V_{CC} + 0.3 V

Input Current
- V_{CC} . . . . . 20 mA
- $\overline{MR}$ . . . . . 20 mA

Output Current
- $\overline{RESET}$ . . . . . 20 mA

Power Dissipation (T_A = 70°C)
- RT-4, (SOT-143) . . . . . 200 mW
- Derate by 4 mW/°C above 70°C
- θ_{JA} Thermal Impedance . . . . . 330°C/W

Operating Temperature Range . . . . . –40°C to +85°C
Storage Temperature Range . . . . . –65°C to +160°C
Lead Temperature (Soldering, 10 sec) . . . . . 300°C
- Vapor Phase (60 sec) . . . . . 215°C
- Infrared (15 secs) . . . . . 220°C

ESD Rating . . . . . 3 kV

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods of time may affect device reliability.

ORDERING GUIDE

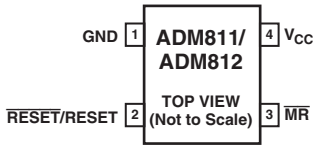
Model*	Reset Threshold (V)	Temperature Range	Branding Information	Quantity (K)
ADM811LART-REEL	4.63	–40°C to +85°C	MBV	10
ADM811LART-REEL-7	4.63	–40°C to +85°C	MBV	3
ADM811MART-REEL	4.38	–40°C to +85°C	MBT	10
ADM811MART-REEL-7	4.38	–40°C to +85°C	MBT	3
ADM811TART-REEL	3.08	–40°C to +85°C	MBG	10
ADM811TART-REEL-7	3.08	–40°C to +85°C	MBG	3
ADM811-3TART-REEL	3.08	–40°C to +85°C	MB3	10
ADM811-3TART-REEL-7	3.08	–40°C to +85°C	MB3	3
ADM811SART-REEL	2.93	–40°C to +85°C	MBE	10
ADM811SART-REEL-7	2.93	–40°C to +85°C	MBE	3
ADM811RART-REEL	2.63	–40°C to +85°C	MBB	10
ADM811RART-REEL-7	2.63	–40°C to +85°C	MBB	3
ADM811ZART-REEL	2.32	–40°C to +85°C	MBZ	10
ADM811ZART-REEL-7	2.32	–40°C to +85°C	MBZ	3
ADM812LART-REEL	4.63	–40°C to +85°C	MCV	10
ADM812LART-REEL-7	4.63	–40°C to +85°C	MCV	3
ADM812MART-REEL	4.38	–40°C to +85°C	MCT	10
ADM812MART-REEL-7	4.38	–40°C to +85°C	MCT	3
ADM812TART-REEL	3.08	–40°C to +85°C	MCG	10
ADM812TART-REEL-7	3.08	–40°C to +85°C	MCG	3
ADM812SART-REEL	2.93	–40°C to +85°C	MCE	10
ADM812SART-REEL-7	2.93	–40°C to +85°C	MCE	3
ADM812RART-REEL	2.63	–40°C to +85°C	MCB	10
ADM812RART-REEL-7	2.63	–40°C to +85°C	MCB	3
ADM812ZART-REEL	2.32	–40°C to +85°C	MCZ	10
ADM812ZART-REEL-7	2.32	–40°C to +85°C	MCZ	3

*Only available in reels.

CAUTION

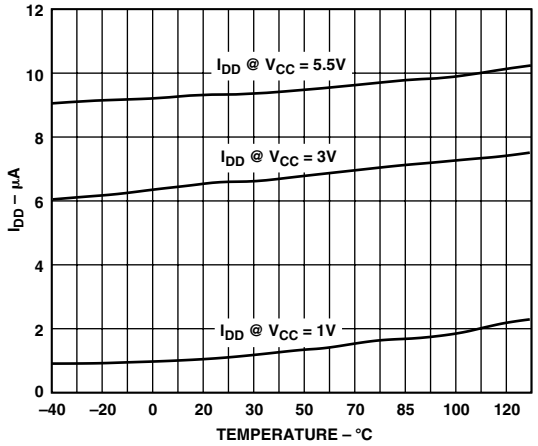
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADM811/ADM812 feature proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION

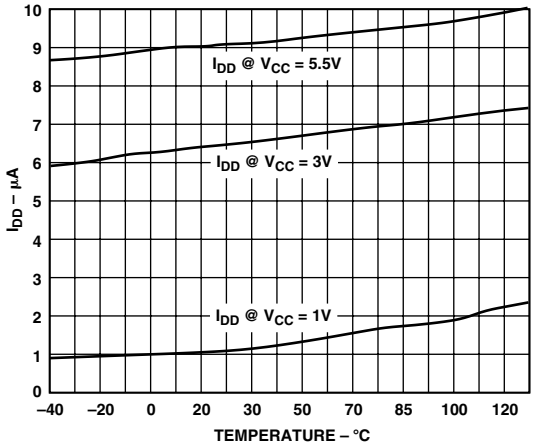


PIN FUNCTION DESCRIPTIONS

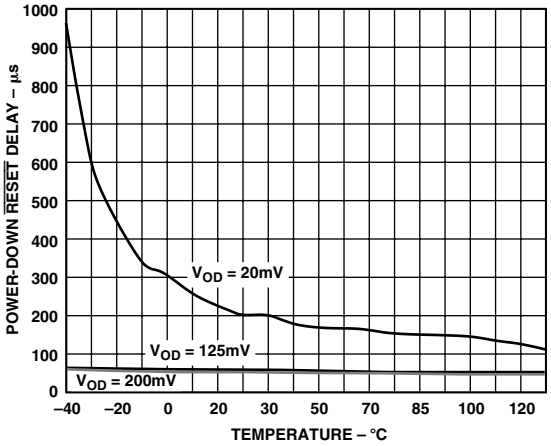
Pin	Mnemonic	Function
1	GND	0 V. Ground reference for all signals.
2	$\overline{RESET}$ (ADM811)	Active Low Logic Output. $\overline{RESET}$ remains low while V_{CC} is below the reset threshold or when $\overline{MR}$ is low; $\overline{RESET}$ then remains low for at least 140 ms (at least 300 ms for the ADM811-3T) after V_{CC} rises above the reset threshold.
	RESET (ADM812)	Active High Logic Output. RESET remains high while V_{CC} is below the reset threshold or when $\overline{MR}$ is low; RESET then remains high for 240 ms (typical) after V_{CC} rises above the reset threshold.
3	$\overline{MR}$	Manual Reset. This active low debounced input will ignore input pulses of 100 ns or less (typical) and is guaranteed to accept input pulses of greater than 10 μs. Leave floating when not used.
4	V_{CC}	2.5 V, 3 V, 3.3 V, or 5 V Monitored Supply Voltage.



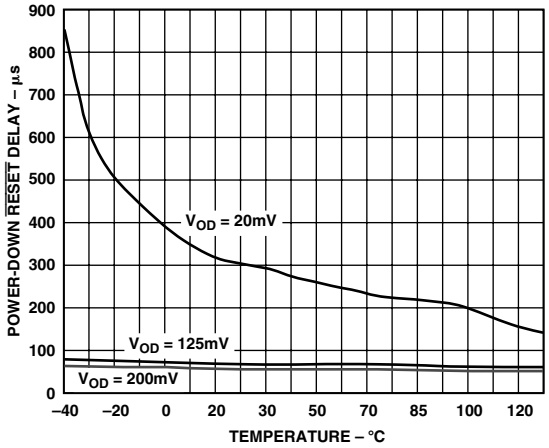
TPC 1. Supply Current vs. Temperature (ADM81_R/S/T/Z)



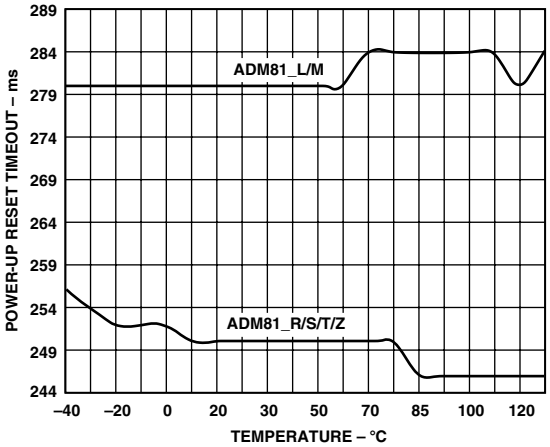
TPC 4. Supply Current vs. Temperature (ADM81_L/M)



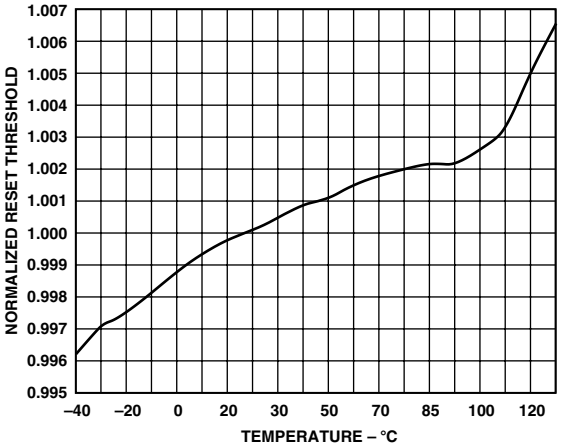
TPC 2. Power-Down $\overline{RESET}$ Delay vs. Temperature (ADM81_R/S/T/Z)



TPC 5. Power-Down $\overline{RESET}$ Delay vs. Temperature (ADM81_L/M)



TPC 3. Power-Up Reset Timeout vs. Temperature



TPC 6. Reset Threshold Deviation vs. Temperature

CIRCUIT INFORMATION

Reset Thresholds

A reset output is provided to the microprocessor whenever the V_{CC} input is below the reset threshold. The actual reset threshold is dependent on whether an L, M, T, S, R, or Z suffix is used. Refer to Table I.

Table I. Reset Threshold Options

Model	Reset Threshold (V)
ADM811LART	4.63
ADM811MART	4.38
ADM811TART	3.08
ADM811-3TART	3.08
ADM811SART	2.93
ADM811RART	2.63
ADM811ZART	2.32
ADM812LART	4.63
ADM812MART	4.38
ADM812TART	3.08
ADM812SART	2.93
ADM812RART	2.63
ADM812ZART	2.32

RESET OUTPUT

On power-up and after V_{CC} rises above the reset threshold, an internal timer holds the reset output active for 240 ms (typical). This is intended as a power-on reset signal for the processor. It allows time for both the power supply and the microprocessor to stabilize after power-up. If a power supply brownout or interruption occurs, the reset output is similarly activated and remains active for 240 ms (typical) after the supply recovers. This allows time for the power supply and microprocessor to stabilize.

The ADM811 provides an active low reset output ($\overline{\text{RESET}}$) while the ADM812 provides an active high output (RESET).

During power-down of the ADM811, the $\overline{\text{RESET}}$ output remains valid (low) with V_{CC} as low as 1 V. This ensures that the microprocessor is held in a stable shutdown condition as the supply falls and also ensures that no spurious activity can occur via the microprocessor as it powers up.

MANUAL RESET

The ADM811/ADM812 is equipped with a manual reset input. This input is designed to operate in a noisy environment where unwanted glitches could be induced. These glitches could be produced by the bouncing action of a switch contact, or where a manual reset switch may be located some distance away from the circuit (the cabling of which may pick-up noise).

The manual reset input is guaranteed to ignore logically valid inputs that are faster than 100 ns and to accept inputs longer in duration than 10 μs.

Glitch Immunity

The ADM811/ADM812 contains internal filtering circuitry providing glitch immunity from fast transient glitches on the power supply line.

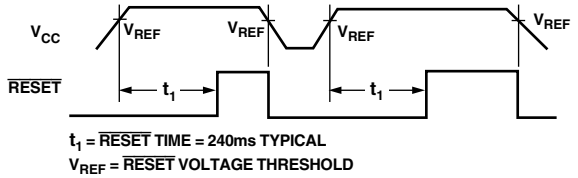


Figure 2. Power Fail $\overline{\text{RESET}}$ Timing

INTERFACING TO OTHER DEVICES

Output

The ADM811/ADM812 is designed to integrate with as many devices as possible. One feature of the ADM811/ADM812 is the reset output, which is directly proportional to V_{CC} (this is guaranteed only while V_{CC} is greater than 1 V). This enables the part to be used with both 3 V and 5 V, or any nominal voltage within the minimum and maximum specifications for V_{CC}.

BENEFITS OF A VERY ACCURATE RESET THRESHOLD

Because the ADM811/ADM812 can operate effectively even when there are large degradations of the supply voltages, the possibility of a malfunction during a power failure is greatly reduced. Another advantage of the ADM811/ADM812 is its very accurate internal voltage reference circuit. Combined, these benefits produce an exceptionally reliable microprocessor supervisory circuit.

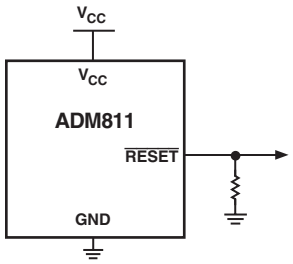


Figure 3. Ensuring a Valid $\overline{\text{RESET}}$ Output Down to V_{CC} = 0 V

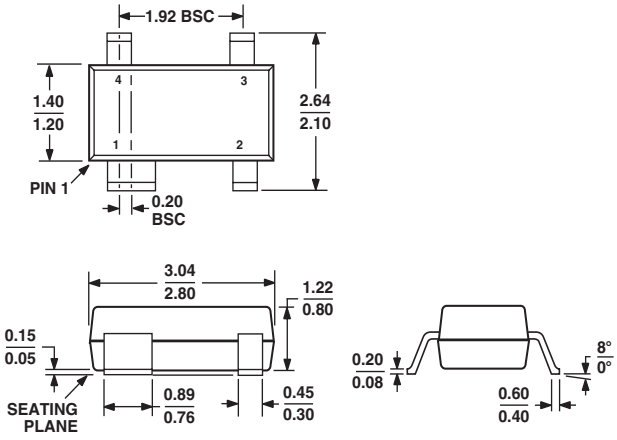
ENSURING A VALID RESET OUTPUT DOWN TO V_{CC} = 0 V

When V_{CC} falls below 0.8 V, the ADM811/ADM812's $\overline{\text{RESET}}$ no longer sinks current. Therefore, a high impedance CMOS logic input connected to $\overline{\text{RESET}}$ may drift to undetermined logic levels. To eliminate this problem, a 100 kΩ resistor should be connected from $\overline{\text{RESET}}$ to ground.

OUTLINE DIMENSIONS

4-Lead Small Outline Transistor Package [SOT-143]
(RT-4)

Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS TO-253D

Revision History

Location	Page
2/03—Data Sheet changed from REV. B to REV. C.	
Changes FEATURES	1
Changes to GENERAL DESCRIPTION	1
Changes to SPECIFICATIONS	2
Removed Note 2 from ORDERING GUIDE	3
Changes to PIN FUNCTION DESCRIPTIONS	4
Removed Note from Table I	6
1/03—Data Sheet changed from REV. A to REV. B.	
Added ADM812	Universal
Changes SPECIFICATIONS	2
Changes to ORDERING GUIDE	3
Changes to PIN CONFIGURATION	4
Changes to PIN FUNCTION DESCRIPTIONS	4
Additions to Table I	6
Changes to Manual Reset section	6
5/02—Data Sheet changed from REV. 0 to REV. A.	
Deletion of ADM812	Universal

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