

S25FL128P

128 Megabit CMOS 3.0 Volt Flash Memory
with 104-MHz SPI (Serial Peripheral Interface) Bus

Data Sheet (Preliminary)



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Data Sheet (Preliminary)



Distinctive Characteristics

Architectural Advantages

- **Single power supply operation**
 - Full voltage range: 2.7 to 3.6 V read and program operations
- **Memory Architecture**
 - 128Mb uniform 256 KB sector product
 - 128Mb uniform 64 KB sector product
- **Program**
 - Page Program (up to 256 bytes) in 1.5 ms (typical)
 - Faster program time in Accelerated Programming mode (8.5 V–9.5 V on #WP/ACC) in 1.2 ms (typical)
- **Erase**
 - 2 s typical 256 KB sector erase time
 - 0.5 s typical 64 KB sector erase time
 - 128 s typical bulk erase time
 - Sector erase (SE) command (D8h) for 256 KB sectors; (20h or D8h) for 64KB sectors
 - Bulk erase command (C7h) for 256 KB sectors; (60h or C7h) for 64KB sectors
- **Cycling Endurance**
 - 100,000 cycles per sector typical
- **Data Retention**
 - 20 years typical
- **Device ID**
 - RDID (9Fh), READ_ID (90h) and RES (ABh) commands to read manufacturer and device ID information
 - RES command one-byte electronic signature for backward compatibility

Process Technology

- Manufactured on 0.09 μm MirrorBit[®] process technology

Package Option

- Industry Standard Pinouts
- 16-pin SO package (300 mils)
- 8-Contact WSON Package (6 x 8 mm)

Performance Characteristics

- **Speed**
 - 104 MHz clock rate (maximum)
- **Power Saving Standby Mode**
 - Standby Mode 200 μA (max)
 - Deep Power Down Mode 3 μA (typical)

Memory Protection Features

- **Memory Protection**
 - WP#/ACC pin works in conjunction with Status Register Bits to protect specified memory areas
 - 256 KB uniform sector product: Status Register Block Protection bits (BP2, BP1, BP0) in status register configure parts of memory as read-only.
 - 64KB uniform sector product: Status Register Block Protection bits (BP3, BP2, BP1, BP0) in status register configure parts of memory as read-only

Software Features

- SPI Bus Compatible Serial Interface

Hardware Features

- **x8 Parallel Programming Mode (for 16-pin SO package only)**

General Description

The S25FL128P is a 3.0 Volt (2.7 V to 3.6 V), single-power-supply Flash memory device. The device consists of 64 sectors of 256 KB memory, or 256 sectors of 64 KB memory.

The device accepts data written to SI (Serial Input) and outputs data on SO (Serial Output). The devices are designed to be programmed in-system with the standard system 3.0 volt V_{CC} supply.

The memory can be programmed 1 to 256 bytes at a time, using the Page Program command. The device supports Sector Erase and Bulk Erase commands.

Each device requires only a 3.0 volt power supply (2.7 V to 3.6 V) for both read and write functions. Internally generated and regulated voltages are provided for the program operations. This device requires a high voltage supply to WP#/ACC pin for the Accelerated Programming mode.

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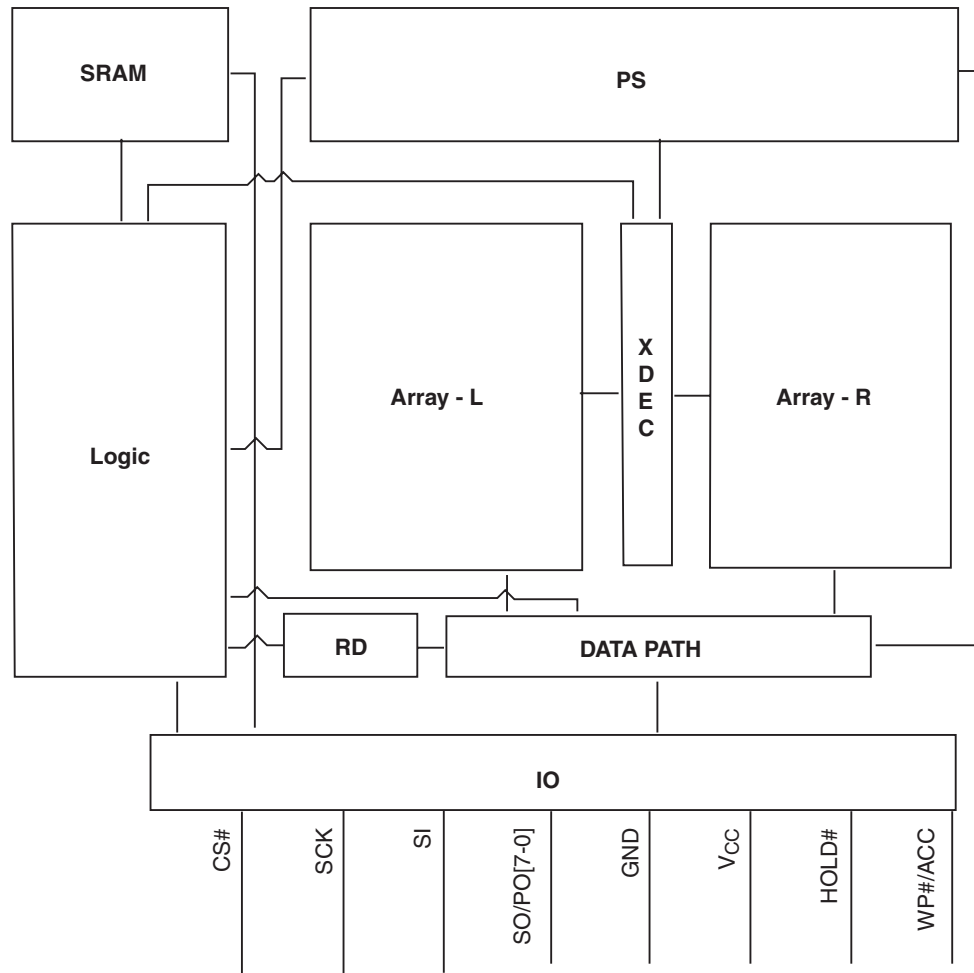
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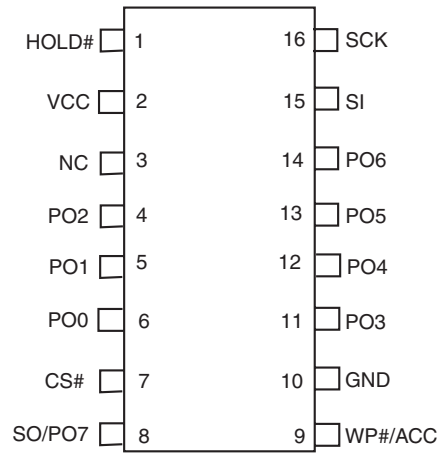
1. Block Diagram



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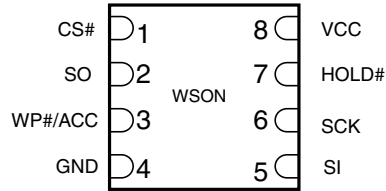
2. Connection Diagrams

Figure 2.1 16-pin Plastic Small Outline Package (SO)



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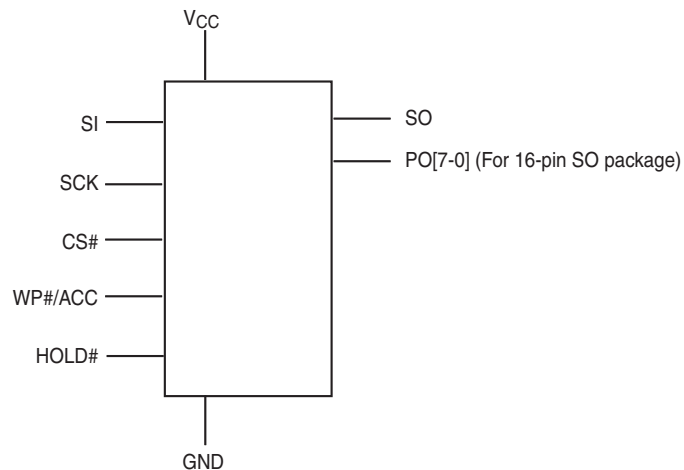
Figure 2.2 8-Pin WSON Package (6 x 8 mm)



3. Input/Output Descriptions

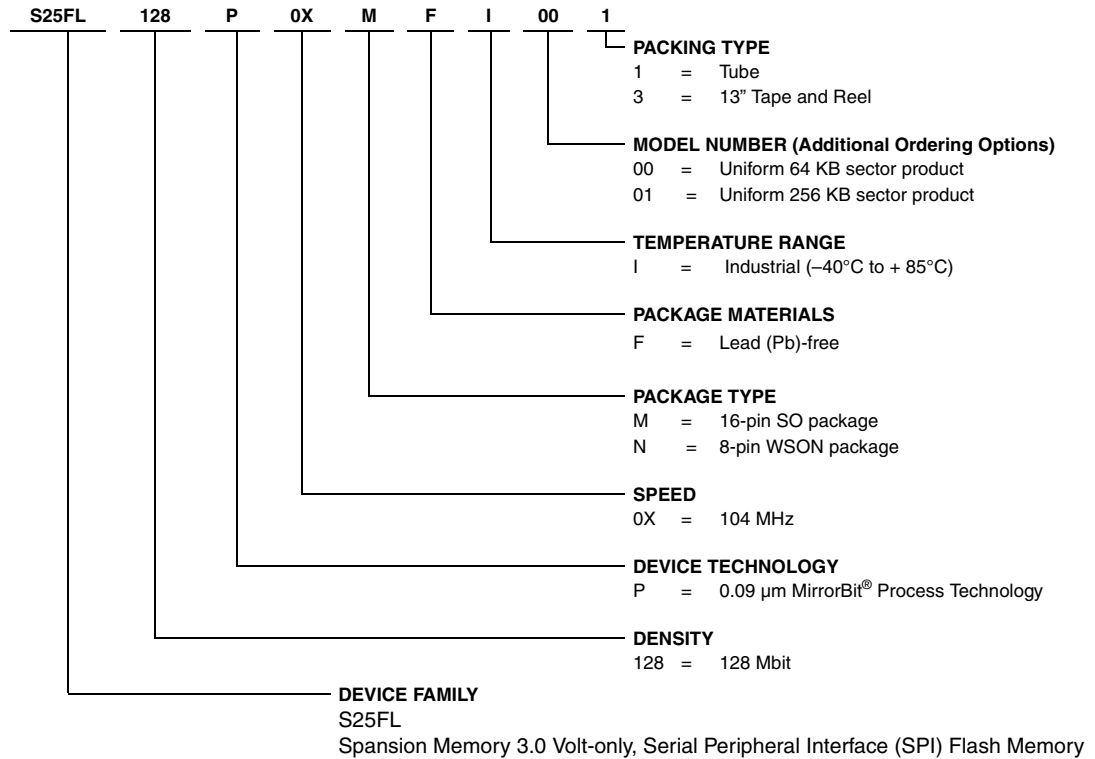
| Signal Name | I/O | Description |
|--|--------------|--|
| SO (Signal Data Output) | Output | Transfers data serially out of the device on the falling edge of SCK. |
| PO[7-0] (Parallel Data Input/Output) | Input/Output | Transfers parallel data into the device on the rising edge of SCK or out of the device on the falling edge of SCK. |
| SI (Serial Data Input) | Input | Transfers data serially into the device. Device latches commands, addresses, and program data on SI on the rising edge of SCK. |
| SCK (Serial Clock) | Input | Provides serial interface timing. Latches commands, addresses, and data on SI on rising edge of SCK. Triggers output on SO after the falling edge of SCK. |
| CS# (Chip Select) | Input | Places device in active power mode when driven low. Deselects device and places SO at high impedance when high. After power-up, device requires a falling edge on CS# before any command is written. Device is in standby mode when a program, erase, or Write Status Register operation is not in progress. |
| HOLD# (Hold) | Input | Pauses any serial communication with the device without deselecting it. When driven low, SO is at high impedance, and all input at SI and SCK are ignored. Requires that CS# also be driven low. |
| WP#/ACC (Write Protect/Accelerated Programming) | Input | When driven low, prevents any program or erase command from altering the data in the protected memory area specified by Status Register bits (BP bits). If the system asserts V_{HH} on this pin, accelerated programming operation is provided. |
| V_{CC} | Input | Supply Voltage |
| GND | Input | Ground |

4. Logic Symbol



5. Ordering Information

The ordering part number is formed by a valid combination of the following:



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Table 5.1 S25FL128P Valid Combinations Table

| S25FL128P Valid Combinations | | | | | Package Marking (See Note) |
|------------------------------|--------------|-----------------------|--------------|--------------|-------------------------------|
| Base Ordering Part Number | Speed Option | Package & Temperature | Model Number | Packing Type | |
| S25FL128P | 0X | MFI, NFI | 00 | 1, 3 | FL128P + I + F |
| | | | 01 | | FL128P + I + FL |

Note

Package marking omits leading "S25" and speed, package, and model number form.

5.1 Valid Combinations

Table 5.1 lists the valid combinations configurations planned to be supported in volume for this device.

6. Spansion SPI Modes

A microcontroller can use either of its two SPI modes to control Spansion SPI Flash memory devices:

- CPOL = 0, CPHA = 0 (Mode 0)
- CPOL = 1, CPHA = 1 (Mode 3)

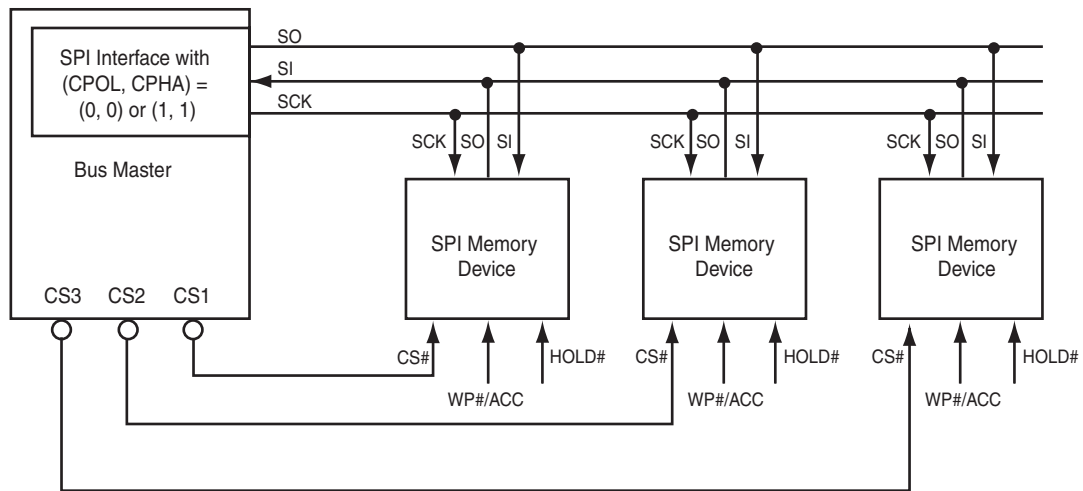
Input data is latched in on the rising edge of SCK, and output data is available from the falling edge of SCK for both modes.

When the bus master is in standby mode, SCK is as shown in [Figure 6.2](#) for each of the two modes:

- SCK remains at 0 for (CPOL = 0, CPHA = 0 Mode 0)
- SCK remains at 1 for (CPOL = 1, CPHA = 1 Mode 3)

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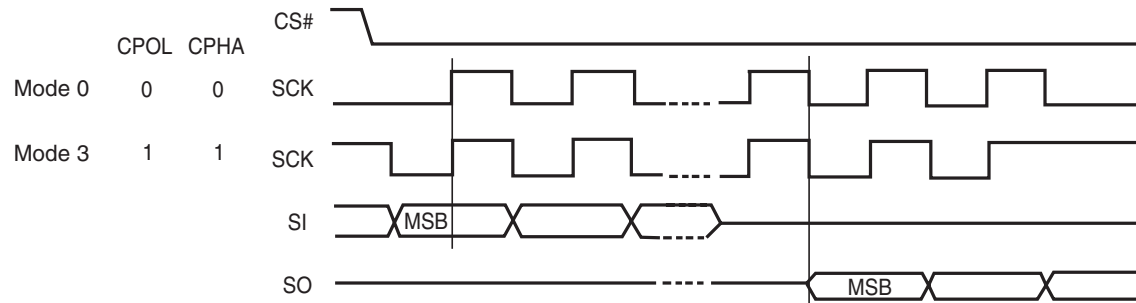
Figure 6.1 Bus Master and Memory Devices on the SPI Bus



Note

The Write Protect/Accelerated Programming (WP#/ACC) and Hold (HOLD#) signals should be driven high (logic level 1) or low (logic level 0) as appropriate.

Figure 6.2 SPI Modes Supported



7. Device Operations

All Spansion SPI devices (S25FL-P) accept and output data in bytes (8 bits at a time).

7.1 Byte or Page Programming

Programming data requires two commands: Write Enable (WREN), which is one byte, and a Page Program (PP) sequence, which consists of four bytes plus data. The Page Program sequence accepts from 1 byte up to 256 consecutive bytes of data (which is the size of one page) to be programmed in one operation. Programming means that bits can either be left at 0, or programmed from 1 to 0. Changing bits from 0 to 1 requires an erase operation. Before this can be applied, the bytes of the memory need to be first erased to all 1's (FFh) before any programming.

7.2 Sector Erase / Bulk Erase

The Sector Erase (SE) and Bulk Erase (BE) commands set all the bits in a sector or the entire memory array to 1. While bits can be individually programmed from a 1 to 0, erasing bits from 0 to 1 must be done on a sector-wide (SE) or array-wide (BE) level. Before this can be applied, the memory array need to be first erased to all 1's (FFh) before any programming.

7.3 Monitoring Write Operations Using the Status Register

The host system can determine when a Write Status Register, program, or erase operation is complete by monitoring the Write in Progress (WIP) bit in the Status Register. The Read from Status Register command provides the state of the WIP bit.

7.4 Active Power and Standby Power Modes

The device is enabled and in the Active Power mode when Chip Select (CS#) is Low. When CS# is high, the device is disabled, but may still be in the Active Power mode until all program, erase, and Write Status Register operations have completed. The device then goes into the Standby Power mode, and power consumption drops to I_{SB} . The Deep Power Down (DP) command provides additional data protection against inadvertent signals. After writing the DP command, the device ignores any further program or erase commands, and reduces its power consumption to I_{DP} .

7.5 Status Register

The Status Register contains the status and control bits that can be read or set by specific commands (see Table [Table 11.6, Command Definitions on page 38](#)):

- **Write In Progress (WIP):** Indicates whether the device is performing a Write Status Register, program or erase operation.
- **Write Enable Latch (WEL):** Indicates the status of the internal Write Enable Latch.
- **Block Protect (BP2, BP1, BP0 for uniform 256 KB sector product: BP3, BP2, BP1, BP0 for uniform 64 KB sector product):** Non-volatile bits that define memory area to be software-protected against program and erase commands.
- **Status Register Write Disable (SRWD):** Places the device in the Hardware Protected mode when this bit is set to 1 and the WP#/ACC input is driven low. In this mode, the non-volatile bits of the Status Register (SRWD, BP3, BP2, BP1, BP0) become read-only bits.

7.6 Data Protection Modes

Spansion SPI Flash memory devices provide the following data protection methods:

- **The Write Enable (WREN) command:** Must be written prior to any command that modifies data. The WREN command sets the Write Enable Latch (WEL) bit. The WEL bit resets (disables writes) on *power-up* or after the device completes the following *commands*:
 - Page Program (PP)

- Sector Erase (SE)
- Bulk Erase (BE)
- Write Disable (WRDI)
- Write Status Register (WRSR)

- **Software Protected Mode (SPM):** The Block Protect (BP2, BP1, BP0 for uniform 256 KB sector product; BP3, BP2, BP1, BP0 for uniform 64 KB sector product) bits define the section of the memory array that can be read but not programmed or erased. Table 7.1 shows the sizes and address ranges of protected areas that are defined by Status Register bits BP2:BP0 for uniform 256 KB sector product, BP3:BP0 for uniform 64 KB sector product).
- **Hardware Protected Mode (HPM):** The Write Protect (WP#/ACC) input and the Status Register Write Disable (SRWD) bit together provide write protection.
- **Clock Pulse Count:** The device verifies that all program, erase, and Write Status Register commands consist of a clock pulse count that is a multiple of eight before executing them.

Table 7.1 S25FL128P Protected Area Sizes (Uniform 256 KB sector)

| Status Register Block Protect Bits | | | Memory Array | | | | Protected Portion of Total Memory Area |
|------------------------------------|-----|-----|-------------------------|-------------------|---------------------------|---------------------|--|
| BP2 | BP1 | BP0 | Protected Address Range | Protected Sectors | Unprotected Address Range | Unprotected Sectors | |
| 0 | 0 | 0 | None | (0) | 000000h-FFFFFFh | (64) SA63:SA0 | 0 |
| 0 | 0 | 1 | FC0000h-FFFFFFh | (1) SA63 | 000000h-FBFFFFh | (32) SA62:SA0 | 1/64 |
| 0 | 1 | 0 | F80000h-FFFFFFh | (2) SA63:SA62 | 000000h-F7FFFFh | (16) SA61:SA0 | 1/32 |
| 0 | 1 | 1 | F00000h-FFFFFFh | (4) SA63:SA60 | 000000h-EFFFFFh | (8) SA59:SA0 | 1/16 |
| 1 | 0 | 0 | E00000h-FFFFFFh | (8) SA63:SA56 | 000000h-DFFFFFh | (4) SA55:SA0 | 1/8 |
| 1 | 0 | 1 | C00000h-FFFFFFh | (16) SA63:SA48 | 000000h-BFFFFFh | (2) SA47:SA0 | 1/4 |
| 1 | 1 | 0 | 800000h-FFFFFFh | (32) SA63:SA32 | 000000h-7FFFFFh | (1) SA31:SA0 | 1/2 |
| 1 | 1 | 1 | 000000h-FFFFFFh | (64) SA63:SA0 | None | (0) | All |

Table 7.2 S25FL128P Protected Area Sizes (Uniform 64 KB sector)

| Status Register Block Protect Bits | | | | Memory Array | | | | Protected Portion of Total Memory Area |
|------------------------------------|-----|-----|-----|-------------------------|-------------------|---------------------------|---------------------|--|
| BP3 | BP2 | BP1 | BP0 | Protected Address Range | Protected Sectors | Unprotected Address Range | Unprotected Sectors | |
| 0 | 0 | 0 | 0 | None | (0) | 000000h-FFFFFFh | (256) SA255:SA0 | 0 |
| 0 | 0 | 0 | 1 | FE0000h-FFFFFFh | (2) SA255:SA254 | 000000h-FDFFFFh | (128) SA253:SA0 | 1/128 |
| 0 | 0 | 1 | 0 | FC0000h-FFFFFFh | (4) SA255:SA252 | 000000h-FBFFFFh | (64) SA251:SA0 | 1/64 |
| 0 | 0 | 1 | 1 | F80000h-FFFFFFh | (8) SA255:SA248 | 000000h-F7FFFFh | (32) SA247:SA0 | 1/32 |
| 0 | 1 | 0 | 0 | F00000h-FFFFFFh | (16) SA255:SA240 | 000000h-EFFFFFh | (16) SA239:SA0 | 1/16 |
| 0 | 1 | 0 | 1 | E00000h-FFFFFFh | (32) SA255:SA224 | 000000h-DFFFFFh | (8) SA223:SA0 | 1/8 |
| 0 | 1 | 1 | 0 | C00000h-FFFFFFh | (64) SA255:SA192 | 000000h-BFFFFFh | (4) SA191:SA0 | 1/4 |
| 0 | 1 | 1 | 1 | 800000h-FFFFFFh | (128) SA255:SA128 | 000000h-7FFFFFh | (2) SA127:SA0 | 1/2 |
| 1 | 0 | 0 | 0 | 000000h-FFFFFFh | (256) SA255:SA0 | None | (0) | All |
| 1 | 0 | 0 | 1 | 000000h-FFFFFFh | (256) SA255:SA0 | None | (0) | All |
| 1 | 0 | 1 | 0 | 000000h-FFFFFFh | (256) SA255:SA0 | None | (0) | All |
| 1 | 0 | 1 | 1 | 000000h-FFFFFFh | (256) SA255:SA0 | None | (0) | All |
| 1 | 1 | 0 | 0 | 000000h-FFFFFFh | (256) SA255:SA0 | None | (0) | All |
| 1 | 1 | 0 | 1 | 000000h-FFFFFFh | (256) SA255:SA0 | None | (0) | All |
| 1 | 1 | 1 | 0 | 000000h-FFFFFFh | (256) SA255:SA0 | None | (0) | All |
| 1 | 1 | 1 | 1 | 000000h-FFFFFFh | (256) SA255:SA0 | None | (0) | All |

7.7 Hold Mode (HOLD#)

The Hold input (HOLD#) stops any serial communication with the device, but does not terminate any Write Status Register, program or erase operation that is currently in progress.

The Hold mode starts on the falling edge of HOLD# if SCK is also low (see [Figure 7.1 on page 14](#), standard use). If the falling edge of HOLD# does not occur while SCK is low, the Hold mode begins after the next falling edge of SCK (non-standard use).

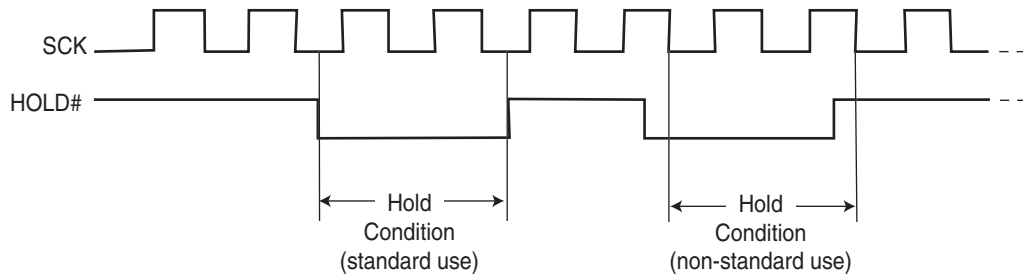
The Hold mode ends on the rising edge of HOLD# signal (standard use) if SCK is also low. If the rising edge of HOLD# does not occur while SCK is low, the Hold mode ends on the next falling edge of CLK (non-standard use) See [Figure 7.1](#).

The SO output is high impedance, and the SI and SCK inputs are ignored (don't care) for the duration of the Hold mode.

CS# must remain low for the entire duration of the Hold mode to ensure that the device internal logic remains unchanged. If CS# goes high while the device is in the Hold mode, the internal logic is reset. To prevent the device from reverting to the Hold mode when device communication is resumed, HOLD# must be held high, followed by driving CS# low.

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Figure 7.1 Hold Mode Operation



8. Sector Address Table

[Table 8.1](#) shows the size of the memory array, sectors, and pages. The device uses *pages* to cache the program data before the data is programmed into the memory array. Each page or byte can be individually programmed (bits are changed from 1 to 0). The data is erased (bits are changed from 0 to 1) on a sector- or device-wide basis using the SE or BE commands. [Table 8.2](#) shows the starting and ending address for each sector. The complete set of sectors comprises the memory array of the Flash device.

Table 8.1 S25FL128P Device Organization

| Each Device has | Each Sector has | Each Page has | |
|--|--|---------------|---------|
| 16,777,216 | 262144 (256 KB sector) 65536 (64 KB sector) | 256 | bytes |
| 65,536 | 1024 (256 KB sector) 256 (64 KB sector) | — | pages |
| 64 (256 KB sector) 256 (64 KB sector) | — | — | sectors |

Table 8.2 S25FL128P Sector Address Table (Uniform 256 KB sector)

| Sector | Address Range | | Sector | Address Range | |
|--------|---------------|----------|--------|---------------|----------|
| 63 | FC0000h | FFFFFFh | 31 | 7C0000h | 7FFFFFFh |
| 62 | F80000h | FBFFFFh | 30 | 780000h | 7BFFFFh |
| 61 | F40000h | F7FFFFh | 29 | 740000h | 77FFFFh |
| 60 | F00000h | F3FFFFh | 28 | 700000h | 73FFFFh |
| 59 | EC0000h | EFFFFFFh | 27 | 6C0000h | 6FFFFFFh |
| 58 | E80000h | EBFFFFh | 26 | 680000h | 6BFFFFh |
| 57 | E40000h | E7FFFFh | 25 | 640000h | 67FFFFh |
| 56 | E00000h | E3FFFFh | 24 | 600000h | 63FFFFh |
| 55 | DC0000h | DFFFFFFh | 23 | 5C0000h | 5FFFFFFh |
| 54 | D80000h | DBFFFFh | 22 | 580000h | 5BFFFFh |
| 53 | D40000h | D7FFFFh | 21 | 540000h | 57FFFFh |
| 52 | D00000h | D3FFFFh | 20 | 500000h | 53FFFFh |
| 51 | CC0000h | CFFFFFFh | 19 | 4C0000h | 4FFFFFFh |
| 50 | C80000h | CBFFFFh | 18 | 480000h | 4BFFFFh |
| 49 | C40000h | C7FFFFh | 17 | 440000h | 47FFFFh |
| 48 | C00000h | C3FFFFh | 16 | 400000h | 43FFFFh |
| 47 | BC0000h | BFFFFFFh | 15 | 3C0000h | 3FFFFFFh |
| 46 | B80000h | BBFFFFh | 14 | 380000h | 3BFFFFh |
| 45 | B40000h | B7FFFFh | 13 | 340000h | 37FFFFh |
| 44 | B00000h | B3FFFFh | 12 | 300000h | 33FFFFh |
| 43 | AC0000h | AFFFFFFh | 11 | 2C0000h | 2FFFFFFh |
| 42 | A80000h | ABFFFFh | 10 | 280000h | 2BFFFFh |
| 41 | A40000h | A7FFFFh | 9 | 240000h | 27FFFFh |
| 40 | A00000h | A3FFFFh | 8 | 200000h | 23FFFFh |
| 39 | 9C0000h | 9FFFFFFh | 7 | 1C0000h | 1FFFFFFh |
| 38 | 980000h | 9BFFFFh | 6 | 180000h | 1BFFFFh |
| 37 | 940000h | 97FFFFh | 5 | 140000h | 17FFFFh |
| 36 | 900000h | 93FFFFh | 4 | 100000h | 13FFFFh |
| 35 | 8C0000h | 8FFFFFFh | 3 | 0C0000h | 0FFFFFFh |
| 34 | 880000h | 8BFFFFh | 2 | 080000h | 0BFFFFh |
| 33 | 840000h | 87FFFFh | 1 | 040000h | 07FFFFh |
| 32 | 800000h | 83FFFFh | 0 | 000000h | 03FFFFh |

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Table 8.3 S25FL128P Sector Address Table (Uniform 64 KB sector) (Sheet 1 of 2)

| Sector | Address Range | | Sector | Address Range | | Sector | Address Range | |
|--------|---------------|---------|--------|---------------|----------|--------|---------------|----------|
| 255 | FF0000h | FFFFFFh | 207 | CF0000h | CFFFFFFh | 159 | 9F0000h | 9FFFFFFh |
| 254 | FE0000h | FEFFFFh | 206 | CE0000h | CEFFFFh | 158 | 9E0000h | 9EFFFFh |
| 253 | FD0000h | FDFFFFh | 205 | CD0000h | CDFFFFh | 157 | 9D0000h | 9DFFFFh |
| 252 | FC0000h | FCFFFFh | 204 | CC0000h | CCFFFFh | 156 | 9C0000h | 9CFFFFh |
| 251 | FB0000h | FBFFFFh | 203 | CB0000h | CBFFFFh | 155 | 9B0000h | 9BFFFFh |
| 250 | FA0000h | FAFFFFh | 202 | CA0000h | CAFFFFh | 154 | 9A0000h | 9AFFFFh |
| 249 | F90000h | F9FFFFh | 201 | C90000h | C9FFFFh | 153 | 990000h | 99FFFFh |
| 248 | F80000h | F8FFFFh | 200 | C80000h | C8FFFFh | 152 | 980000h | 98FFFFh |
| 247 | F70000h | F7FFFFh | 199 | C70000h | C7FFFFh | 151 | 970000h | 97FFFFh |
| 246 | F60000h | F6FFFFh | 198 | C60000h | C6FFFFh | 150 | 960000h | 96FFFFh |
| 245 | F50000h | F5FFFFh | 197 | C50000h | C5FFFFh | 149 | 950000h | 95FFFFh |
| 244 | F40000h | F4FFFFh | 196 | C40000h | C4FFFFh | 148 | 940000h | 94FFFFh |
| 243 | F30000h | F3FFFFh | 195 | C30000h | C3FFFFh | 147 | 930000h | 93FFFFh |
| 242 | F20000h | F2FFFFh | 194 | C20000h | C2FFFFh | 146 | 920000h | 92FFFFh |
| 241 | F10000h | F1FFFFh | 193 | C10000h | C1FFFFh | 145 | 910000h | 91FFFFh |
| 240 | F00000h | F0FFFFh | 192 | C00000h | C0FFFFh | 144 | 900000h | 90FFFFh |
| 239 | EF0000h | EFFFFFh | 191 | BF0000h | BFFFFFFh | 143 | 8F0000h | 8FFFFFFh |
| 238 | EE0000h | EEFFFFh | 190 | BE0000h | BEFFFFh | 142 | 8E0000h | 8EFFFFh |
| 237 | ED0000h | EDFFFFh | 189 | BD0000h | BDFFFFh | 141 | 8D0000h | 8DFFFFh |
| 236 | EC0000h | ECFFFFh | 188 | BC0000h | BCFFFFh | 140 | 8C0000h | 8CFFFFh |
| 235 | EB0000h | EBFFFFh | 187 | BB0000h | BBFFFFh | 139 | 8B0000h | 8BFFFFh |
| 234 | EA0000h | EAFFFFh | 186 | BA0000h | BAFFFFh | 138 | 8A0000h | 8AFFFFh |
| 233 | E90000h | E9FFFFh | 185 | B90000h | B9FFFFh | 137 | 890000h | 89FFFFh |
| 232 | E80000h | E8FFFFh | 184 | B80000h | B8FFFFh | 136 | 880000h | 88FFFFh |
| 231 | E70000h | E7FFFFh | 183 | B70000h | B7FFFFh | 135 | 870000h | 87FFFFh |
| 230 | E60000h | E6FFFFh | 182 | B60000h | B6FFFFh | 134 | 860000h | 86FFFFh |
| 229 | E50000h | E5FFFFh | 181 | B50000h | B5FFFFh | 133 | 850000h | 85FFFFh |
| 228 | E40000h | E4FFFFh | 180 | B40000h | B4FFFFh | 132 | 840000h | 84FFFFh |
| 227 | E30000h | E3FFFFh | 179 | B30000h | B3FFFFh | 131 | 830000h | 83FFFFh |
| 226 | E20000h | E2FFFFh | 178 | B20000h | B2FFFFh | 130 | 820000h | 82FFFFh |
| 225 | E10000h | E1FFFFh | 177 | B10000h | B1FFFFh | 129 | 810000h | 81FFFFh |
| 224 | E00000h | E0FFFFh | 176 | B00000h | B0FFFFh | 128 | 800000h | 80FFFFh |
| 223 | DF0000h | DFFFFFh | 175 | AF0000h | AFFFFFFh | 127 | 7F0000h | 7FFFFFFh |
| 222 | DE0000h | DEFFFFh | 174 | AE0000h | AFFFFFFh | 126 | 7E0000h | 7EFFFFh |
| 221 | DD0000h | DDFFFFh | 173 | AD0000h | ADFFFFh | 125 | 7D0000h | 7DFFFFh |
| 220 | DC0000h | DCFFFFh | 172 | AC0000h | ACFFFFh | 124 | 7C0000h | 7CFFFFh |
| 219 | DB0000h | DBFFFFh | 171 | AB0000h | ABFFFFh | 123 | 7B0000h | 7BFFFFh |
| 218 | DA0000h | DAFFFFh | 170 | AA0000h | AAFFFFh | 122 | 7A0000h | 7AFFFFh |
| 217 | D90000h | D9FFFFh | 169 | A90000h | A9FFFFh | 121 | 790000h | 79FFFFh |
| 216 | D80000h | D8FFFFh | 168 | A80000h | A8FFFFh | 120 | 780000h | 78FFFFh |
| 215 | D70000h | D7FFFFh | 167 | A70000h | A7FFFFh | 119 | 770000h | 77FFFFh |
| 214 | D60000h | D6FFFFh | 166 | A60000h | A6FFFFh | 118 | 760000h | 76FFFFh |
| 213 | D50000h | D5FFFFh | 165 | A50000h | A5FFFFh | 117 | 750000h | 75FFFFh |
| 212 | D40000h | D4FFFFh | 164 | A40000h | A4FFFFh | 116 | 740000h | 74FFFFh |
| 211 | D30000h | D3FFFFh | 163 | A30000h | A3FFFFh | 115 | 730000h | 73FFFFh |
| 210 | D20000h | D2FFFFh | 162 | A20000h | A2FFFFh | 114 | 720000h | 72FFFFh |
| 209 | D10000h | D1FFFFh | 161 | A10000h | A1FFFFh | 113 | 710000h | 71FFFFh |
| 208 | D00000h | D0FFFFh | 160 | A00000h | A0FFFFh | 112 | 700000h | 70FFFFh |

Table 8.3 S25FL128P Sector Address Table (Uniform 64 KB sector) (Sheet 2 of 2)

| Sector | Address Range | | Sector | Address Range | | Sector | Address Range | |
|--------|---------------|-----------|--------|---------------|-----------|--------|---------------|-----------|
| 111 | 6F0000h | 6FFFFFFh | 71 | 470000h | 47FFFFFFh | 31 | 1F0000h | 1FFFFFFh |
| 110 | 6E0000h | 6EFFFFFFh | 70 | 460000h | 46FFFFFFh | 30 | 1E0000h | 1EFFFFFFh |
| 109 | 6D0000h | 6DFFFFFFh | 69 | 450000h | 45FFFFFFh | 29 | 1D0000h | 1DFFFFFFh |
| 108 | 6C0000h | 6CFFFFFFh | 68 | 440000h | 44FFFFFFh | 28 | 1C0000h | 1CFFFFFFh |
| 107 | 6B0000h | 6BFFFFFFh | 67 | 430000h | 43FFFFFFh | 27 | 1B0000h | 1BFFFFFFh |
| 106 | 6A0000h | 6AFFFFFFh | 66 | 420000h | 42FFFFFFh | 26 | 1A0000h | 1AFFFFFFh |
| 105 | 690000h | 69FFFFFFh | 65 | 410000h | 41FFFFFFh | 25 | 190000h | 19FFFFFFh |
| 104 | 680000h | 68FFFFFFh | 64 | 400000h | 40FFFFFFh | 24 | 180000h | 18FFFFFFh |
| 103 | 670000h | 67FFFFFFh | 63 | 3F0000h | 3FFFFFFh | 23 | 170000h | 17FFFFFFh |
| 102 | 660000h | 66FFFFFFh | 62 | 3E0000h | 3EFFFFFFh | 22 | 160000h | 16FFFFFFh |
| 101 | 650000h | 65FFFFFFh | 61 | 3D0000h | 3DFFFFFFh | 21 | 150000h | 15FFFFFFh |
| 100 | 640000h | 64FFFFFFh | 60 | 3C0000h | 3CFFFFFFh | 20 | 140000h | 14FFFFFFh |
| 99 | 630000h | 63FFFFFFh | 59 | 3B0000h | 3BFFFFFFh | 19 | 130000h | 13FFFFFFh |
| 98 | 620000h | 62FFFFFFh | 58 | 3A0000h | 3AFFFFFFh | 18 | 120000h | 12FFFFFFh |
| 97 | 610000h | 61FFFFFFh | 57 | 390000h | 39FFFFFFh | 17 | 110000h | 11FFFFFFh |
| 96 | 600000h | 60FFFFFFh | 56 | 380000h | 38FFFFFFh | 16 | 100000h | 10FFFFFFh |
| 95 | 5F0000h | 5FFFFFFh | 55 | 370000h | 37FFFFFFh | 15 | 0F0000h | 0FFFFFFh |
| 94 | 5E0000h | 5EFFFFFFh | 54 | 360000h | 36FFFFFFh | 14 | 0E0000h | 0EFFFFFFh |
| 93 | 5D0000h | 5DFFFFFFh | 53 | 350000h | 35FFFFFFh | 13 | 0D0000h | 0DFFFFFFh |
| 92 | 5C0000h | 5CFFFFFFh | 52 | 340000h | 34FFFFFFh | 12 | 0C0000h | 0CFFFFFFh |
| 91 | 5B0000h | 5BFFFFFFh | 51 | 330000h | 33FFFFFFh | 11 | 0B0000h | 0BFFFFFFh |
| 90 | 5A0000h | 5AFFFFFFh | 50 | 320000h | 32FFFFFFh | 10 | 0A0000h | 0AFFFFFFh |
| 89 | 590000h | 59FFFFFFh | 49 | 310000h | 31FFFFFFh | 9 | 090000h | 09FFFFFFh |
| 88 | 580000h | 58FFFFFFh | 48 | 300000h | 30FFFFFFh | 8 | 080000h | 08FFFFFFh |
| 87 | 570000h | 57FFFFFFh | 47 | 2F0000h | 2FFFFFFh | 7 | 070000h | 07FFFFFFh |
| 86 | 560000h | 56FFFFFFh | 46 | 2E0000h | 2EFFFFFFh | 6 | 060000h | 06FFFFFFh |
| 85 | 550000h | 55FFFFFFh | 45 | 2D0000h | 2DFFFFFFh | 5 | 050000h | 05FFFFFFh |
| 84 | 540000h | 54FFFFFFh | 44 | 2C0000h | 2CFFFFFFh | 4 | 040000h | 04FFFFFFh |
| 83 | 530000h | 53FFFFFFh | 43 | 2B0000h | 2BFFFFFFh | 3 | 030000h | 03FFFFFFh |
| 82 | 520000h | 52FFFFFFh | 42 | 2A0000h | 2AFFFFFFh | 2 | 020000h | 02FFFFFFh |
| 81 | 510000h | 51FFFFFFh | 41 | 290000h | 29FFFFFFh | 1 | 010000h | 01FFFFFFh |
| 80 | 500000h | 50FFFFFFh | 40 | 280000h | 28FFFFFFh | 0 | 000000h | 00FFFFFFh |
| 79 | 4F0000h | 4FFFFFFh | 39 | 270000h | 27FFFFFFh | | | |
| 78 | 4E0000h | 4EFFFFFFh | 38 | 260000h | 26FFFFFFh | | | |
| 77 | 4D0000h | 4DFFFFFFh | 37 | 250000h | 25FFFFFFh | | | |
| 76 | 4C0000h | 4CFFFFFFh | 36 | 240000h | 24FFFFFFh | | | |
| 75 | 4B0000h | 4BFFFFFFh | 35 | 230000h | 23FFFFFFh | | | |
| 74 | 4A0000h | 4AFFFFFFh | 34 | 220000h | 22FFFFFFh | | | |
| 73 | 490000h | 49FFFFFFh | 33 | 210000h | 21FFFFFFh | | | |
| 72 | 480000h | 48FFFFFFh | 32 | 200000h | 20FFFFFFh | | | |

9. Parallel Mode (for 16-pin SO package only)

The parallel mode provides 8 bits of input/output to increase factory production throughput at the customer manufacturing facilities. This function is recommended for increasing production throughput. Entering Parallel mode requires issuing the Enter Parallel Mode command (55h). After writing the Parallel Mode Entry command and pulling CS# high, the available commands are Read, Write Enable (WREN), Write Disable (WRDI), Page Program (PP), Sector Erase (SE), Bulk Erase (BE), Write Status Register (WRSR), Read Status Register (RDSR), Release from Deep Power Down/Release from Deep Power Down and Read Electronic Signature (RES), Write Enable (WREN), Write Disable (WRDI), Deep Power Down (DP), Read Identification (RDID) and Read ID (READ_ID).

The flash memory will remain in Parallel mode until either the Parallel Mode Exit command (45h) is issued, or until a power-down / power-up sequence has been completed, after which the flash memory will exit parallel mode automatically and switch back to serial mode (no power-down will be necessary to switch back to serial mode if the Parallel Mode Exit command is issued).

In parallel mode, the maximum SCK clock frequency is limited to 6 MHz for Read Data Bytes and 10 MHz for other operations. PO[6-0] can be left unconnected if the Parallel Mode functions are not needed. Fast-Read command is not applicable in Parallel mode.

10. Accelerated Programming Operation

The device offers accelerated program operations through the ACC function. This function is primarily intended to allow faster manufacturing throughput at the factory. If the system asserts V_{HH} on this pin, the device uses the higher voltage on the pin to reduce the time required for program operations. Removing V_{HH} from the WP#/ACC pin returns the device to normal operation. Note that the WP#/ACC pin must not be at V_{HH} for operations other than accelerated programming, or device damage may result. In addition, the WP#/ACC pin must not be left floating or unconnected; inconsistent behavior of the device may result.

11. Command Definitions

The host system must shift all commands, addresses, and data in and out of the device, beginning with the most significant bit. On the first rising edge of SCK after CS# is driven low, the device accepts the one-byte command on SI (all commands are one byte long), most significant bit first. Each successive bit is latched on the rising edge of SCK. [Table 11.6 on page 38](#) lists the complete set of commands.

Every command sequence begins with a one-byte command code. The command may be followed by address, data, both, or nothing, depending on the command. CS# must be driven high after the last bit of the command sequence has been written.

The Read Data Bytes (READ), Read Status Register (RDSR), Read Data Bytes at Higher Speed (FAST_READ) and Read Identification (RDID) command sequences are followed by a data output sequence on SO. CS# can be driven high after any bit of the sequence is output to terminate the operation.

The Page Program (PP), Sector Erase (SE), Bulk Erase (BE), Write Status Register (WRSR), Write Enable (WREN), or Write Disable (WRDI) commands require that CS# be driven high at a byte boundary, otherwise the command is not executed. Since a byte is composed of eight bits, CS# must therefore be driven high when the number of clock pulses after CS# is driven low is an exact multiple of eight.

The device ignores any attempt to access the memory array during a Write Status Register, program, or erase operation, and continues the operation uninterrupted.

11.1 Read Data Bytes (READ: 03h)

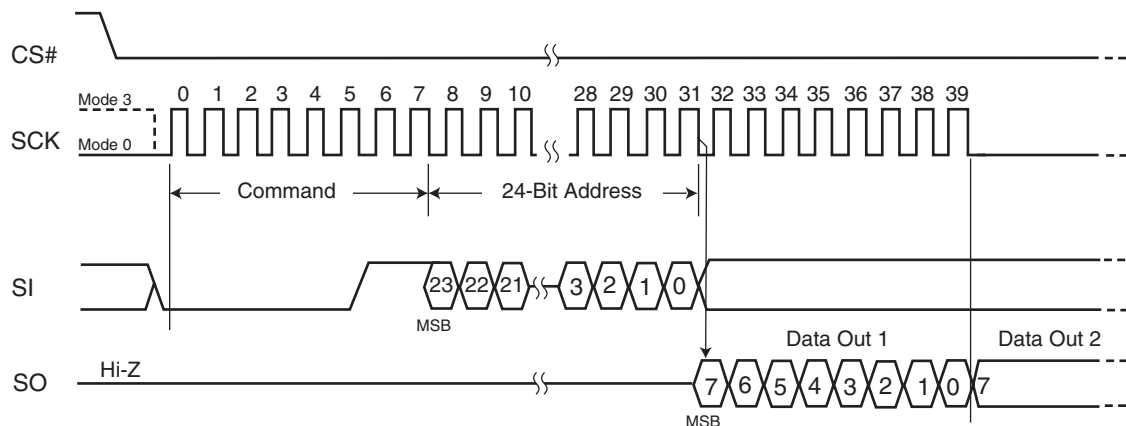
11.1.1 Serial Mode

The Read Data Bytes (READ-Serial Mode) command reads data from the memory array at the frequency (f_{SCK}) presented at the SCK input, with a maximum speed of 40 MHz. The host system must first select the device by driving CS# low. The READ command is then written to SI, followed by a 3-byte address (A23-A0). Each bit is latched on the rising edge of SCK. The memory array data, at that address, are output serially on SO at a frequency f_{SCK} , on the falling edge of SCK.

[Figure 11.1](#) and [Table 11.6](#) detail the READ command sequence. The first byte specified can be at any location. The device automatically increments to the next higher address after each byte of data is output. The entire memory array can therefore be read with a single READ command. When the highest address is reached, the address counter reverts to 00000h, allowing the read sequence to continue indefinitely.

The READ command is terminated by driving CS# high at any time during data output. The device rejects any READ command issued while it is executing a program, erase, or Write Status Register operation, and continues the operation uninterrupted.

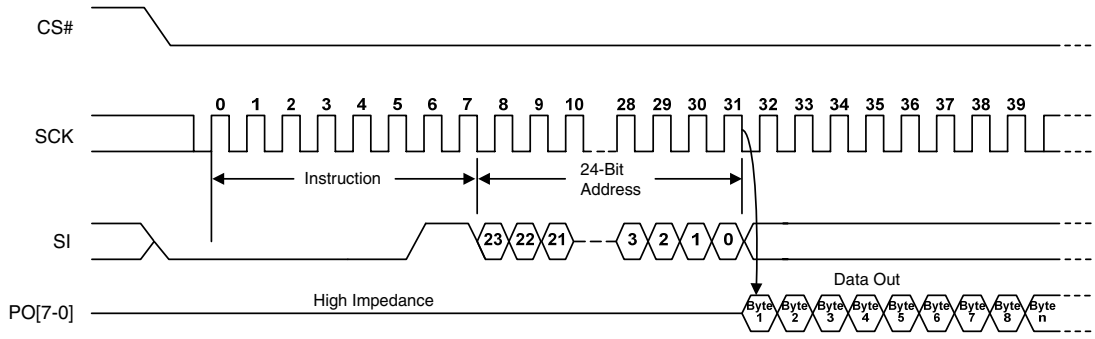
Figure 11.1 Read Data Bytes (READ) Command Sequence



11.1.2 Parallel Mode

In parallel mode, the maximum SCK clock frequency is 6 MHz. The device requires a single clock cycle instead of eight clock cycles to access the next data byte. The memory array output will be the same as in the serial mode. The only difference is that a byte of data is output per clock cycle instead of a single bit. This means that 256 bytes of data can be copied into the 256 byte wide page write buffer in 256 clock cycles instead of in 2,048 clock cycles.

Figure 11.2 Parallel Read Instruction Sequence



Notes

1. 1st Byte = "03h".
2. 2nd Byte = Address 1, MSB first (bits 23 through 16).
3. 3rd Byte = Address 2, MSB first (bits 15 through 8).
4. 4th Byte = Address 3, MSB first (bits 7 through 0).
5. From the 5th Byte, SO will output the array data.
6. In parallel mode, the maximum clock frequency (Fsck) is 6 MHz.
7. For parallel mode operation, the device requires an Enter Parallel Mode command (55h) before the READ command. An Exit Parallel Mode (45h) command or a power-down / power-up sequence is required to exit the parallel mode.

11.2 Read Data Bytes at Higher Speed (FAST_READ: 0Bh)

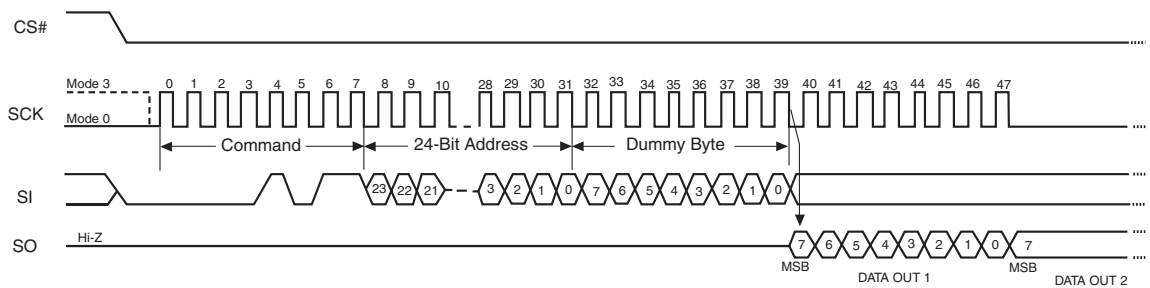
The FAST_READ command reads data from the memory array at the frequency (f_{SCK}) presented at the SCK input, with a maximum speed of 104 MHz. The host system must first select the device by driving CS# low. The FAST_READ command is then written to SI, followed by a 3-byte address (A23-A0) and a dummy byte. Each bit is latched on the rising edge of SCK. The memory array data, at that address, are output serially on SO at a frequency f_{SCK} , on the falling edge of SCK.

The FAST_READ command sequence is shown in Figure 11.3 and Table 11.6. The first byte specified can be at any location. The device automatically increments to the next higher address after each byte of data is output. The entire memory array can therefore be read with a single FAST_READ command. When the highest address is reached, the address counter reverts to 00000h, allowing the read sequence to continue indefinitely.

The FAST_READ command is terminated by driving CS# high at any time during data output. The device rejects any FAST_READ command issued while it is executing a program, erase, or Write Status Register operation, and continues the operation uninterrupted. Note that the FAST_READ command is not valid in parallel mode.

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Figure 11.3 Read Data Bytes at Higher Speed (FAST_READ) Command Sequence



11.3 Read Identification (RDID: 9Fh)

11.3.1 Serial Mode

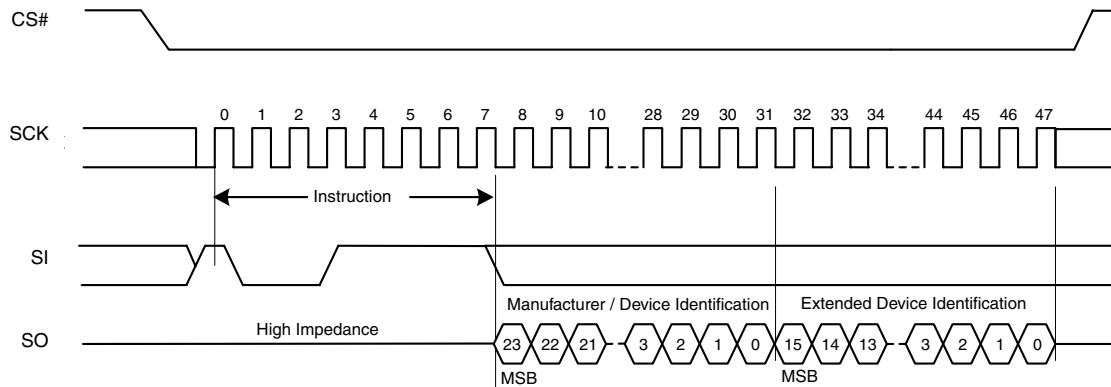
The Read Identification (RDID) instruction opcode allows the 8-bit manufacturer identification to be read, follow by two bytes of device identification. The manufacturer identification is assigned by JEDEC. The device identification is assigned by the device manufacturer.

Any Read Identification (RDID) instruction opcode issued while a program, erase, or write cycle is in progress is not decoded and has no effect on execution of the program, erase, or write cycle that is in progress.

The device is first selected by driving the CS# chip select input pin to the logic low state. After this, the RDID 8-bit instruction opcode is shifted in onto the SI serial input pin. After the last bit of the RDID instruction opcode is shifted into the device, a byte of manufacturer identification, two bytes of device identification and two bytes of extended device identification will be shifted sequentially out of the SO serial output pin. Each bit is shifted out during the falling edge of the SCK serial clock signal. The maximum clock frequency for the RDID (9Fh) command is at 40MHz (Normal Read).

The Read Identification (RDID) instruction sequence is terminated by driving the CS# chip select input pin to the logic high state anytime during data output. After issuing any Read ID instruction opcodes (90h, 9Fh, ABh), driving the CS# chip select input pin to the logic high state will automatically send the device into the standby mode. Driving the CS# chip select input pin to the logic low state again will automatically send the device out of the standby mode and into the active mode.

Figure 11.4 Read Identification Command Sequence and Data Out Sequence



11.3.2 Parallel Mode

In parallel mode, the maximum SCK clock frequency is 10 MHz. The device requires a single clock cycle instead of eight clock cycles to access the next data byte. The method of memory content output will be the same compared to the serial mode. The only difference is that a byte of data is output per clock cycle instead of a single bit. In this case, the manufacturer identification will be output during the first byte cycle and the device identification during the second and third byte cycles out of the PO7-PO0 serial output pins. To read ID in parallel mode requires a Parallel Mode Entry command (55h) to be issued before the RDID command. Once in the parallel mode, the flash memory will not exit parallel mode until a Parallel Mode Exit (45h) command is given to the flash device, or upon power down/power up sequence.

Figure 11.5 Parallel Read_ID Command Sequence and Data Out Sequence

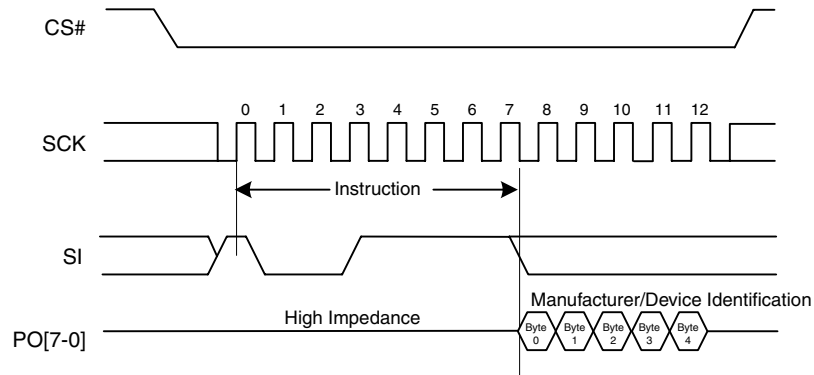


Table 11.1 Manufacturer & Device Identification, RDID (9Fh)

| Device | Manufacturer Identification | | Device Identification | | Extended Device Identification | |
|-----------------------|-----------------------------|--------|-----------------------|--------|--------------------------------|--------|
| | Byte 0 | Byte 1 | Byte 2 | Byte 3 | Byte 4 | Byte 5 |
| Uniform 256 KB Sector | 01h | 20h | 18h | 03h | 00h | |
| Uniform 64 KB Sector | 01h | 20h | 18h | 03h | 01h | |

11.4 Read Manufacturer and Device ID (READ_ID: 90h)

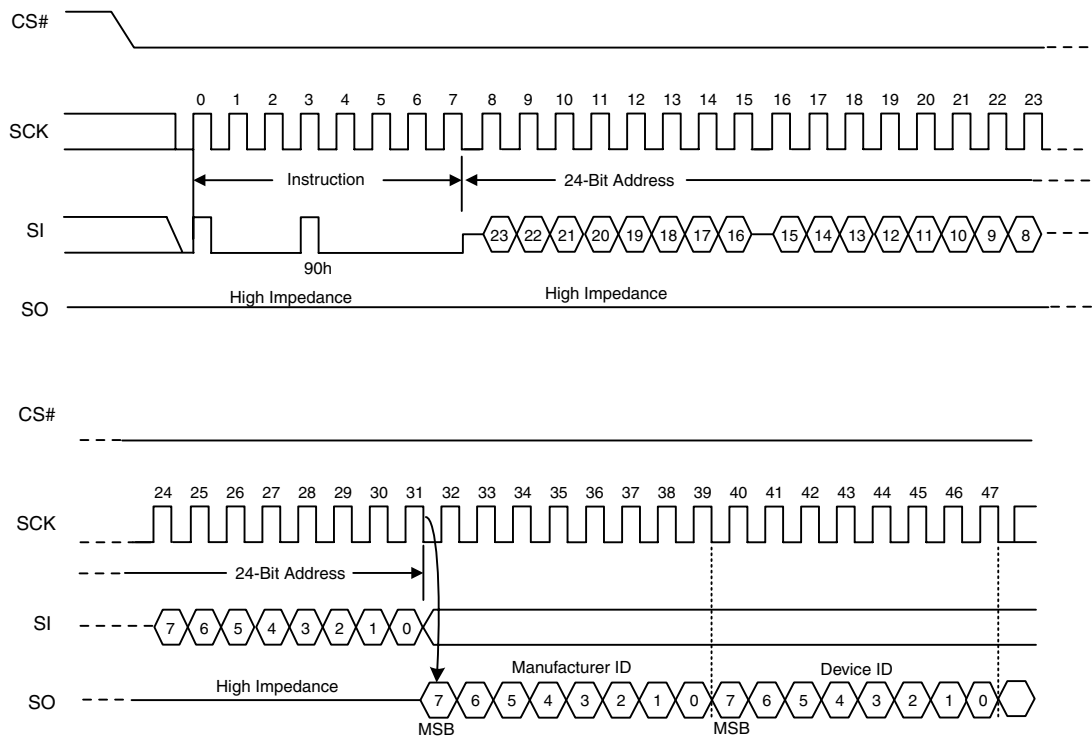
11.4.1 Serial Mode

The READ_ID (90h) instruction identifies the Device Manufacturer ID and the Device ID. The instruction is initiated by driving the CS# pin low and shifting in (via the SI input pin) the instruction code “90h” followed by a 24-bit address of XXXXX0h. (X: High or Low) Following this, the Manufacturer ID and the Device ID are shifted out on SO output pin starting after the falling edge of the SCK serial clock input signal. The Manufacturer ID and the Device ID are always shifted out on the SO output pin with the MSB first, as shown in Figure 11.6. If the 24-bit address is set to XXXXX1h, then the Device ID is read out first followed by the Manufacturer ID. Note that the upper 23 bits of the address do not have to be 0’s and can be don’t cares. Once the device is in READ_ID mode, the Manufacturer ID and Device ID output data toggles between address 000000H and 000001H until terminated by a low to high transition on the CS# input pin. After the first 24-bit address is provided, the user must wait 16 clock cycles for both the Manufacturer ID and Device ID to be output on the SO output pin. The maximum clock frequency for the READ_ID (90h) command is at 104MHz (Fast Read). Parallel Mode the maximum clock frequency is 10Mhz.

The Manufacturer ID & Device ID is output continuously until terminated by a low to high transition on CS# chip select input pin.

After issuing READ_ID instruction, driving the CS# chip select input pin to the logic high state will automatically send the device into the standby mode. Driving the CS# chip select input pin to the logic low state again will automatically sent the device out of the standby mode and into the active mode.

Figure 11.6 Serial READ_ID Instruction Sequence



11.4.2 Parallel Mode

The maximum clock frequency allowed on the SCK input pin in parallel mode is 10 MHz. The Parallel Mode Entry command (55h) must be issued before writing the READ_ID command. Once in the parallel mode, the flash memory will not exit parallel mode until a Parallel Mode Exit (45h) command is given to the flash device, or upon power-down/power-up sequence.

Figure 11.7 Parallel Read_ID Instruction Sequence

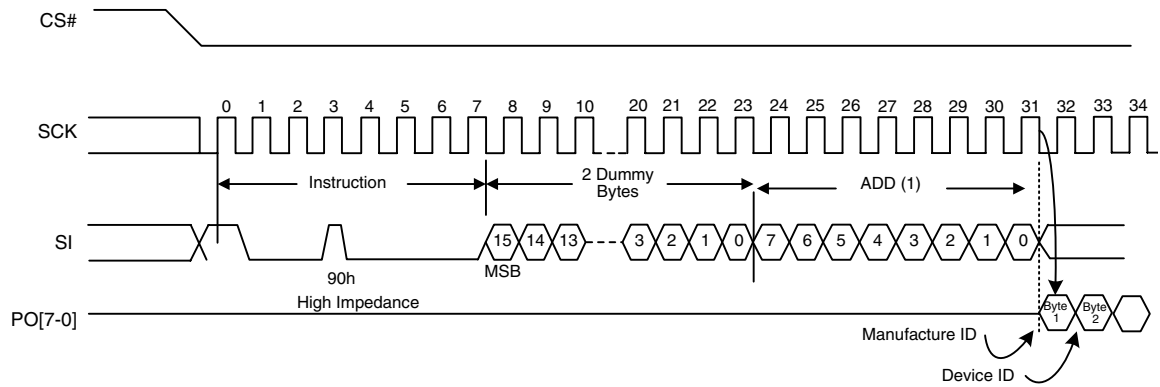


Table 11.2 READ_ID Command and Data

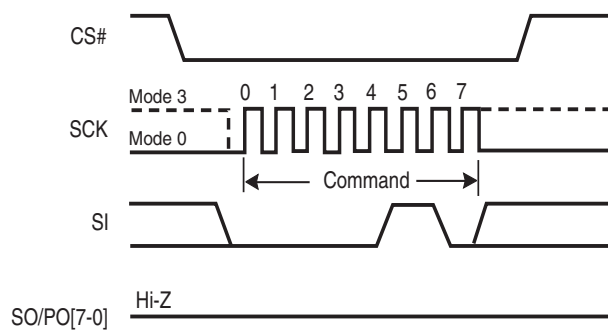
| Description | Address | Data |
|---|---------|------|
| Manufacturer Identification | 00000h | 01h |
| Device Identification (Memory Capacity) | 00001h | 17h |

11.5 Write Enable (WREN: 06h)

The Write Enable (WREN) command (see Figure 11.8) sets the Write Enable Latch (WEL) bit to a 1, which enables the device to accept a Write Status Register, program, or erase command. The WEL bit must be set prior to every Page Program (PP), Erase (SE or BE) and Write Status Register (WRSR) command.

The host system must first drive CS# low, write the WREN command, and then drive CS# high.

Figure 11.8 Write Enable (WREN) Command Sequence



11.6 Write Disable (WRDI: 04h)

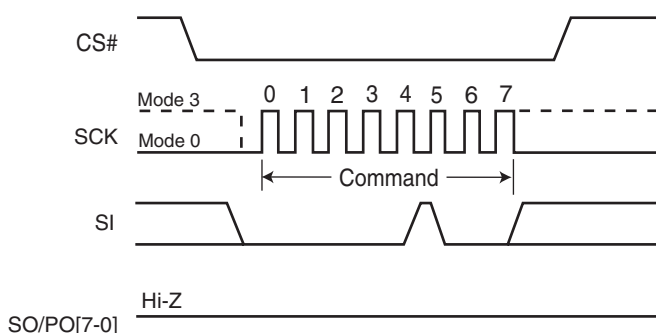
The Write Disable (WRDI) command (see [Figure 11.9](#)) resets the Write Enable Latch (WEL) bit to a 0, which disables the device from accepting a Write Status Register, program, or erase command. The host system must first drive CS# low, write the WRDI command, and then drive CS# high.

Any of following conditions resets the WEL bit:

- Power-up
- Write Disable (WRDI) command completion
- Write Status Register (WRSR) command completion
- Page Program (PP) command completion
- Sector Erase (SE) command completion
- Bulk Erase (BE) command completion

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Figure 11.9 Write Disable (WRDI) Command Sequence



11.7 Read Status Register (RDSR: 05h)

11.7.1 Serial Mode

The Read Status Register (RDSR) command outputs the state of the Status Register bits. [Table 11.3](#) shows the status register bits and their functions.

The RDSR command may be written at any time, even while a program, erase, or Write Status Register operation is in progress. The host system should check the Write In Progress (WIP) bit before sending a new command to the device if an operation is already in progress. [Figure 11.10](#) shows the RDSR command sequence, which also shows that it is possible to read the Status Register continuously until CS# is driven high.

Table 11.3 S25FL128P Status Register (Uniform 256 KB sector)

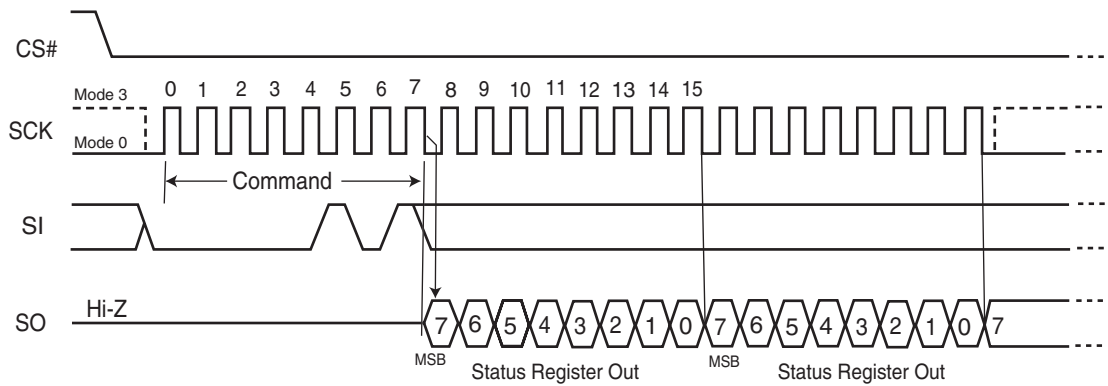
| Bit | Status Register Bit | Bit Function | Description |
|-----|---------------------|-------------------------------|---|
| 7 | SRWD | Status Register Write Disable | 1 = Protects when WP#/ACC is low 0 = No protection, even when WP#/ACC is low |
| 6 | Don't Care | — | — |
| 5 | 0 | — | Not used |
| 4 | BP2 | Block Protect | 000–111 = Protects upper half of address range in 7 sizes. |
| 3 | BP1 | | |
| 2 | BP0 | | |
| 1 | WEL | Write Enable Latch | 1 = Device accepts Write Status Register, program, or erase commands 0 = Ignores Write Status Register, program, or erase commands |
| 0 | WIP | Write in Progress | 1 = Device Busy. A Write Status Register, program, or erase operation is in progress 0 = Ready. Device is in standby mode and can accept commands. |

Table 11.4 S25FL128P Status Register (Uniform 64 KB sector)

| Bit | Status Register Bit | Bit Function | Description |
|-----|---------------------|-------------------------------|---|
| 7 | SRWD | Status Register Write Disable | 1 = Protects when WP#/ACC is low 0 = No protection, even when WP#/ACC is low |
| 6 | Don't Care | — | — |
| 5 | BP3 | Block Protect | 0000–1111= Protects upper half of address range in 8 sizes. |
| 4 | BP2 | | |
| 3 | BP1 | | |
| 2 | BP0 | | |
| 1 | WEL | Write Enable Latch | 1 = Device accepts Write Status Register, program, or erase commands 0 = Ignores Write Status Register, program, or erase commands |
| 0 | WIP | Write in Progress | 1 = Device Busy. A Write Status Register, program, or erase operation is in progress 0 = Ready. Device is in standby mode and can accept commands. |

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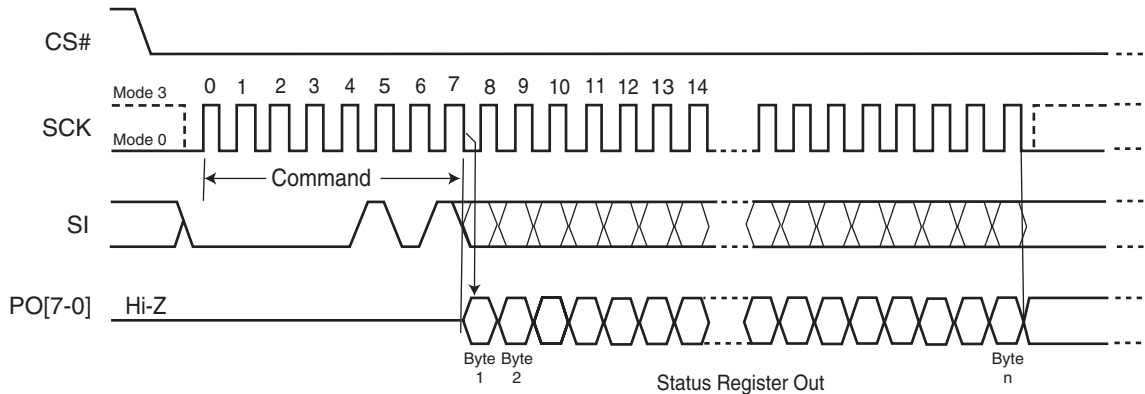
Figure 11.10 Read Status Register (RDSR) Command Sequence



11.7.2 Parallel Mode

When the device is in Parallel Mode, the maximum SCK clock frequency is 10 MHz. The device requires a single clock cycle instead of eight clock cycles to access the next data byte. The method of memory content output will be the same compared to outside of Parallel Mode. The only difference is that a byte of data is output per clock cycle instead of a single bit. The Status Register contents can be read out on the PO[7-0] serial output pins continuously by applying multiples of clock cycles.

Figure 11.11 Parallel Read Status Register (RDSR) Instruction Sequence



Notes

1. Instruction byte = 05h.
2. Under parallel mode, the fastest access clock frequency (F_{sck}) will be changed to a maximum of 10MHz (SCK pin clock frequency).
3. To read Status Register in parallel mode requires a Parallel Mode Entry command (55h) to be issued before the RDSR command. Once in the parallel mode, the flash memory will not exit the parallel mode until a Parallel Mode Exit (45h) command is given to the flash device, or upon power down / power up sequence.

11.7.3 Status Register Bit Descriptions

The following describes the status and control bits of the Status Register, and applies to both serial and parallel modes.

Write In Progress (WIP) bit: Indicates whether the device is busy performing a Write Status Register, program, or erase operation. This bit is read-only, and is controlled internally by the device. If WIP is 1, one of these operations is in progress; if WIP is 0, no such operation is in progress.

Write Enable Latch (WEL) bit: Determines whether the device will accept and execute a Write Status Register, program, or erase command. When set to 1, the device accepts these commands; when set to 0, the device rejects the commands. This bit is set to 1 by writing the WREN command, and set to 0 by the WRDI command, and is also automatically reset to 0 after the completion of a Write Status Register, program, or erase operation. WEL cannot be directly set by the WRSR command.

Block Protect (BP2, BP1, BP0) bits for uniform 256KB sector product: (BP3, BP2, BP1, BP0) for uniform 64KB sector product: Define the portion of the memory area that will be protected against any changes to the stored data. The Write Status Register (WRSR) command controls these bits, which are non-volatile. When one or more of these bits is set to 1, the corresponding memory area (see [Table 7.1 on page 13](#)) is protected against Page Program (PP) and Sector Erase (SE) commands. If the Hardware Protected mode is enabled, BP2:BP0 (or BP3:BP0) cannot be changed. The Bulk Erase (BE) command is executed only if all Block Protect bits are 0.

Status Register Write Disable (SRWD) bit: Provides data protection when used together with the Write Protect (WP#/ACC) signal. When SRWD is set to 1 and WP#/ACC is driven low, the device enters the Hardware Protected mode. The non-volatile bits of the Status Register (SRWD, BP2, BP1, BP0) become read-only bits and the device ignores any Write Status Register (WRSR) command.

11.8 Write Status Register (WRSR: 01h)

The Write Status Register (WRSR) command changes the bits in the Status Register. A Write Enable (WREN) command, which itself sets the Write Enable Latch (WEL) in the Status Register, is required prior to writing the WRSR command. [Table 11.3, S25FL128P Status Register \(Uniform 256 KB sector\) on page 26](#) shows the status register bits and their functions.

The host system must drive CS# low, write the WRSR command, and the appropriate data byte on SI ([Figure 11.12](#)).

The WRSR command cannot change the state of the Write Enable Latch (bit 1). The WREN command must be used for that purpose. Bit 0 is a status bit controlled internally by the Flash device. Bits 6 and 5 are always read as 0 and have no user significance.

The WRSR command also controls the value of the Status Register Write Disable (SRWD) bit. The SRWD bit and WP#/ACC together place the device in the Hardware Protected Mode (HPM). The device ignores all WRSR commands once it enters the Hardware Protected Mode (HPM). [Table 11.5](#) shows that WP#/ACC must be driven low and the SRWD bit must be 1 for this to occur.

Figure 11.12 Write Status Register (WRSR) Command Sequence

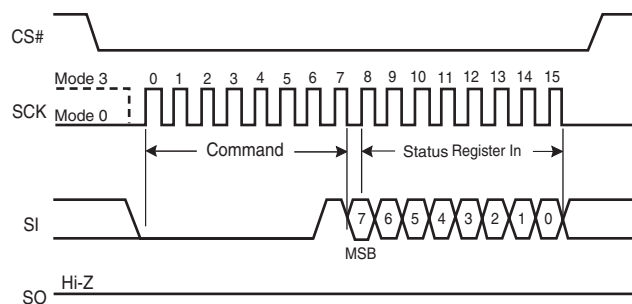
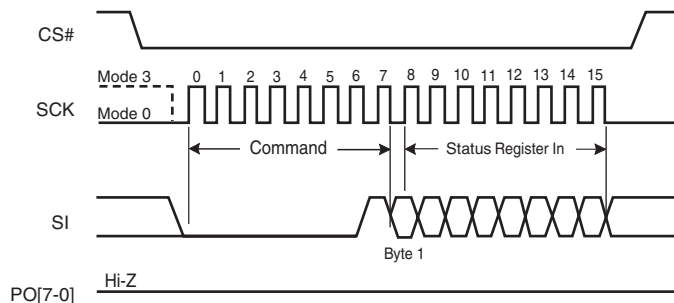


Figure 11.13 Parallel Write Status Register (WRSR) Command Sequence



Notes

1. Instruction byte = 01h
2. In parallel mode, the maximum access clock frequency (F_{sck}) is 10 MHz (SCK pin clock frequency).
3. Writing to the Status Register in parallel mode requires a Parallel Mode Entry command (55h) to be issued before the RDSR command. Once in the parallel mode, the flash memory will not exit the parallel mode until a Parallel Mode Exit (45h) command is given to the flash device, or upon power-down or power-up sequence.

Table 11.5 Protection Modes

| WP#/ACC Signal | SRWD Bit | Mode | Write Protection of the Status Register | Protected Area (See Note) | Unprotected Area (See Note) |
|----------------|----------|--------------------------|---|--|--|
| 1 | 1 | Software Protected (SPM) | Status Register is writable (if the WREN command has set the WEL bit). The values in the SRWD, BP2, BP1 and BP0 (or BP3, BP2, BP1 and BP0) bits can be changed. | Protected against program and erase commands | Ready to accept Page Program and Sector Erase commands |
| 1 | 0 | | | | |
| 0 | 0 | | | | |
| 0 | 1 | Hardware Protected (HPM) | Status Register is Hardware write protected. The values in the SRWD, BP2, BP1 and BP0 (or BP3, BP2, BP1 and BP0) bits cannot be changed. | Protected against program and erase commands | Ready to accept Page Program and Sector Erase commands |

Note

As defined by the values in the Block Protect (BP2, BP1, BP0) bits of the Status Register, as shown in Table 7.1 on page 13.

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Table 11.5 shows that neither WP#/ACC or SRWD bit by themselves can enable HPM. The device can enter HPM either by setting the SRWD bit after driving WP#/ACC low, or by driving WP#/ACC low after setting the SRWD bit. However, the device disables HPM only when WP#/ACC is driven high.

Note that HPM only protects against changes to the status register. Since BP2:BP0 (or BP3:BP0) cannot be changed in HPM, the size of the protected area of the memory array cannot be changed. Note that HPM provides no protection to the memory array area outside that specified by Block Protect bits (Software Protected Mode, or SPM).

If WP#/ACC is permanently tied high, HPM can never be activated, and only the SPM (Block Protect bits of the Status Register) can be used.

11.9 Page Program (PP: 02h)

11.9.1 Serial Mode

The Page Program (PP) command changes specified bytes in the memory array (from 1 to 0 only). A WREN command is required prior to writing the PP command.

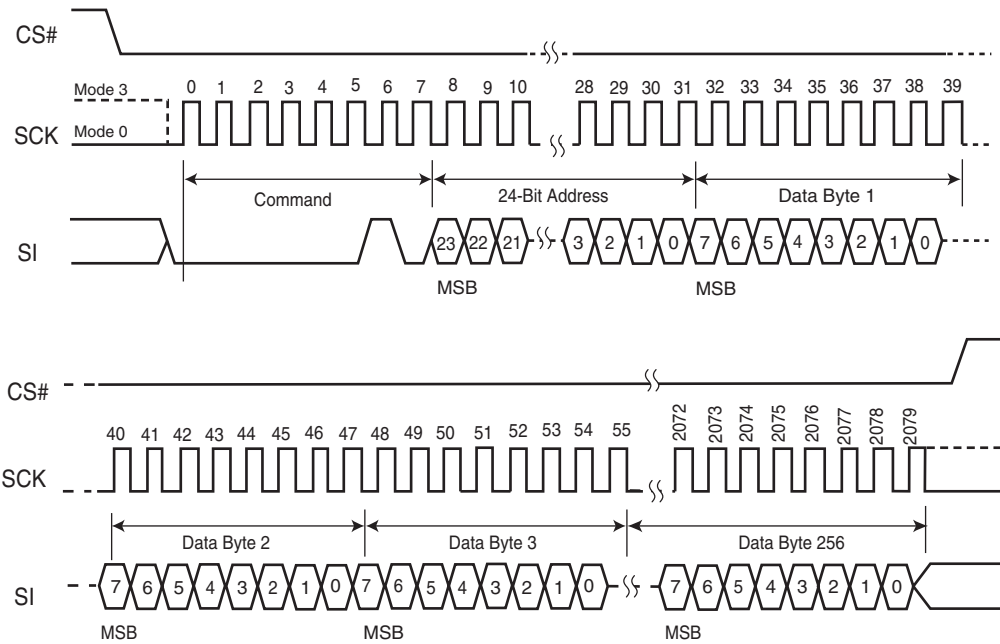
The host system must drive CS# low, and then write the PP command, three address bytes, and at least one data byte on SI. CS# must be driven low for the entire duration of the PP sequence. The command sequence is shown in Figure 11.14 and Table 11.6.

The device programs only the last 256 data bytes sent to the device. If the number of data bytes exceeds this limit, the bytes sent before the last 256 bytes are discarded, and the device begins programming the last 256 bytes sent at the starting address of the specified page. This may result in data being programmed into different addresses within the same page than expected. If fewer than 256 data bytes are sent to device, they are correctly programmed at the requested addresses.

The host system must drive CS# high after the device has latched the 8th bit of the data byte, otherwise the device does not execute the PP command. The PP operation begins as soon as CS# is driven high. The device internally controls the timing of the operation, which requires a period of t_{PP} . The Status Register may be read to check the value of the Write In Progress (WIP) bit while the PP operation is in progress. The WIP bit is 1 during the PP operation, and is 0 when the operation is completed. The device internally resets the Write Enable Latch to 0 before the operation completes (the exact timing is not specified).

The device does not execute a Page Program (PP) command that specifies a page that is protected by the Block Protect bits (see Table 7.1 on page 13).

Figure 11.14 Page Program (PP) Command Sequence

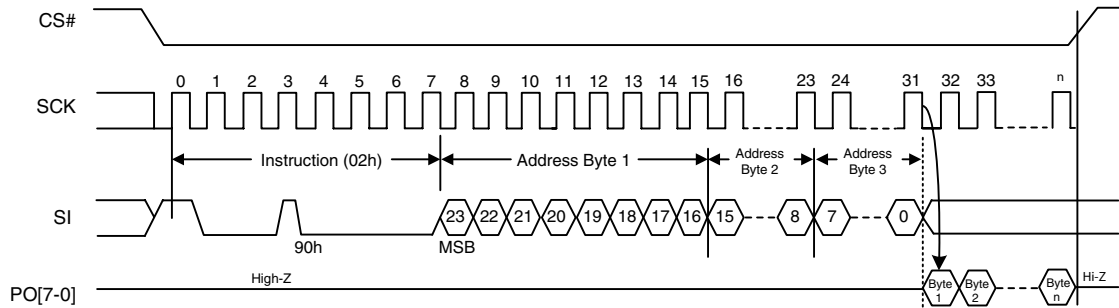


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11.9.2 Parallel Mode

In parallel mode, the maximum SCK clock frequency is 10 MHz. The device requires a single clock cycle instead of eight clock cycles to access the next data byte. The memory content input method is the same as serial mode. The only difference is that a byte of data is input per clock cycle instead of a single bit. This means that 256 bytes of data can be copied into the 256 byte wide page write buffer in 256 clock cycles instead of in 2,048 clock cycles.

Figure 11.15 Parallel Page Program (PP) Instruction Sequence



Notes

1. 1st Byte = "02h".
2. 2nd Byte = Address 1, MSB first (bits 23 through 16).
3. 3rd Byte = Address 2, MSB first (bits 15 through 8).
4. 4th Byte = Address 3, MSB first (bits 7 through 0).
5. 5th Byte = first write data byte.
6. In parallel mode, the fastest access clock frequency (F_{sck}) is 10 MHz (SCK pin clock frequency).
7. Programming in parallel mode requires an "Parallel mode Entry" command (55h) before the program command. Once in the parallel mode, the flash memory will not exit parallel mode until an "Exit Parallel Mode" (45h) command is given to the flash device, or upon power down / power up sequence completion.

11.10 Sector Erase (SE: 20h, D8h)

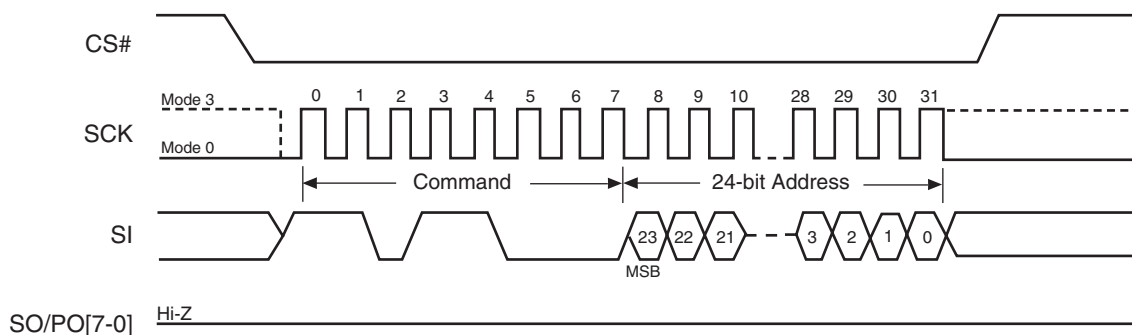
The Sector Erase (SE) command sets all bits at all addresses within a specified sector to a logic 1. A WREN command is required prior to writing the PP command.

The host system must drive CS# low, and then write the SE command plus three address bytes on SI. Any address within the sector (see [Table 7.1 on page 13](#)) is a valid address for the SE command. CS# must be driven low for the entire duration of the SE sequence. The command sequence is shown in [Figure 11.16](#) and [Table 11.6](#).

The host system must drive CS# high after the device has latched the 8th bit of the SE command, otherwise the device does not execute the command. The SE operation begins as soon as CS# is driven high. The device internally controls the timing of the operation, which requires a period of t_{SE} . The Status Register may be read to check the value of the Write In Progress (WIP) bit while the SE operation is in progress. The WIP bit is 1 during the SE operation, and is 0 when the operation is completed. The device internally resets the Write Enable Latch to 0 before the operation completes (the exact timing is not specified).

The device does not execute an SE command that specifies a sector that is protected by the Block Protect bits (see [Table 7.1 on page 13](#)).

Figure 11.16 Sector Erase (SE) Command Sequence



11.11 Bulk Erase (BE: C7h, 60h)

The Bulk Erase (BE) command sets all the bits within the entire memory array to logic 1s. A WREN command is required prior to writing the PP command.

For 64 KB sector devices, the bulk erase command may be written as either C7h or 60h. For 256 KB sector devices, only the C7h command is valid.

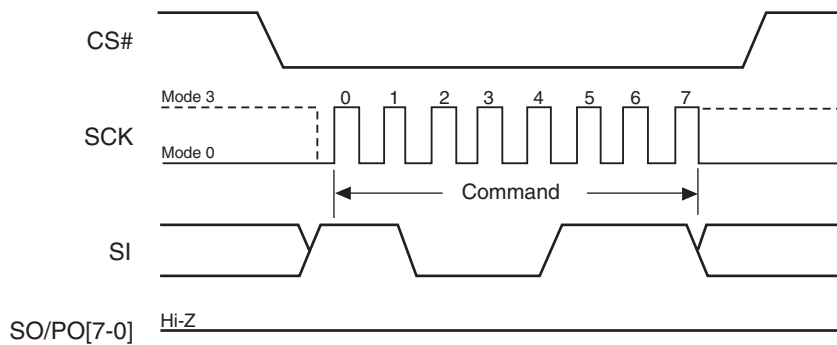
The host system must drive CS# low, and then write the BE command on SI. CS# must be driven low for the entire duration of the BE sequence. The command sequence is shown in [Figure 11.17](#) and [Table 11.6](#).

The host system must drive CS# high after the device has latched the 8th bit of the CE command, otherwise the device does not execute the command. The BE operation begins as soon as CS# is driven high. The device internally controls the timing of the operation, which requires a period of t_{BE} . The Status Register may be read to check the value of the Write In Progress (WIP) bit while the BE operation is in progress. The WIP bit is 1 during the BE operation, and is 0 when the operation is completed. The device internally resets the Write Enable Latch to 0 before the operation completes (the exact timing is not specified).

The device only executes a BE command if all Block Protect bits (BP2:BP0 or BP3:BP0) are 0 (see [Table 7.1 on page 13](#)). Otherwise, the device ignores the command.

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Figure 11.17 Bulk Erase (BE) Command Sequence



11.12 Deep Power Down (DP: B9h)

The Deep Power Down (DP) command provides the lowest power consumption mode of the device. It is intended for periods when the device is not in active use, and ignores all commands except for the Release from Deep Power Down (RES) command. *The DP mode therefore provides the maximum data protection against unintended write operations.* The standard standby mode, which the device goes into automatically when CS# is high (and all operations in progress are complete), should generally be used for the lowest power consumption when the quickest return to device activity is required.

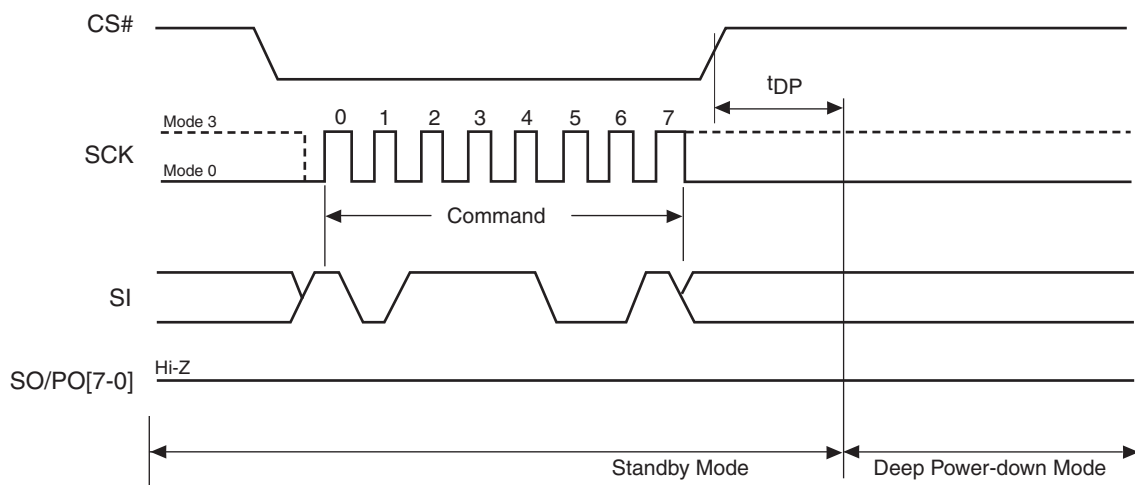
The host system must drive CS# low, and then write the DP command on SI. CS# must be driven low for the entire duration of the DP sequence. The command sequence is shown in Figure 11.18 and Table 11.6.

The host system must drive CS# high after the device has latched the 8th bit of the DP command, otherwise the device does not execute the command. After a delay of t_{DP} , the device enters the DP mode and current reduces from I_{SB} to I_{DP} (see Table 17.1 on page 41).

Once the device has entered the DP mode, all commands are ignored except the RES command (which releases the device from the DP mode). The RES command also provides the Electronic Signature of the device to be output on SO, if desired (see sections 11.13 and 11.14).

DP mode automatically terminates when power is removed, and the device always powers up in the standard standby mode. The device rejects any DP command issued while it is executing a program, erase, or Write Status Register operation, and continues the operation uninterrupted.

Figure 11.18 Deep Power Down (DP) Command Sequence



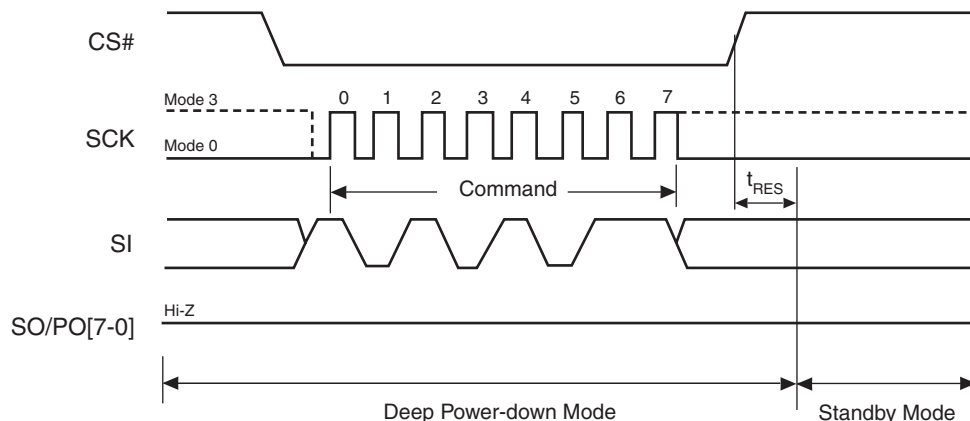
11.13 Release from Deep Power Down (RES: ABh)

The device requires the Release from Deep Power Down (RES) command to exit the Deep Power Down mode. When the device is in the Deep Power Down mode, all commands except RES are ignored.

The host system must drive CS# low and write the RES command to SI. CS# must be driven low for the entire duration of the sequence. The command sequence is shown in Figure 11.19 and Table 11.6.

The host system must drive CS# high $t_{RES(max)}$ after the 8-bit RES command byte. The device transitions from DP mode to the standby mode after a delay of t_{RES} (see Table 19.1 on page 42). In the standby mode, the device can execute any read or write command.

Figure 11.19 Release from Deep Power Down (RES) Command Sequence



11.14 Release from Deep Power Down and Read Electronic Signature (RES: ABh)

11.14.1 Serial Mode

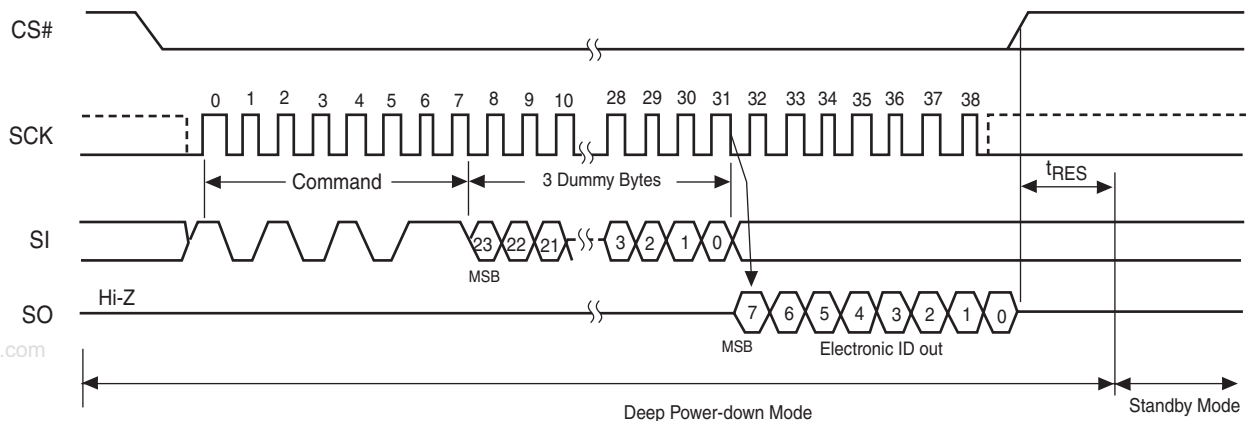
This command reads the old-style Electronic Signature from the SO serial output pin. See Figure 11.20 and Table 11.6 for the command sequence and signature value. Please note that the Electronic Signature only consists of the Device ID portion of the 16-bit JEDEC ID that is read by the Read Identifier (RDID) instruction. The old style Electronic Signature is supported for backward compatibility, and should not be used for new software designs, which should instead use the JEDEC 16-bit Electronic Signature by issuing the Read Identifier (RDID) command.

The device is first selected by driving the CS# chip select input pin to the logic low state. The RES command is shifted in followed by three dummy bytes onto the SI serial input pin. After the last bit of the three dummy bytes is shifted into the device, a byte of Electronic Signature will be shifted out of the SO serial output pin. Each bit is shifted out during the falling edge of the SCK serial clock signal. The maximum clock frequency for the RES (ABh) command is at 104 MHz.

The Electronic Signature can be read repeatedly by applying multiples of eight clock cycles.

The RES instruction sequence is terminated by driving the CS# chip select input pin to the logic high state anytime during data output. After issuing any Read ID commands (90h, 9Fh, ABh), driving the CS# chip select input pin to the logic high state will automatically send the device into the standby mode. Driving the CS# chip select input pin to the logic low state again will automatically sent the device out of the standby mode and into the active mode.

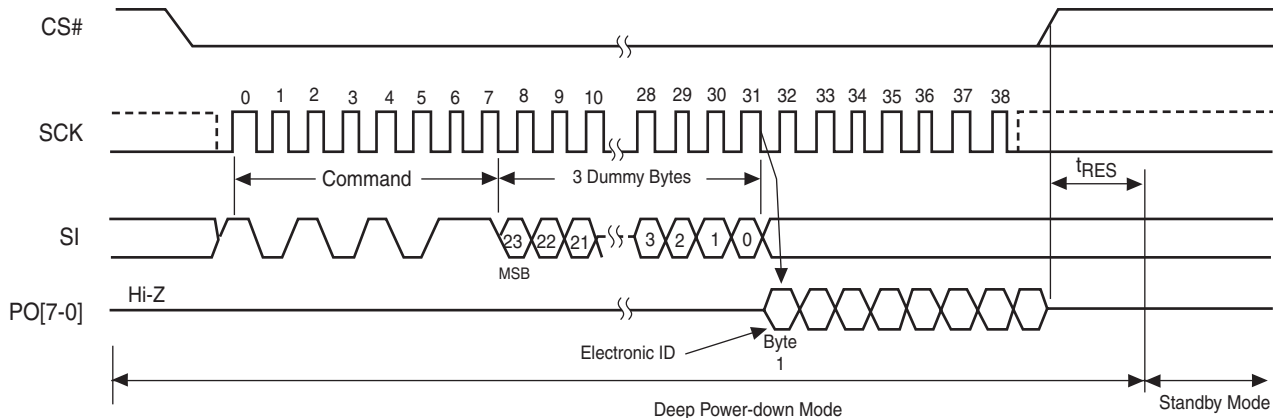
Figure 11.20 Serial Release from Deep Power Down and Read Electronic Signature (RES) Command Sequence



11.14.2 Parallel Mode

When the device is in parallel mode, the maximum SCK clock frequency is 10 MHz. The device requires a single clock cycle instead of eight clock cycles to access the next data byte. The method of memory content output will be the same compared to outside of parallel mode. The only difference is that a byte of data is output per clock cycle instead of a single bit. In this case, the Electronic Signature will be output onto the PO[7-0] serial output pins.

Figure 11.21 Parallel Release from Deep Power Down and Read Electronic Signature (RES) Command Sequence



Notes

1. In parallel mode, the maximum access clock frequency (F_{sck}) is 10 MHz (SCK pin clock frequency).
2. To release the device from Deep Power Down and read Electronic ID in parallel mode, a Parallel Mode Enter command (55h) must be issued before the RES command. The device will not exit parallel mode until a Parallel Mode Exit command (45h) is written, or upon power-down or power-up sequence.
3. Byte 1 will output the Electronic Signature.

11.15 Command Definitions

Table 11.6 Command Definitions

| Operation | Command | Description | One-Byte Command Code | Address Bytes | Dummy Byte | Data Bytes |
|-----------------|-----------|--|------------------------------------|---------------|------------|------------|
| Read | READ | Read Data Bytes | 03h (0000 0011) | 3 | 0 | 1 to ∞ |
| | FAST_READ | Read Data Bytes at Higher Speed | 0Bh (0000 1011) | 3 | 1 | 1 to ∞ |
| | RDID | Read Identification | 9Fh (1001 1111) | 0 | 0 | 1 to 3 |
| | READ_ID | Read Manufacturer ID and Device ID | 90h (1001 0000) | 3 | 0 | 1 to ∞ |
| Write Control | WREN | Write Enable | 06h (0000 0110) | 0 | 0 | 0 |
| | WRDI | Write Disable | 04h (0000 0100) | 0 | 0 | 0 |
| Erase | SE | 64 KB Sector Erase (See Note) | 20h (0010 0000) or D8h (1101 1000) | 3 | 0 | 0 |
| | | 256 KB Sector Erase | D8h (1101 1000) | 3 | 0 | 0 |
| | BE | Bulk (Chip) Erase, Uniform 64 KB Sector Product (See Note) | C7h (1100 0111) or 60h (0110 0000) | 0 | 0 | 0 |
| | | Bulk (Chip) Erase, Uniform 256 KB Sector Product | C7h (1100 0111) | 0 | 0 | 0 |
| Program | PP | Page Program | 02h (0000 0010) | 3 | 0 | 1 to 256 |
| Status Register | RDSR | Read from Status Register | 05h (0000 0101) | 0 | 0 | 1 to ∞ |
| | WRSR | Write to Status Register | 01h (0000 0001) | 0 | 0 | 1 |
| Parallel Mode | Entry | Enter x8 Parallel Mode | 55h (0101 0101) | 0 | 0 | 0 |
| | Exit | Exit x8 Parallel Mode | 45h (0100 0101) | 0 | 0 | 0 |
| Power Saving | DP | Deep Power Down | B9h (1011 1001) | 0 | 0 | 0 |
| | RES | Release from Deep Power Down | ABh (1010 1011) | 0 | 0 | 0 |
| | | Release from Deep Power Down and Read Electronic Signature | ABh (1010 1011) | 0 | 3 | 1 to ∞ |

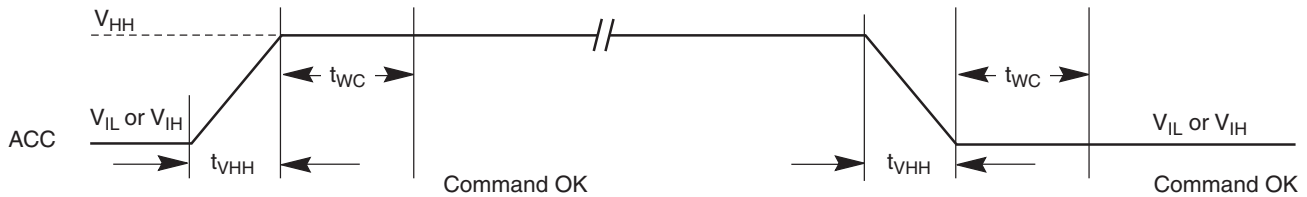
Note

For 64 KB sector devices, either command is valid and performs the same function.

12. Program Acceleration via WP#/ACC pin

The program acceleration function requires applying V_{HH} to the WP#/ACC input, and then waiting a period of t_{WC} . Minimum t_{VHH} rise and fall times is required for WP#/ACC to change to V_{HH} from V_{IL} or V_{IH} . Removing V_{HH} from the WP#/ACC pin returns the device to normal operation after a period of t_{WC} .

Figure 12.1 ACC Program Acceleration Timing Requirements



Note

Only Read Status Register (RDSR) and Page Program (PP) operations are allow when ACC is at (V_{HH}).

Table 12.1 ACC Program Acceleration Specifications

| Parameter | Description | Min. | Max. | Unit |
|-----------|---|------|------|------|
| V_{HH} | ACC Pin Voltage High | 8.5 | 9.5 | V |
| t_{VHH} | ACC Voltage Rise and Fall Time | 250 | | ns |
| t_{WC} | ACC at V_{HH} and V_{IL} or V_{IH} to First command | 5 | | ns |

13. Power-up and Power-down

During power-up and power-down, certain conditions must be observed. CS# must follow the voltage applied on V_{CC} , and must not be driven low to select the device until V_{CC} reaches the allowable values as follows (see Figure 13.1 and Table 13.1):

- At power-up, V_{CC} (min.) plus a period of t_{PU}
- At power-down, V_{SS}

A pull-up resistor on Chip Select (CS#) typically meets proper power-up and power-down requirements.

No Write Status Register, program, or erase command should be sent to the device until V_{CC} rises to the V_{CC} minimum, plus a delay of t_{PU} . At power-up, the device is in standby mode (not Deep Power Down mode) and the WEL bit is reset (0).

Each device in the host system should have the V_{CC} rail decoupled by a suitable capacitor close to the package pins (this capacitor is generally of the order of 0.1 μF), as a precaution to stabilizing the V_{CC} feed.

When V_{CC} drops from the operating voltage to below the minimum V_{CC} threshold at power-down, all operations are disabled and the device does not respond to any commands. Note that data corruption may result if a power-down occurs while a Write Register, program, or erase operation is in progress.

Figure 13.1 Power-Up Timing Diagram

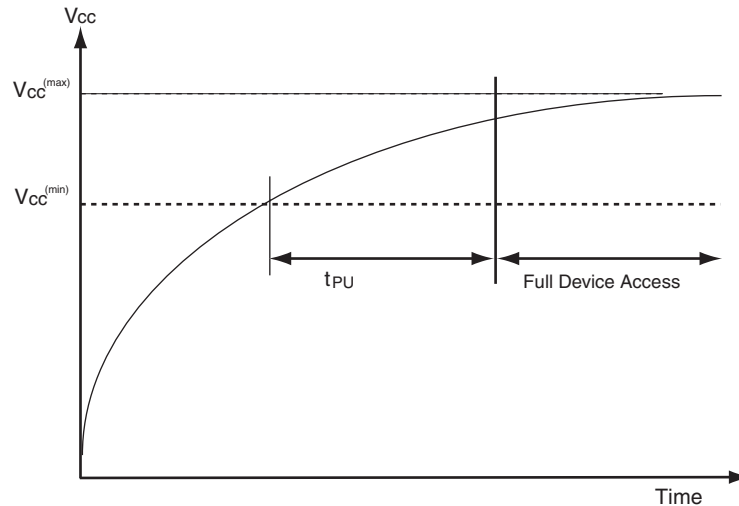


Table 13.1 Power-Up Timing Characteristics

| Symbol | Parameter | Min | Max | Unit |
|----------------------|------------------------------------|-----|-----|------|
| $V_{CC(\text{min})}$ | V_{CC} (minimum) | 2.7 | | V |
| t_{PU} | V_{CC} (min) to device operation | 15 | | ms |

14. Initial Delivery State

The device is delivered with all bits set to 1 (each byte contains FFh) upon initial factory shipment. The Status Register contains 00h (all Status Register bits are 0).

15. Absolute Maximum Ratings

Do not stress the device beyond the ratings listed in this section, or serious, permanent damage to the device may result. These are stress ratings only and device operation at these or any other conditions beyond those indicated in this section and in the *Operating Ranges* section of this document is not implied. Device operation for extended periods at the limits listed in this section may affect device reliability.

Table 15.1 Absolute Maximum Ratings

| Description | Rating |
|---|--------------------------|
| Ambient Storage Temperature | -65°C to +150°C |
| Voltage with Respect to Ground: All Inputs and I/Os | -0.5 V to $V_{CC}+0.5$ V |

Notes

1. Minimum DC voltage on input or I/O pins is -0.5 V. During voltage transitions, input at I/O pins may overshoot V_{SS} to -2.0 V for periods of up to 20 ns. See [Figure 15.2](#). Maximum DC voltage on output and I/O pins is 3.6 V. During voltage transitions output pins may overshoot to $V_{CC} + 2.0$ V for periods up to 20 ns. See [Figure 15.2](#).
2. No more than one output may be shorted to ground at a time. Duration of the short circuit should not be greater than one second.
3. Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 15.1 Maximum Negative Overshoot Waveform

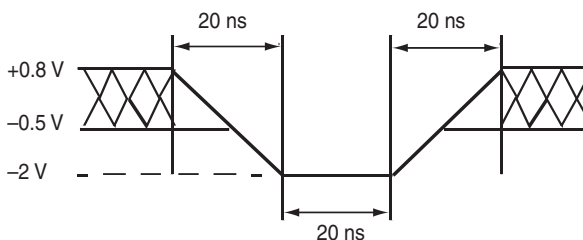
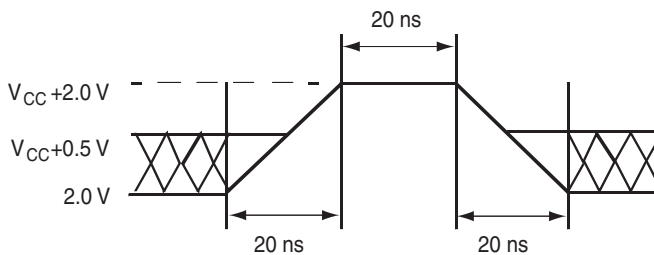


Figure 15.2 Maximum Positive Overshoot Waveform



16. Operating Ranges

Table 16.1 Operating Ranges

| Description | Rating | |
|---|---------------|----------------|
| Ambient Operating Temperature (T_A) | Industrial | -40°C to +85°C |
| Positive Power Supply | Voltage Range | 2.7 V to 3.6 V |

Note

Operating ranges define those limits between which functionality of the device is guaranteed.

17. DC Characteristics

This section summarizes the DC Characteristics of the device. Designers should check that the operating conditions in their circuit match the measurement conditions specified in the Test Specifications in [Table 18.1 on page 41](#), when relying on the quoted parameters.

Table 17.1 DC Characteristics (CMOS Compatible)

| Parameter | Description | Test Conditions (See Note) | Min | Typ. | Max | Unit |
|-----------|-----------------------------|---|---------------------------------|------|----------------|---------|
| V_{CC} | Supply Voltage | | 2.7 | | 3.6 | V |
| I_{CC1} | Active Read Current | $SCK = 0.1 V_{CC} / 0.9V_{CC}$ | | | 22 | mA |
| | | $SCK = 0.1 V_{CC} / 0.9V_{CC}$ | 104 MHz (Serial) | | | |
| | | | 40 MHz (Serial: Fast Read Mode) | | | 10 |
| | | 3 MHz (Parallel Mode) | | | 10 | mA |
| I_{CC2} | Active Page Program Current | $CS\# = V_{CC}$ | | | 26 | mA |
| I_{CC3} | Active WRSR Current | $CS\# = V_{CC}$ | | | 26 | mA |
| I_{CC4} | Active Sector Erase Current | $CS\# = V_{CC}$ | | | 26 | mA |
| I_{CC5} | Active Bulk Erase Current | $CS\# = V_{CC}$ | | | 26 | mA |
| I_{SB} | Standby Current | $V_{IN} = GND$ or V_{CC} , $CS\# = V_{CC}$ | | | 200 | μA |
| I_{DP} | Deep Power Down Current | $V_{IN} = GND$ or V_{CC} , $CS\# = V_{CC}$ | | 3 | 20 | μA |
| I_{LI} | Input Leakage Current | $V_{IN} = GND$ or V_{CC} , $V_{CC} = V_{CCmax}$ | | | 2 | μA |
| I_{LO} | Output Leakage Current | $V_{IN} = GND$ to V_{CC} , $V_{CC} = V_{CCmax}$ | | | 2 | μA |
| V_{IL} | Input Low Voltage | | -0.3 | | $0.3 V_{CC}$ | V |
| V_{IH} | Input High Voltage | | $0.7 V_{CC}$ | | $V_{CC} + 0.5$ | V |
| V_{OL} | Output Low Voltage | $I_{OL} = 1.6$ mA, $V_{CC} = V_{CCmin}$ | | | 0.4 | V |
| V_{OH} | Output High Voltage | $I_{OH} = -0.1$ mA | $V_{CC} - 0.6$ | | | V |

Note

Typical values are at $T_A = 25^\circ C$ and 3.0 V.

18. Test Conditions

Figure 18.1 AC Measurements I/O Waveform

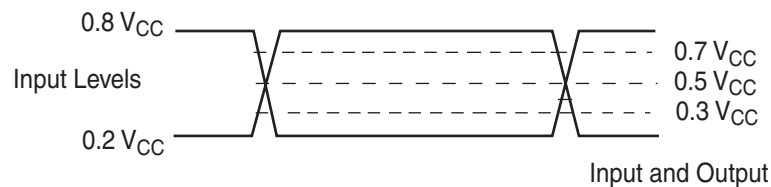


Table 18.1 Test Specifications

| Symbol | Parameter | Min | Max | Unit |
|--------|---------------------------------|------------------------------|-----|------|
| C_L | Load Capacitance | | 30 | pF |
| | Input Rise and Fall Times | | 5 | ns |
| | Input Pulse Voltage | $0.2 V_{CC}$ to $0.8 V_{CC}$ | | V |
| | Input Timing Reference Voltage | $0.3 V_{CC}$ to $0.7 V_{CC}$ | | V |
| | Output Timing Reference Voltage | $0.5 V_{CC}$ | | V |

19. AC Characteristics

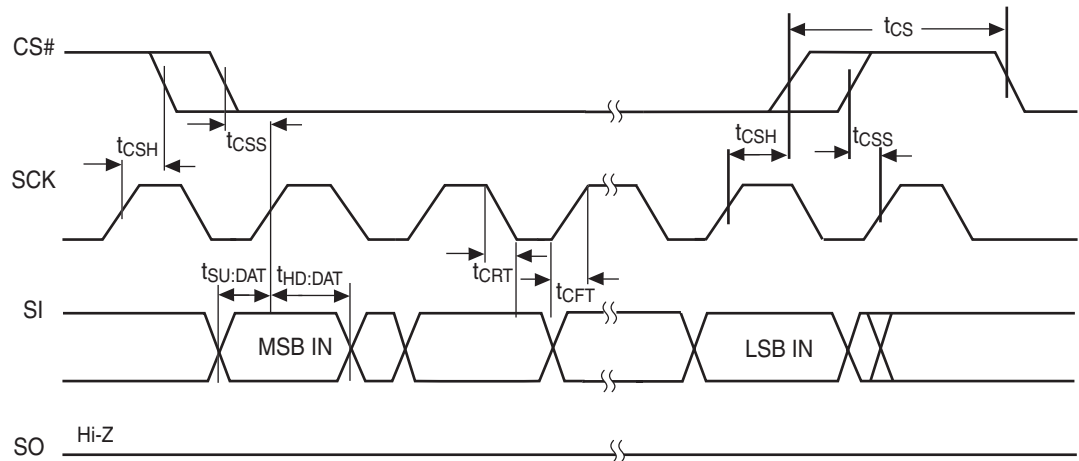
Table 19.1 AC Characteristics

| Symbol | Parameter | Min | Typ (Notes) | Max (Notes) | Unit |
|--------------|---|---------------------------------|--------------|-------------------------------|---------|
| F_{SCK} | SCK Clock Frequency READ command | D.C. | | 40 (Serial) 6 (Parallel) | MHz |
| F_{SCK} | SCK Clock Frequency for: FAST_READ, RDID, READ_ID, PP, SE, BE, DP, RES, WREN, WRDI, RDSR, WRSR (Note 4) | D.C. | | 104 (Serial) 10 (Parallel) | MHz |
| t_{CRT} | Clock Rise Time (Slew Rate) | 0.1 (Serial) 0.25 (Parallel) | | | V/ns |
| t_{CFT} | Clock Fall Time (Slew Rate) | 0.1 (Serial) 0.25 (Parallel) | | | V/ns |
| t_{WH} | SCK High Time | 4.5 (Serial) 50 (Parallel) | | | ns |
| t_{WL} | SCK Low Time | 4.5 (Serial) 50 (Parallel) | | | ns |
| t_{CS} | CS# High Time | 100 (Serial) 20 (Parallel) | | | ns |
| t_{CSS} | CS# Setup Time (Note 3) | 3 | | | ns |
| t_{CSH} | CS# HOLD Time (Note 3) | 3 | | | ns |
| t_{HD} | HOLD# Setup Time (relative to SCK) (Note 3) | 3 | | | ns |
| t_{CD} | HOLD# Non-Active Hold Time (relative to SCK) (Note 3) | 3 | | | ns |
| t_{HC} | HOLD# Non-Active Setup Time (relative to SCK) | 3 | | | ns |
| t_{CH} | HOLD# Hold Time (relative to SCK) | 3 | | | ns |
| t_V | Output Valid | 0 | | 8 (Serial) 20 (Parallel) | ns |
| t_{HO} | Output Hold Time | 0 | | | ns |
| t_{HD-DAT} | Data in Hold Time | 2 (Serial) 10 (Parallel) | | | ns |
| t_{SU-DAT} | Data in Setup Time | 3 (Serial) 10 (Parallel) | | | ns |
| t_R | Input Rise Time | | | 5 | ns |
| t_F | Input Fall Time | | | 5 | ns |
| t_{LZ} | HOLD# to Output Low Z (Note 3) | | | 8 (Serial) 20 (Parallel) | ns |
| t_{HZ} | HOLD# to Output High Z (Note 3) | | | 8 (Serial) 20 (Parallel) | ns |
| t_{DIS} | Output Disable Time (Note 3) | | | 8 (Serial) 20 (Parallel) | ns |
| t_{WPS} | Write Protect Setup Time (Notes 3, 5) | 20 | | | ns |
| t_{WPH} | Write Protect Hold Time (Notes 3, 5) | 100 | | | ns |
| t_W | Write Status Register Time | | | 100 | ms |
| t_{DP} | CS# High to Deep Power Down Mode | | | 3 | μ s |
| t_{RES} | Release DP Mode | | | 30 | μ s |
| t_{PP} | Page Programming Time | | 1.5 (Note 1) | 3 (Note 2) | ms |
| t_{EP} | Page Programming Time (WP#/ACC = 9 V) | | 1.2 (Note 1) | 2.4 (Note 2) | sec |
| t_{SE} | Sector Erase Time (64 KB) | | 0.5 (Note 1) | 3 (Note 2) | sec |
| t_{SE} | Sector Erase Time (256 KB) | | 2 (Note 1) | 12 (Note 2) | sec |
| t_{BE} | Bulk Erase Time | | 128 (Note 1) | 768 (Note 2) | sec |

Notes

1. Typical program and erase times assume the following conditions: 25°C, $V_{CC} = 3.0$ V; 10,000 cycles; checkerboard data pattern
2. Under worst-case conditions of 90°C; $V_{CC} = 2.7$ V; 100,000 cycles
3. Not 100% tested.
4. FAST_READ is not valid in parallel mode.
5. Only applicable as a constraint for WRSR command when SRWD is set to a '1'.

Figure 19.1 SPI Mode 0 (0,0) Input Timing



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Figure 19.2 SPI Mode 0 (0,0) Output Timing

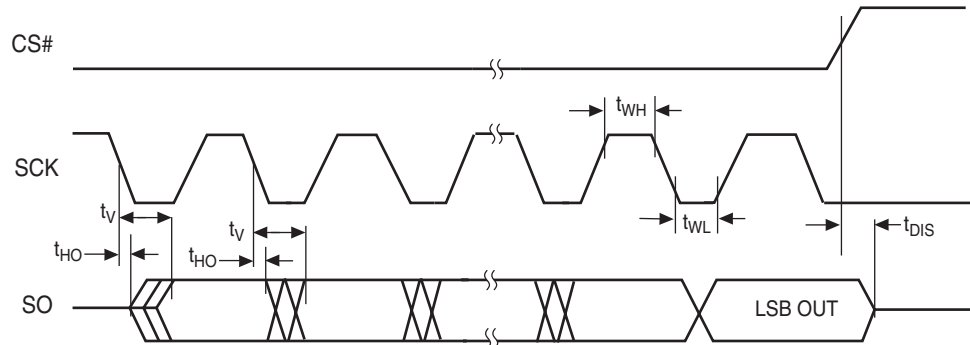
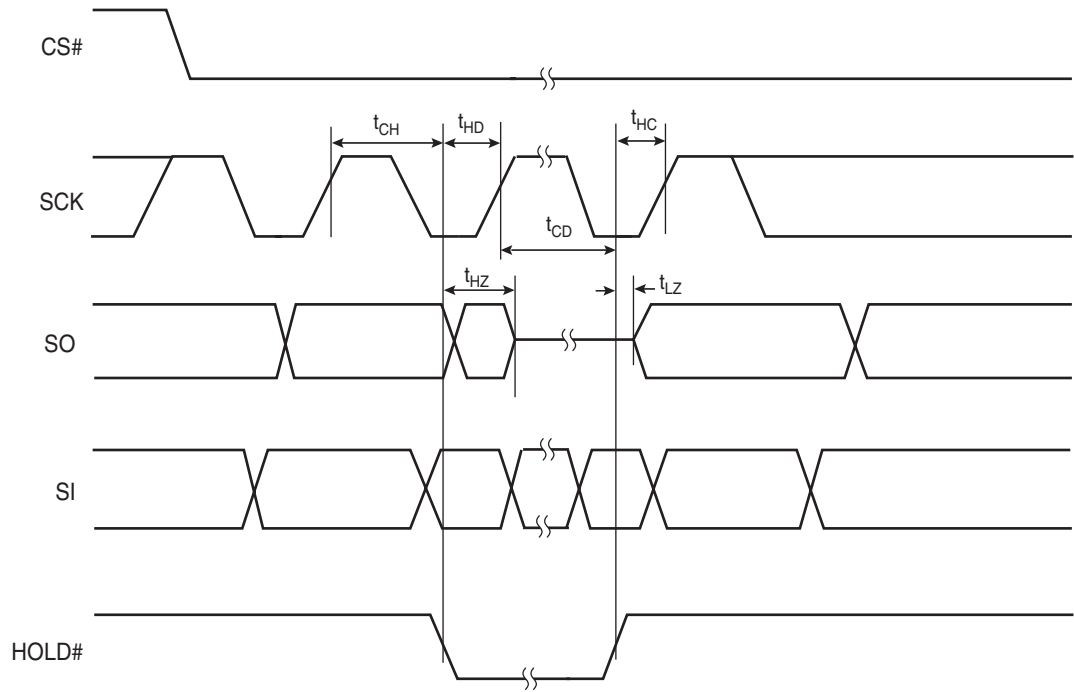
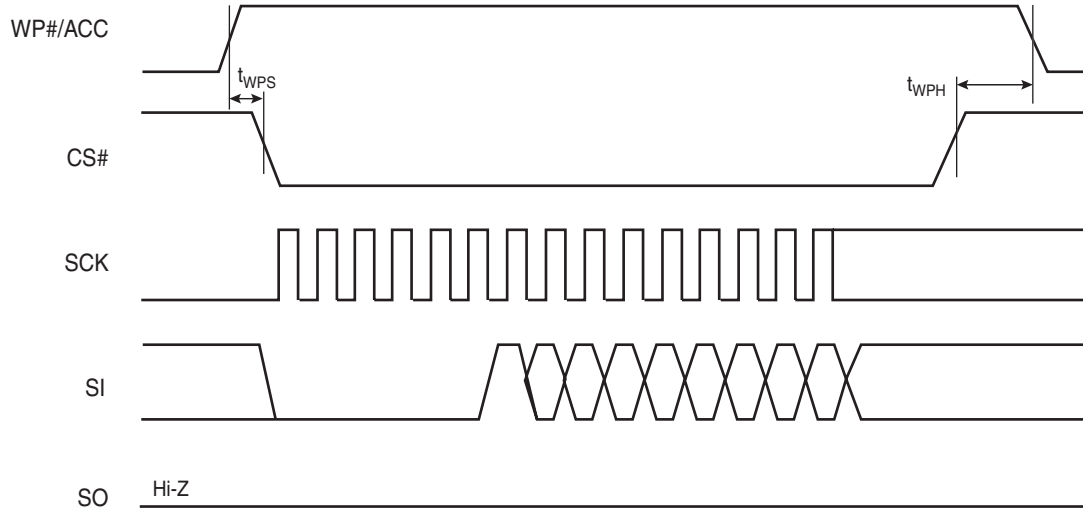


Figure 19.3 HOLD# Timing



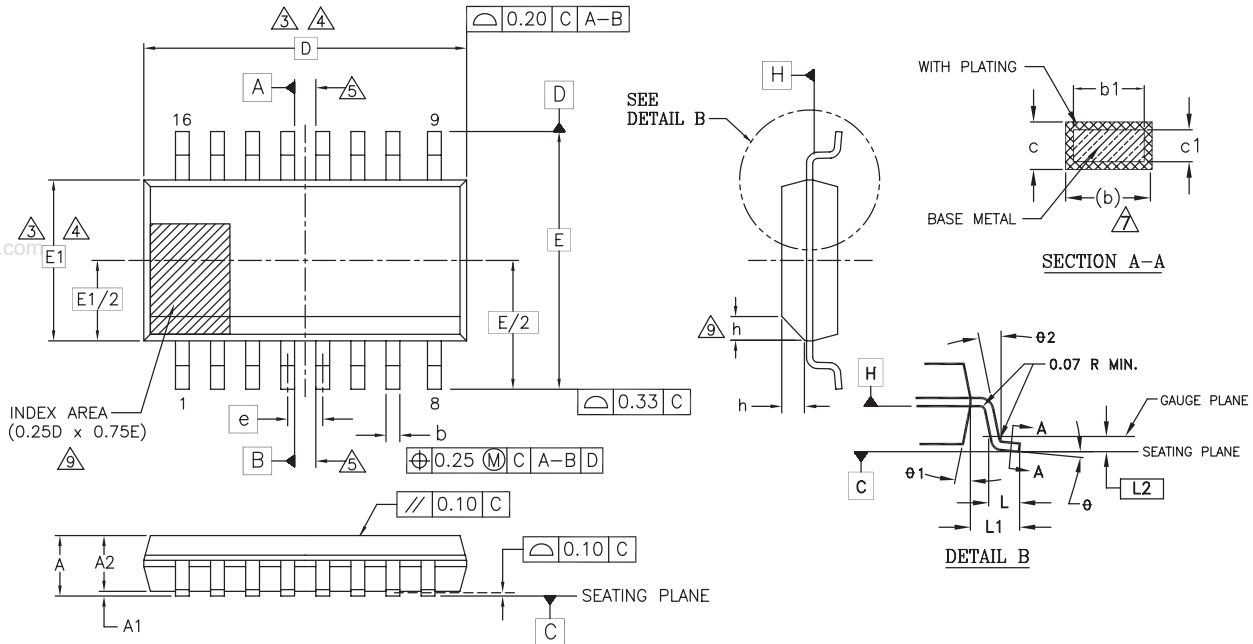
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Figure 19.4 Write Protect Setup and Hold Timing during WRSR when SRWD=1



20. Physical Dimensions

20.1 SO3 016 wide—16-pin Plastic Small Outline Package (300-mil Body Width)



NOTES:

1. ALL DIMENSIONS ARE IN BOTH INCHES AND MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M - 1994.
3. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER END. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 mm PER SIDE. D AND E1 DIMENSIONS ARE DETERMINED AT DATUM H.
4. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. DIMENSIONS D AND E1 ARE DETERMINED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH. BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
5. DATUMS A AND B TO BE DETERMINED AT DATUM H.
6. "N" IS THE MAXIMUM NUMBER OF TERMINAL POSITIONS FOR THE SPECIFIED PACKAGE LENGTH.
7. THE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 TO 0.25 mm FROM THE LEAD TIP.
8. DIMENSION "b" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.10 mm TOTAL IN EXCESS OF THE "b" DIMENSION AT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE LEAD FOOT.
9. THIS CHAMFER FEATURE IS OPTIONAL. IF IT IS NOT PRESENT, THEN A PIN 1 IDENTIFIER MUST BE LOCATED WITHIN THE INDEX AREA INDICATED.
10. LEAD COPLANARITY SHALL BE WITHIN 0.10 mm AS MEASURED FROM THE SEATING PLANE.

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| PACKAGE | SO3 016 (inches) | | SO3 016 (mm) | |
|---------|------------------|-------|--------------|------|
| | MIN | MAX | MIN | MAX |
| JEDEC | MS-013(D)AA | | MS-013(D)AA | |
| SYMBOL | MIN | MAX | MIN | MAX |
| A | 0.093 | 0.104 | 2.35 | 2.65 |
| A1 | 0.004 | 0.012 | 0.10 | 0.30 |
| A2 | 0.081 | 0.104 | 2.05 | 2.55 |
| b | 0.012 | 0.020 | 0.31 | 0.51 |
| b1 | 0.011 | 0.019 | 0.27 | 0.48 |
| c | 0.008 | 0.013 | 0.20 | 0.33 |
| c1 | 0.008 | 0.012 | 0.20 | 0.30 |
| D | 0.406 BSC | | 10.30 BSC | |
| E | 0.406 BSC | | 10.30 BSC | |
| E1 | 0.295 BSC | | 7.50 BSC | |
| e | .050 BSC | | 1.27 BSC | |
| L | 0.016 | 0.050 | 0.40 | 1.27 |
| L1 | .055 REF | | 1.40 REF | |
| L2 | .010 BSC | | 0.25 BSC | |
| N | 16 | | 16 | |
| h | 0.10 | 0.30 | 0.25 | 0.75 |
| θ | 0° | 8° | 0° | 8° |
| θ1 | 5° | 15° | 5° | 15° |
| θ2 | 0° | | 0° | |

21. Revision History

| Section | Description |
|---|---|
| Revision 01 (January 12, 2007) | |
| | Initial release. |
| Revision 02 (March 13, 2007) | |
| Distinctive Characteristics | Changed standby mode current. |
| S25FL128P Sector Address Table (Uniform 64 KB sector) | Corrected addresses for sectors 0 and 32. |
| Parallel Mode (for 16-pin SO package only) | Added last sentence in section. |
| Read Status Register (RDSR: 05h) | Separated status register bit descriptions into an additional subsection. |
| Page Program (PP: 02h) | Modified Parallel Page Program (PP) Instruction Sequence figure to match format of other parallel mode figures. |
| Command Definitions | Changed code for Bulk Erase (BE) 256 KB product in table. |
| Read Manufacturer and Device ID (READ_ID: 90h) | Corrected SI and CLK in Parallel Read_ID Instruction Sequence figure. |
| Absolute Maximum Ratings | Added overshoot and undershoot information. |
| DC Characteristics | Changed maximum specifications for I_{CC1} (parallel mode), I_{SB} , and I_{DP} |
| Revision 03 (April 24, 2007) | |
| Ordering Information | Changed Valid Combinations table. |
| Revision 04 (July 2, 2007) | |
| Device Operations | Added a sentence to Byte or Page programming |
| Parallel Mode (for 16-pin SO package only) | Added a sentence. |

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