LZ95D42/M

Timing Pulse Generator LSI for CCD

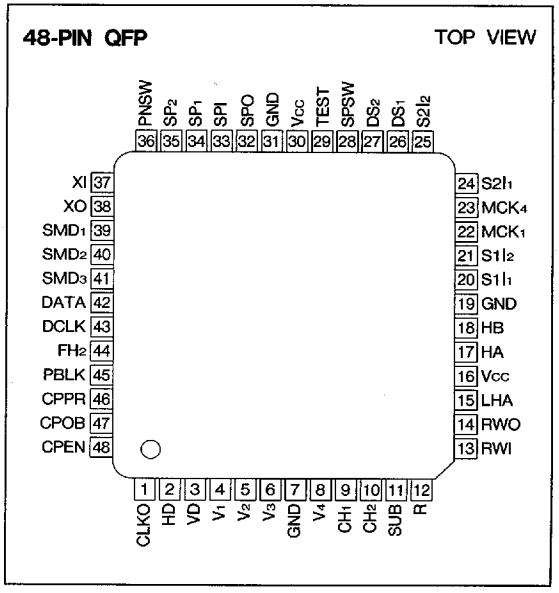
DESCRIPTION

The LZ95D42/M is a CMOS timing generator LSI which provides timing pulses used to drive a CCD area sensor, in combination with the SSG LSI (LZ95D52/M).

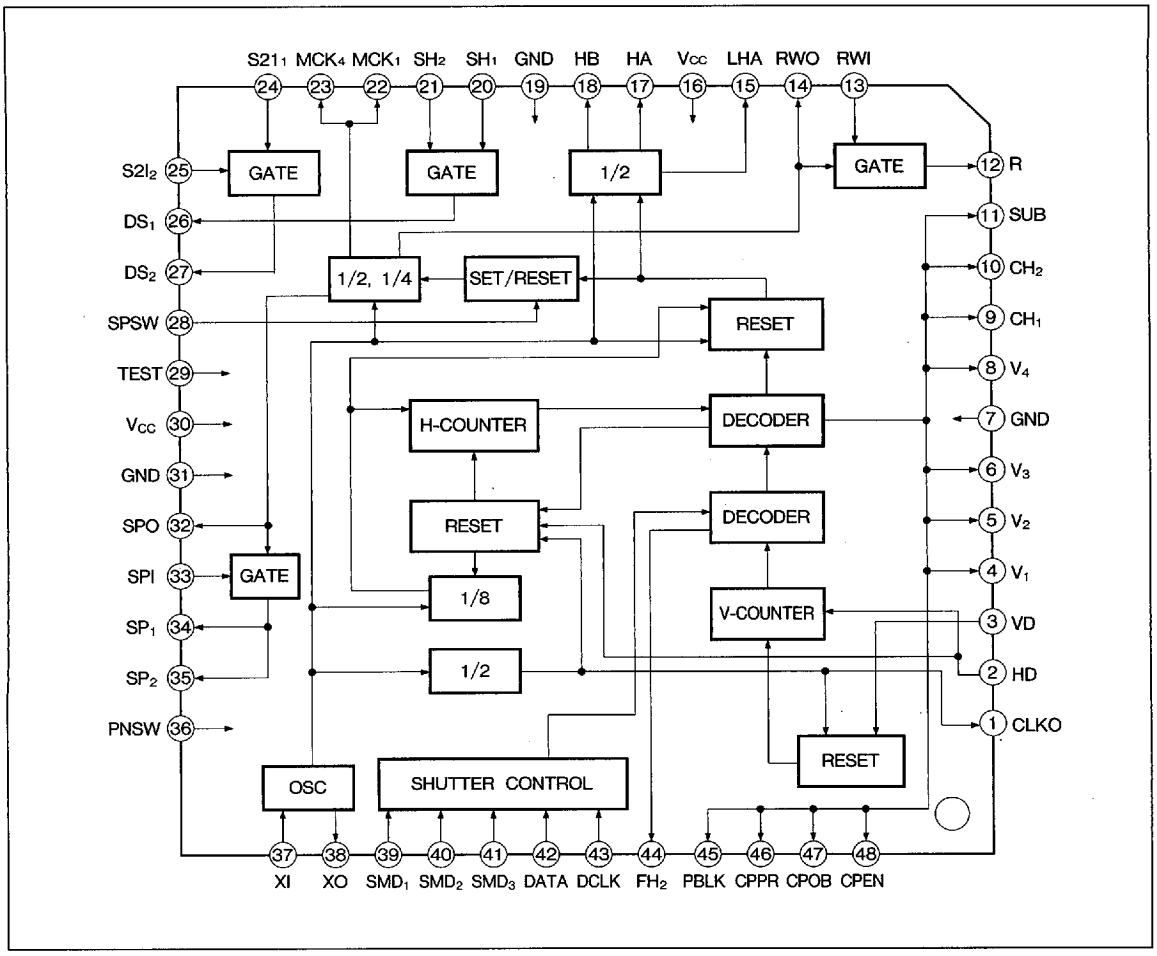
FEATURES

- Switchable between 410 000 pixels CCD and 470 000 pixels CCD
- Switchable between NTSC (EIA) and PAL (CCIR) systems
- Internal electronic shutter:
  Shutter speed is selectable from 1/60 (PAL : 1/50), 1/250, 1/500, 1/1 000, 1/2 000, 1/4 000 and 1/10 000 s, in addition to this, 1/100 s (PAL : 1/125 s) in Flicker-less mode using serial or parallel code. Shutter speed can also be controlled in 2 H periods using a serial code
- Single +5 V power supply
- Packages :
  LZ95D42 : 48-pin QFP(QFP048-P-1010)
  LZ95D42M : 48-pin QFP(QFP048-P-0707)

PIN CONNECTIONS



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Power voltage	V_{CC}	−0.3 to 7.0	V
Input voltage	V_I	−0.3 to V_{CC}+0.3	V
Output voltage	V_O	−0.3 to V_{CC}+0.3	V
Operating temperature	Topr	−30 to +75	°C
Storage temperature	Tstg	−55 to +150	°C

DC CHARACTERISTICS

(V_{CC} = +5 V±10%, Ta = −30 to +75°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Low level input voltage	V_{IL}				1.5	V	1
High level input voltage	V_{IH}		3.5			V	
Low level input current	$\lvert I_{IL1} \rvert$	V_I = 0 V			1.0	μA	2
	$\lvert I_{IL2} \rvert$	V_I = 0 V	6.0		75	μA	3
High level input current	$\lvert I_{IL1} \rvert$	V_I = V_{CC}			1.0	μA	4
	$\lvert I_{IL2} \rvert$	V_I = V_{CC}	6.0		75	μA	5
Low level output voltage	V_{OL1}	I_{OL} = 3.2 mA			0.4	V	6
High level output voltage	V_{OH1}	I_{OH} = −1.6 mA	4.0			V	
Low level output voltage	V_{OL2}	I_{OL} = 6.4 mA			0.4	V	7
High level output voltage	V_{OH2}	I_{OH} = −3.2 mA	4.0			V	
Low level output voltage	V_{OL3}	I_{OL} = 12.8 mA			0.4	V	8
High level output voltage	V_{OH3}	I_{OH} = −6.4 mA	4.0			V	

NOTES :

1. Applied to inputs (IC, ICD, ICU, OSCI).
2. Applied to inputs (IC, ICD, OSCI).
3. Applied to input (ICU).
4. Applied to inputs (IC, ICU, OSCI).
5. Applied to input (ICD).
6. Applied to outputs (O, OR1, OSCO).
7. Applied to output (OR12).
8. Applied to output (OR14).

PIN FUNCTION

PIN NO.	SYMBOL	I/O	POLARITY	PIN NAME	FUNCTION
1	CLKO	O		Delay-line clock.	A Pin output 1/2 dividing pulse of a reference clock XI (pin 37). To be connected to the clockinput pin of SSG-LSI. At NTSC mode : 14.318 18 MHz (910 fH) At PAL mode : 14.187 50 MHz (908 fH)
2	HD	IC		Horizontal drive pulse	A pin to input the Horizontal reference pulse. To be connected to the HD pin of SSG-LSI.
3	VD	IC		Vertical drive pulse	A pin to input the vertical reference pulse. To be connected to the VD pin of SSG-LSI.
4	V_1	O		Vertical transfer pulse 1	Vertical transfer pulse. To be connected to the 1AX pin of the LR36683N vertical driver LSI.
5	V_2	O		Vertical transfer pulse 2	Vertical transfer pulse. To be connected to the 2AX pin of the LR36683N vertical driver LSI.
6	V_3	O		Vertical transfer pulse 3	Vertical transfer pulse. To be connected to the 3AX pin of the LR36683N vertical driver LSI.
7	GND	–	–	Ground	A grounding pin. To be connected to the GND level.
8	V_4	O		Vertical transfer pulse 4	Vertical transfer pulse. To be connected to the 4AX pin of the LR36683N vertical driver LSI.
9	CH_1	O		Read out pulse	An output pin to transfer the photo diode charge of CCD to the vertical shift register. To be connected to the 1BX pin of the LR36683N vertical driver LSI.
10	CH_2	O		Read out pulse	An output pin to transfer the photo diode charge of CCD to the vertical shift register. To be connected to the 3BX pin of the LR36683N vertical driver LSI.
11	SUB	O		OFD pulse output	A output pin to sweep the photo diode charge of CCD. When electrical shutter is Normal mode, this output becomes High level.
12	R	OR12		Reset pulse	A output pin to reset the CCD output signals. To be connected to ϕ_{RS} pin of the CCD through the DC-offset circuit.
13	RWI	IC	–	Width of FR control input	An input pin to set the width of reset pulse (pin 12).
14	RWO	OR1	–	Width of FR control output	A output pin to set the width of reset pulse (pin 12). It is input to RWI (pin 13) through the RC integral circuit.
15	LHA	OR1		Horizontal transfer last pulse	Horizontal transfer pulse for last-gate of CCD. To be connected to ϕ_{LH1} pin of the CCD area sensor without inverting driver.

PIN NO.	SYMBOL	I/O	POLARITY	PIN NAME	FUNCTION
16	V_{CC}	–	–	Power supply	To be connected to +5 V.
17	HA	OR14		Horizontal transfer pulse 1	Horizontal transfer pulse for CCD. To be connected to ϕ_{H1} pin of the CCD area sensor without inverting driver.
18	HB	OR14		Horizontal transfer pulse 2	Horizontal transfer pulse for CCD. To be connected to ϕ_{H2} pin of the CCD area sensor without inverting driver.
19	GND	–	–	Ground	A grounding pin. To be connected to the GND level.
20	$S1I_1$	IC	–	Phase of DS_1 control input 1	An input pin to set the phase of DS_1 (pin 26) pulse output. It inputs the signal from MCK_4 (pin 23) output through the RC integral circuit.
21	$S1I_2$	IC	–	Phase of DS_1 control input 2	An input pin to set the width of DS_1 (pin 26) pulse output. It inputs the signal from MCK_1 (pin 22) output through the RC integral circuit.
22	MCK_1	O		Clock output 1	A pin to output 1/2 dividing pulse of a reference clock XI (pin 37). It is the same phase with the HA (pin 17).
23	MCK_4	O		Clock output 4	A pin to output 1/2 dividing pulse of reference clock XI (pin 37). It is delayed by approximately 90° in phase with respect HB (pin 18).
24	$S2I_1$	IC	–	Phase of DS_2 control input 1	An input pin to set the phase of DS_2 (pin 27) pulse output. It inputs the signal from MCK_4 (pin 23) output through the RC integral circuit.
25	$S2I_2$	IC	–	Phase of DS_2 control input 2	An input pin to set the phase of DS_2 (pin 27) pulse output. It inputs the signal from MCK_1 (pin 22) output through the RC integral circuit.
26	DS_1	OR1		CDS pulse 1	A pulse to clamp the signals from CCD.
27	DS_2	OR1		CDS pulse 2	A pulse to sample-hold the signals from CCD.
28	SPSW	ICU	–	Phase of SP_1, SP_2 select input	An input pin to switch the SP_1 (pin 34) and SP_2 (pin 35). For details, see "TIMING DIAGRAM (HIGH SPEED PULSE TIMING)".
29	TEST	ICD	–	Test terminal	Testing pin. Set open or to L level in the Normal mode. Typically connected to the GND level.
30	V_{CC}	–	–	Power supply	To be connected to +5 V.
31	GND	–	–	Ground	A grounding pin. To be connected to the GND level.
32	SPO	OR1		Phase of SP_1, SP_2 control output	A pin to output the pulse to set the phase of SP_1 (pin 34) and SP_2 (pin 35).

PIN NO.	SYMBOL	I/O	POLARITY	PIN NAME	FUNCTION
33	SPI	IC	–	Phase of SP_1, SP_2 control input	An input pin to set the pulse of SP_1 (pin 34) and SP_2 (pin 35). It inputs the signal from SPO (pin 32) output through the RC integral circuit.
34	SP_1	OR1	⎍	Color sampling pulse 1	A pin to output the sampling pulse for color demodulation based upon the output signal from CCD. For details, see "TIMING DIAGRAM (HORIZONTAL TIMING)".
35	SP_2	OR1	⎍	Color sampling pulse 2	A pin to output the sampling pulse for color demodulation based upon the output signal from CCD. For details, see "TIMING DIAGRAM (HORIZONTAL TIMING)".
36	PNSW	ICU	–	TV mode select	An input pin to select TV standards. Low level : NTSC mode High level : PAL mode
37	XI	OSCI	⎍⎍	Clock input	A pin for oscillation inverter input. The frequencies are as follows : At NTSC mode : 28.636 36 MHz (1820 fH) At PAL mode : 28.375 00 MHz (1816 fH) (fH = Horizontal frequency)
38	XO	OSCO	⎍⎍	Clock output	A pin for oscillation inverter output.
39	SMD_1	ICD	–	Shutter control 1	An input pin to select of the Shutter mode. For details, see "NOTES (Shutter Speed Control)".
40	SMD_2	ICD	–	Shutter control 2	An input pin to select of the Shutter mode. For details, see "NOTES (Shutter Speed Control)".
41	SMD_3	ICD	–	Shutter control 3	An input pin to select of the Shutter mode. For details, see "NOTES (Shutter Speed Control)".
42	DATA	ICD	–	Shutter speed switching input	An input pin to control the Shutter Speed. For details, see "NOTES (Shutter Speed Control)".
43	DCLK	ICD	–	Shutter speed switching input	An input pin to control the Shutter Speed. For details, see "NOTES (Shutter Speed Control)".
44	FH_2	O	–	Line index pulse	A pin to output the color separate pulse. The signal switches between High and Low at every line. It resets at the 273th line when in NTSC mode, and at the 326th line when in PAL mode.
45	PBLK	O	⎍	Pre-Blanking pulse	Equivalent to CBLK pulse except for shorter pulse width with cut-off falling edge. For details, see "TIMING DIAGRAM".
46	CPPR	O	⎍	Dummy clamp pulse	A pin to output the clamp pulse for CCD dummy signals. For details, see "TIMING DIAGRAM".

PIN NO.	SYMBOL	I/O	POLARITY	PIN NAME	FUNCTION
47	CPOB	O	⎍	Optical Black clamp	A pulse to clamp the optical black signals. For details, see "TIMING DIAGRAM".
48	CPEN	O	⎍	DC clamp pulse	A pin to output the clamp pulse for recovering DC level. The repetition is at a horizontal frequency. For details, see "TIMING DIAGRAM".

IC : Input pin (CMOS level).
ICU : Input pin (CMOS level with pull-up resistor).
ICD : Input pin (CMOS level with pull-down resistor).
O : Output pin.
OR1, OR12, OR14 : Output pin (Through rate controlled buffer).
OSCI : Input pin for oscillation.
OSCO : Output pin for oscillation.

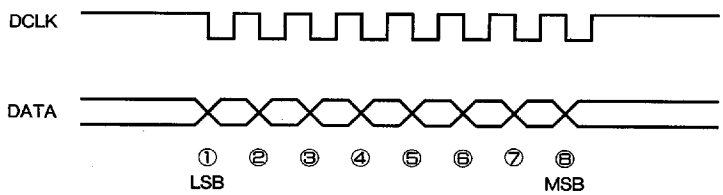
NOTES :

Shutter Speed Control

Pararell data input

SMD_1 (Pin 39)	SMD_2 (Pin 40)	SMD_3 (Pin 41)	SHUTTER SPEED (s)	
			NTSC	PAL
L	L	L	SERIAL CONTROL	SERIAL CONTROL
H	L	L	1/100	1/120
L	H	L	1/250	1/250
H	H	L	1/500	1/500
L	L	H	1/1000	1/1000
H	L	H	1/2000	1/2000
L	H	H	1/4000	1/4000
H	H	H	1/60	1/50

Serial data input

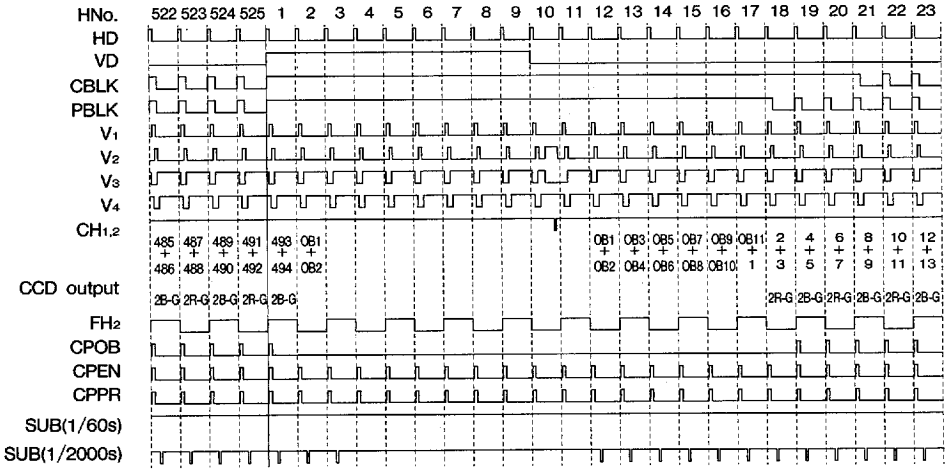


The caluculate method of shutter speed.
NTSC : $(261-2\times n)\times 63.56\ [\mu s]\ (0\leq n\leq 130)$
PAL : $(311-2\times n)\times 64.00\ [\mu s]\ (0\leq n\leq 155)$

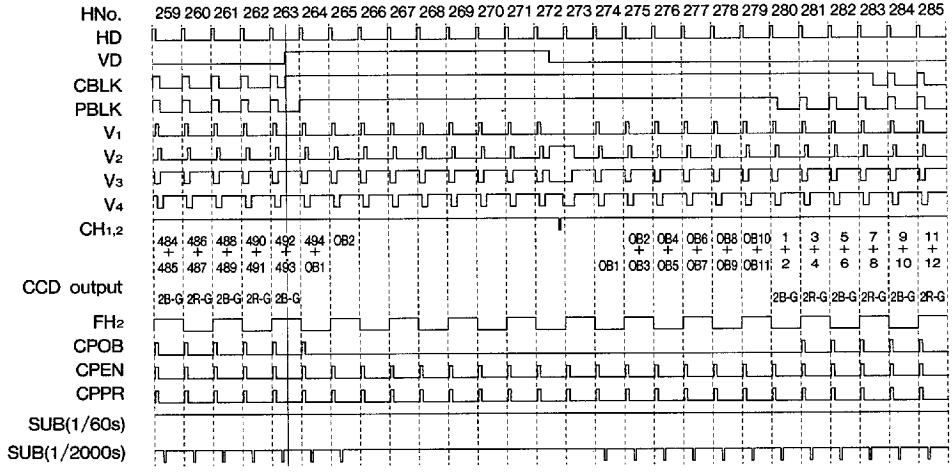
TIMING DAIGRAM

VERTICAL TIMING < NTSC >

(ODD FIELD)

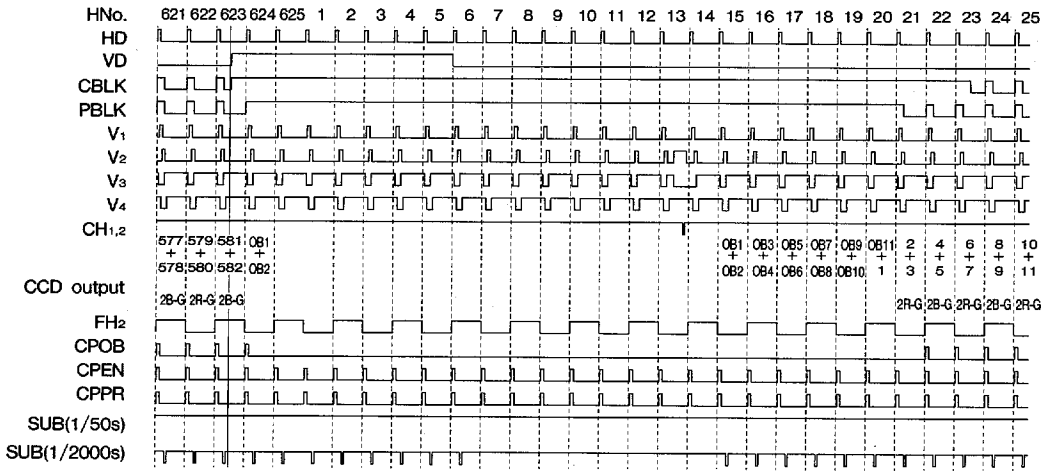


(EVEN FIELD)

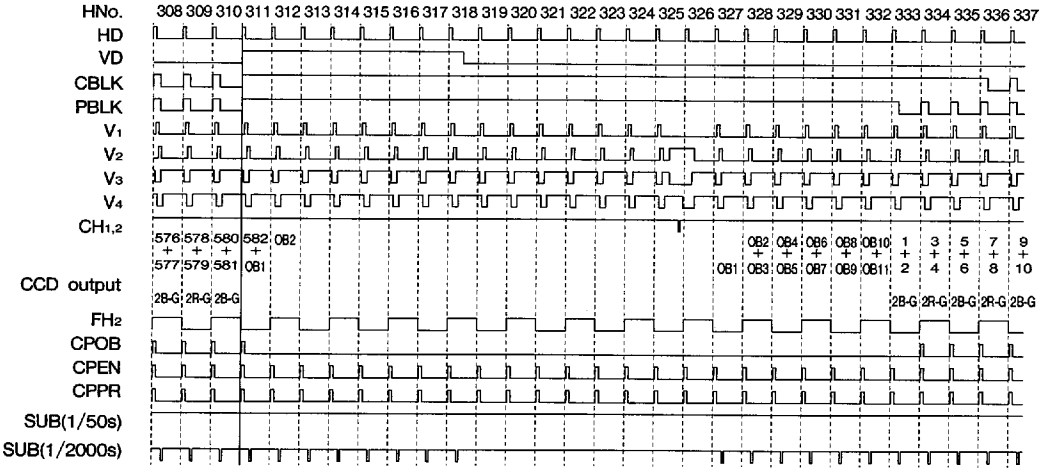


VERTICAL TIMING < PAL >

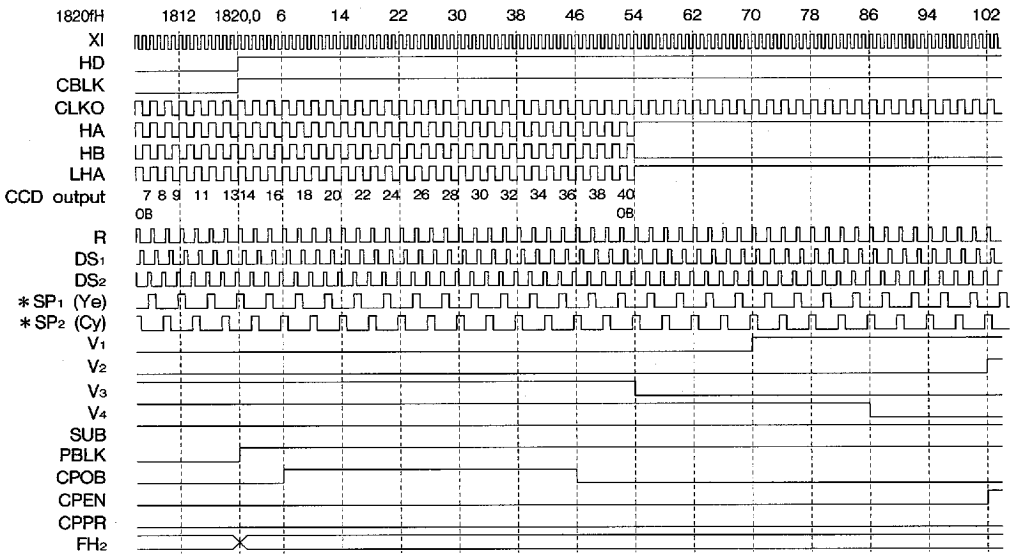
(1st, 3rd FIELD)



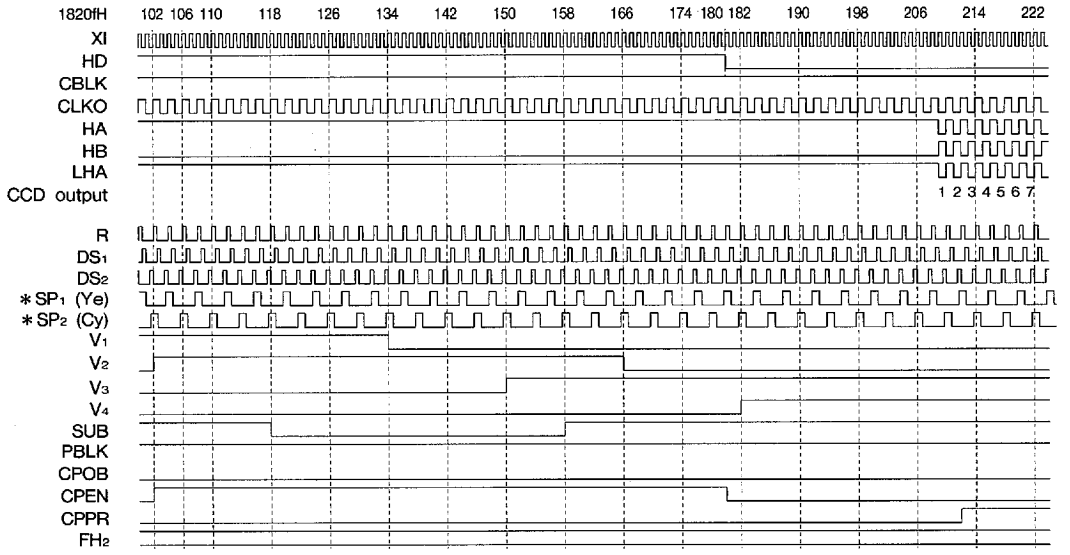
(2nd, 4th FIELD)



HORIZONTAL TIMING < NTSC >

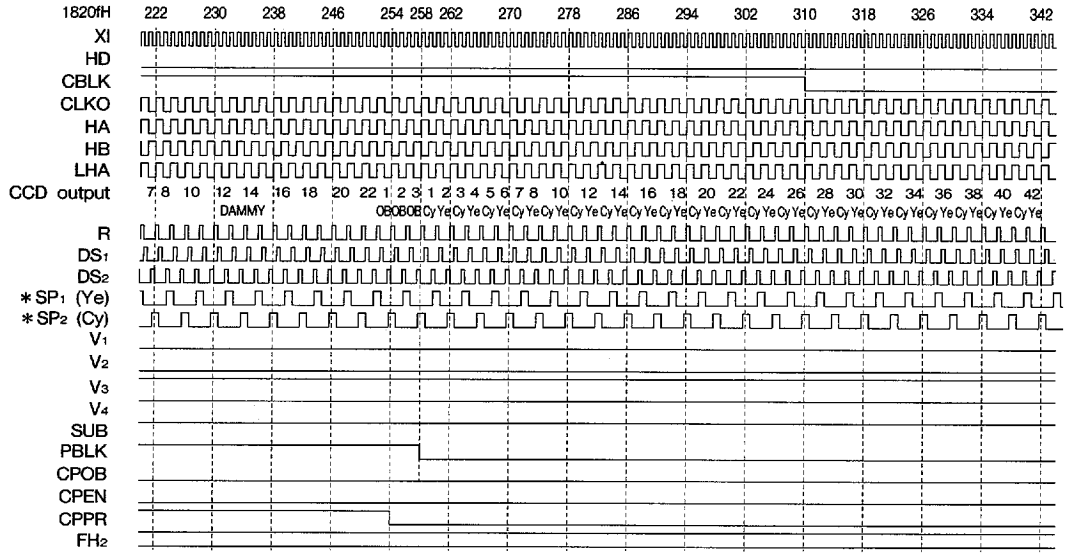


*SPSW = L level



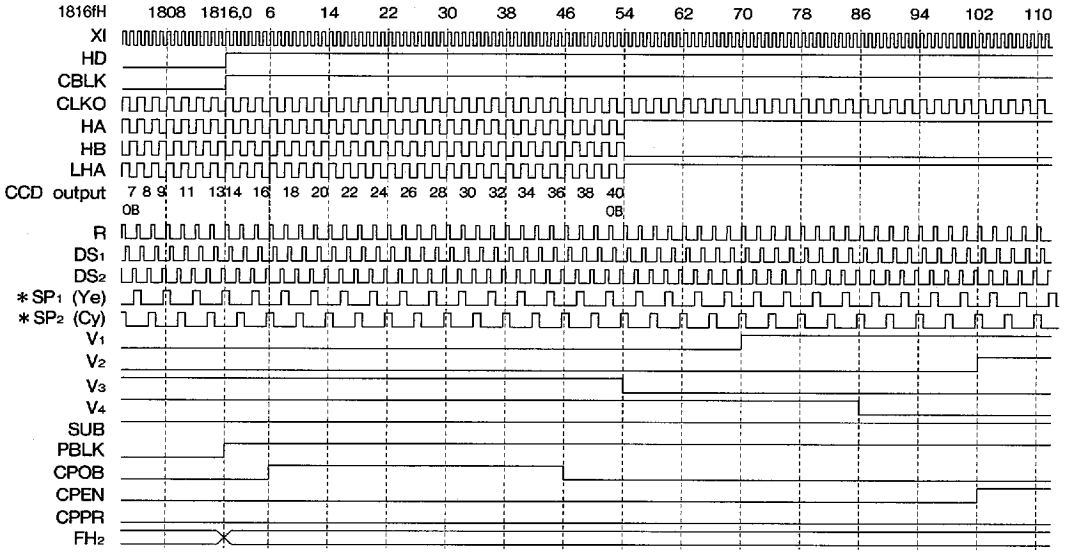
*SPSW = L level

HORIZONTAL TIMING < NTSC > (cont'd)



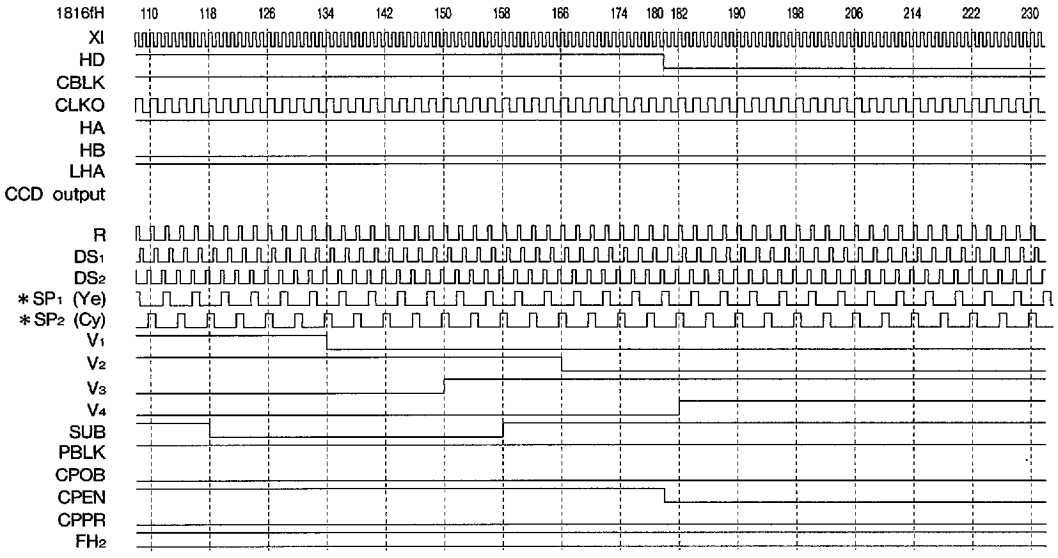
*SPSW = L level

HORIZONTAL TIMING < PAL >

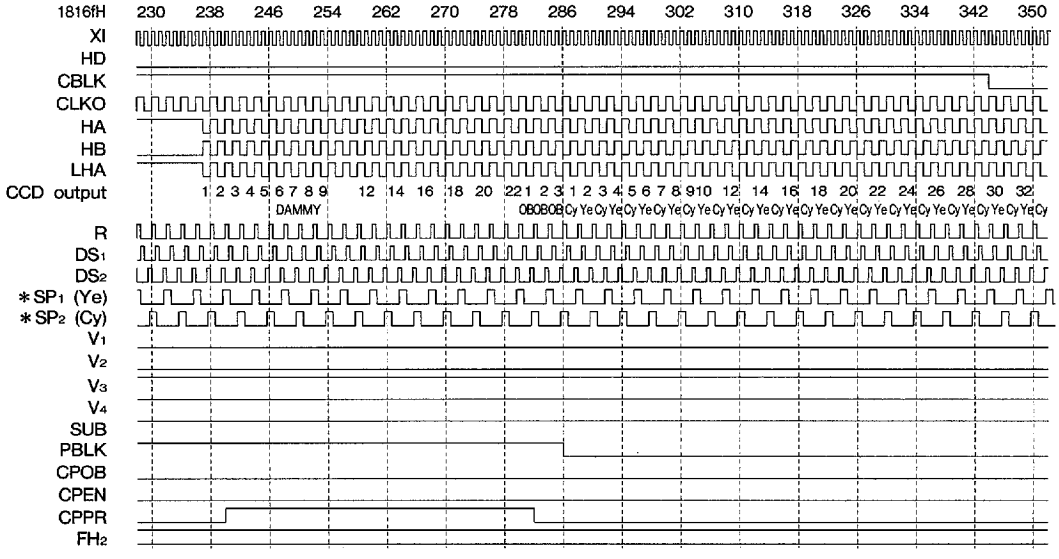


*SPSW = L level

HORIZONTAL TIMING < PAL > (cont'd)



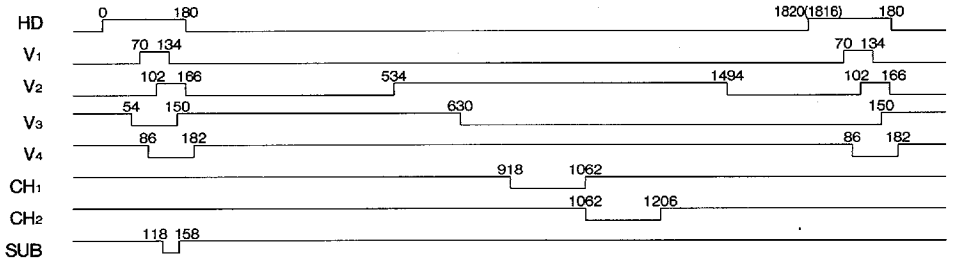
*SPSW = L level



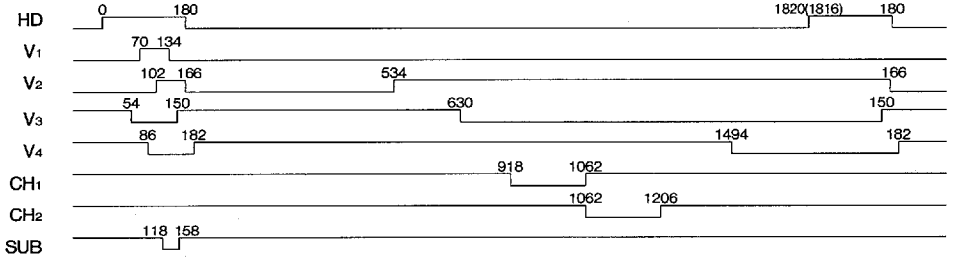
*SPSW = L level

CHARGE READ TIMING ( ) : PAL

(ODD or 1st, 3rd FIELD)



(EVEN or 2nd, 4th FIELD)



HIGH SPEED PULSE TIMING