NexFlash® Technologies, Inc.

PRELIMINARY
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spiflash™

1M-BIT, 2M-BIT AND 4M-BIT
Serial Flash Memory with 40MHz SPI
NX25P10, NX25P20 AND NX25P40

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FEATURES

- **1M / 2M / 4M-bit Serial Flash Memories**
- **Family of Serial Flash Memories**
  - NX25P10: 1M-bit / 128K-byte (131,072) 512 pages
  - NX25P20: 2M-bit / 256K-byte (262,144) 1024 pages
  - NX25P40: 4M-bit / 512K-byte (524,288) 2048 pages
  - 256-bytes per programmable page
  - Compatible migration path to 8M/16M/32M-bit
- **4-pin SPI Serial Interface**
  - Clock, Chip Select, Data In, Data Out
  - Easily interfaces to popular microcontrollers
  - Compatible with SPI Modes 0 and 3
  - Optional Hold function for SPI flexibility
- **Low Power Consumption, Wide Temperature Range**
  - Single 2.7 to 3.6V supply
  - 4mA active current, 1µA Power-down (typ)
  - -40° to +85°C operating range
- **Fast and Flexible Serial Data Access**
  - Clock operation to 40MHz Fast Read, 33MHz Standard Read
  - Byte-addressable Read and Program
  - Auto-increment Read capability
  - Manufacturer and Device ID
- **Programming Features**
  - Page program up to 256 bytes <2ms
  - Sector Erase (64K-byte) 2 seconds
  - Chip erase: 3 seconds (25P10/20), 5 seconds (25P40)
  - 100,000 erase/write cycles
  - Twenty year data retention
- **Software and Hardware Write Protection**
  - Write-Protect all or portion of memory via software
  - Enable/Disable protection with $\overline{WP}$ pin
- **Space Saving Package**
  - Tiny 8-pin SOIC
- **Ideal for systems with limited pins, space, and power**
  - ASIC and Controller-based serial code-download
  - Microcontroller systems storing data, text or voice
  - Battery-operated and portable products

GENERAL DESCRIPTION

The NX25P10 (1M-bit), NX25P20 (2M-bit) and NX25P40 (4M-bit) Serial Flash memories provide a storage solution for systems with limited space, pins and power. They are ideal for code download applications as well as storing voice, text and data. The devices operate on a single 2.7V to 3.6V power supply with current consumption as low as 4mA active and 1µA for power-down. All devices are offered in space-saving 8-pin SOIC type packages as shown below. Contact NexFlash for availability of alternate packages. As part of a family of Serial Flash products, NexFlash also provides a compatible migration path to 8M/16M/32M-bit densities.

The NX25P10/20/40 array is organized into 512/1024/2048 programmable pages of 256-bytes each. A single byte or, up to 256 bytes, can be programmed at a time using the Page Program instruction. Pages are grouped into 2/4/8 erasable sectors of 256 pages (64K-byte) each as shown in figure 1. Both Sector Erase and Bulk (full chip) Erase instructions are supported.

The Serial Peripheral Interface (SPI) consists of four pins (Serial Clock, Chip Select, Serial Data In and Serial Data Out) that support high speed serial data transfers up to 40MHz. A Hold pin, Write Protect pin and programmable write protect features provide further control flexibility. Additionally, the device can be queried for manufacturer and device ID. Special customer ID (for copy authentication) and factory programming is available, contact NexFlash for more information.

8-Pin SOIC 150-mil (Package Code N)

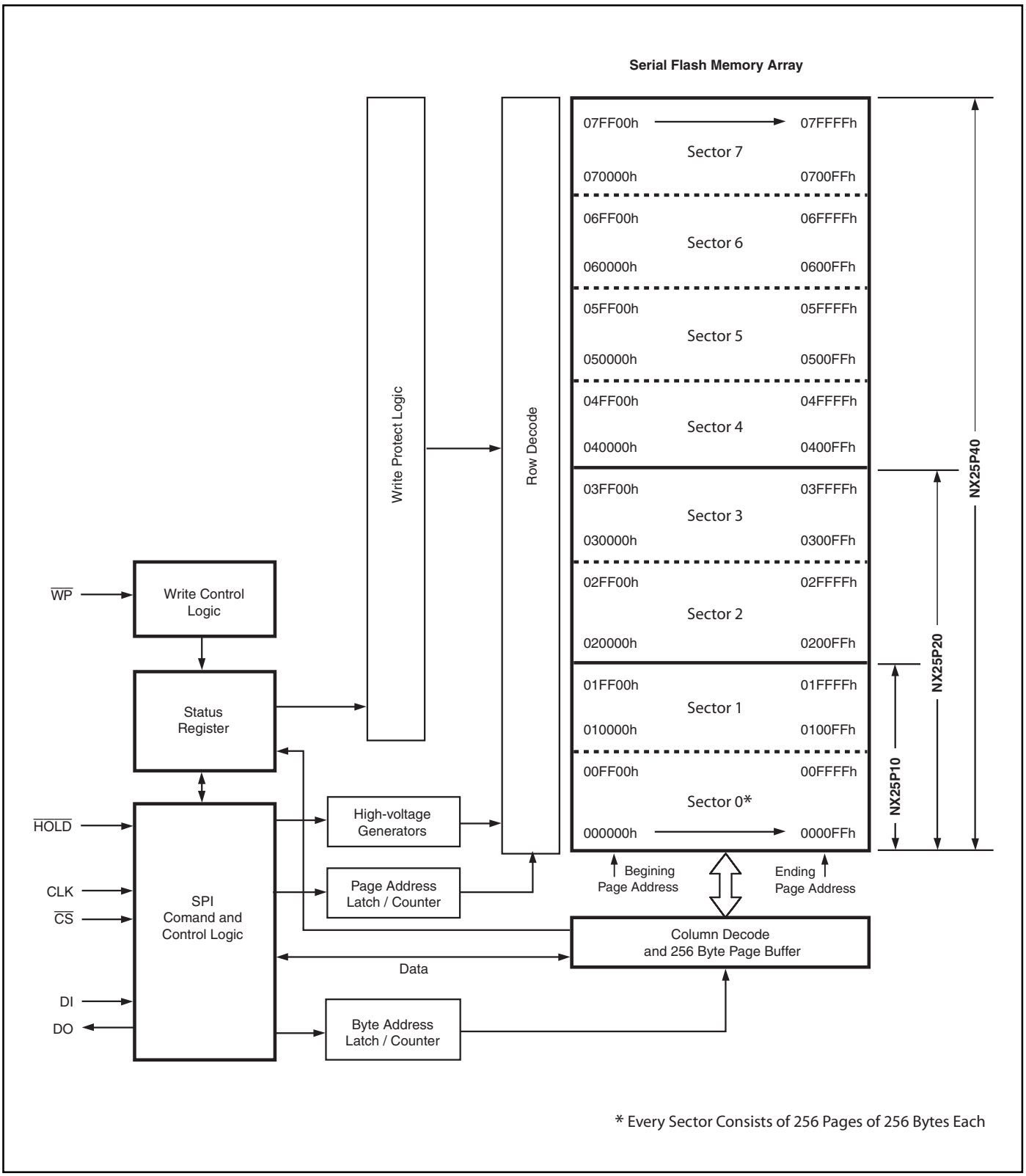


Figure 1. NX25P10, NX25P20 and NX25P40 Block Diagram

PIN DESCRIPTIONS

Package Types
The standard package for the NX25P10/20/40 is an 8-pin plastic SOIC with 150 mil body (NexFlash package code N). It also allows a package migration path to higher density Serial Flash devices. The pinout for the "N" package is shown in Figure 2. Package diagrams and dimensions are illustrated at the end of this data sheet. Optional 8-contact MLP packages may be available. Please contact NexFlash for further MLP package information.

Serial Data Input (DI)
The SPI Serial Data Input (DI) pin provides a means for instructions, addresses and data to be serially written to (shifted into) the device. Data is latched on the rising edge of the Serial Clock (CLK) input pin.

Serial Data Output (DO)
The SPI Serial Data Output (DO) pin provides a means for data and status to be serially read from (shifted out of) the device. Data is shifted out on the falling edge of the Serial Clock (CLK) input pin.

Serial Clock (CLK)
The SPI Serial Clock Input (CLK) pin provides the timing for serial input and output operations. ("See SPI "Operations")

Chip Select ($\overline{CS}$)
The SPI Chip Select ($\overline{CS}$) pin enables and disables device operation. When $\overline{CS}$ is high the device is deselected and the Serial Data Output (DO) pin is at high impedance. When deselected, the devices power consumption will be at standby levels unless an internal erase, program or status register cycle is in progress. When $\overline{CS}$ is brought low the device will be selected, power consumption will increase to active levels and instructions can be written to and data read from the device. After power-up, $\overline{CS}$ must transition from high to low before a new instruction will be accepted. The $\overline{CS}$ input must track the Vcc supply level at power-up (see "Write Protection" and figure 17). If needed a pull-up resister on $\overline{CS}$ can be used to accomplish this.

Hold ($\overline{HOLD}$)
The $\overline{HOLD}$ pin allows the device to be paused while it is actively selected. When $\overline{HOLD}$ is brought low, while $\overline{CS}$ is low, the DO pin will be at high impedance and signals on the DI and CLK pins will be ignored (don't care). When $\overline{HOLD}$ is brought high, device operation can resume. The hold function can be useful when multiple devices are sharing the same SPI signals. ("See Hold function")

Write Protect ($\overline{WP}$)
The Write Protect ($\overline{WP}$) pin can be used to prevent the Status Register from being written. Used in conjunction with the Status Register's Block Protect (BP0 and BP1) bits and Status Register Protect (SRP) bits, a portion or the entire memory array can be hardware protected. The $\overline{WP}$ pin is active low.

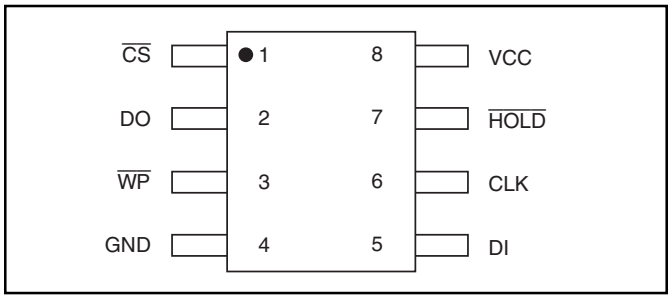


Figure 2. NX25P10, NX25P20 and NX25P40 Pin Assignments, 8-pin SOIC (Package Code N)

Table 1. Pin Descriptions

DI	Data Input
DO	Data Output
CLK	Serial Clock Input
$\overline{CS}$	Chip Select Input
$\overline{WP}$	Write Protect Input
$\overline{HOLD}$	Hold Input
Vcc, GND	Power Supply

SPI OPERATION

SPI Modes

The NX25P10/20/40 is accessed through an SPI compatible bus consisting of four signals: Serial Clock (CLK), Chip Select ($\overline{CS}$), Serial Data Input (DI) and Serial Data Output (DO). Both SPI bus operation Modes 0 (0,0) and 3 (1,1) are supported. The primary difference between Mode 0 and Mode 3 concerns the normal state of the CLK signal when the SPI bus master is in standby and data is not being transferred to the Serial Flash. For Mode 0 the CLK signal is normally low. For Mode 3 the CLK signal is normally high. In either case data input on the DI pin is sampled on the rising edge of the CLK. Data output on the DO pin is clocked out on the falling edge of CLK.

Hold Function

The $\overline{HOLD}$ signal allows the NX25P10/20/40 operation to be paused while it is actively selected (when $\overline{CS}$ is low). The hold function may be useful in cases where the SPI data and clock signals are shared with other devices. For example, consider if the page buffer was only partially written when a priority interrupt requires use of the SPI bus. In this case the hold function can save the state of the instruction and the data in the buffer so programming can resume where it left off once the bus is available again.

To initiate a hold condition, the device must be selected with $\overline{CS}$ low. A hold condition will activate on the falling edge of the $\overline{HOLD}$ signal if the CLK signal is already low. If the CLK is not already low the hold condition will activate after the next falling edge of CLK. The hold condition will terminate on the rising edge of the hold signal if the CLK signal is already low. If the CLK is not already low the hold condition will terminate after the next falling edge of CLK.

During a hold condition, the Serial Data Output (DO) is high impedance, and Serial Data Input (DI) and Serial Clock (CLK) are ignored. The Chip Select ($\overline{CS}$) signal should be kept active (low) for the full duration of the hold operation to avoid resetting the internal logic state of the device.

WRITE PROTECTION

Applications that use non-volatile memory must take into consideration the possibility of noise and other adverse system conditions that may compromise data integrity. To address this concern the NX25P10/20/40 provides several means to protect data from inadvertent writes.

Write Protect Features

- Device resets when Vcc is below threshold.
- Time delay write disable after Power-up.
- Write enable/disable instructions.
- Automatic write disable after program and erase.
- Software write protection using Status Register.
- Hardware write protection using Status Register and $\overline{WP}$ pin.
- Write Protection using Power-down instruction.

Upon power-up or at power-down the NX25P10/20/40 will maintain a reset condition while Vcc is below the threshold value of V_{WI}, (See Power-up Timing and Voltage Levels: Table 7 and Figure 17). While reset, all operations are disabled and no instructions are recognized. During power-up and after the Vcc voltage exceeds V_{WI}, all program and erase related instructions are further disabled for a time delay of t_{PUW}. This includes the Write Enable, Page Program, Sector Erase, Bulk Erase and the Write Status Register instructions. Note that the chip select pin ($\overline{CS}$) must track the Vcc supply level at power-up until the Vcc-min level and t_{VSL} time delay is reached. If needed a pull-up resister on $\overline{CS}$ can be used to accomplish this.

After power-up the device in automatically placed in a write-disabled state with the Status Register Write Enable Latch (WEL) set to a 0. A Write Enable instruction must be issued before a Page Program, Sector Erase, Bulk Erase or Write Status Register instruction will be accepted. After completing a program, erase or write instruction the Write Enable Latch (WEL) is automatically cleared to a write-disabled state of 0.

Software controlled write protection is facilitated using the Write Status Register instruction and setting the Status Register Protect (SRP) and Block Protect (BP0, BP2) bits. These Status Register bits allow a portion or all of the memory to be configured as read only. Used in conjunction with the Write Protect ($\overline{WP}$) pin, changes to the Status Register can be enabled or disabled under hardware control. See Status Register for further information.

Additionally, the Power-down instruction offers an extra level of write protection as all instructions are ignored except for the Release Power-down instruction.

STATUS REGISTER

The Read Status Register instruction can be used to provide status on the availability of the Flash memory array, if the device is write enabled or disabled, and the state of write protection. The Write Status Register instruction can be used to configure the devices write protection features. See Figure 3.

BUSY
BUSY is a read only bit in the status register (S0) that is set to a 1 state when the device is executing a Page Program, Sector Erase, Bulk Erase or Write Status Register instruction. During this time the device will ignore further instructions except for the Read Status Register instruction (see t_W, t_{PP}, t_{SE} and t_{BE} in AC Characteristics). When the program, erase or write status register instruction has completed, the BUSY bit will be cleared to a 0 state indicating the device is ready for further instructions.

Write Enable Latch (WEL)
Write Enable Latch (WEL) is a read only bit in the status register (S1) that is set to a 1 after executing a Write Enable Instruction. The WEL status bit is cleared to a 0 when the device is write disabled. A write disable state occurs upon power-up or after any of the following instructions: Write Disable, Page Program, Sector Erase, Bulk Erase and Write Status Register.

Block Protect Bits (BP2, BP1, BP0)
The Block Protect Bits (BP2, BP1, BP0) are non-volatile read/write bits in the status register (S4, S3, S2) that provide Write Protection control and status. Block Protect bits can be set using the Write Status Register Instruction (see tW in AC characteristics). All, none or a portion of the memory array can be protected from Program and Erase instructions (see table 2). The factory default setting for the Block Protection Bits is 0, none of the array protected. The Block Protect bits can not be written to if the Status Register Protect (SRP) bit is set to 1 and the Write Protect ($\overline{WP}$) pin is low. The NX25P20 and NX25P10 do not use BP2.

Reserved Bits
Status register bit locations 5 and 6 are reserved for future use. Current devices will read 0 for these bit locations. It is recommended to mask out the reserved bit when testing the Status Register. Doing this will ensure compatibility with future devices.

Status Register Protect (SRP)
The Status Register Protect (SRP) bit is a non-volatile read/write bit in the status register (S7) that can be used in conjunction with the Write Protect ($\overline{WP}$) pin to disable writes to the status register. When the SRP bit is set to a 0 state (factory default) the $\overline{WP}$ pin has no control over the status register. When the SRP pin is set to a 1, the Write Status Register instruction is locked out while the $\overline{WP}$ pin is low. When the $\overline{WP}$ pin is high the Write Status Register instruction is allowed.

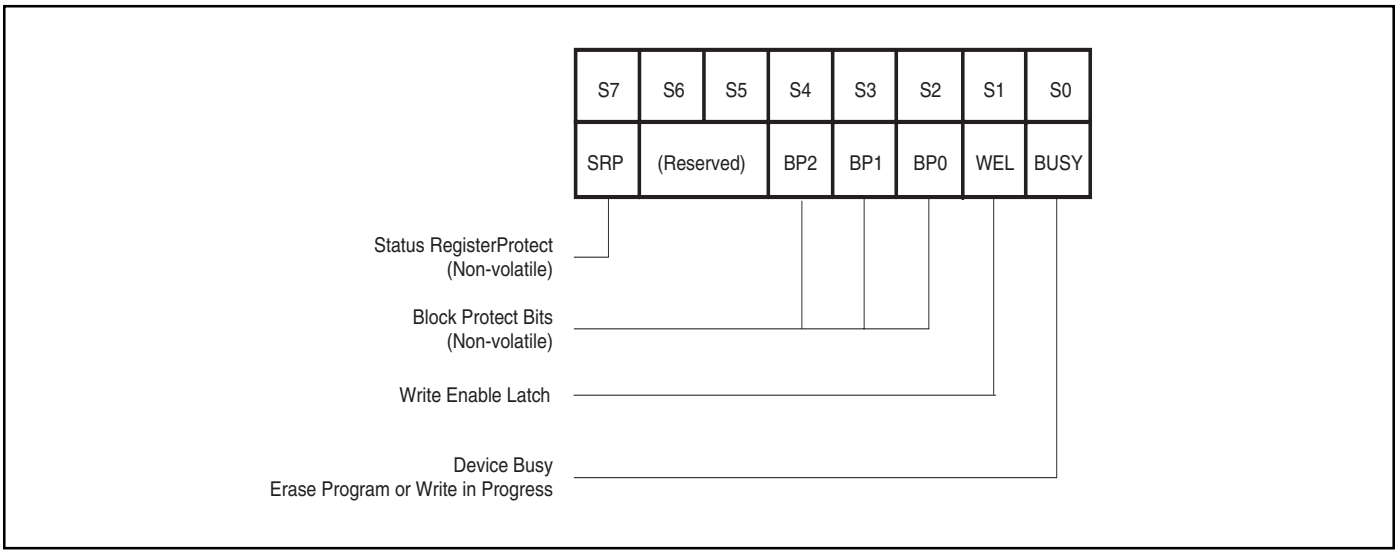


Figure 3. Status Register Bit Locations

Table 2: Status Register Memory Protection

Status Register (1)			NX25P40 (4M-bit) Memory Protection			
BP2	**BP1**	**BP0**	**Sector(s)**	**Addresses**	**Density**	**Portion**
0	0	0	NONE	NONE	NONE	NONE
0	0	1	7	070000h - 07FFFFh	512K-bit	Upper 1/8
0	1	0	6 and 7	060000h - 07FFFFh	1M-bit	Upper 1/4
0	1	1	4 thru 7	040000h - 07FFFFh	2M-bit	Upper 1/2
1	x	x	ALL	000000h - 07FFFFh	4M-bit	ALL

Status Register (1)			NX25P20 (2M-bit) Memory Protection			
BP2	**BP1**	**BP0**	**Sector(s)**	**Addresses**	**Density**	**Portion**
x	0	0	NONE	NONE	NONE	NONE
x	0	1	3	030000h - 03FFFFh	512K-bit	Upper 1/4
x	1	0	2 and 3	020000h - 03FFFFh	1M-bit	Upper 1/2
x	1	1	ALL	000000h - 03FFFFh	2M-bit	ALL

Status Register (1)			NX25P10 (1M-bit) Memory Protection			
BP2	**BP1**	**BP0**	**Sector(s)**	**Addresses**	**Density**	**Portion**
x	0	x	NONE	NONE	NONE	NONE
x	1	0	NONE	NONE	NONE	NONE
x	1	1	ALL	000000h - 01FFFFh	1M-bit	ALL

Notes:
1. x = don't care.

INSTRUCTIONS

The instruction set of the NX25P10/20/40 consists of twelve basic instructions that are fully controlled through the SPI bus (see Table 3). Instructions are initiated with the falling edge of Chip Select ($\overline{CS}$). The first byte of data clocked into the DI input provides the instruction code. Data on the DI input is sampled on the rising edge of clock with most significant bit (MSB) first.

Instructions vary in length from a single byte to several bytes and may be followed by address bytes, data bytes, dummy bytes (don't care), and in some cases, a combination. Instructions are completed with the rising edge of edge $\overline{CS}$. Clock relative timing diagrams for each instruction are included in figures 5 through 17. All read instructions can be completed after any clocked bit. However, all instructions that Write, Program or Erase must complete on a byte boundary ($\overline{CS}$ driven high after a full 8-bits have been clocked) otherwise the instruction will be terminated. This feature further protects the device from inadvertent writes. Additionally, while the memory is being programmed or erased, or when the Status Register is being written, all instructions except for Read Status Register will be ignored until the program or erase cycle has completed.

Table 4: Manufacturer and Device Identification

Manufacturer ID	(M7-M0)
NexFlash	EFh
Device ID	**(ID7-ID0)**
NX25P10	10h
NX25P20	11h
NX25P40	12h

Table 3: Instruction Set (1)

Instruction Name	Byte 1 Code	Byte 2 (5)	Byte 3	Byte 4	Byte 5	Byte 6	n-Bytes
Write Enable	06h						
Write Disable	04h						
Read Status Register	05h	(S7–S0)(1)					(2)
Write Status Register	01h	S7–S0					
Read Data	03h	A23–A16	A15–A8	A7–A0	(D7–D0)	(Next byte)	continuous
Fast Read	0Bh	A23–A16	A15–A8	A7–A0	dummy	(D7–D0)	(Next Byte) continuous
Page Program	02h	A23–A16	A15–A8	A7–A0	(D7–D0)	(Next byte)	up to 256 bytes
Sector Erase	D8h	A23–A16	A15–A8	A7–A0(6)			
Bulk Erase	C7h						
Power-down	B9h						
Release Power-down and Device ID	ABh	dummy	dummy	dummy	(ID7-ID0)		(3)
Manufacturer/Device ID	90h	dummy	dummy	00h	(M7-M0)	(ID7-ID0)	(4)

Notes:
1. Data bytes are shifted with Most Significant Bit first. Byte fields with data in parenthesis "( )" indicate data being read from the device on the DO pin.
2. The Status Register contents will repeat continuously until $\overline{CS}$ terminate the instruction.
3. The Device ID will repeat continuously until $\overline{CS}$ terminate the instruction.
4. The Manufacturer ID and Device ID bytes will repeat continuously until $\overline{CS}$ terminate the instruction.
5. Unused upper address bits must be set to a 0 for the NX25P10.
6. The lowest 16 address bits (A15-A0) must be set to 0.

Write Enable (06h)

The Write Enable instruction (Figure 4) sets the Write Enable Latch (WEL) bit in the Status Register to a 1. The WEL bit must be set prior to every Page Program, Sector Erase, Bulk Erase and Write Status Register instruction.

The Write Enable instruction is entered by driving $\overline{CS}$ low, shifting the instruction code "06h" into the Data Input (DI) pin on the rising edge of CLK, and then driving $\overline{CS}$ high.

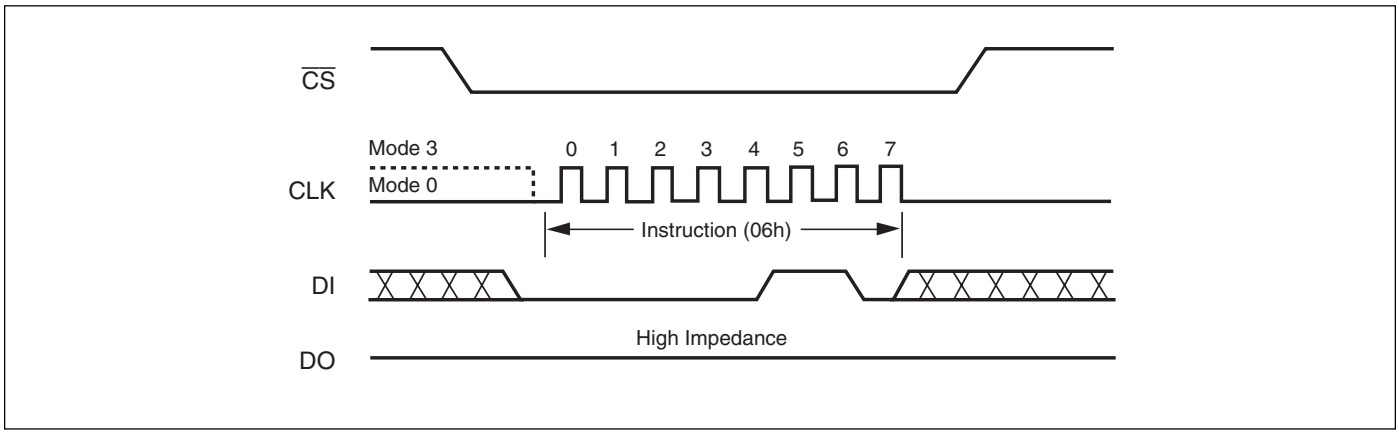


Figure 4. Write Enable Instruction Sequence Diagram

Write Disable (04h)

The Write Disable instruction (Figure 5) resets the Write Enable Latch (WEL) bit in the Status Register to a 0. The Write Disable instruction is entered by driving $\overline{CS}$ low, shifting the instruction code "04h" into the DI pin and then driving $\overline{CS}$ high. Note that the WEL bit is automatically reset after Power-up and upon completion of the Write Status Register, Page Program, Sector Erase, and Bulk Erase instructions.

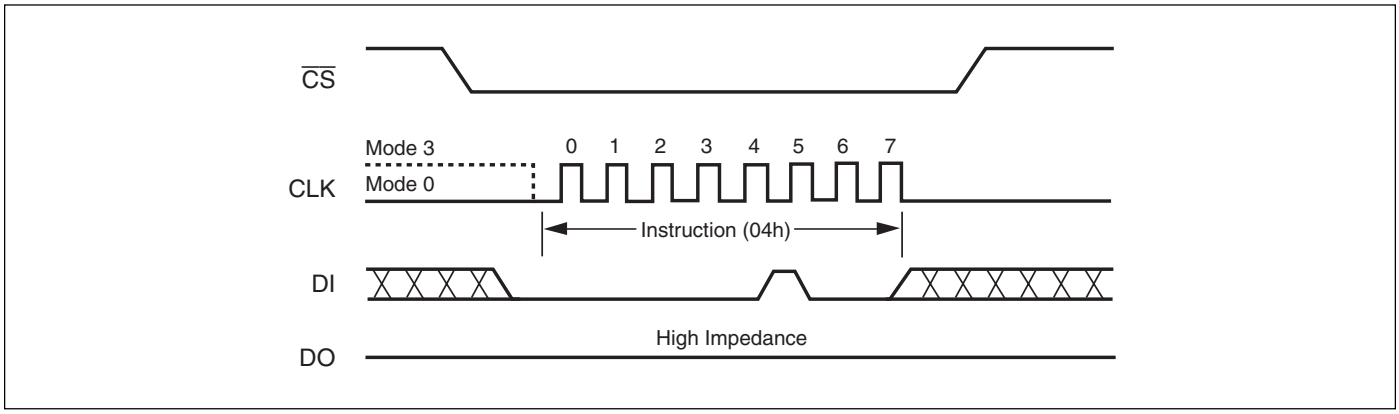


Figure 5. Write Disable Instruction Sequence Diagram

Read Status Register (05h)

The Read Status Register instruction allows the 8-bit Status Register to be read. The instruction is entered by driving $\overline{CS}$ low and shifting the instruction code "05h" into the DI pin on the rising edge of CLK. The status register bits are then shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first as shown in figure 6. The Status Register bits are shown in figure 3 and include the BUSY, WEL, BPO-BP2, and STP bits (see description of the Status Register earlier in this data sheet).

The Status Register instruction may be used at any time, even while a Program, Erase or Write Status Register cycle is in progress. This allows the BUSY status bit to be checked to determine when the cycle is complete and if the device can accept another instruction. The Status Register can be read continuously, as shown in Figure 6. The instruction is completed by driving $\overline{CS}$ high.

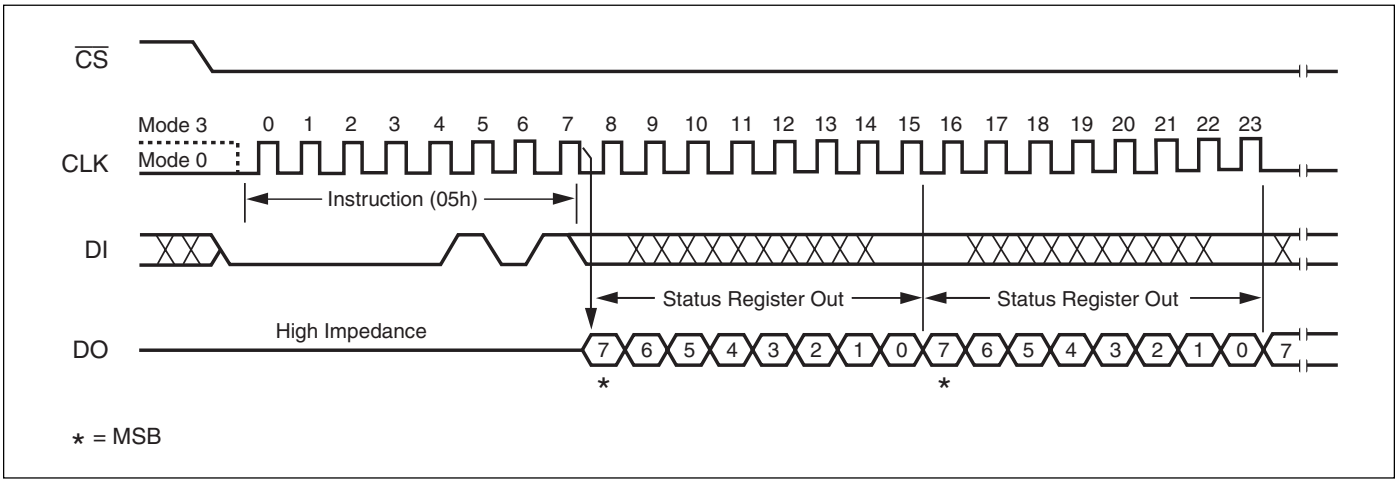


Figure 6. Read Status Register Instruction Sequence Diagram

Write Status Register (01h)

The Write Status Register instruction allows the Status Register to be written. A Write Enable instruction must previously have been executed for the device to accept the Write Status Register Instruction (Status Register bit WEL must equal 1). Once write enabled, the instruction is entered by driving $\overline{CS}$ low, sending the instruction code "01h", and then writing the status register data byte as illustrated in figure 7. The Status Register bits are shown in figure 3 and described earlier in this data sheet.

For the NX25P40, only non-volatile Status Register bits STP, BP2, BP1 and BP0 (bits 7, 4, 3 and 2) can be written to. For the NX25P20 and NX25P10 only Status Register bits STP, BP1 and BP0 (bits 7, 3 and 2) can be written to. All other Status Register bit locations are read-only and will not be affected by the Write Status Register instruction.

The $\overline{CS}$ pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Write Status Register instruction will not be executed. After $\overline{CS}$ is driven high, the self-timed Write Status Register cycle will commence for a time duration of tw (See AC Characteristics).

While the Write Status Register cycle is in progress, the Read Status Register instruction may still accessed to check the status of the BUSY bit. The BUSY bit is a 1 during the Write Status Register cycle and a 0 when the cycle is finished and ready to accept other instructions again. After the Write Register cycle has started the Write Enable Latch (WEL) bit in the Status Register will be cleared to 0.

The Write Status Register instruction allows the Block Protect bits (BP2, BP1 and BP0) to be set for protecting all, a portion, or none of the memory from erase and program instructions. Protected areas become read-only (see table 2). The Write Status Register instruction also allows the Status Register Protect bit (SRP) to be set. This bit is used in conjunction with the Write Protect ($\overline{WP}$) pin to disable writes to the status register. When the SRP bit is set to a 0 state (factory default) the $\overline{WP}$ pin has no control over the status register. When the SRP pin is set to a 1, the Write Status Register instruction is locked out while the $\overline{WP}$ pin is low. When the $\overline{WP}$ pin is high the Write Status Register instruction is allowed.

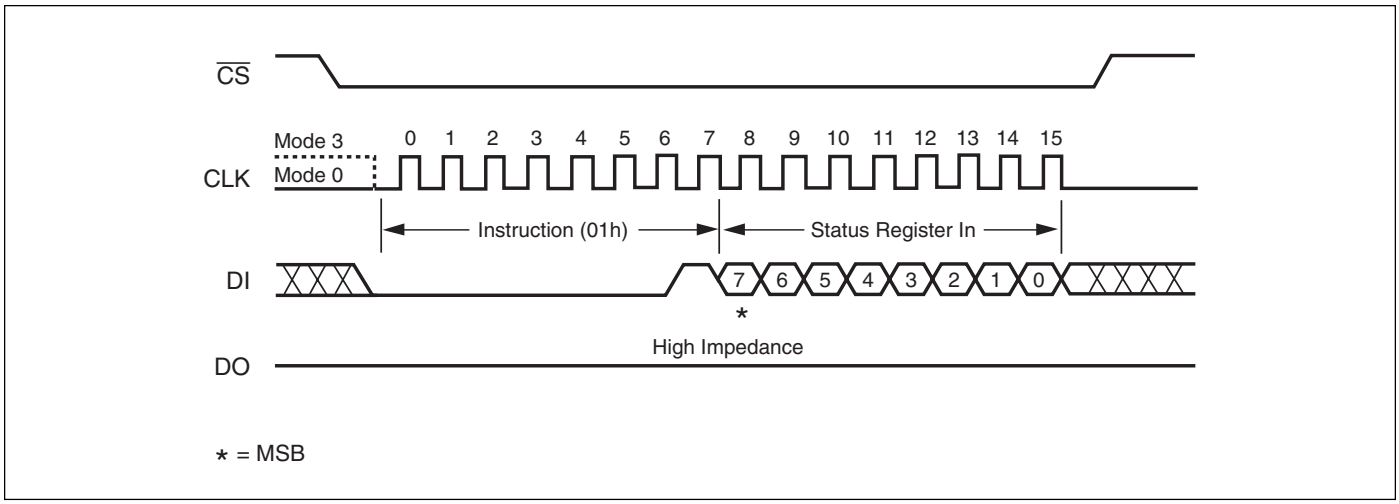


Figure 7. Write Status Register Instruction Sequence Diagram

Read Data (03h)

The Read Data instruction allows one or more data bytes to be sequentially read from the memory. The instruction is initiated by driving the $\overline{CS}$ pin low and then shifting the instruction code "03h" followed by a 24-bit address (A23-A0) into the DI pin. The code and address bits are latched on the rising edge of the CLK pin. After the address is received, the data byte of the addressed memory location will be shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first. The address is automatically incremented to the next higher address after each byte of data is shifted out allowing for a continuous stream of data. This means that the entire memory can be accessed with a single instruction as long as the clock continues. The instruction is completed by driving $\overline{CS}$ high. The Read Data instruction sequence is shown in figure 8. If a Read Data instruction is issued while an Erase, Program or Write cycle is in process (BUSY=1) the instruction is ignored and will not have any effects on the current cycle. The Read Data instruction allows clock rates from D.C. to a maximum of f_R (see AC Electrical Characteristics).

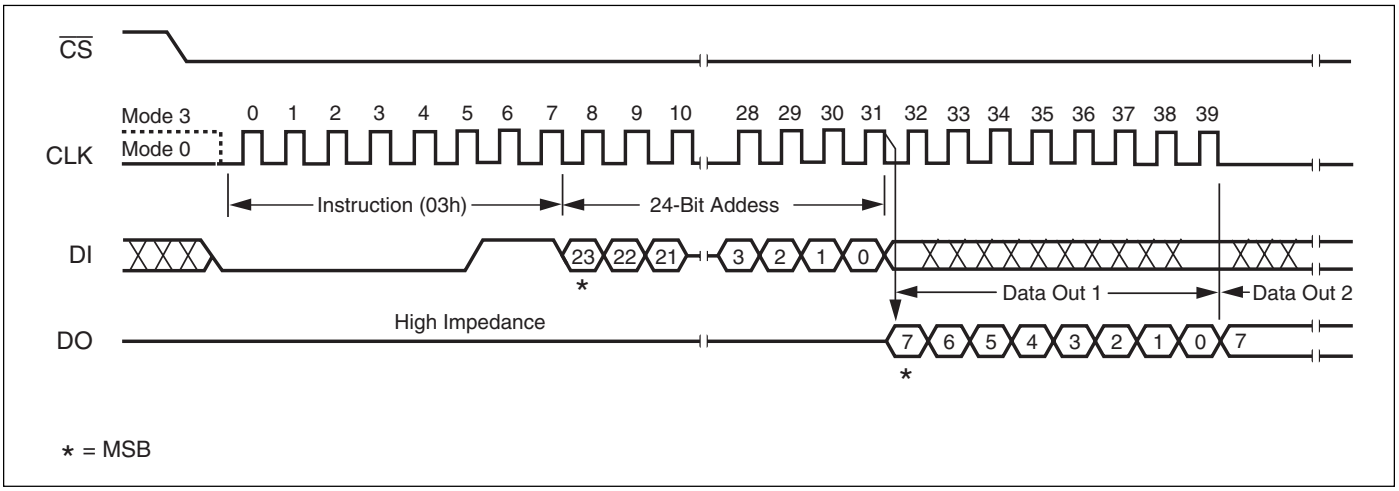


Figure 8. Read Data Instruction Sequence Diagram

Fast Read (0Bh)

The Fast Read instruction is similar to the Read Data instruction except that it can operate at the highest possible frequency of F_R (see AC Electrical Characteristics). This is accomplished by adding a "dummy" byte after the 24-bit address as shown in figure 9. The dummy byte allows the devices internal circuits additional time for setting up the initial address. The dummy byte data value on the DI pin is a "don't care".

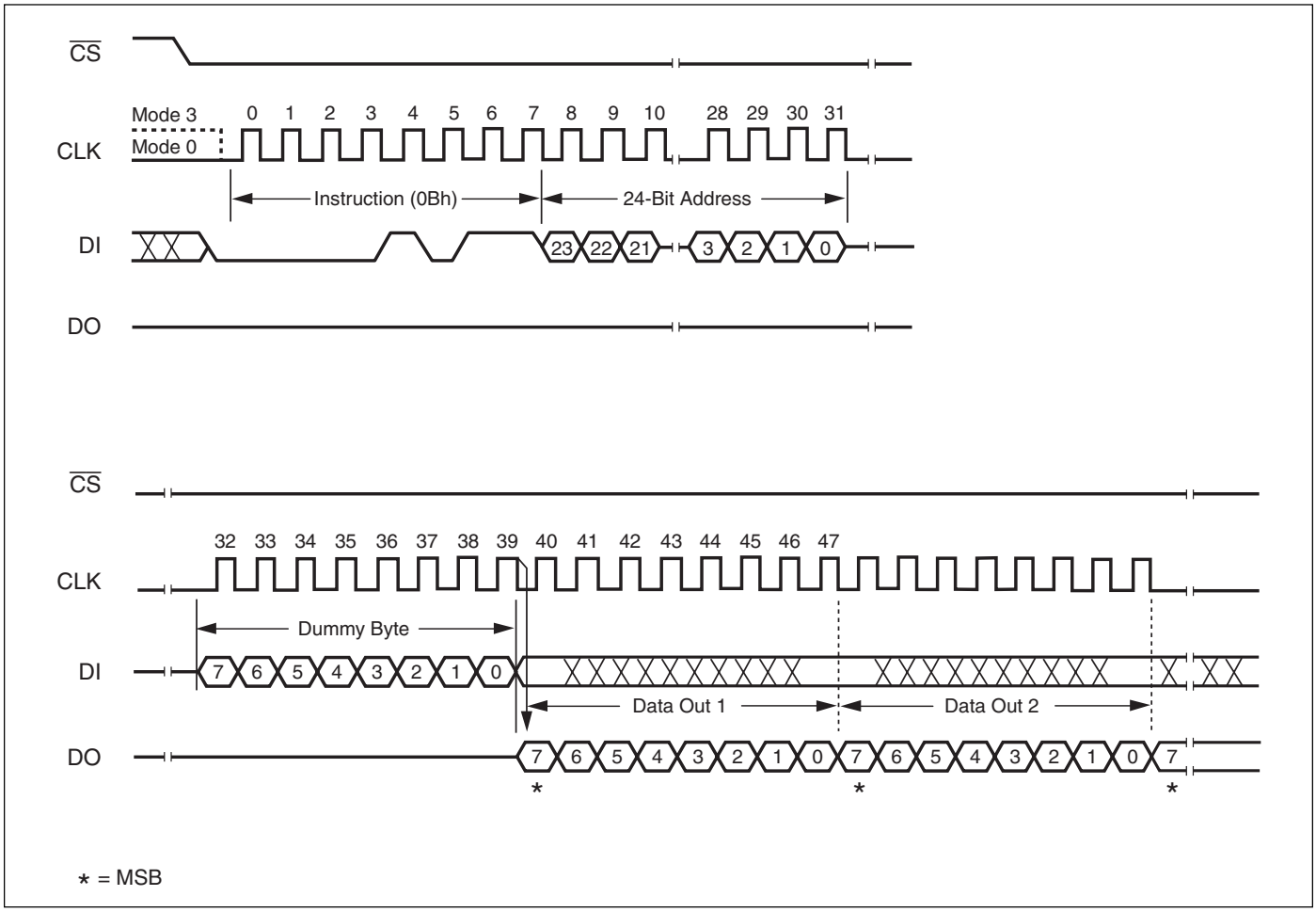


Figure 9. Fast Read Instruction Sequence Diagram

Page Program (02h)

The Page Program instruction allows from one byte to 256 bytes of data to be programmed at memory locations previously erased to all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Page Program Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the $\overline{CS}$ pin low then shifting the instruction code "02h" followed by a 24-bit address (A23-A0) and at least one data byte, into the DI pin. The $\overline{CS}$ pin must be driven low for the entire length of the instruction while data is being sent to the device. The Page Program instruction sequence is shown in figure 10.

If an entire 256 byte page is to be programmed, the last address byte (the 8 least significant address bits) should be set to 0. If the last address byte is not zero, and the number of clocks exceed the remaining page length, the addressing will wrap to the beginning of the page. Less than 256 bytes can be programmed without having any effect on other bytes within the same page. If more than 256 bytes are sent to the device the addressing will wrap to the beginning of the page and overwrite previously sent data.

As with the write and erase instructions, the $\overline{CS}$ pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Page Program instruction will not be executed. After $\overline{CS}$ is driven high, the self-timed Page Program instruction will commence for a time duration of tpp (See AC Characteristics). While the Page Program cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Page Program cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Page Program cycle has started the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Page Program instruction will not be executed if the addressed page is protected by the Block Protect (BP2, BP1, BP0) bits (see Table 2).

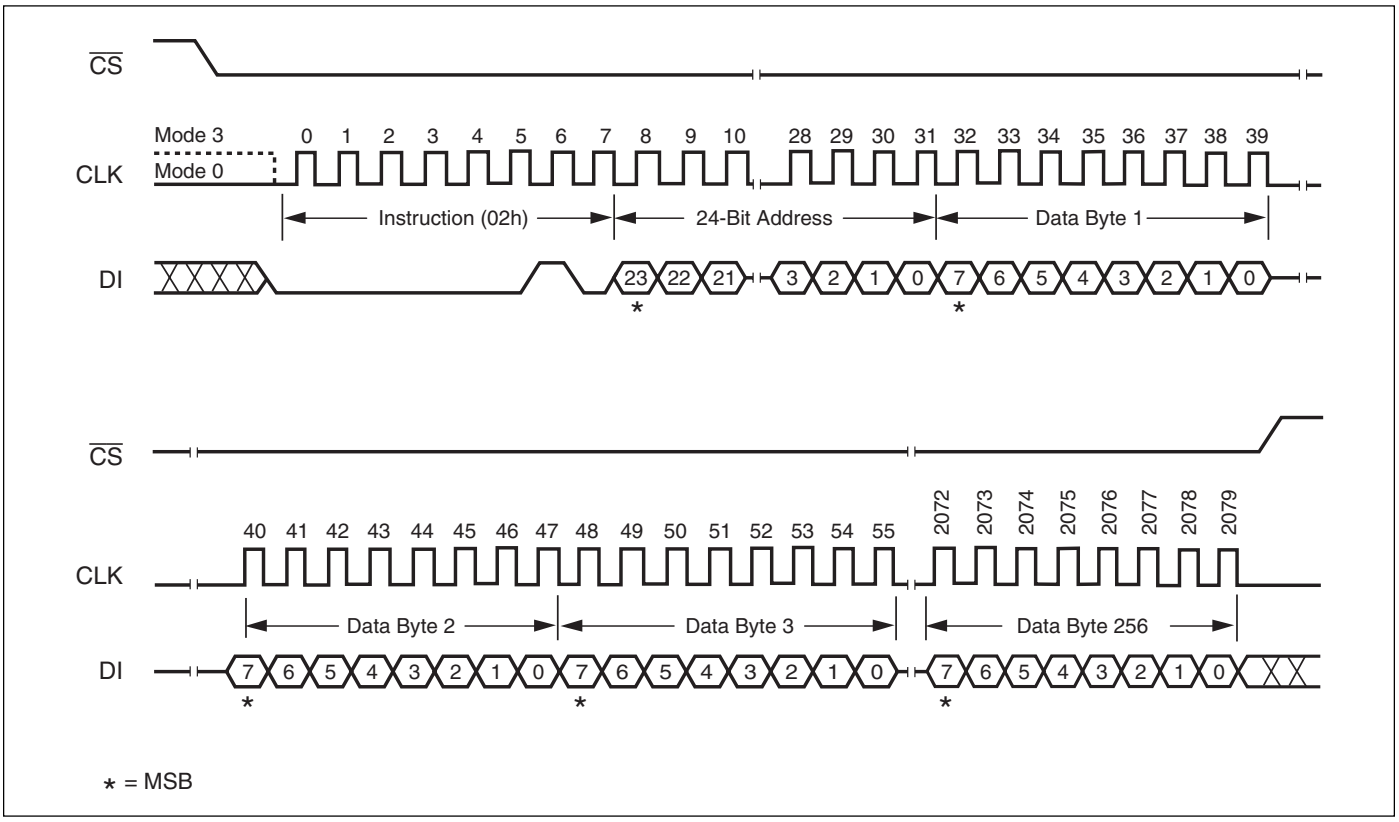


Figure 10. Page Program Instruction Sequence Diagram

Sector Erase (D8h)

The Sector Erase instruction sets all memory within a specified sector to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Erase Sector Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the $\overline{CS}$ pin low and shifting the instruction code "D8h" followed a 24-bit sector address (A23-A0) (see Figure 1). The lowest 16 address bits (A15-A0) must be set to 0. The Sector Erase instruction sequence is shown in figure 11.

The $\overline{CS}$ pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Sector Erase instruction will not be executed. After $\overline{CS}$ is driven high, the self-timed Sector Erase instruction will commence for a time duration of t_{SE} (See AC Characteristics). While the Sector Erase cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Sector Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Sector Erase cycle has started the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Sector Erase instruction will not be executed if the addressed page is protected by the Block Protect (BP2, BP1, BP0) bits (see Table 2).

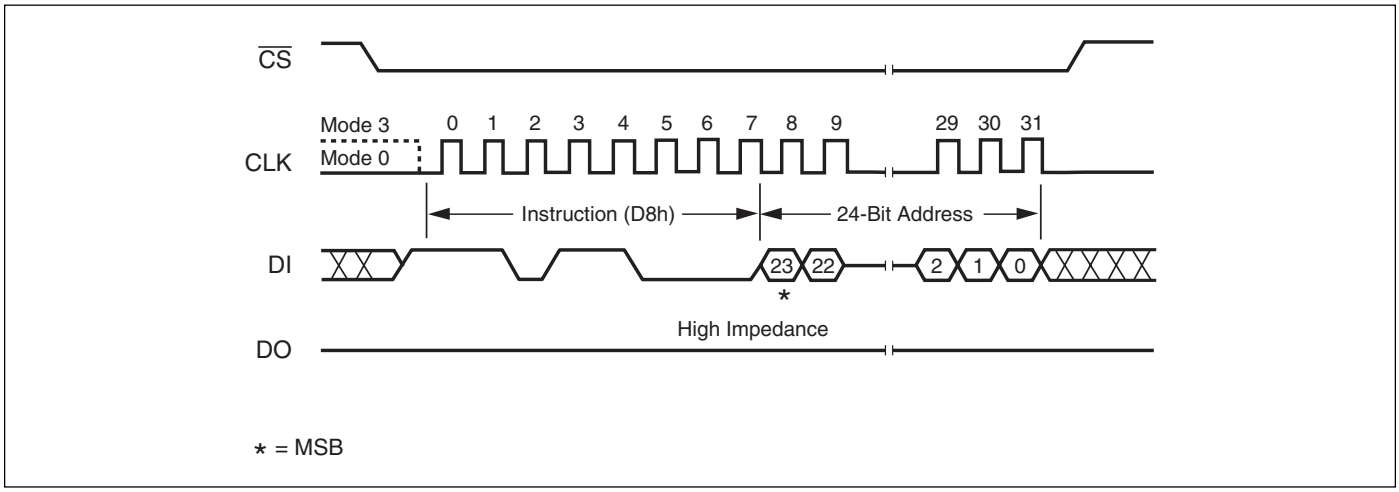


Figure 11. Sector Erase Instruction Sequence Diagram

Bulk Erase (C7h)

The Bulk Erase instruction sets all memory within the device to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Bulk Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the $\overline{CS}$ pin low and shifting the instruction code "C7h". The Bulk Erase instruction sequence is shown in figure 12.

The $\overline{CS}$ pin must be driven high after the eighth bit has been latched. If this is not done the Bulk Erase instruction will not be executed. After $\overline{CS}$ is driven high, the self-timed Bulk Erase instruction will commence for a time duration of t_{BE} (See AC Characteristics). While the Bulk Erase cycle is in progress, the Read Status Register instruction may still be accessed to check the status of the BUSY bit. The BUSY bit is a 1 during the Bulk Erase cycle and becomes a 0 when finished and the device is ready to accept other instructions again. After the Bulk Erase cycle has started the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Bulk Erase instruction will not be executed if any page is protected by the Block Protect (BP2, BP1, BP0) bits (see Table 2).

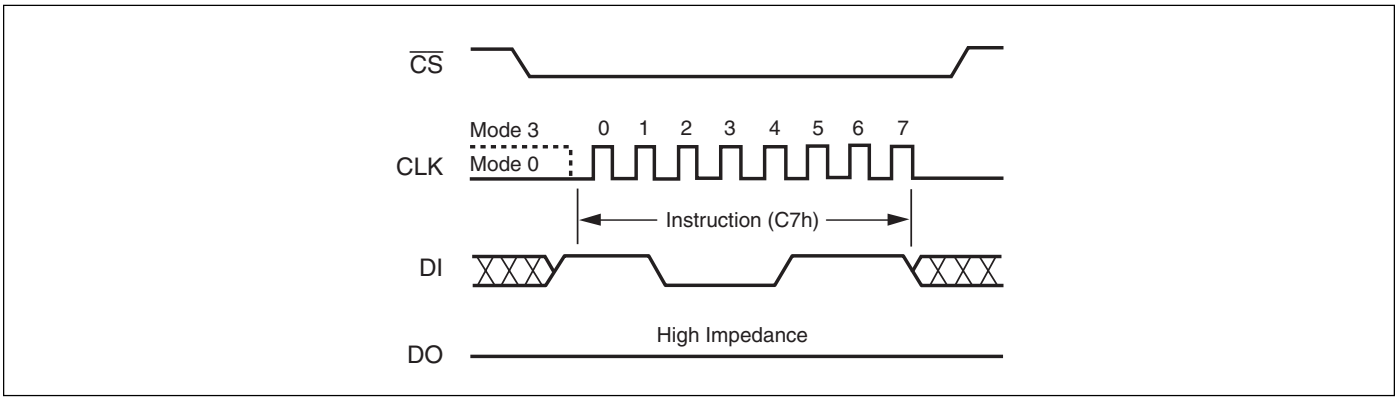


Figure 12. Bulk Erase Instruction Sequence Diagram

Power-down (B9h)

Although the standby current during normal operation is relatively low, standby current can be further reduced with the Power-down instruction. The lower power consumption makes the Power-down instruction especially useful for battery powered applications (See ICC1 and ICC2 in AC Characteristics). The instruction is initiated by driving the $\overline{CS}$ pin low and shifting the instruction code "B9h" as shown in figure 13.

The $\overline{CS}$ pin must be driven high after the eighth bit has been latched. If this is not done the Power-down instruction will not be executed. After $\overline{CS}$ is driven high, the power-down state will entered within the time duration of t_{DP} (See AC Characteristics). While in the power-down state only the Release from Power-down / Device ID instruction, which restores the device to normal operation, will be recognized. All other instructions are ignored. This includes the Read Status Register instruction, which is always available during normal operation. Ignoring all but one instruction makes the Power Down state a useful condition for securing maximum write protection. The device always powers-up in the normal operation with the standby current of ICC1.

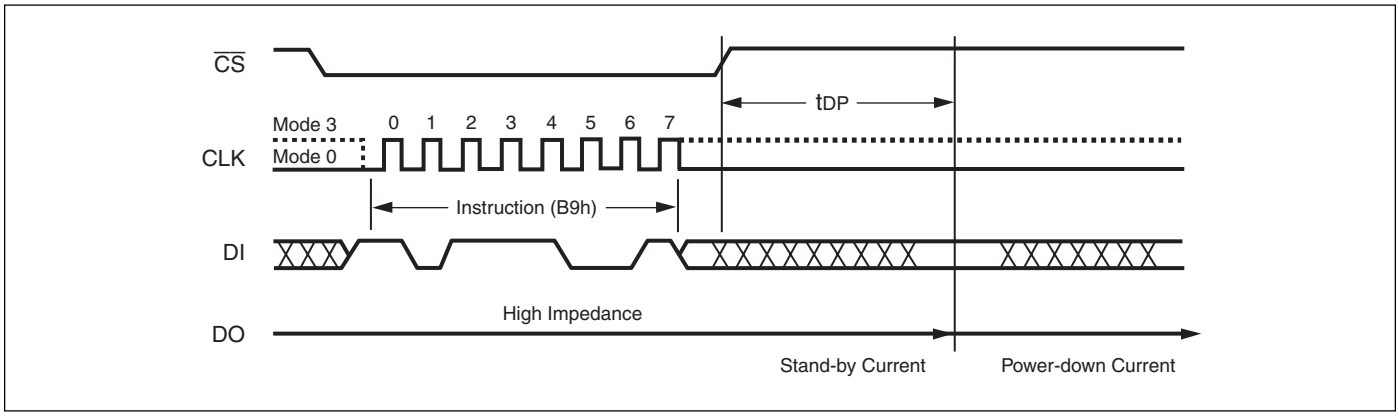


Figure 13. Deep Power-down Instruction Sequence Diagram

Release Power-down / Device ID (ABh)

The Release from Power-down / Device ID instruction is a multi-purpose instruction. It can be used to release the device from the power-down state, obtain the devices electronic identification (ID) number or do both.

When used only to release the device from the power-down state, the instruction is issued by driving the $\overline{CS}$ pin low, shifting the instruction code "ABh" and driving $\overline{CS}$ high as shown in figure 14. After the time duration of t_{RES1} (See AC Characteristics) the device will resume normal operation and other instructions will be accepted. The $\overline{CS}$ pin must remain high during the t_{RES1} time duration.

When used only to obtain the Device ID while not in the power-down state, the instruction is initiated by driving the $\overline{CS}$ pin low and shifting the instruction code "ABh" followed by 3-dummy bytes. The Device ID bits are then shifted out on the falling edge of CLK with most significant bit (MSB) first as shown in figure 15. The Device ID values for the NX25P10, NX25P20, and NX25P40 are listed in Table 4. The Device ID can be read continuously. The instruction is completed by driving $\overline{CS}$ high.

When used to release the device from the power-down state and obtain the Device ID, the instruction is the same as previously described, and shown in figure 13, except that after $\overline{CS}$ is driven high it must remain high for a time duration of t_{RES2} (See AC Characteristics). After this time duration the device will resume normal operation and other instructions will be accepted.

If the Release from Power-down / Device ID instruction is issued while an Erase, Program or Write cycle is in process (when BUSY equals 1) the instruction is ignored and will not have any effects on the current cycle.

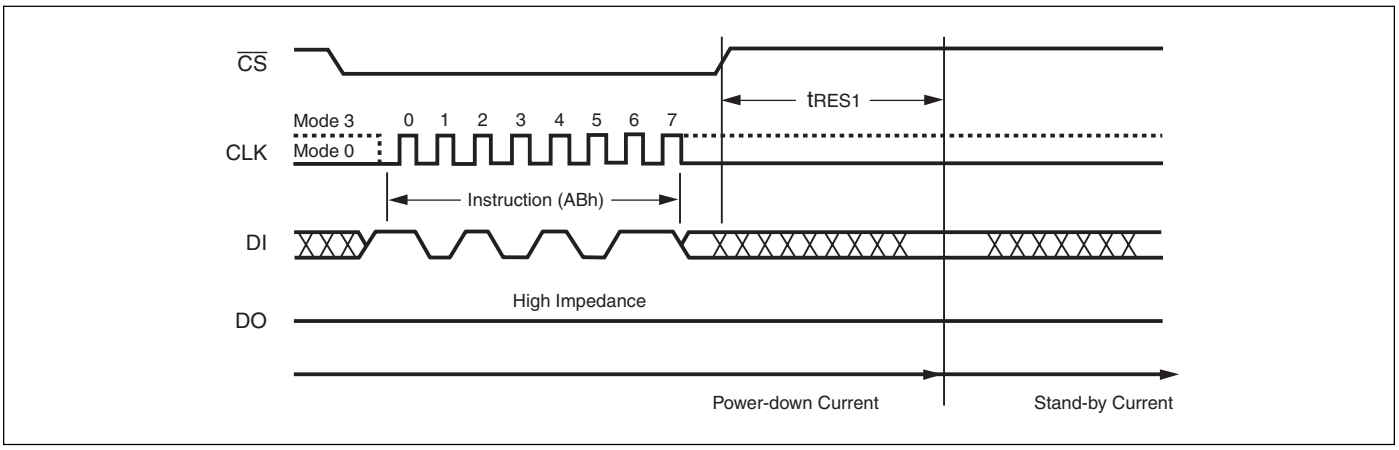


Figure 14. Release Power-down Instruction Sequence

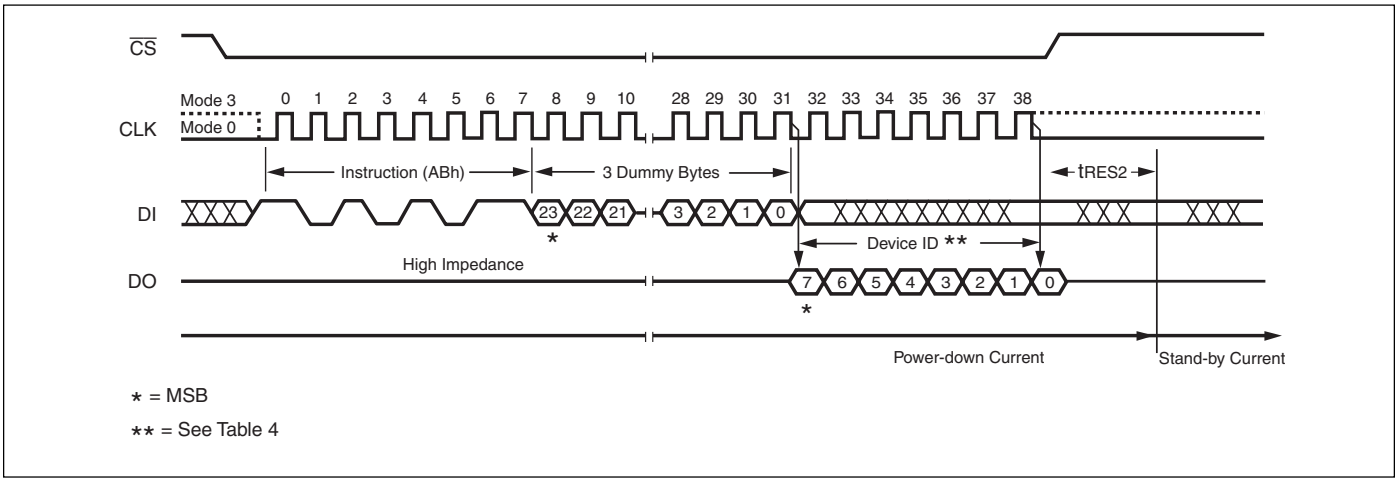


Figure 15. Release Power-down / Device ID Instruction Sequence Diagram

Read Manufacturer / Device ID (90h)

The Read Manufacturer/Device ID instruction is an alternative to the Release from Power-down / Device ID instruction that provides both the JEDEC assigned manufacturer ID and the specific device ID.

The Read Manufacturer/Device ID instruction is very similar to the Release from Power-down / Device ID instruction. The instruction is initiated by driving the $\overline{CS}$ pin low and shifting the instruction code "90h" followed by a 24-bit address (A23-A0) of 000000h. After which, the Manufacturer ID for NexFlash (EFh) and the Device ID are shifted out on the falling edge of CLK with most significant bit (MSB) first as shown in figure 16. The Device ID values for the NX25P10, NX25P20, and NX25P40 are listed in Table 4. If the 24-bit address is initially set to 000001h the Device ID will be read first and then followed by the Manufacturer ID. The Manufacturer and Device IDs can be read continuously, alternating from one to the other. The instruction is completed by driving $\overline{CS}$ high.

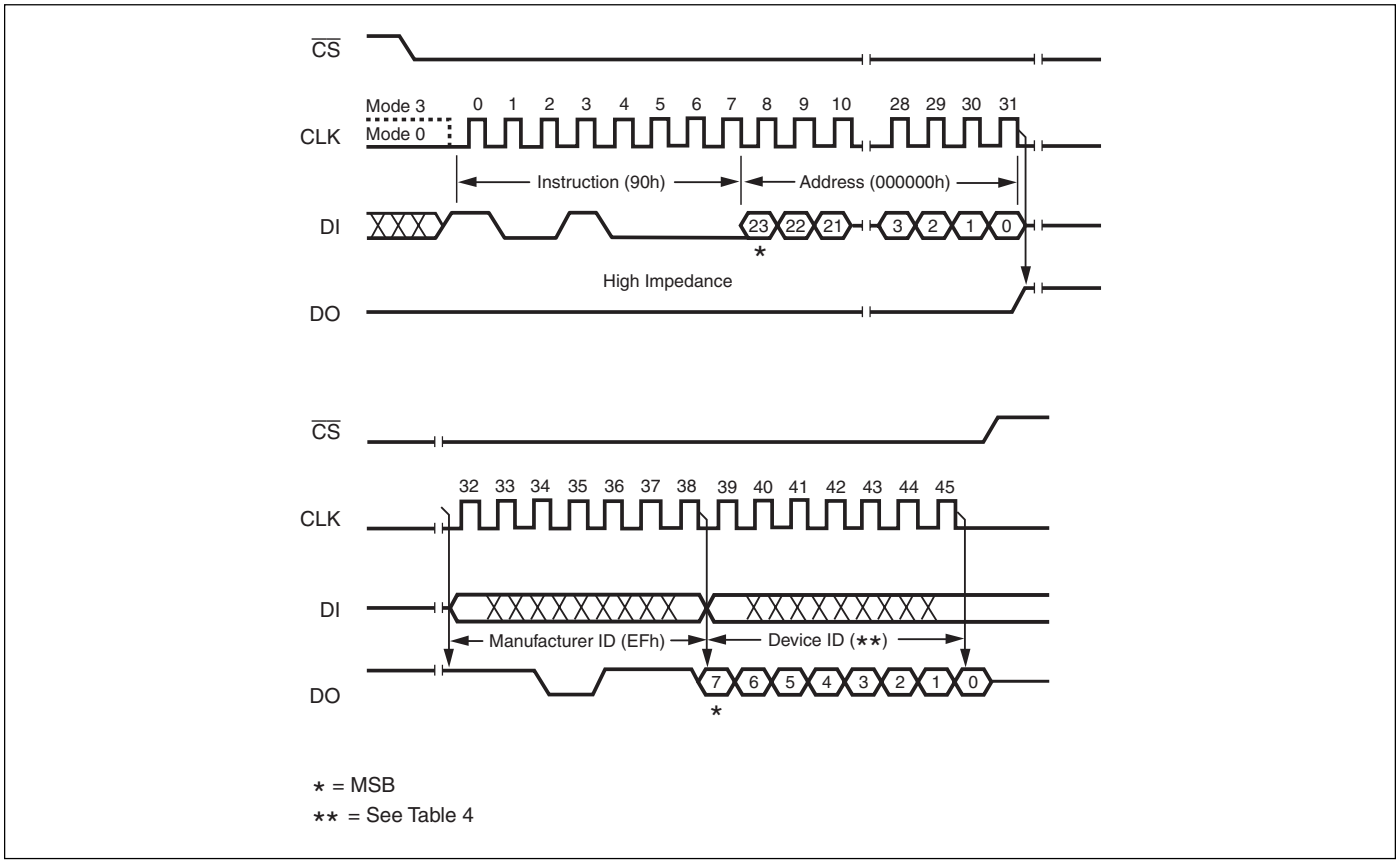


Figure 16. Read Manufacturer / Device ID Diagram

SPECIFICATIONS AND TIMING DIAGRAMS

Table 5. Absolute Maximum Ratings (1)

Symbol	Parameters	Conditions	Range	Unit
Vcc	Supply Voltage		–0.6 to +4.0	V
V_{IO}	Voltage Applied to Any Pin	Relative to Ground	–0.6 to Vcc + 0.4	V
T_{STG}	Storage Temperature		–65 to +150	°C
T_{LEAD}	Lead Temperature		See Note 2	°C
V_{ESD}	Electrostatic Discharge Voltage	Human Body Model(3)	–2000 to +2000	V

Note:
1. This device has been designed and tested for the specified operation ranges. Proper operation outside of these levels is not guaranteed. Exposure beyond absolute maximum ratings (listed above) may cause permanent damage.
2. Compliant with JEDEC Standard J-STD-20C for small body Sn-Pb or Pb-free (Green) assembly and the European directive on restrictions on hazardous substances (RoHS) 2002/95/EU.
3. JEDEC Std JESD22-A114A (C1=100 pF, R1=1500 ohms, R2=500 ohms).

Table 6. Operating Ranges

Symbol	Parameter	Conditions	Min	Max	Unit
Vcc	Supply Voltage(1)	F_R = 33MHz, f_R = 20MHz	2.7	3.6	V
		F_R = 40MHz, f_R = 33MHz	3.0	3.6	V
T_A	Ambient Temperature, Operating	Industrial	–40	+85	°C

Note:
1. Vcc voltage during Read can operate across the min and max range but should not exceed ±10% of the programming (erase/write) voltage.

Table 7. Power-up Timing and Write Inhibit Threshold

Symbol	Parameter	Min	Max	Unit
t_{VSL}(1)	VCC(min) to $\overline{CS}$ Low	10		µs
t_{PUW}(1)	Time Delay Before Write Instruction	1	10	ms
V_{WI}(1)	Write Inhibit Threshold Voltage	1	2	V

Note:
1. These parameters are characterized only.

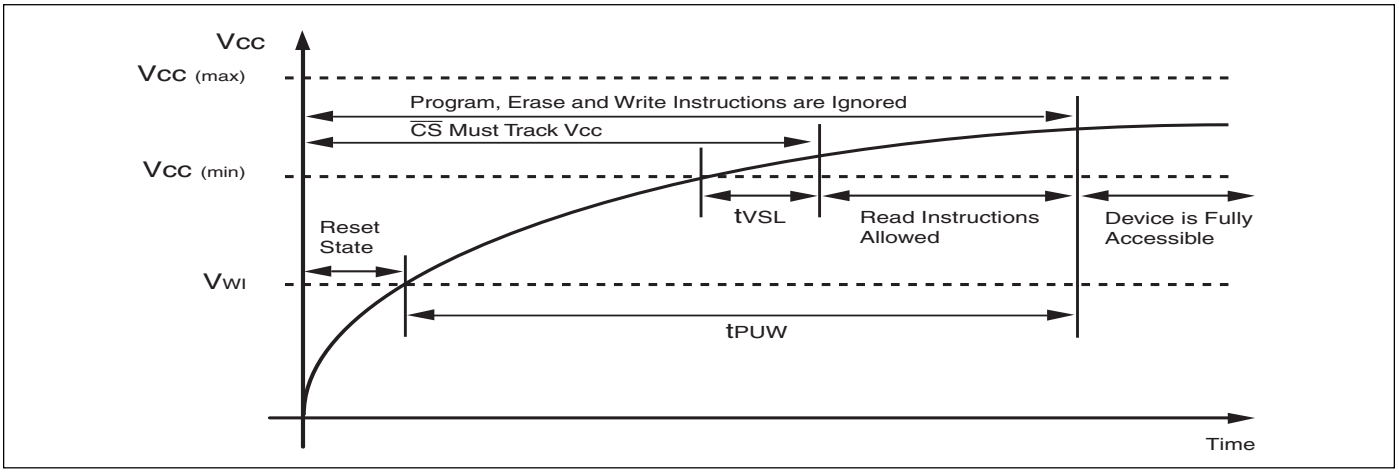


Figure 17. Power-up Timing and Voltage Levels

Table 8. DC Electrical Characteristics (Preliminary) (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{IN}(2)	Input Capacitance	V_{IN} = 0V(2)			6	pf
Cout(2)	Output Capacitance	V_{OUT} = 0V(2)			8	pf
I_{LI}	Input Leakage				±2	µA
I_{LO}	I/O Leakage				±2	µA
I_{CC1}	Standby Current	$\overline{CS}$ = VCC, VIN = GND or VCC		25	50	µA
I_{CC2}	Power-down Current	$\overline{CS}$ = VCC, VIN = GND or VCC		<1	5	µA
I_{CC3}	Current Read Data 1MHz	C = 0.1VCC / 0.9 VCC DO = Open		4	7	mA
	Current Read Data 20MHz	C = 0.1VCC / 0.9 VCC DO = Open		10	14	mA
	Current Read Data 33MHz	C = 0.1VCC / 0.9 VCC DO = Open		14	18	mA
I_{CC4}	Current Page Program	$\overline{CS}$ = VCC		15	20	mA
I_{CC5}	Current Write Status Register	$\overline{CS}$ = VCC		8	20	mA
I_{CC6}	Current Sector Erase	$\overline{CS}$ = VCC		15	25	mA
I_{CC7}	Current Bulk Erase	$\overline{CS}$ = VCC		17	25	mA
V_{IL}	Input Low Voltage		–0.5		Vccx0.3	V
V_{IH}	Input High Voltage		Vccx0.7		Vcc +0.4	V
V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = –100 µA	V_{CC}–0.2			V

Notes:
1. See Preliminary Designation.
2. Tested on sample basis and specified through design and characterization data. TA=25° C, Vcc 3V, Frequency 20MHz.

Table 9. AC Measurement Conditions

Symbol	Parameter	Min	Max	Unit
C_L	Load Capacitance	30	30	pF
T_R, T_F	Input Rise and Fall Times		5	ns
V_{IN}	Input Pulse Voltages	0.2VCC to	0.8VCC	V
O_{UT}	Output Timing Reference Voltages	0.3VCC to	0.7VCC	V

Note:
1. Output Hi-Z is defined as the point where data out is no longer driven.

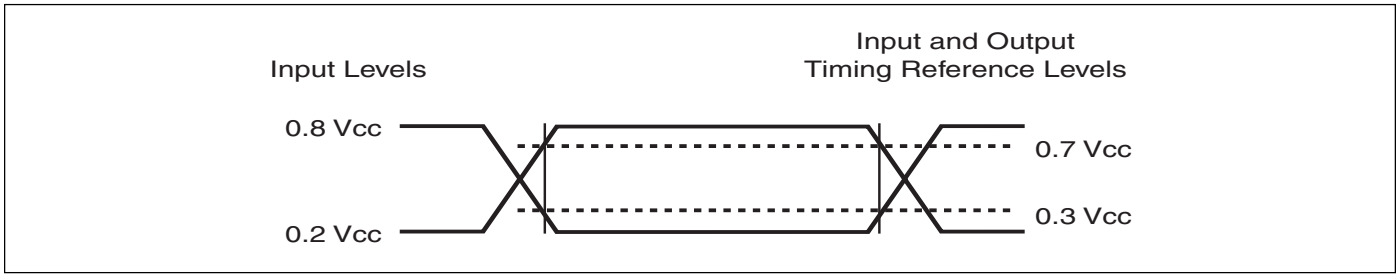


Figure 18. AC Measurement I/O Waveform

Table 10. AC Electrical Characteristics (Preliminary)

Symbol	Alt	Description	Min	Typ	Max	Unit
F_R	f_C	Clock frequency, for Fast Read (0Bh) and all other instructions except Read Data (03h) 2.7V-3.6V Vcc	D.C.		33	MHz
		3.0V-3.6V Vcc	D.C.		40	MHz
f_R		Clock freq. Read Data instruction (03h) 2.7V-3.6V Vcc	D.C.		20	MHz
		3.0V-3.6V Vcc	D.C.		33	MHz
t_{CLH}, t_{CLL}(1)		Clock High, Low Time, for Fast Read (0Bh) and all other instructions except Read Data (03h)	11			ns
t_{CRLH}, t_{CRLL}(1)		Clock High, Low Time for Read Data instruction (20 / 33-40MHz)	18 / 11			ns
t_{CLCH}(2)		Clock Rise Time peak to peak	0.1			V / ns
t_{CHCL}(2)		Clock Fall Time peak to peak	0.1			V / ns
t_{SLCH}	t_{CSS}	$\overline{CS}$ Active Setup Time relative to CLK (20 / 33-40MHz)	10 / 5			ns
t_{CHSL}		$\overline{CS}$ Not Active Hold Time relative to CLK (20 / 33-40MHz)	10 / 5			ns
t_{DVCH}	t_{DSU}	Data In Setup Time (20 / 33-40MHz)	5 / 2			ns
t_{CHDX}	t_{DH}	Data In Hold Time	5			ns
t_{CHSH}		$\overline{CS}$ Active Hold Time relative to CLK (20 / 33-40MHz)	10 / 5			ns
t_{SHCH}		$\overline{CS}$ Not Active Setup Time relative to CLK (20 / 33-40MHz)	10 / 5			ns
t_{SHSL}	t_{CSH}	$\overline{CS}$ Deselect Time	100			ns
t_{SHQZ}(2)	t_{DIS}	Output Disable Time (20 / 33-40MHz)			15 / 9	ns
t_{CLQV}	t_V	Clock Low to Output Valid (20 / 33-40MHz)			15 / 10	ns
t_{CLQX}	t_{HO}	Output Hold Time	0			ns
t_{HLCH}		$\overline{HOLD}$ Active Setup Time relative to CLK (20 / 33-40MHz)	10 / 5			ns
t_{CHHH}		$\overline{HOLD}$ Active Hold Time relative to CLK (20 / 33-40MHz)	10 / 5			ns
t_{HHCH}		$\overline{HOLD}$ Not Active Setup Time relative to CLK (20 / 33-40MHz)	10 / 5			ns
t_{CHHL}		$\overline{HOLD}$ Not Active Hold Time relative to CLK (20 / 33-40MHz)	10 / 5			ns
t_{HHQX}(2)	t_{LZ}	$\overline{HOLD}$ to Output Low-Z (20 / 33-40MHz)			15 / 9	ns
t_{HLQZ}(2)	t_{HZ}	$\overline{HOLD}$ to Output High-Z (20 / 33-40MHz)			20 / 9	ns
t_{WHSL}(4)		Write Protect Setup Time Before $\overline{CS}$ Low	20			ns
t_{SHWL}(4)		Write Protect Hold Time After $\overline{CS}$ High	100			ns
t_{DP}(2)		$\overline{CS}$ High to Power-down Mode			3	µs
t_{RES1}(2)		$\overline{CS}$ High to Standby Mode without Electronic Signature Read			3	µs
t_{RES2}(2)		$\overline{CS}$ High to Standby Mode with Electronic Signature Read			1.8	µs
t_W		Write Status Register Cycle Time		10	15	ms
t_{PP}		Page Program Cycle Time		2	5	ms
t_{SE}		Sector Erase Cycle Time		0.7	3	s
t_{BE}		Bulk Erase Cycle Time 25P10 and 25P20		3	6	s
		Bulk Erase Cycle Time 25P40		5	10	s

Notes:
1. Clock high + Clock low must be less than or equal to 1/f_C.
2. Value guaranteed by design and/or characterization, not 100% tested in production.
3. Expressed as a slew-rate.
4. Only applicable as a constraint for a Write Status Register instruction when Sector Protect Bit is set at 1.

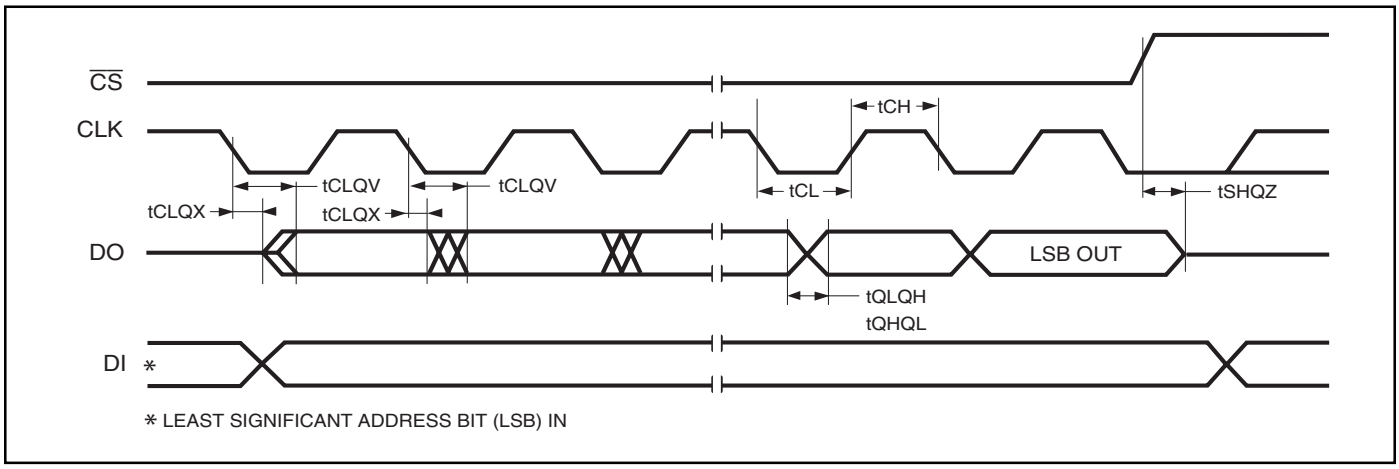


Figure 19. Serial Output Timing

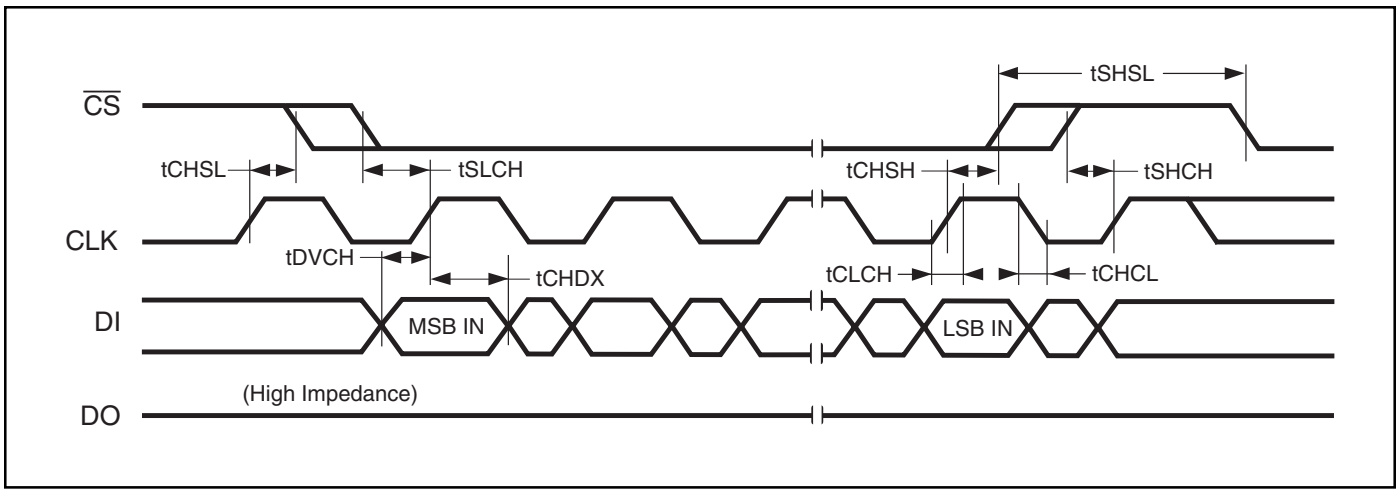


Figure 20. Input Timing

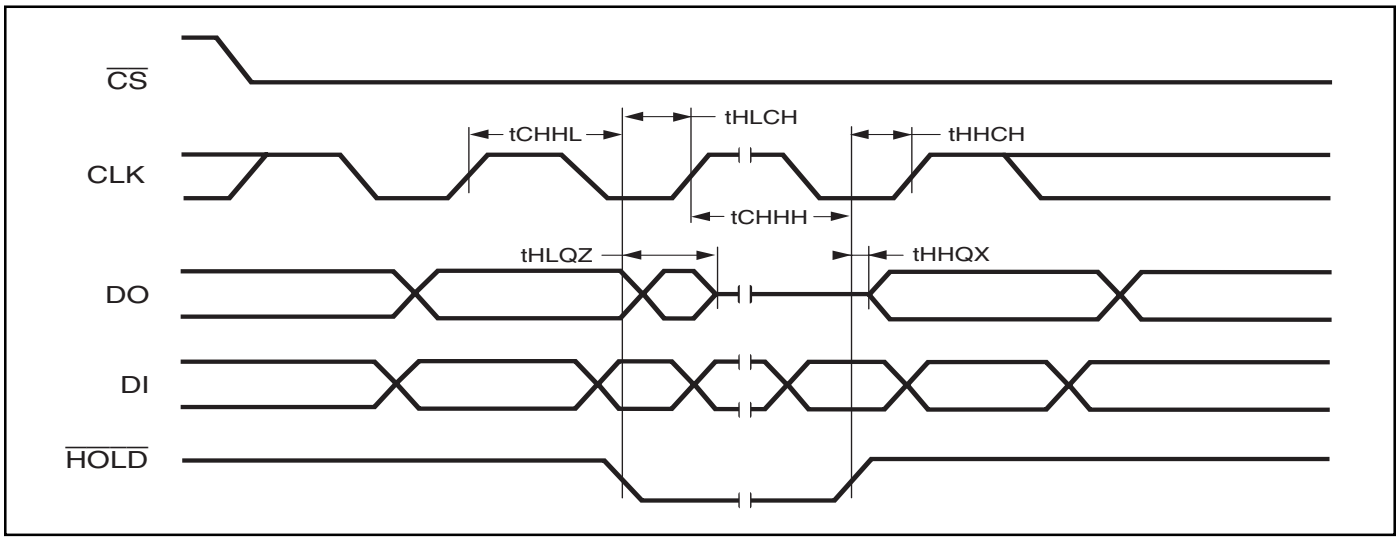
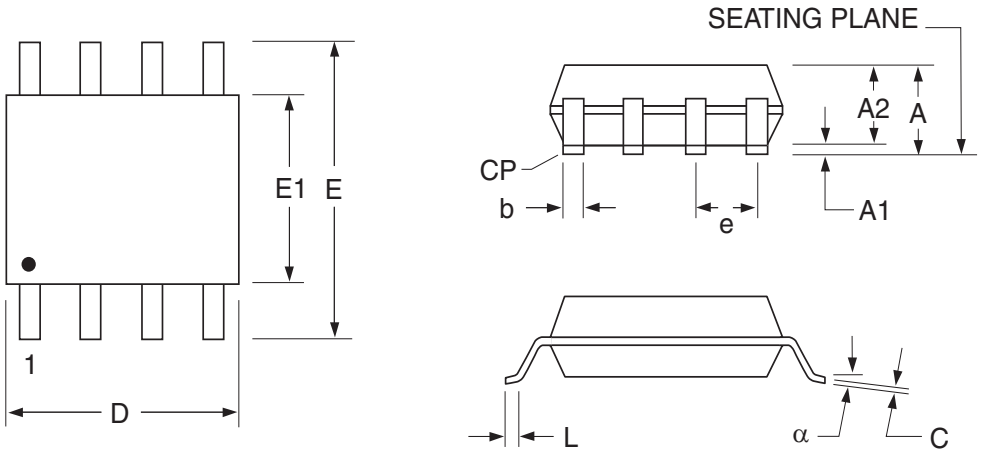


Figure 21. Hold Timing

PACKAGING INFORMATION

8-Pin SOIC 150-mil (Package Code N)



Package Dimensions[1]

	Millimeters			Inches		
Symbol	**Min**	**Typ.**	**Max**	**Min**	**Typ.**	**Max**
A	1.47	1.60	1.72	0.058	0.063	0.068
A1	0.10		0.24	0.004		0.009
A2		1.45			0.057	
b	0.33	0.41	0.50	0.013	0.016	0.020
C	0.19	0.20	0.25	0.0075	0.008	0.0098
D[3]	4.80	4.85	4.95	0.189	0.191	0.195
E	5.80	6.00	6.19	0.228	0.236	0.244
E1[3]	3.80	3.90	4.00	0.150	0.154	0.157
e[2]		1.27 BSC			0.050 BSC	
L	0.40	0.71	1.27	0.015	0.028	0.050
α	0°		8°	0°		8°
CP			0.10			0.004

Notes:
1. Controlling dimensions: inches, unless otherwise specified.
2. BSC = Basic lead spacing between centers.
3. Dimensions D and E1 do not include mold flash protrusions and should be measured from the bottom of the package.
4. Formed leads shall be planar with respect to one another within .0004 inches at the seating plane.

PRELIMINARY DESIGNATION

The "Preliminary" designation on a *NexFlash* data sheet indicates that the product is not fully characterized. The specifications are subject to change and are not guaranteed. *NexFlash* or an authorized sales representative should be consulted for current information before using this product.

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(c) potential liability of *NexFlash* is adequately protected under the circumstances.

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ORDERING INFORMATION

NX 25P xx - V x I - xx..

Company Prefix
NX = NexFlash

Product Family
25P = spiFlash Serial Flash Memory

Product Number / Density
10 = 1M-bit
20 = 2M-bit
40 = 4M-bit

Supply Voltage
V = 2.7V to 3.6V

Package Type
N = 8-pin SOIC 150-mil
P = 8-contact MLP 6x5mm*

Temperature Range
I = Industrial (–40˚C to +85˚C)

Special Options
(Blank) Standard Package
G = Green Package (Lead-Free, RoHS compliant)
C = Customer Specification (For factory programming and other custom specifications)
T = Tape and Reel

* Contact NexFlash for availability of this package.

Document Revision History

Date	Rev	Description of Revision
04/29/03	A	Document Written
09/12/03	B	Incorporated spiFlash trademark for NX25P10, 20 and 40 product family. Adjusted data for consistency
03/09/04	C	Adjusted pages 10, 11, 14, 16 and 24 for technical clarity. Updated Special Options and Ordering Information
03/24/04	D	MLP metal die pad notification; Under "Package Types," figure 3 and packaging information.
05/11/04	E	Corrected dimensions in Packaging Information section for 6x5mm MLP. Updated Characterization information DC (Table 8) & AC (Table 10).
06/16/04	F	Modified dimensional data in the Packaging Information for the 6x5mm MLP package
11/23/04	G	Added FR = 40MHz @ 3.0V to 3.6V Vcc. Added fR = 33MHz @ 3.0V to 3.6V Vcc. Modified t_{LEAD} in Absolute Maximum Ratings (Table 5) to reference JEDEC Standard information. Added F_R and f_R conditions to Operating Ranges (Table 6). Updated $I_{CC}3$ and $I_{CC}5$ data in DC Electrical Characteristics (Table 8). Added 20/33MHz call outs and updated min, max and typ data in AC Electrical Characteristics (Table 10).
12/08/04	H	Updated 8-pin 150mil SOIC package information.
04/04/05	I	Removed 8-contact 6x5 MLP package from document.

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