T-52-33-05

# Z8536 Military CIO Counter/Timer and Parallel I/O Unit

Zilog

## Military Electrical Specification

July 1985

## FEATURES

- Two independent 8-bit, double-buffered, bidirectional I/O ports plus a 4-bit special-purpose I/O port. I/O ports feature programmable polarity, programmable direction (Bit mode), "pulse catchers," and programmable open-drain outputs.
- Four handshake modes, including 3-Wire (like the IEEE-488).
- REQUEST/$\overline{\text{WAIT}}$ signal for high-speed data transfer.
- Flexible pattern-recognition logic, programmable as a 16-vector interrupt controller.
- Three independent 16-bit counter/timers with up to four external access lines per counter/timer (count input, output, gate, and trigger), and three output duty cycles (pulsed, one-shot, and square-wave), programmable as retriggerable or nonretriggerable.
- Easy to use since all registers are read/write.

## GENERAL DESCRIPTION

The Z8536 CIO Counter/Timer and Parallel I/O element is a general-purpose peripheral circuit, satisfying most counter/timer and parallel I/O needs encountered in system designs. This versatile device contains three I/O ports and three counter/timers. Many programmable options tailor its configuration to specific applications. The use of the device is simplified by making all internal registers (command, status, and data) readable and (except for status bits) writable. In addition, each register is given its own unique internal address, so that any register can be accessed in two operations. All data registers can be directly accessed in a single operation. The CIO is easily interfaced to all popular microprocessors.

## TIMING

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**Read Cycle.** At the beginning of a read cycle, the CPU places an address on the address bus. Bits $A_0$ and $A_1$ specify a CIO register; the remaining address bits and status information are combined and decoded to generate a Chip Enable ($\overline{CE}$) signal that selects the CIO. When Read ($\overline{RD}$) goes Low, data from the specified register is gated onto the data bus.

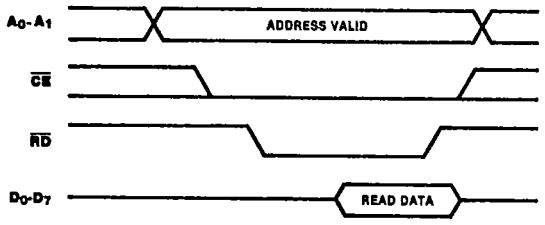


**Figure 1. Read Cycle Timing**

**Write Cycle.** At the beginning of a write cycle, the CPU places an address on the data bus. Bits $A_0$ and $A_1$ specify a CIO register; the remaining address bits and status information are combined and decoded to generate a Chip Enable ($\overline{CE}$) signal that selects the CIO. When $\overline{WR}$ goes Low, data placed on the bus by the CPU is strobed into the specified CIO register.

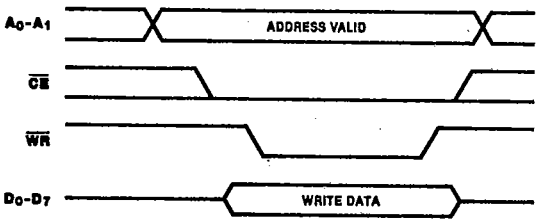


**Figure 2. Write Cycle Timing**

**Interrupt Acknowledge.** The CIO pulls its Interrupt Request ($\overline{INT}$) line Low, requesting interrupt service from the CPU, if an Interrupt Pending (IP) bit is set and Interrupts are enabled. The CPU responds with an Interrupt Acknowledge cycle. When Interrupt Acknowledge ($\overline{INTACK}$) goes true and the IP is set, the CIO forces Interrupt Enable Out (IEO) Low, disabling all lower priority devices in the interrupt daisy chain. If the CIO is the highest priority device requesting service (IEI is High), it places its interrupt vector on the data bus and sets the Interrupt Under Service (IUS) bit when Read ($\overline{RD}$) goes Low.

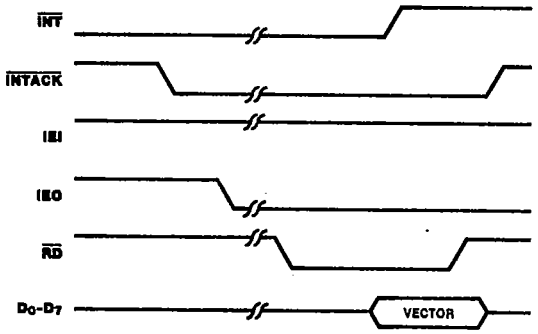


**Figure 3. Interrupt Acknowledge Timing**

## ABSOLUTE MAXIMUM RATINGS

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Guaranteed by characterization/design.

Voltages on all pins with respect to ground ..... −0.3V to +7V
Operating Case Temperature ..... −55°C to −125°C
Storage Temperature Range ..... −65°C to +150°C
Absolute Maximum Power Dissipation ..... 1.2 W

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## STANDARD TEST CONDITIONS

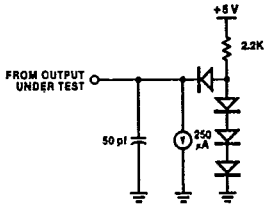
The DC Characteristics and Capacitance sections listed below apply for the following standard test conditions, unless otherwise noted.

Military Operating Temperature Range ($T_C$)
−55°C to +125°C

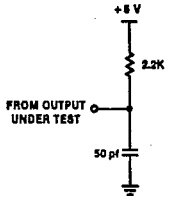
Standard Military Test Condition
$+4.5V \leq V_{CC} \leq +5.5V$

All voltages are referenced to GND (0V). Positive current flows into the referenced pin.

All ac parameters assume a load capacitance of 50 pf max.




**Standard Test Load**




**Open-Drain Test Load**

## DC CHARACTERISTICS

| Symbol | Parameter | Min | Max | Unit | Condition |
|---|---|---|---|---|---|
| $V_{IH}$ | Input High Voltage | 2.2[a] | $V_{CC}+0.3$[c] | V | |
| $V_{IL}$ | Input Low Voltage | −0.3[c] | 0.8[a] | V | |
| $V_{OH}$ | Output High Voltage | 2.4[a] | | V | $I_{OH} = -250\,\mu A$ |
| $V_{OL}$ | Output Low Voltage | | 0.4[a] | V | $I_{OL} = +2.0$ mA |
| | | | 0.5[b] | V | $I_{OL} = +3.2$ mA |
| $I_{IL}$ | Input Leakage | | ±10.0[a] | µA | $0.4 \leq V_{IN} \leq +2.4$ V |
| $I_{OL}$ | Output Leakage | | ±10.0[a] | µA | $0.4 \leq V_{OUT} \leq +2.4$ V |
| $I_{CC}$ | $V_{CC}$ Supply Current | | 200[a] | mA | |

$V_{CC} = 5\,V \pm 5\%$ unless otherwise specified, over specified temperature range.

Parameter Test Status:
[a] Tested
[b] Guaranteed
[c] Guaranteed by characterization/design

## CAPACITANCE

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | | 10[b] | pf |
| $C_{OUT}$ | Output Capacitance | | 15[b] | pf |
| $C_{I/O}$ | Bidirectional Capacitance | | 20[b] | pf |

f = 1 MHz, over specified temperature range.
Unmeasured pins returned to ground.

Parameter Test Status:
[a] Tested
[b] Guaranteed
[c] Guaranteed by characterization/design

## AC CHARACTERISTICS

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| Number | Symbol | Parameter | 4 MHz Min | 4 MHz Max | 6 MHz Min | 6 MHz Max | Notes*† |
|---|---|---|---|---|---|---|---|
| 1 | TcPC | PCLK Cycle Time | 250[a] | 4000[a] | 165[a] | 4000[a] | |
| 2 | TwPCh | PCLK Width (High) | 105[b] | 2000[a] | 70[a] | 2000[a] | |
| 3 | TwPCl | PCLK Width (Low) | 105[b] | 2000[a] | 70[a] | 2000[a] | |
| 4 | TrPC | PCLK Rise Time | | 20[b] | | 10[a] | |
| 5 | TfPC | PCLK Fall Time | | 20[b] | | 15[b] | |
| 6 | TsIA(PC) | $\overline{INTACK}$ to PCLK ↑ Setup Time | 100[b] | | 100[b] | | |
| 7 | ThIA(PC) | $\overline{INTACK}$ to PCLK ↑ Hold Time | 0[b] | | 0[b] | | |
| 8 | TsIA(RD) | $\overline{INTACK}$ to $\overline{RD}$ ↓ Setup Time | 200[b] | | 200[b] | | |
| 9 | ThIA(RD) | $\overline{INTACK}$ to $\overline{RD}$ ↑ Hold Time | 0[b] | | 0[b] | | |
| 10 | TsIA(WR) | $\overline{INTACK}$ to $\overline{WR}$ ↓ Setup Time | 200[b] | | 200[b] | | |
| 11 | ThIA(WR) | $\overline{INTACK}$ to $\overline{WR}$ ↑ Hold Time | 0[b] | | 0[b] | | |
| 12 | TsA(RD) | Address to $\overline{RD}$ ↓ Setup Time | 80[a] | | 80[a] | | |
| 13 | ThA(RD) | Address to $\overline{RD}$ ↑ Hold Time | 0[b] | | 0[b] | | |
| 14 | TsA(WR) | Address to $\overline{WR}$ ↓ Setup Time | 80[a] | | 80[a] | | |
| 15 | ThA(WR) | Address to $\overline{WR}$ ↑ Hold Time | 0[b] | | 0[b] | | |
| 16 | TsCEl(RD) | $\overline{CE}$ Low to $\overline{RD}$ ↓ Setup Time | 0[a] | | 0[a] | | 1 |
| 17 | TsCEh(RD) | $\overline{CE}$ High to $\overline{RD}$ ↓ Setup Time | 100[b] | | 70[b] | | 1 |
| 18 | ThCE(RD) | $\overline{CE}$ to $\overline{RD}$ ↑ Hold Time | 0[a] | | 0[a] | | 1 |
| 19 | TsCEl(WR) | $\overline{CE}$ Low to $\overline{WR}$ ↓ Setup Time | 0[a] | | 0[a] | | |
| 20 | TsCEh(WR) | $\overline{CE}$ High to $\overline{WR}$ ↓ Setup Time | 100[b] | | 70[b] | | |
| 21 | ThCE(WR) | $\overline{CE}$ to $\overline{WR}$ ↑ Hold Time | 0[a] | | 0[a] | | |
| 22 | TwRDl | $\overline{RD}$ Low Width | 390[b] | | 250[b] | | 1 |
| 23 | TdRD(DRA) | $\overline{RD}$ ↓ to Read Data Active Delay | 0[b] | | 0[b] | | |
| 24 | TdRDf(DR) | $\overline{RD}$ ↓ to Read Data Valid Delay | | 255[b] | | 180[b] | |
| 25 | TdRDr(DR) | $\overline{RD}$ ↑ to Read Data Not Valid Delay | 0[b] | | 0[b] | | |
| 26 | TdRD(DRz) | $\overline{RD}$ ↑ to Read Data Float Delay | | 70[b] | | 45[b] | 2 |
| 27 | TwWRl | $\overline{WR}$ Low Width | 390[b] | | 250[b] | | |
| 28 | TsDW(WR) | Write Data to $\overline{WR}$ ↓ Setup Time | 0[b] | | 0[b] | | |
| 29 | ThDW(WR) | Write Data to $\overline{WR}$ ↑ Hold Time | 0[b] | | 0[b] | | |
| 30 | Trc | Valid Access Recovery Time | 1000[b]* | | 650[b] | | 3 |
| 31 | TdPM(INT) | Pattern Match to $\overline{INT}$ Delay (Bit Port) | | 2+800[b] | | 2[b] | 6 |
| 32 | TdACK(INT) | $\overline{ACKIN}$ to $\overline{INT}$ Delay (Port with Handshake) | | 10+600[b] | | 10[b] | 4, 6 |
| 33 | TdCl(INT) | Counter Input to $\overline{INT}$ Delay (Counter Mode) | | 2+700[b] | | 2[b] | 6 |
| 34 | TdPC(INT) | PCLK to $\overline{INT}$ Delay (Timer Mode) | | 3+700[b] | | 3[b] | 6 |
| 35 | TsIA(RDA) | $\overline{INTACK}$ to $\overline{RD}$ ↓ (Acknowledge) Setup Time | 350[b] | | 250[b] | | 5 |

NOTES:

[1] Parameter does not apply to Interrupt Acknowledge transactions.

[2] Float delay is measured to the time when the output has changed 0.5 V with minimum ac load and maximum dc load.

[3] Trc is the specified number or 3 TcPC, whichever is longer.

[4] The delay is from $\overline{DAV}$ ↓ for 3-Wire Input Handshake. The delay is from DAC ↑ for 3-Wire Output Handshake.

[5] The parameters for the devices in any particular daisy chain must meet the following constraint: The delay from $\overline{INTACK}$ ↓ to $\overline{RD}$↓ must be greater than the sum of TdIA(IEO) for the highest priority peripheral, TsIEI(RDA) for the lowest priority peripheral, and TdIEI(IEO) for each peripheral separating them in the chain.

[6] Units are equal to TcPC plus ns.

* All timing references assume 2.0 V for a logic "1" and 0.8 V for a logic "0".

† Units in nanoseconds (ns), except as noted.

Parameter Test Status:

a Tested

b Guaranteed

c Guaranteed by characterization/design

d Parameter not tested, not guaranteed

## AC CHARACTERISTICS (Continued)

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| Number | Symbol | Parameter | 4 MHz Min | 4 MHz Max | 6 MHz Min | 6 MHz Max | Notes*† |
|---|---|---|---|---|---|---|---|
| 36 | TwRDA | $\overline{RD}$ (Acknowledge) Width | 350[b] | | 250[b] | | |
| 37 | TdRDA(DR) | $\overline{RD}$ ↓ (Acknowledge) to Read Data Valid Delay | | 250[b] | | 180[b] | |
| 38 | TdIA(IEO) | $\overline{INTACK}$ ↓ to IEO ↓ Delay | | 350[b] | | 250[b] | 5 |
| 39 | TdIEI(IEO) | IEI to IEO Delay | | 150[b] | | 100[b] | 5 |
| 40 | TsIEI(RDA) | IEI to $\overline{RD}$ ↓ (Acknowledge) Setup Time | 100[b] | | 70[b] | | 5 |
| 41 | ThIEI(RDA) | IEI to $\overline{RD}$ ↑ (Acknowledge) Hold Time | 100[b] | | 70[b] | | |
| 42 | TdRDA(INT) | $\overline{RD}$ ↓ (Acknowledge) to $\overline{INT}$ ↑ Delay | | 600[b] | | 600[b] | |

NOTES:

[1] Parameter does not apply to Interrupt Acknowledge transactions.

[2] Float delay is measured to the time when the output has changed 0.5 V with minimum ac load and maximum dc load.

[3] Trc is the specified number or 3 TcPC, whichever is longer.

[4] The delay is from $\overline{DAV}$ ↓ for 3-Wire Input Handshake. The delay is from DAC ↑ for 3-Wire Output Handshake.

[5] The parameters for the devices in any particular daisy chain must meet the following constraint: The delay from $\overline{INTACK}$ ↓ to $\overline{RD}$ ↓ must be greater than the sum of TdIA(IEO) for the highest priority peripheral, TsIEI(RDA) for the lowest priority peripheral, and TdIEI(IEO) for each peripheral separating them in the chain.

[6] Units are equal to TcPC plus ns.

* All timing references assume 2.0 V for a logic "1" and 0.8 V for a logic "0".

† Units in nanoseconds (ns), except as noted.

Parameter Test Status:

[a] Tested

[b] Guaranteed

[c] Guaranteed by characterization/design

[d] Parameter not tested, not guaranteed

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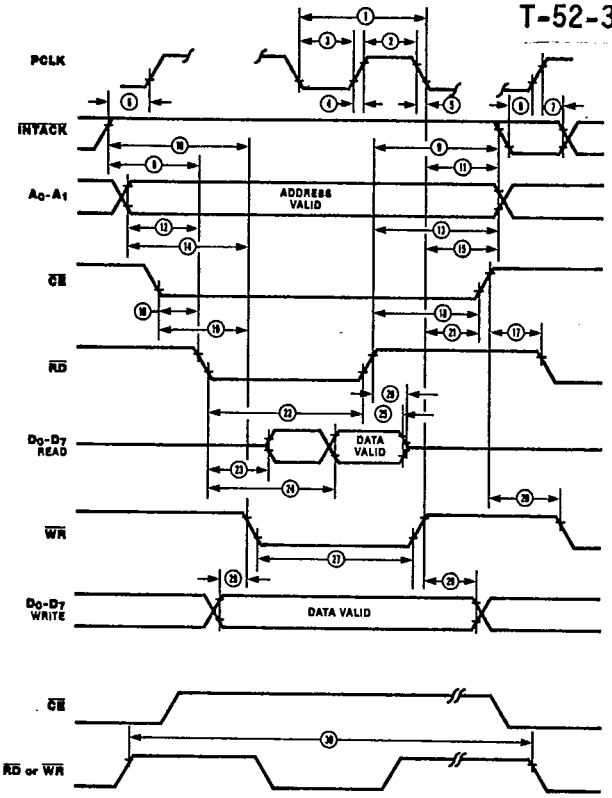
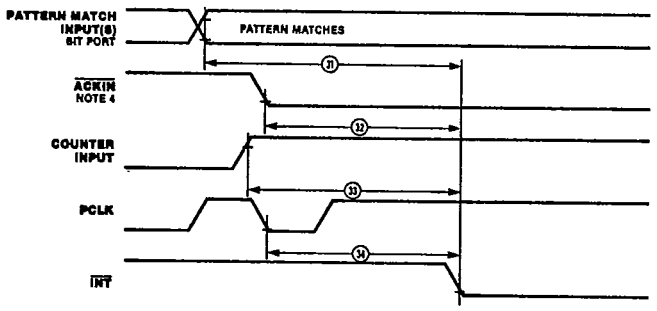
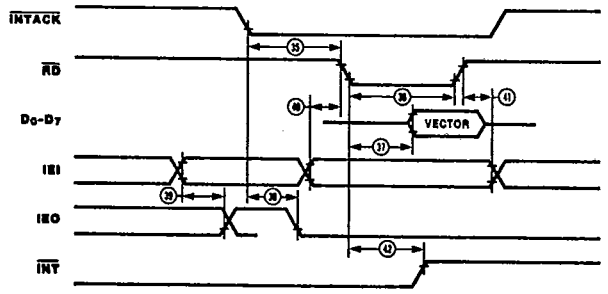
## CPU INTERFACE TIMING




## INTERRUPT TIMING



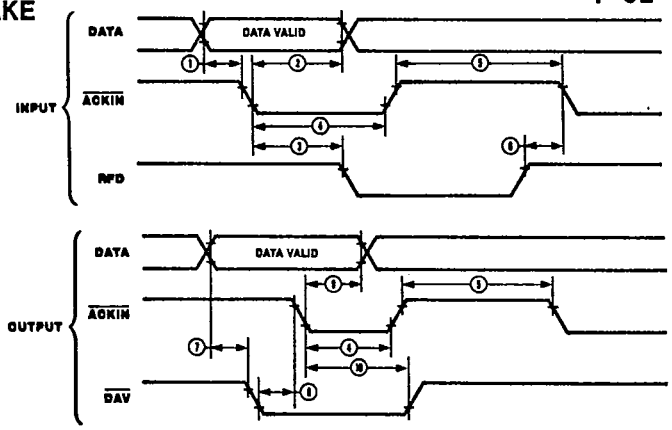

## INTERRUPT ACKNOWLEDGE TIMING



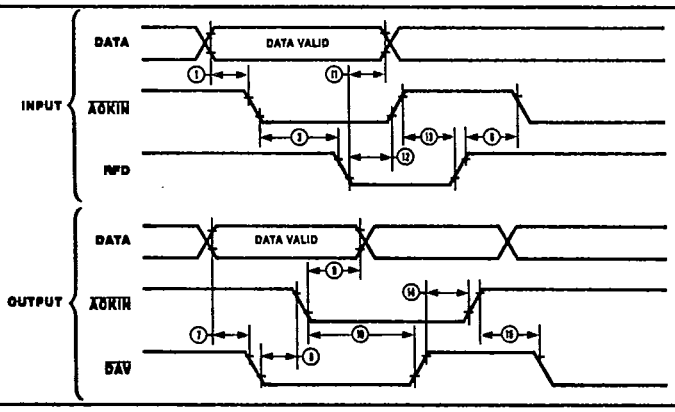



2021-006, 007, 008

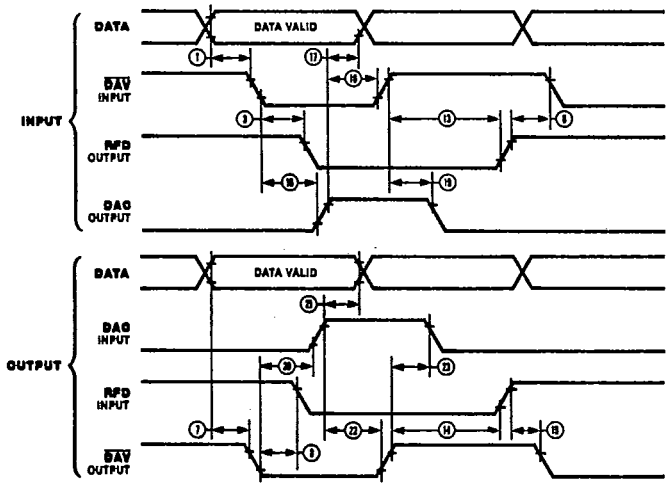
## STROBED HANDSHAKE




## INTERLOCKED HANDSHAKE




## 3-WIRE HANDSHAKE



## AC CHARACTERISTICS

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| Number | Symbol | Parameter | 4 MHz Min | 4 MHz Max | 6 MHz Min | 6 MHz Max | Notes*† |
|---|---|---|---|---|---|---|---|
| 1 | TsDI(ACK) | Data Input to $\overline{ACKIN}$ ↓ Setup Time | 0[b] | | 0[b] | | |
| 2 | ThDI(ACK) | Data Input to $\overline{ACKIN}$ ↓ Hold Time—Strobed Handshake | 500[d] | | d | | |
| 3 | TdACKf(RFD) | $\overline{ACKIN}$ ↓ to RFD ↓ Delay | 0[b] | | 0[b] | | |
| 4 | TwACKl | $\overline{ACKIN}$ Low Width—Strobed Handshake | 250[d] | | d | | |
| 5 | TwACKh | $\overline{ACKIN}$ High Width—Strobed Handshake | 250[d] | | d | | |
| 6 | TdRFDr(ACK) | RFD ↑ to $\overline{ACKIN}$ ↓ Delay | 0[b] | | 0[b] | | |
| 7 | TsDO(DAV) | Data Out to $\overline{DAV}$ ↓ Setup Time | 25[b] | | 20[b] | | 1 |
| 8 | TdDAVf(ACK) | $\overline{DAV}$ ↓ to $\overline{ACKIN}$ ↓ Delay | 0[b] | | 0[b] | | |
| 9 | ThDO(ACK) | Data Out to $\overline{ACKIN}$ ↓ Hold Time | 2[b] | | 2[b] | | 2 |
| 10 | TdACK(DAV) | $\overline{ACKIN}$ ↓ to $\overline{DAV}$ ↑ Delay | 2[b] | | 2[b] | | 2 |
| 11 | THDI(RFD) | Data Input to RFD ↓ Hold Time—Interlocked Handshake | d | | d | | |
| 12 | TdRFDf(ACK) | RFD ↓ to $\overline{ACKIN}$ ↑ Delay Interlocked Handshake | 0[b] | | 0[b] | | |
| 13 | TdACKr(RFD) | $\overline{ACKIN}$ ↑ ($\overline{DAV}$ ↑) to RFD ↑ Delay—Interlocked and 3-Wire Handshake | 0[b] | | 0[b] | | |
| 14 | TdDAVr(ACK) | $\overline{DAV}$ ↑ to $\overline{ACKIN}$ ↑ (RFD ↑)—Interlocked and 3-Wire Handshake | 0[b] | | 0[b] | | |
| 15 | TdACK(DAV) | $\overline{ACKIN}$ ↑ (RFD ↑) to $\overline{DAV}$ ↓ Delay—Interlocked and 3-Wire Handshake | 0[b] | | 0[b] | | |
| 16 | TdDAVlf(DAC) | $\overline{DAV}$ ↓ to DAC ↑ Delay—Input 3-Wire Handshake | 0[b] | | 0[b] | | |
| 17 | ThDI(DAC) | Data Input to DAC ↑ Hold Time—3-Wire Handshake | 0[b] | | 0[b] | | |
| 18 | TdDACOr(DAV) | DAC ↑ to $\overline{DAV}$ ↑ Delay—Input 3-Wire Handshake | 0[b] | | 0[b] | | |
| 19 | TdDAVlr(DAC) | $\overline{DAV}$ ↑ to DAC ↓ Delay—Input 3-Wire Handshake | 0[b] | | 0[b] | | |
| 20 | TdDAVOf(DAC) | $\overline{DAV}$ ↓ to DAC ↑ Delay—Output 3-Wire Handshake | 0[b] | | 0[b] | | |
| 21 | ThDO(DAC) | Data Output to DAC ↑ Hold Time—3-Wire Handshake | 2[b] | | 2[b] | | 2 |
| 22 | TdDACIr(DAV) | DAC ↑ to $\overline{DAV}$ ↑ Delay—Output 3-Wire Handshake | 2[b] | | 2[b] | | 2 |
| 23 | TdDAVOr(DAC) | $\overline{DAV}$ ↑ to DAC ↓ Delay—Output 3-Wire Handshake | 0[b] | | 0[b] | | |

NOTES:
[1] This time can be extended through the use of deskew timers.
[2] Units equal to TcPC.

* All timing references assume 2.0 V for a logic "1" and 0.8 V for a logic "0".
† Units in nanoseconds (ns), except as noted.

Parameter Test Status:
[a] Tested
[b] Guaranteed
[c] Guaranteed by characterization/design
[d] Parameter not tested, not guaranteed

## COUNTER/TIMER

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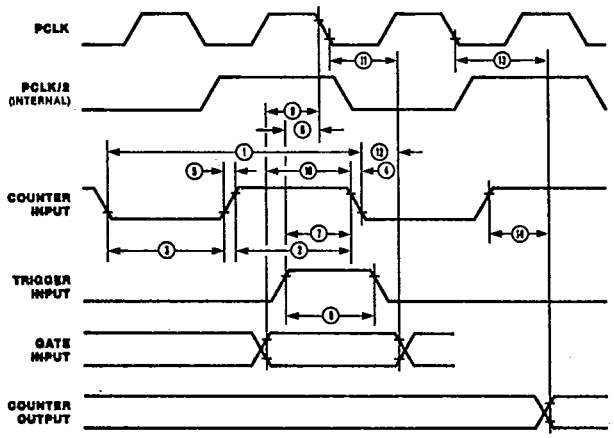


## AC CHARACTERISTICS

Counter/Timer

| Number | Symbol | Parameter | 4 MHz Min | 4 MHz Max | 6 MHz Min | 6 MHz Max | Notes*† |
|---|---|---|---|---|---|---|---|
| 1 | TcCI | Counter Input Cycle Time | 500[b] | | 330[b] | | |
| 2 | TCIh | Counter Input High Width | 230[b] | | 150[b] | | |
| 3 | TWCIl | Counter Input Low Width | 230[b] | | 150[b] | | |
| 4 | TfCI | Counter Input Fall Time | | 20[b] | | 15[b] | |
| 5 | TrCI | Counter Input Rise Time | | 20[b] | | 15[b] | |
| 6 | TsTI(PC) | Trigger Input to PCLK ↓ Setup Time (Timer Mode) | 150[d] | | | d | 1 |
| 7 | TsTI(CI) | Trigger Input to Counter Input ↓ Setup Time (Counter Mode) | 150[d] | | | d | 1 |
| 8 | TwTI | Trigger Input Pulse Width (High or Low) | 200[d] | | | d | |
| 9 | TsGI(PC) | Gate Input to PCLK ↓ Setup Time (Timer Mode) | 100[d] | | | d | 1 |
| 10 | TsGI(CI) | Gate Input to Counter Input ↓ Setup Time (Counter Mode) | 100[d] | | | d | 1 |
| 11 | ThGI(PC) | Gate Input to PCLK ↓ Hold Time (Timer Mode) | 100[d] | | | d | 1 |
| 12 | ThGI(CI) | Gate Input to Counter Input ↓ Hold Time (Counter Mode) | 100[d] | | | d | 1 |
| 13 | TdPC(CO) | PCLK to Counter Output Delay (Timer Mode) | | 475[d] | | d | |
| 14 | TdCI(CO) | Counter Input to Counter Output Delay (Counter Mode) | | 475[d] | | d | |

NOTES:

[1] These parameters must be met to guarantee trigger or gate are valid for the next counter/timer cycle.

* All timing references assume 2.0 V for a logic "1" and 0.8 V for a logic "0".

† Units in nanoseconds (ns).

Parameter Test Status:

[a] Tested
[b] Guaranteed
[c] Guaranteed by characterization/design
[d] Parameter not tested, not guaranteed

## REQUEST/WAIT TIMING

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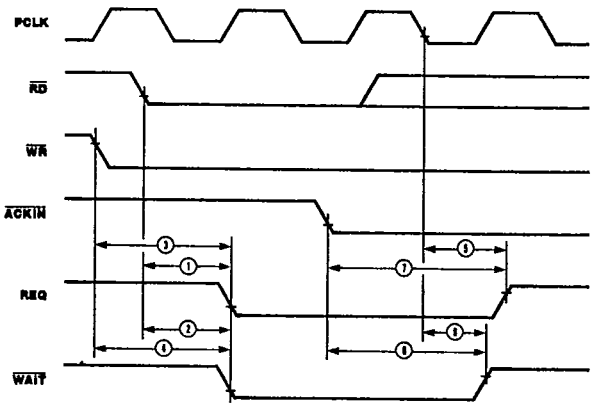


## AC CHARACTERISTICS

REQUEST/WAIT Timing

| Number | Symbol | Parameter | 4 MHz Min | 4 MHz Max | 6 MHz Min | 6 MHz Max | Notes*† |
|---|---|---|---|---|---|---|---|
| 1 | TdRD(REQ) | RD ↓ to REQ ↓ Delay | | 500[b] | | d | |
| 2 | TdRD(WAIT) | RD ↓ to WAIT ↓ Delay | | 500[b] | | d | |
| 3 | TdWR(REQ) | WR ↓ to REQ ↓ Delay | | 500[b] | | d | |
| 4 | TdWR(WAIT) | WR ↓ to WAIT ↓ Delay | | 500[b] | | d | |
| 5 | TdPC(REQ) | PCLK ↓ to REQ ↑ Delay | | 300[b] | | d | |
| 6 | TdPC(WAIT) | PCLK ↓ to WAIT ↑ Delay | | 300[b] | | d | |
| 7 | TdACK(REQ) | ACKIN ↓ to REQ ↑ Delay | | 8 + 1000[b] | | d | 1, 2 |
| 8 | TdACK(WAIT) | ACKIN ↓ to WAIT ↑ Delay | | 10 + 600[b] | | d | 1, 2 |

NOTES:
[1] The delay is from DAV ↓ for 3-Wire Input Handshake. The delay is from DAC ↑ for 3-Wire Output Handshake.
[2] Units equal to TcPC + ns.

* All timing references assume 2.0 V for a logic "1" and 0.8 V for a logic "0".
† Units in nanoseconds (ns), except as noted.

Parameter Test Status:
[a] Tested
[b] Guaranteed
[c] Guaranteed by characterization/design
[d] Parameter not tested, not guaranteed

## RESET TIMING

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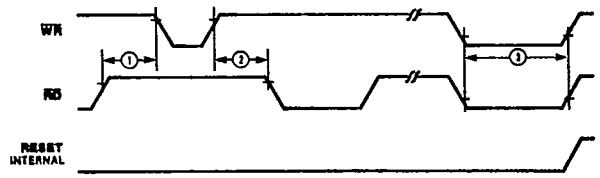



## AC CHARACTERISTICS

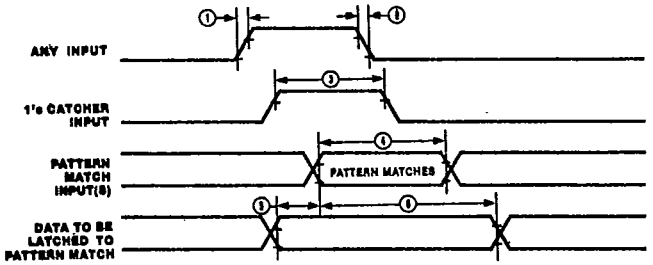
Reset Timing

| Number | Symbol | Parameter | 4 MHz Min | 4 MHz Max | 6 MHz Min | 6 MHz Max | Notes*† |
|---|---|---|---|---|---|---|---|
| 1 | TdRD(WR) | Delay from $\overline{RD}$ ↑ to $\overline{WR}$ ↓ for No Reset | 50[b] | | 50[b] | | |
| 2 | TdWR(RD) | Delay from $\overline{WR}$ ↑ to $\overline{RD}$ ↓ for No Reset | 50[b] | | 50[b] | | |
| 3 | TwRES | Minimum Width of $\overline{RD}$ and $\overline{WR}$ both Low for Reset | 250[a] | | 250[a] | | |

* All timing references assume 2.0 V for a logic "1" and 0.8 V for a logic "0".
† Units in nanoseconds (ns).

Parameter Test Status:
[a] Tested
[b] Guaranteed
[c] Guaranteed by characterization/design
[d] Parameter not tested, not guaranteed

## MISCELLANEOUS PORT TIMING




## AC CHARACTERISTICS

Port Timing

| Number | Symbol | Parameter | 4 MHz Min | 4 MHz Max | 6 MHz Min | 6 MHz Max | Notes*† |
|---|---|---|---|---|---|---|---|
| 1 | Trl | Any Input Rise Time | | 100[b] | | 100[b] | |
| 2 | Tfl | Any Input Fall Time | | 100[b] | | 100[b] | |
| 3 | Tw1's | 1's Catcher High Width | 250[b] | | 170[b] | | 1 |
| 4 | TwPM | Pattern Match Input Valid (Bit Port) | 750[b] | | 500[b] | | |
| 5 | TsPMD | Data Latched on Pattern Match Setup Time (Bit Port) | 0[b] | | 0[b] | | |
| 6 | ThPMD | Dta Latched on Pattern Match Hold Time (Bit Port) | 1000[b] | | 650[b] | | |

NOTES:
[1] If the input is programmed inverting, a Low-going pulse of the same width will be detected.

* All timing references assume 2.0 V for a logic "1" and 0.8 V for a logic "0".
† Units in nanoseconds (ns).

Parameter Test Status:
[a] Tested
[b] Guaranteed
[c] Guaranteed by characterization/design

## PIN DESCRIPTION

T-52-33-05

**$A_0$-$A_1$.** *Address Lines* (Input). These two lines are used to select the register involved in the CPU transaction: Port A's Data register, Port B's Data register, Port C's Data register, or a control register.

**$\overline{CE}$.** *Chip Enable* (Input, active Low). A Low level on this input enables the CIO to be read from or written to.

**$D_0$-$D_7$.** *Data Bus* (bidirectional 3-state). These eight data lines are used for transfers between the CPU and the CIO.

**IEI.** *Interrupt Enable In* (Input, active High). IEI is used with IEO to form an interrupt daisy chain when there is more than one interrupt-driven device. A High IEI indicates that no other higher priority device has an interrupt under service or is requesting an interrupt.

**IEO.** *Interrupt Enable Out* (output, active High). IEO is High only if IEI is High and the CPU is not servicing an interrupt from the requesting CIO or is not requesting an interrupt (Interrupt Acknowledge cycle only). IEO is connected to the next lower priority device's IEI input and thus inhibits interrupts from lower priority devices.

**$\overline{INT}$.** *Interrupt Request* (output, open-drain, active Low). This signal is pulled Low when the CIO requests an interrupt.

**$\overline{INTACK}$.** *Interrupt Acknowledge* (input, active Low). This input indicates to the CIO that an Interrupt Acknowledge cycle is in progress. $\overline{INTACK}$ must be synchronized to PCLK, and it must be stable throughout the Interrupt Acknowledge cycle.

**$PA_0$-$PA_7$.** *Port A I/O lines* (bidirectional, 3-state, or open-drain). These eight I/O lines transfer information between the CIO's Port A and external devices.

**$PB_0$-$PB_7$.** *Port B I/O lines* (bidirectional, 3-state, or open-drain). These eight I/O lines transfer information between the CIO's Port B and external devices. May also be used to provide external access to Counter/Timers 1 and 2.

**$PC_0$-$PC_3$.** *Port C I/O lines* (bidirectional, 3-state, or open-drain). These four I/O lines are used to provide handshake, $\overline{WAIT}$, and REQUEST lines for Ports A and B or to provide external access to Counter/Timer 3 or access to the CIO's Port C.

**PCLK.** *Peripheral Clock* (Input, TTL-compatible). This is the clock used by the internal control logic and the counter/timers in timer mode. It does not have to be the CPU clock.

**$\overline{RD}$*.** *Read* (Input, active Low). This signal indicates that a CPU is reading from the CIO. During an Interrupt Acknowledge cycle, this signal gates the interrupt vector onto the data bus if the CIO is the highest priority device requesting an interrupt.

**$\overline{WR}$*.** *Write* (Input, active Low). This signal indicates a CPU write to the CIO.

*When $\overline{RD}$ and $\overline{WR}$ are detected Low at the same time (normally an illegal condition), the CIO is reset.

## PACKAGE PINOUTS

T-52-33-05

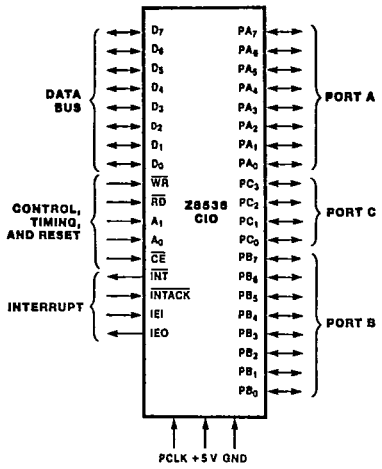



Figure 4. Pin Functions

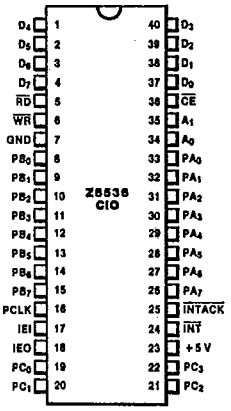



Figure 5. 40-Pin Dual-In-Line Package (DIP) Pin Assignments

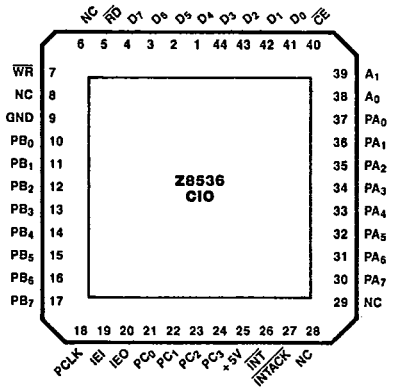



Figure 6. 44-Pin Chip Carrier, Pin Assignments

## MIL-STD-883 MILITARY PROCESSED PRODUCT

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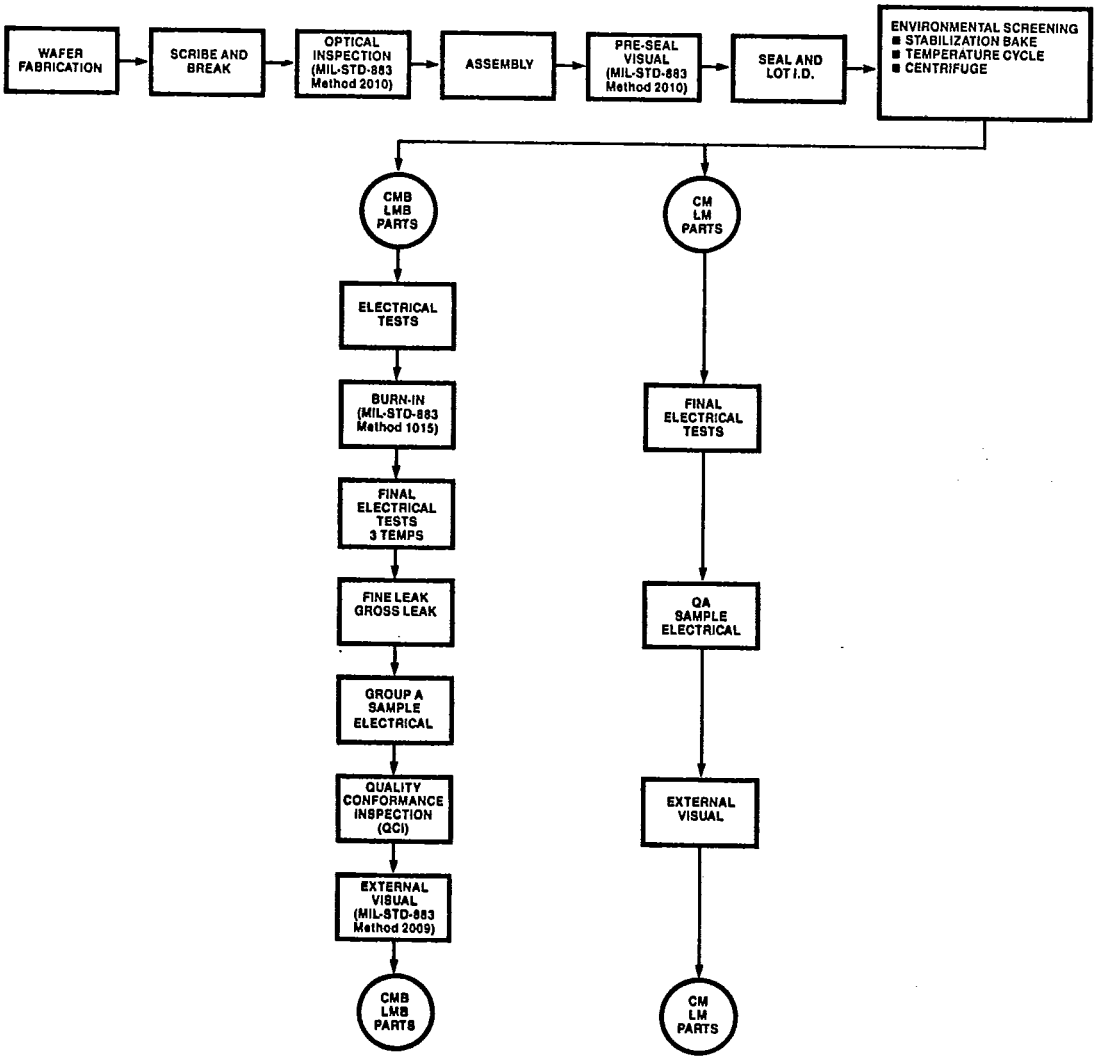
- Mil-Std-883 establishes uniform methods and procedures for testing microelectronic devices to insure the electrical, mechanical, and environmental integrity and reliability that is required for military applications.
- Mil-Std-883 Class B is the industry standard product assurance level for military ground and aircraft application.
- The total reliability of a system depends upon tests that are designed to stress specific quality and reliability concerns that affect microelectronic products.
- The following tables detail the 100% screening and electrical tests, sample electrical tests, and Qualification/ Quality Conformance testing required.

### Zilog Military Product Flow



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## Table I
## MIL-STD-883 Class B Screening Requirements
## Method 5004

| Test | Mil-Std-883 Method | Test Condition | Requirement |
|---|---|---|---|
| Internal Visual | 2010 | Condition B | 100% |
| Stabilization Bake | 1008 | Condition C | 100% |
| Temperature Cycle | 1010 | Condition C | 100% |
| Constant Acceleration (Centrifuge) | 2001 | Condition E or D(Note 1), $Y_1$ Axis Only | 100% |
| Initial Electrical Tests | | Zilog Military Electrical Specification Static/DC $T_C$ = +25°C | 100% |
| Burn-In | 1015 | Condition D(Note 2), 160 hours, $T_A$ = +125°C | 100% |
| Interim Electrical Tests | | Zilog Military Electrical Specification Static/DC $T_C$ = +25°C | 100% |
| PDA Calculation | | PDA = 5% | 100% |
| Final Electrical Tests | | Zilog Military Electrical Specification Static/DC $T_C$ = +125°C, −55°C Functional, Switching/AC $T_C$ = +25°C | 100% |
| Fine Leak | 1014 | Condition $A_2$ | 100% |
| Gross Leak | 1014 | Condition C | 100% |
| Quality Conformance Inspection (QCI) | | | |
| Group A Each Inspection Lot | 5005 | (See Table II) | Sample |
| Group B Every Week | 5005 | (See Table III) | Sample |
| Group C Periodically (Note 3) | 5005 | (See Table IV) | Sample |
| Group D Periodically (Note 3) | 5005 | (See Table V) | Sample |
| External Visual | 2009 | | 100% |
| QA—Ship | | | 100% |

NOTES:
1. Applies to larger packages which have an inner seal or cavity perimeter of two inches or more in total length or have a package mass of ≥5 grams.
2. In process of fully implementing of Condition D Burn-In Circuits. Contact factory for copy of specific burn-in circuit available.
3. Performed periodically as required by Mil-Std-883, paragraph 1.2.1 b(17).

## Table II Group A

T-52-33-05

**Sample Electrical Tests**
**MIL-STD-883 Method 5005**

| Subgroup | Tests | Temperature ($T_C$) | LTPD Max Accept = 2 |
|---|---|---|---|
| **Subgroup 1** | Static/DC | +25°C | 2 |
| **Subgroup 2** | Static/DC | +125°C | 3 |
| **Subgroup 3** | Static/DC | −55°C | 5 |
| **Subgroup 7** | Functional | +25°C | 2 |
| **Subgroup 8** | Functional | −55°C and +125°C | 5 |
| **Subgroup 9** | Switching/AC | +25°C | 2 |
| **Subgroup 10** | Switching/AC | +125°C | 3 |
| **Subgroup 11** | Switching/AC | −55°C | 5 |

NOTES:
- The specific parameters to be included for tests in each subgroup shall be as specified in the applicable detail electrical specification. Where no parameters have been identified in a particular subgroup or test within a subgroup, no Group A testing is required for that subgroup or test.
- A single sample may be used for all subgroup testing. Where required size exceeds the lot size, 100% inspection shall be allowed.
- Group A testing by subgroup or within subgroups may be performed in any sequence unless otherwise specified.

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## Table III Group B

**Sample Test Performed Every Week to Test Construction and Insure Integrity of Assembly Process. MIL-STD-883 Method 5005**

| Subgroup | Mil-Std-883 Method | Test Condition | Quantity or LTPD/Max Accept |
|---|---|---|---|
| **Subgroup 1** | | | |
| Physical Dimensions | 2016 | | 2/0 |
| **Subgroup 2** | | | |
| Resistance to Solvents | 2015 | | 4/0 |
| **Subgroup 3** | | | |
| Solderability | 2003 | Solder Temperature +245°C ± 5°C | 15(Note 1) |
| **Subgroup 4** | | | |
| Internal Visual and Mechanical | 2014 | | 1/0 |
| **Subgroup 5** | | | |
| Bond Strength | 2011 | C | 15(Note 2) |
| **Subgroup 6**(Note 3) | | | |
| Internal Water Vapor Content | 1018 | 1000 ppm. maximum at +100°C | 3/0 or 5/1 |
| **Subgroup 7**(Note 4) | | | |
| Seal | 1014 | | 5 |
| 7a) Fine Leak | | 7a) $A_2$ | |
| 7b) Gross Leak | | 7b) C | |
| **Subgroup 8**(Note 5) | | | |
| Electrostatic Discharge Sensitivity | 3015 | Zilog Military Electrical Specification Static/DC $T_C$ = +25°C A = 20-2000V B = >2000V Zilog Military Electrical Specification Static/DC $T_C$ = +25°C | 15/0 |

NOTES:
1. Number of leads inspected selected from a minimum of 3 devices.
2. Number of bond pulls selected from a minimum of 4 devices.
3. Test applicable only if the package contains a dessicant.
4. Test not required if either 100% or sample seal test is performed between final electrical tests and external visual during Class B screening.
5. Test required for initial qualification and product redesign.

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## Table IV Group C

**Sample Test Performed Periodically to Verify Integrity of the Die.**
**MIL-STD-883 Method 5005**

| Subgroup | Mil-Std-883 Method | Test Condition | Quantity or LTPD/Max Accept |
|---|---|---|---|
| **Subgroup 1** | | | |
| Steady State Operating Life | 1005 | Condition D(Note 1), 1000 hours at +125°C | 5 |
| End Point Electrical Tests | | Zilog Military Electrical Specification $T_C$ = +25°C, +125°C, −55°C | |
| **Subgroup 2** | | | |
| Temperature Cycle | 1010 | Condition C | |
| Constant Acceleration (Centrifuge) | 2001 | Condition E or D(Note 2), $Y_1$ Axis Only | |
| Seal | 1014 | | 15 |
| 2a) Fine Leak | | 2a) Condition $A_2$ | |
| 2b) Gross Leak | | 2b) Condition C | |
| Visual Examination | 1010 or 1011 | | |
| End Point Electrical Tests | | Zilog Military Electrical Specification $T_C$ = +25°C, +125°C, −55°C | |

NOTE:
1. In process of fully implementing Condition D Burn-In Circuits. Contact factory for copy of specific burn-in circuit available.
2. Applies to larger packages which have an inner seal or cavity perimeter of two inches or more in total length or have a package mass of ≥5 grams.

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## Table V Group D

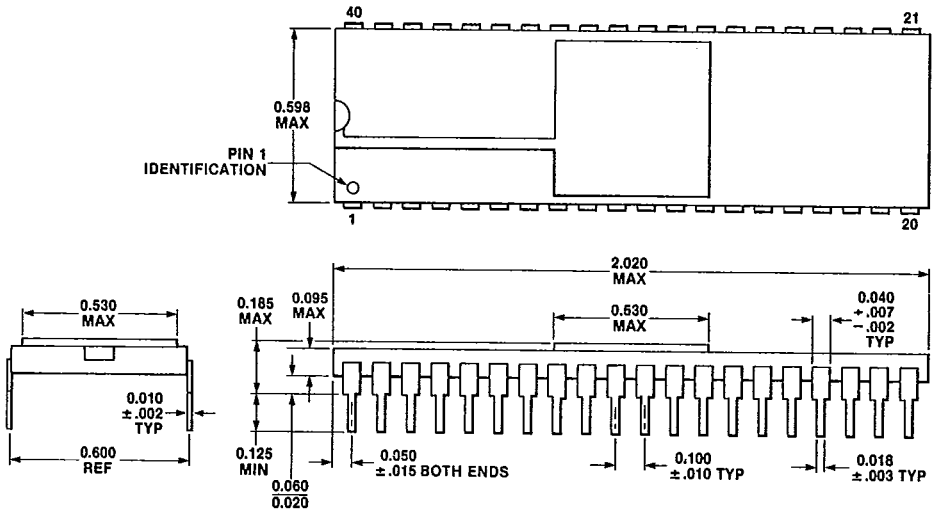
**Sample Test Performed Periodically to Insure Integrity of the Package.**
**MIL-STD-883 Method 5005**

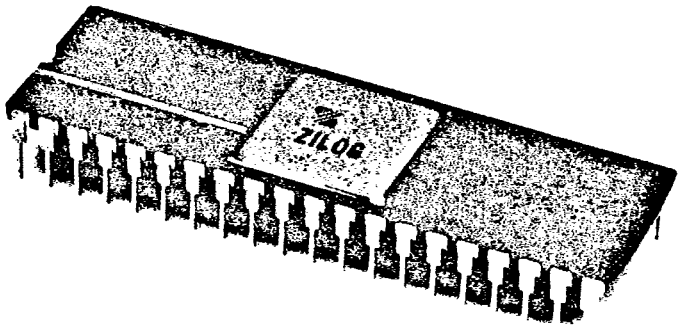
| Subgroup | Mil-Std-883 Method | Test Condition | Quantity or LTPD/Max Accept |
|---|---|---|---|
| **Subgroup 1** | | | |
| Physical Dimensions | 2016 | | 15 |
| **Subgroup 2** | | | |
| Lead Integrity | 2004 | Condition $B_2$ or D(Note 1) | 15 |
| **Subgroup 3** | | | |
| Thermal Shock | 1011 | Condition B minimum, 15 cycles minimum | |
| Temperature Cycling | 1010 | Condition C, 100 cycles minimum | 15 |
| Moisture Resistance | 1004 | | |
| Seal | 1014 | | |
| 3a) Fine Leak | | 3a) Condition $A_2$ | |
| 3b) Gross Leak | | 3b) Condition C | |
| Visual Examination | 1004 or 1010 | | |
| End Point Electrical Tests | | Zilog Military Electrical Specification $T_C$ = +25°C, +125°C, −55°C | |
| **Subgroup 4** | | | |
| Mechanical Shock | 2002 | Condition B minimum | |
| Vibration Variable Frequency | 2007 | Condition A minimum | |
| Constant Acceleration (Centrifuge) | 2001 | Condition E or D(Note 2), $Y_1$ Axis Only | 15 |
| Seal | 1014 | | |
| 4a) Fine Leak | | 4a) Condition $A_2$ | |
| 4b) Gross Leak | | 4b) Condition C | |
| Visual Examination | 1010 or 1011 | | |
| End Point Electrical Tests | | Zilog Military Electrical Specification $T_C$ = +25°C, +125°C, −55°C | |
| **Subgroup 5** | | | |
| Salt Atmosphere | 1009 | Condition A minimum | |
| Seal | 1014 | | 15 |
| 5a) Fine Leak | | 5a) Condition $A_2$ | |
| 5b) Gross Leak | | 5b) Condition C | |
| Visual Examination | 1009 | | |
| **Subgroup 6** | | | |
| Internal Water Vapor Content | 1018 | 5,000 ppm. maximum water content at +100°C | 3/0 or 5/1 |
| **Subgroup 7**(Note 3) | | | |
| Adhesion of Lead Finish | 2025 | | 15(Note 4) |
| **Subgroup 8**(Note 5) | | | |
| Lid Torque | 2024 | | 5/0 |

NOTES:
1. Lead Integrity Condition D for leadless chip carriers.
2. Applies to larger packages which have an inner seal or cavity perimeter of two inches or more in total length or have a package mass of ≥5 grams.
3. Not applicable to leadless chip carriers.
4. LTPD based on number of leads.
5. Not applicable for solder seal packages.

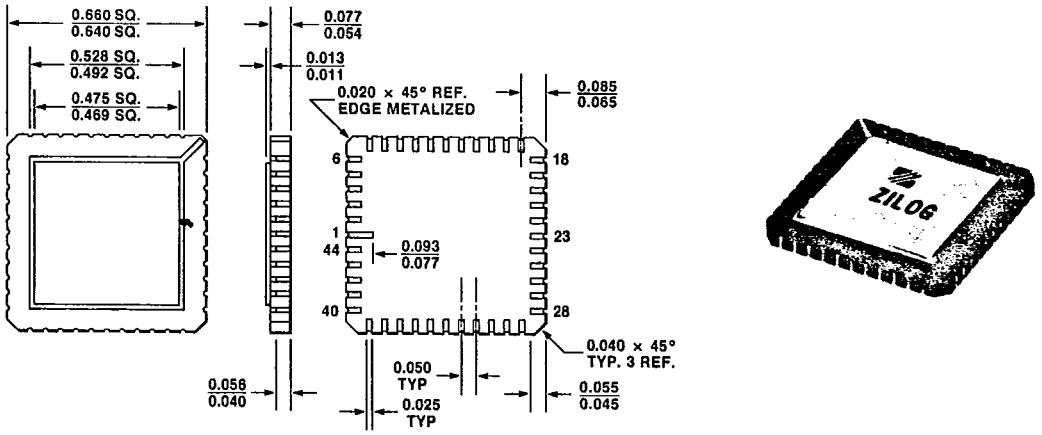
## PACKAGE INFORMATION

T-52-33-05



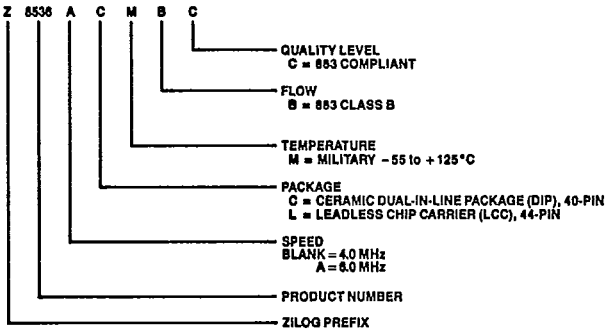

40-Pin Ceramic Dual In-line Package (DIP)




44-Pin Ceramic Leadless Chip Carrier (LCC)

## ZILOG ORDERING INFORMATION

T-52-33-05




## AVAILABLE MILITARY PRODUCTS

| Z8536 CIO, 4.0 MHz | | Z8536A CIO, 6.0 MHz | |
|---|---|---|---|
| **40-pin DIP** | **44-pin LCC** | **40-pin DIP** | **44-pin LCC** |
| Z8536 CM | Z8536 LM | Z8536A CM | Z8536A LM |
| Z8536 CMBC | Z8536 LMBC | Z8536A CMBC | Z8536A LMBC |