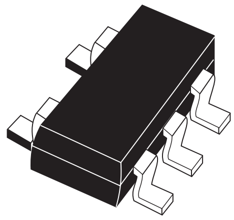
TSC101

High side current sense amplifier

Target Specification

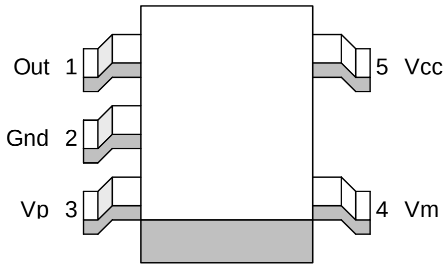
Features

- Independent supply and input common-mode voltages
- Wide common-mode operating range: 2.8 to 30V
- Wide common-mode surviving range: -0.3 to 60V (load-dump)
- Wide supply voltage range: 4 to 28V
- Low current consumption: I_{CC} max = 300µA
- Internally fixed gain: 20V/V, 50V/V or 100V/V
- Buffered output



L
SOT23-5
(Plastic package)

Pin connections
(top view)



Applications

- Battery chargers
- Automotive current monitoring
- Notebook computers
- DC motor control
- Precision current sources

Description

The TSC101 measures a small differential voltage on a high-side shunt resistor and translates it into a ground-referenced output voltage. The gain is internally fixed.

Wide input common-mode voltage range, low quiescent current, and tiny SOT23 packaging enable use in a wide variety of applications.

Input common-mode and power supply voltages are independent. Common-mode voltage can range from 2.8V to 30V in operating conditions and up to 60V in absolute maximum ratings.

Current consumption lower than 300µA and wide supply voltage range allow to connect the power supply to either side of the current measurement shunt with minimal error.

Contents

1 Application schematic and pin description

The TSC101 high-side current-sense amplifier features a 2.8V to 30V input common-mode range that is independent of supply voltage. The main advantage of this feature is to allow high-side current sensing at voltages much greater than the supply voltage (V_{CC}).

Figure 1. Application schematic

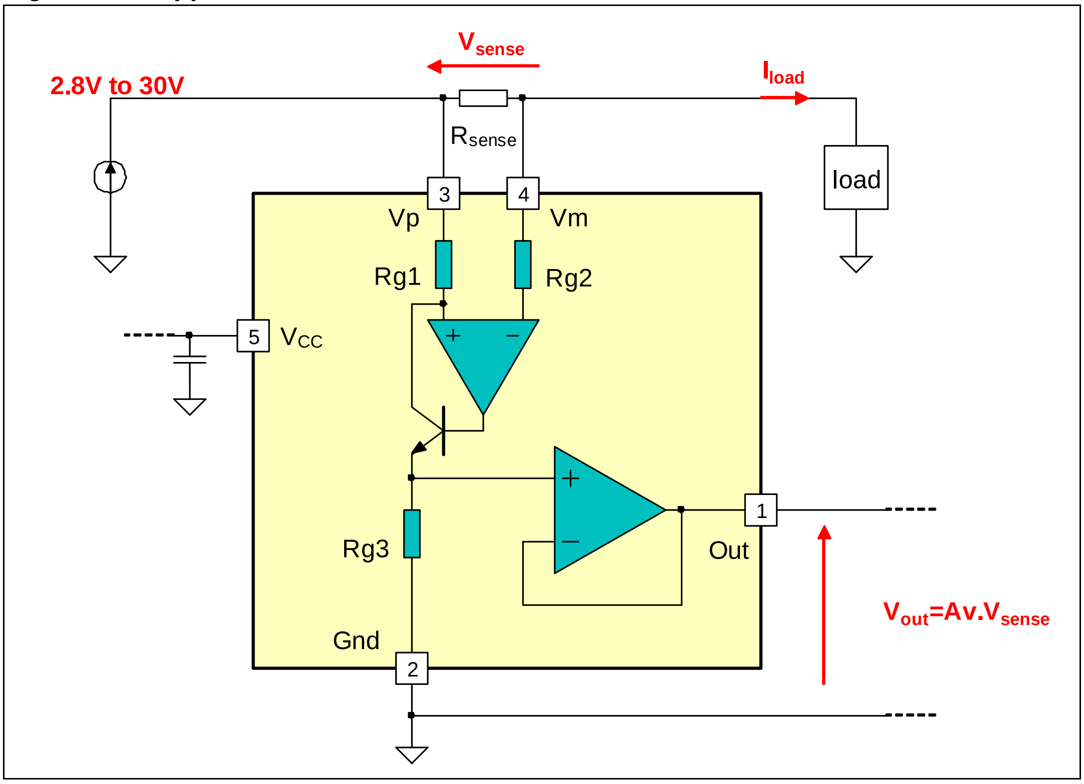


Table 1 below describes the function of each pin. Their position is shown in the illustration on the cover page and in *Figure 1* above.

Table 1. Pin description

Symbol	Type	Function
Out	Analog output	The OUT voltage is proportional to the magnitude of the sense voltage V_p-V_m.
Gnd	Power supply	Ground line.
V_{CC}	Power supply	Positive power supply line.
V_p	Analog input	Connection for the external sense resistor. The measured current enters the shunt on the V_p side.
V_m	Analog input	Connection for the external sense resistor. The measured current exits the shunt on the V_m side.

2 Absolute maximum ratings and operating conditions

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{id}	Input pins differential voltage (V_p-V_m)	±60	V
V_i	Input pin voltages (V_p, V_m)(1)	-0.3 to 60	V
V_{CC}	DC supply voltage(1)	-0.3 to 30	V
V_{out}	DC output pin voltage(1)	-0.3 to 28	V
T_{stg}	Storage temperature	-55 to 150	°C
T_j	Maximum junction temperature	150	°C
ESD(2)	Human body model (HBM)	2	kV
	Machine model (MM)	200	V

1. Voltage values are measured with respect to the GND pin.
2. ESD test for each couple of pins.

Table 3. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage from T_{min} to T_{max}	4.0 to 28	V
T_{oper}	Operational temperature range (T_{min} to T_{max})	-40 to 125	°C
R_{thja}	SOT23-5 thermal resistance junction to ambient	250	°C/W

3 Electrical characteristics

The electrical characteristics given in the following tables are measured under the following test conditions unless otherwise specified:

T_{amb}=25°C, V_{CC}=12V, V_{sense}=V_p-V_m=50mV, V_m=12V, no load on Out

Table 4. Supply

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{CC}	Total supply current	V_{sense} = 0 T_{min} < T_{amb} < T_{max}			300	µA

Table 5. Input

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{icm}	Common mode voltage range	T_{min} < T_{amb} < T_{max}	2.8		30	V
DC CMR	DC common mode rejection Variation of V_{out} versus V_{icm} referred to input(1)	2.8V< V_{icm} < 30V T_{min} < T_{amb} < T_{max}	90	105		dB
AC CMR	AC common mode rejection Variation of V_{out} versus V_{icm} referred to input (peak-to-peak voltage variation)	2.8V< V_{icm} < 30V 1kHz sine wave		95		dB
		2.8V< V_{icm} < 30V 10kHz sine wave		80		dB
SVR	Supply voltage rejection Variation of V_{out} versus V_{CC}(2)	4.0V< V_{CC} < 28V V_{sense}=30mV T_{min} < T_{amb} < T_{max}	90	105		dB
V_{os}	Input offset voltage(3)	T_{amb}=25°C T_{min} < T_{amb} < T_{max}		±0.2 ±0.9	±1.5 ±2.3	mV
dV_{os}/dT	Input offset drift vs. T	T_{min} < T_{amb} < T_{max}	0		4.5	µV/°C
I_{lk}	Input leakage current	V_{CC}=0V T_{min} < T_{amb} < T_{max}			1	µA
I_{ib}	Input bias current	V_{sense}=0V T_{min} < T_{amb} < T_{max}		5.5	8	µA

1. See *Section 4: Parameter definitions on page 8* for the definition of CMR.
2. See *Section 4: Parameter definitions on page 8* for the definition of SVR.
3. See *Section 4: Parameter definitions on page 8* for the definition of V_{os}.

Table 6. Output

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Av	Gain	TSC101A TSC101B TSC101C		20 50 100		V/V
ΔAv	Gain accuracy	T_{amb}=25°C $T_{min} < T_{amb} < T_{max}$			±3 ±5	%
$\Delta V_{out}/\Delta T$	Output voltage drift vs. T(1)	$T_{min} < T_{amb} < T_{max}$	-600	-300	0	µV/°C
$\Delta V_{out}/\Delta I_{out}$	Output stage load regulation	-10mA < I_{out} <1 0mA I_{out} sink or source current		2	tbd	mV/mA
ΔV_{out}	Total output voltage accuracy(2)	V_{sense}=10mV T_{amb}=25° C $T_{min} < T_{amb} < T_{max}$			tbd tbd	%
ΔV_{out}	Total output voltage accuracy	V_{sense}=20mV T_{amb}=25° C $T_{min} < T_{amb} < T_{max}$			tbd tbd	%
ΔV_{out}	Total output voltage accuracy	V_{sense}=50mV T_{amb}=25° C $T_{min} < T_{amb} < T_{max}$			tbd tbd	%
ΔV_{out}	Total output voltage accuracy	V_{sense}=100mV T_{amb}=25° C $T_{min} < T_{amb} < T_{max}$			tbd tbd	%
I_{sc}	Short-circuit current	OUT connected to V_{CC} or GND	15	40		mA
V_{OH}	Output stage high-state saturation voltage $V_{OH}=V_{CC}-V_{out}$	V_{sense}=1V I_{out}=1mA		0.8	1	V
V_{OL}	Output stage low-state saturation voltage	V_{sense}=-1V I_{out}=1mA		50	100	mV

1. See *Section 4: Parameter definitions on page 8* for the definition of output voltage drift versus temperature.
2. Output voltage accuracy is the difference with the expected theoretical output voltage $V_{out-th}=Av*V_{sense}$. See *Section 4: Parameter definitions on page 8* for a more detailed definition.

Table 7. Frequency response

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
ts	Output settling to 1% final value	V_{sense}=10mV to 100mV, C_{load}=47pF				
		TSC101A		3		µs
		TSC101B		6		µs
		TSC101C		10		µs
SR	Slew rate	V_{sense}=10mV to 100mV	0.55	0.9		V/µs
BW	3dB bandwidth	C_{load}=47pF V_{icm}=12V V_{sense}=100mV				
		TSC101A		650		kHz
		TSC101B		710		kHz
		TSC101C		540		kHz

Table 8. Noise

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
	Total output voltage noise			50		$nV/\sqrt{Hz}$

4 Parameter definitions

Common mode rejection ratio (CMR)

The common-mode rejection ratio (CMR) measures the ability of the current-sensing amplifier to reject any DC voltage applied on both inputs V_p and V_m. The CMR is referred back to the input so that its effect can be compared with the applied differential signal. The CMR is defined by the formula:

$$CMR = -20 \cdot \log \frac{\Delta V_{out}}{\Delta V_{icm} \cdot Av}$$

Supply voltage rejection ratio (SVR)

The supply-voltage rejection ratio (SVR) measures the ability of the current-sensing amplifier to reject any variation of the supply voltage V_{CC}. The SVR is referred back to the input so that its effect can be compared with the applied differential signal. The SVR is defined by the formula:

$$SVR = -20 \cdot \log \frac{\Delta V_{out}}{\Delta V_{CC} \cdot Av}$$

Gain (Av) and input offset voltage (V_{os})

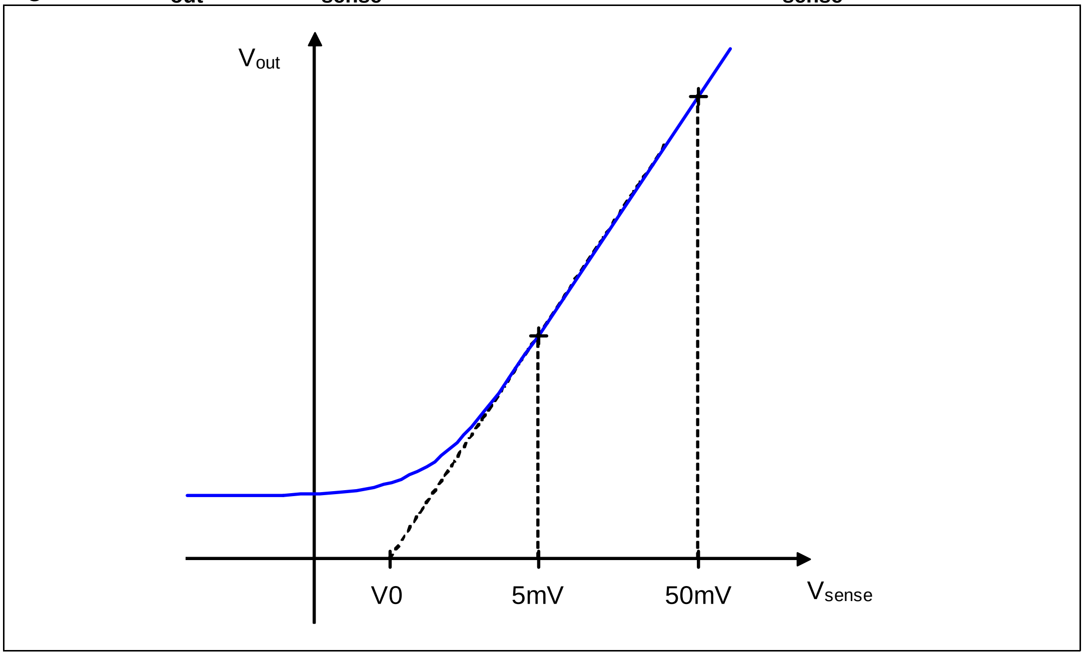
The input offset voltage is defined as the intersection between the linear regression of V_{out} vs. V_{sense} curve with the X-axis (see *Figure 2*). If V_{out1} is the output voltage with $V_{sense}=V_{sense1}=50mV$ and V_{out2} is the output voltage with $V_{sense}=V_{sense2}=5mV$, then V_{os} can be calculated with the following formula:

$$V_{os} = V_{sense1} - \left(\frac{V_{sense1} - V_{sense2}}{V_{out1} - V_{out2}} \cdot V_{out1}\right)$$

The amplification gain Av is defined as the ratio between output voltage and input differential voltage:

$$Av = \frac{V_{out}}{V_{sense}}$$

Figure 2. V_{out} versus V_{sense} characteristics: detail for low V_{sense} values



Output voltage drift versus temperature

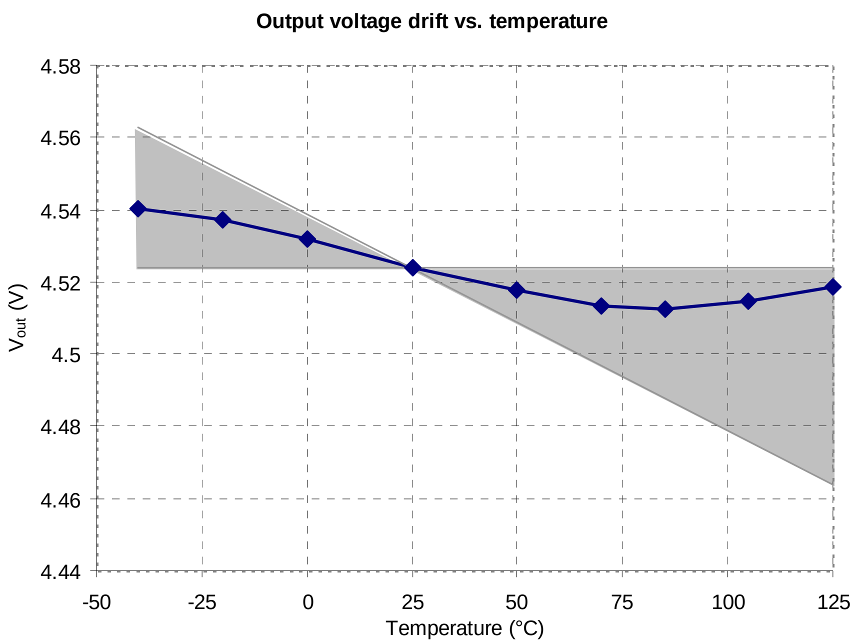
The output voltage drift versus temperature is defined as the maximum variation of V_{out} with respect to its value at 25°C, over the temperature range.It is calculated as follows:

$$\frac{\Delta V_{out}}{\Delta T} = \max \frac{V_{out}(T_{amb}) - V_{out}(25^\circ C)}{T_{amb} - 25^\circ C}$$

with $T_{min} < T_{amb} < T_{max}$.

Figure 3 provides a graphical definition of output voltage drift versus temperature. On this chart, V_{out} is always comprised in the grey area defined by the maximum and minimum variation of V_{out} vs. T, and T=25°C is considered to be the reference.

Figure 3. Output voltage drift versus temperature



Output voltage accuracy

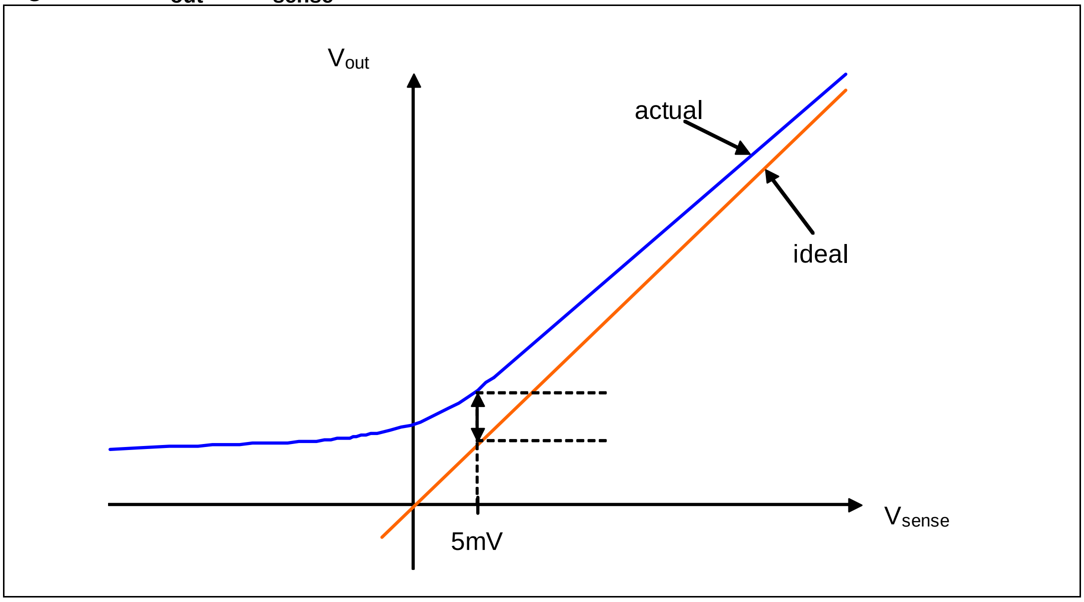
The output voltage accuracy is the difference between the actual output voltage and the theoretical output voltage. Ideally, the current sensing output voltage should be equal to the input differential voltage multiplied by the theoretical gain, as in the following formula:

$V_{out\text{-}th} = Av \cdot V_{sense}$

The actual value is very slightly different, mainly due to the effects of:

- the input offset voltage V_{os},
- non-linearity,
- V_{OL} and V_{OH} voltage saturation (see *Figure 5 on page 12*)

Figure 4. V_{out} vs. V_{sense} theoretical and actual characteristics



The output voltage accuracy, expressed in percentage, can be calculated with the following formula:

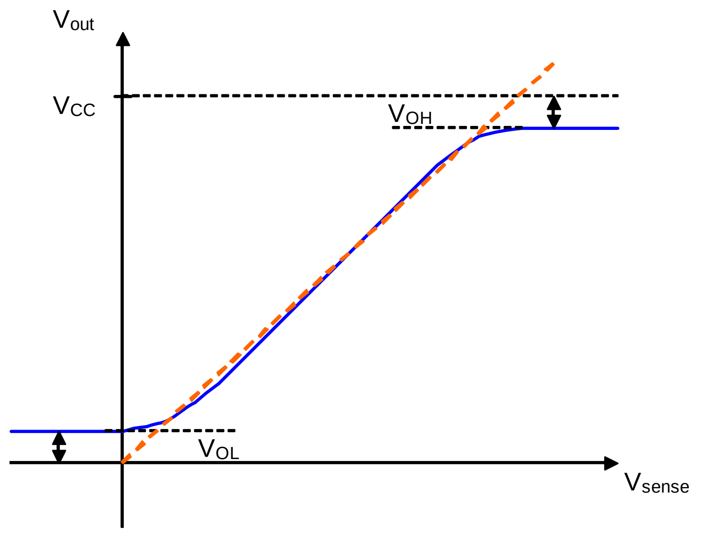
$$\Delta V_{out} = \frac{abs(V_{out} - (Av \cdot V_{sense}))}{Av \cdot V_{sense}}$$

with Av=20V/V for TSC101A, Av=50V/V for TSC101B and Av=100V/V for TSC101C.

Output voltage range

The output voltage versus input differential voltage is linear in a range of output voltage limited by high-level and low-level saturation voltage.

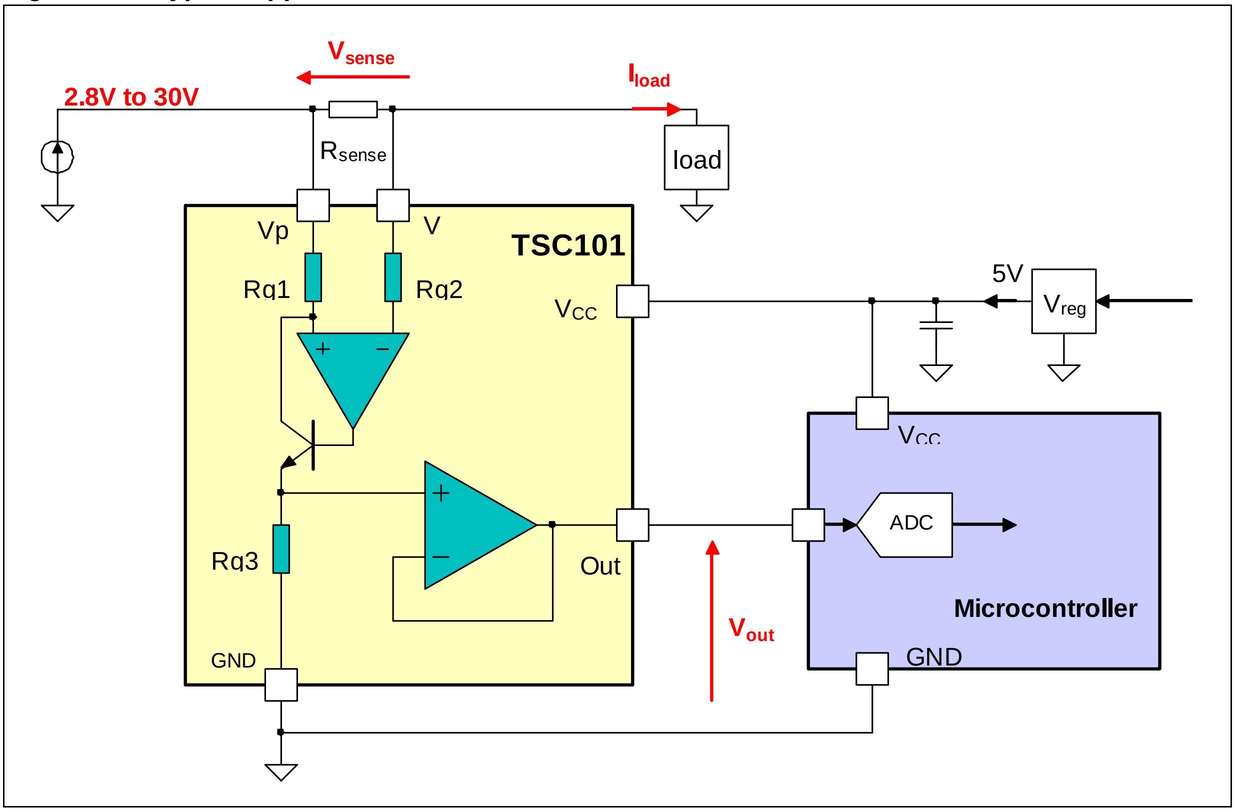
Figure 5. V_{out} vs. V_{sense} over the full voltage range



5 Application information

TSC101 can be used to measure current and to feed back the information to a micro controller, as shown in *Figure 6* below.

Figure 6. Typical application schematic



The current from the supply flows to the load through the R_{sense} resistor causing a voltage drop equal to V_{sense} across R_{sense}. The amplifier input currents are negligible, therefore its inverting input voltage is equal to V_m. The amplifier's open-loop gain forces its non-inverting input to the same voltage as the inverting input. As a consequence, the amplifier will adjust current flowing through Rg1 so that the voltage drop across Rg1 will exactly match V_{sense}.

Therefore, the drop across Rg1 is:

$$V_{Rg1}=V_{sense}=R_{sense}.I_{load}$$

If I_{Rg1} is the current flowing through Rg1, then I_{Rg1} is given by the formula:

$$I_{Rg1}=V_{sense}/Rg1$$

The I_{Rg1} current flows entirely into resistor R_{g3} (the input bias current of the buffer is negligible). Therefore, the voltage drop on the R_{g3} resistor can be calculated as follows:

$$V_{Rg3}=R_{g3}.I_{Rg1}=(R_{g3}/R_{g1}).V_{sense}$$

Because the voltage across the R_{g3} resistor is buffered to the Out pin, V_{out} can be expressed as:

$$V_{out}=(R_{g3}/R_{g1}).V_{sense}$$

or

$$V_{out}=(R_{g3}/R_{g1}).R_{sense}.I_{load}$$

The resistor ratio R_{g3}/R_{g1} is internally set to 20V/V for TSC101A, to 50V/V for TSC101B and to 100V/V for TSC101C.

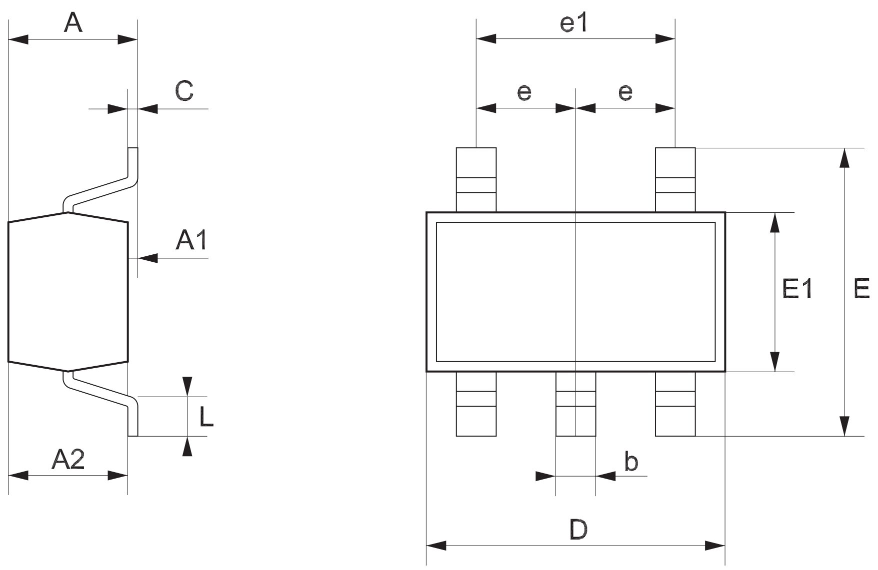
Because they define the full scale output range of your application, the R_{sense} resistor and the R_{g3}/R_{g1} resistor ratio (equal to Av) are important parameters, and therefore must be selected carefully.

6 Package information

In order to meet environmental requirements, STMicroelectronics offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an STMicroelectronics trademark. ECOPACK specifications are available at: www.st.com.

Figure 7. SOT23-5 package

Ref.	Dimensions					
	Millimeters			Mils		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.90		1.45	35.4		57.1
A1	0.00		0.15	0.00		5.9
A2	0.90		1.30	35.4		51.2
b	0.35		0.50	13.7		19.7
C	0.09		0.20	3.5		7.8
D	2.80		3.00	110.2		118.1
E	2.60		3.00	102.3		118.1
E1	1.50		1.75	59.0		68.8
e		0.95			37.4	
e1		1.9			74.8	
L	0.35		0.55	13.7		21.6



7 Ordering information

Table 9. Order codes

Part number	Temperature range	Package	Packaging	Marking	Gain
TSC101AILT	-40°C, +125°C	SOT23-5	Tape & reel	O104	20
TSC101BILT				O105	50
TSC101CILT				O106	100
TSC101AIYLT[1]	-40°C, +125°C automotive grade	SOT23-5	Tape & reel	O101	20
TSC101BIYLT[1]				O102	50
TSC101CIYLT[1]				O103	100

1. Qualified and characterized according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 & Q 002 or equivalent.

8 Revision history

Date	Revision	Changes
5-Mar-2007	Rev 1	First release, preliminary data.

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