

## Features

- **AUDIO CODEC**
  - 100dB Dynamic Range Stereo Audio DAC - 8 to 96 kHz sampling frequency
  - 96dB Dynamic Range Stereo Audio ADC - 8 to 96 kHz sampling frequency
  - 16 / 32 Ohms headset amplifier with capless operation
    - SNR: 97 dB A-Weighted
    - THD: -60 dB (16Ohms / 20mW / 3.3V supply)
    - Maximum output power: 55mW (16Ohms / 3.3V supply)
  - Stereo line inputs, stereo auxiliary inputs
  - Stereo microphone inputs with bias generator for electret device
  - Low power Analog Bypass mode (Line / Aux in to Headset Out)
  - Low power Analog sidetone mode (Microphone in to Headset Out)
  - Automatic Audio path control with smooth fade in / fade out operation
  - I<sup>2</sup>S port
    - Master / Slave Operation
    - I<sup>2</sup>S / Left / Right justified modes
    - 16 / 18 / 20 / 24 bit operation
- **6x SUPPLY CHANNEL VOLTAGE REGULATORS**
  - DCDC0:
    - 1.85V - 600mA. 0.8 to 3.6V / 50mV step.
    - 2 MHz switching buck regulator
    - Fast load transient response - PWM / PFM modes.
    - Efficiency up to 92%
  - DCDC1:
    - 1.2V - 600mA. 0.8 to 3.6V / 50mV step.
    - 2 MHz switching buck regulator
    - Fast load transient response - PWM / PFM modes.
    - Efficiency up to 90%
  - LDO2: 1V - 300mA. 0.8 to 1.35V / 50mV step - Fast transient response
  - LDO3: 3.3V - 200mA. 2.7 to 3.6V / 50mV step - Fast transient response
  - LDO4: 3.3V - 200mA. 2.7 to 3.6V / 50mV step - Audio codec supply
  - LDO5: 2.5V - 10mA - Backup battery charger and RTC supply
- **LOW CONSUMPTION POWER MANAGER**
  - 2.5V - 5.5V VIN Operation
  - 20uA typical consumption OFF mode
  - VIN monitor, CPU supplies monitor
  - Die temperature and over-current protections
  - Reset and Interrupt generation
  - Automatic Voltage Ramping on supply channels for DVS applications
  - Standby mode with selectable supplies OFF
- **RTC**
  - Ultra Low power crystal oscillator (<1uA typ.)
  - Wake up function with programmable alarm or selectable inputs
- 10-b / 300kS/s ADC with 4 external / 6 internal selectable inputs
- Two-Wire Interface for PMU and Audio controls
- Available in 7.5 x 7.5 x 0.9 mm 64-pin QFN Package
- Applications: Multimedia, Audio + Supply solution for MPU+DDR2 designs.



## Power Management and Analog Companions (PMAAC)

### AT73C246 6 Supply Channel PMU With Audio Codec

11050A-PMAAC-07-Apr-10



## 1. Description

The AT73C246 is an integrated high performance Power Management and Audio IC. It is specifically designed for advanced technology application processors with complex and low voltage supplies targeting audio applications from low to high end. This System-on-Chip allows significant savings in both cost and board area over previous discrete solutions.

Directly operated from a 2.9V to 5.5V input voltage, the PMU generates a set of 4 regulated power supplies and an associated delayed reset signal. These 4 voltages are built up with 2 high efficiency DCDC buck converters and 2 low noise LDOs. Featuring ultra fast transient responses and integrating automatic voltage scaling function, these supplies perfectly fit with modern low voltage MCU cores and memory supplies (DDR, Flash, ...). An additional 200mA LDO under software control is provided for auxiliary application functions. The high performances of this LDO (high PSRR, low noise, fast transient response) makes it ideal for analog front-ends (Audio, RF...) as well digital peripherals.

Aside from the PMU, the AT73C246 integrates a complete state-of-the art low power audio codec with headphone amplifier. On the input side, a stereo microphone preamplifier with differential or single ended connection (MICDIFF / MIC) and 2 selectable stereo inputs (LINE / AUX) are directed to a 96dB Dynamic Range stereo audio ADC through an input mixer. On the output side a 100dB dynamic range stereo audio DAC drives, through an output mixer, a 60 mW stereo headphone amplifier which comes along with a VCM buffer. This VCM buffer allows to save two large on-board coupling capacitors for area constrained applications. Additionally two fully analog paths called bypass and sidetone from line / aux and microphone inputs to headphone outputs allow to reduce the audio power consumption to minimum when needed.

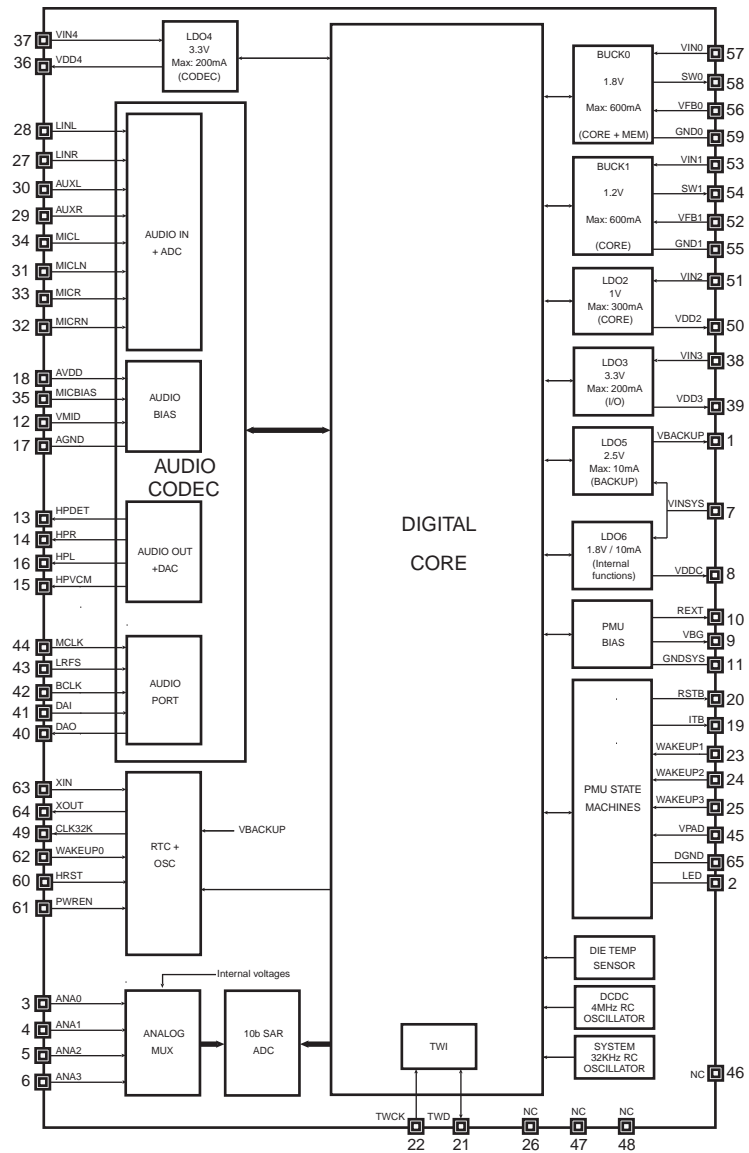
The PMU is complemented with a low power RTC system including a recharging LDO, a crystal oscillator and a programmable alarm that is fully integrated in the PMU digital core. Thus, the RTC function is able to wake up the PMU, i.e the regulated power supplies, at a programmed instant.

Also, a 10-bit ADC equipped with a 10:1 analog multiplexer is provided to the application to perform voltage measurements.

Finally, to reduce power consumption to minimum, the PMU features a flexible STANDBY mode where the MCU is placed in reset state with selectable supplies ON, OFF or in low-power mode. Power consumption in OFF mode is typically 20uA.

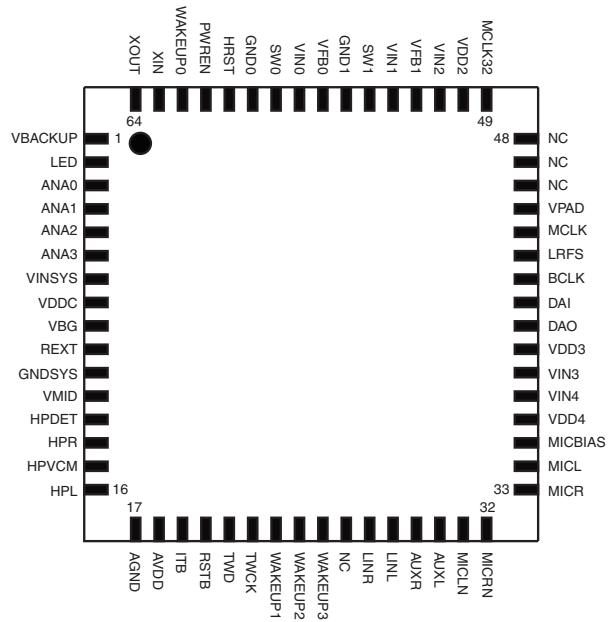
## 2. Block Diagram

Figure 2-1. AT73C246 functional block diagram



### 3. Package and Pinout

Figure 3-1. AT73C246 QFN64 package pinout - Top view





## 4. Pin Description

**Table 4-1.** Pin Description

| Pin Name | I/O          | Pin Number | Type    | Function  |
|----------|--------------|------------|---------|---|
| VBACKUP  | Output       | 1          | Analog  | RTC supply  |
| LED      | Output       | 2          | Digital | Output for blinking led. Leave not connected if a LED is not wired. |
| ANA0     | Input        | 3          | Analog  | Measurement input 0   |
| ANA1     | Input        | 4          | Analog  | Measurement Input 1   |
| ANA2     | Input        | 5          | Analog  | Measurement Input 2   |
| ANA3     | Input        | 6          | Analog  | Measurement Input 3   |
| VINSYS   | Input        | 7          | Power   | PMU core supply   |
| VDDC     | Output       | 8          | Analog  | PMU / Audio digital supply. Internal use only. No resistive load.   |
| VBG      | Output       | 9          | Analog  | PMU Voltage reference   |
| REXT     | Output       | 10         | Analog  | Resistor connection for PMU bias current                            |
| GNDSYS   | GND          | 11         | Analog  | PMU ground  |
| VMID     | Output       | 12         | Analog  | Audio Codec Mid-Supply reference                                    |
| HPDET    | Input        | 13         | Analog  | Headset detector  |
| HPR      | Output       | 14         | Analog  | Headset output right  |
| HPVCM    | Output       | 15         | Analog  | Headset virtual ground output                                       |
| HPL      | Output       | 16         | Analog  | Headset output left   |
| AGND     | GND          | 17         | Analog  | Audio Codec ground  |
| AVDD     | Input        | 18         | Power   | Audio Codec supply input  |
| ITB      | Output       | 19         | Digital | Interrupt request - Active low - Open-drain                         |
| RSTB     | Output       | 20         | Digital | CPU reset - Active low - Open drain                                 |
| TWD      | Input/Output | 21         | Digital | Two Wire Interface - Data   |
| TWCK     | Input        | 22         | Digital | Two Wire Interface - Clock  |
| WAKEUP1  | Input        | 23         | Digital | Wake up 1 Input - VPAD level - 100k Pull down                       |
| WAKEUP2  | Input        | 24         | Digital | Wake up 2 Input - VPAD level - 100k Pull down                       |
| WAKEUP3  | Input        | 25         | Digital | Wake up 3 input - VPAD level - 100k Pull down                       |
| NC       | -            | 26         | -       | Connect to DGND   |
| LINR     | Input        | 27         | Analog  | Audio Line input right  |
| LINL     | Input        | 28         | Analog  | Audio Line input left   |
| AUXR     | Input        | 29         | Analog  | Audio auxiliary input right   |
| AUXL     | Input        | 30         | Analog  | Audio auxiliary input left  |

**Table 4-1. Pin Description**

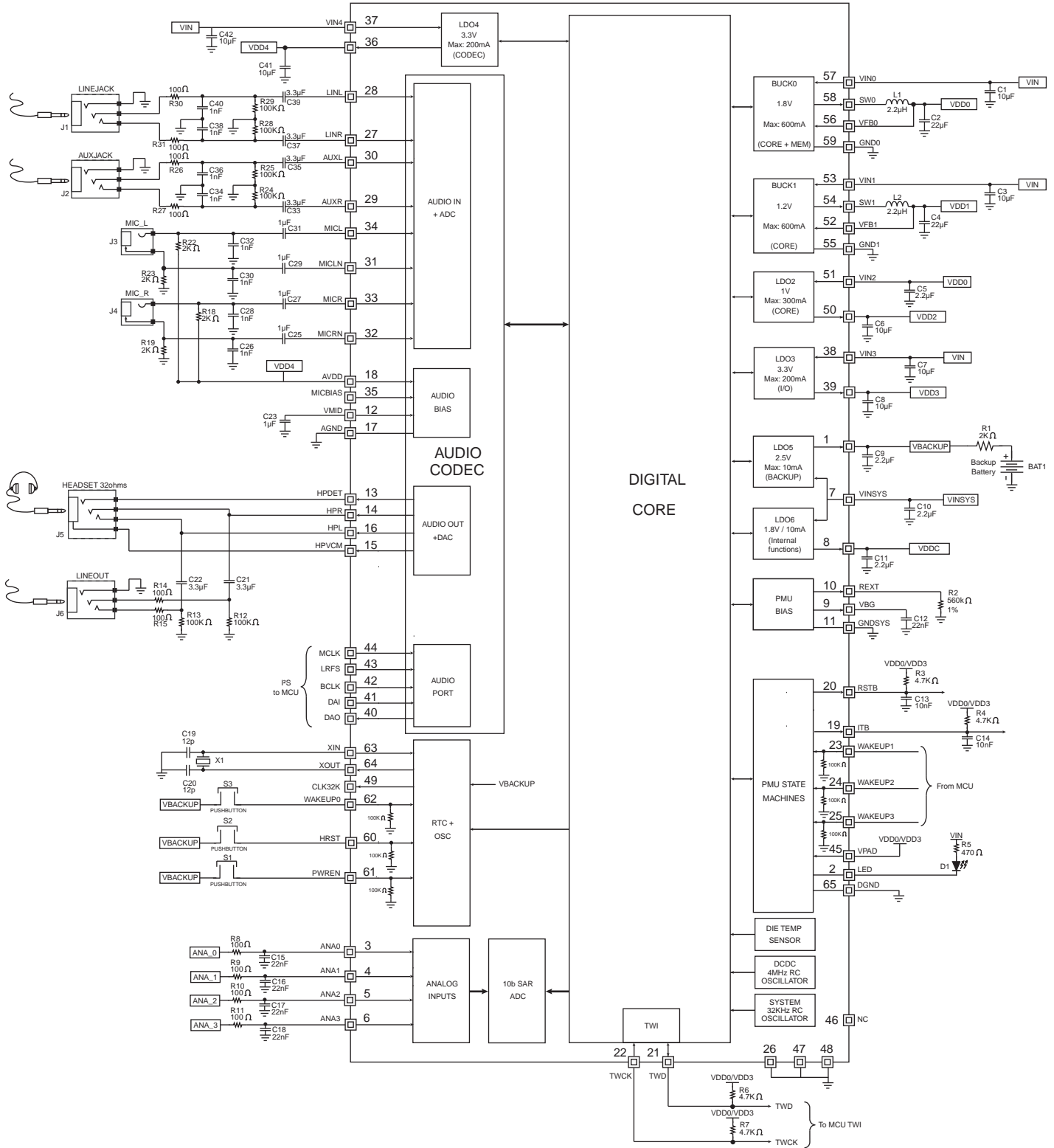
| Pin Name | I/O          | Pin Number | Type    | Function   |
|----------|--------------|------------|---------|--|
| MICLN    | Input        | 31         | Analog  | Audio negative microphone input left             |
| MICRN    | Input        | 32         | Analog  | Audio negative microphone input right            |
| MICR     | Input        | 33         | Analog  | Audio positive microphone input right            |
| MICL     | Input        | 34         | Analog  | Audio positive microphone input left             |
| MICBIAS  | Output       | 35         | Analog  | Voltage bias for electret microphone             |
| VDD4     | Output       | 36         | Power   | LDO4 output - 3.3V typ                           |
| VIN4     | Input        | 37         | Analog  | LDO4 input                                       |
| VIN3     | Input        | 38         | Power   | LDO3 input                                       |
| VDD3     | Output       | 39         | Analog  | LDO3 output - 3.3V typ                           |
| DAO      | Output       | 40         | Digital | Digital audio port data output                   |
| DAI      | Input        | 41         | Digital | Digital audio port data input                    |
| BCLK     | Input/Output | 42         | Digital | Digital audio port bit clock                     |
| LRFS     | Input/Output | 43         | Digital | Digital audio port left/right clock              |
| MCLK     | Input        | 44         | Digital | Audio codec master clock input                   |
| VPAD     | Input        | 45         | Power   | PMU I/O ring supply                              |
| NC       | -            | 46         | -       | Leave open                                       |
| NC       | -            | 47         | -       | Connect to DGND                                  |
| NC       | -            | 48         | -       | Connect to DGND                                  |
| MCLK32   | Output       | 49         | Digital | RTC clock output - VPAD level                    |
| VDD2     | Output       | 50         | Analog  | LDO2 output                                      |
| VIN2     | Input        | 51         | Power   | LDO2 input                                       |
| VFB1     | Input        | 52         | Analog  | DCDC1 Voltage feedback input                     |
| VIN1     | Input        | 53         | Power   | DCDC1 power stage supply                         |
| SW1      | Output       | 54         | Analog  | DCDC1 power stage output                         |
| GND1     | Ground       | 55         | Analog  | DCDC1 power stage ground                         |
| VFB0     | Input        | 56         | Analog  | DCDC0 Voltage feedback input                     |
| VIN0     | Input        | 57         | Analog  | DCDC0 power stage supply                         |
| SW0      | Output       | 58         | Analog  | DCDC0 power stage output                         |
| GND0     | Ground       | 59         | Analog  | DCDC0 power stage ground                         |
| HRST     | Input        | 60         | Digital | Hard reset - VBACKUP level - 100k Pull down      |
| PWREN    | Input        | 61         | Digital | Power on/off - VBACKUP level - 100k Pull down    |
| WAKEUP0  | Input        | 62         | Digital | Wake up 0 input - VBACKUP level - 100k Pull down |

**Table 4-1.** Pin Description

| Pin Name | I/O    | Pin Number | Type   | Function                          |
|----------|--------|------------|--------|-----------------------------------|
| XIN      | Input  | 63         | Analog | RTC crystal oscillator input      |
| XOUT     | Output | 64         | Analog | RTC crystal oscillator output     |
| DGND     | Ground | 65         | Analog | PMU digital ground + Thermal pad. |

## 5. Application Block Diagram

Figure 5-1. AT73C246 Application Block Diagram



**Table 5-1.** Typical Application Components Design

| Schematic Reference                               | Value         | Description   |
|---|---------------|---|
| R1, R18, R19, R22, R23                            | 2k $\Omega$   | 5% / 0.063W   |
| R2  | 560k $\Omega$ | 1% / 0.063W   |
| R3, R4, R6,R7                                     | 4.7k $\Omega$ | 5% / 0.063W   |
| R5  | 470 $\Omega$  | 5% / 0.063W   |
| R8, R9, R10, R11, R14, R15,<br>R26, R27, R30, R31 | 100 $\Omega$  | 5% / 0.063W   |
| R12, R13, R24, R25, R28,<br>R29                   | 100k $\Omega$ | 5% / 0.063W   |
| C1, C3, C6, C7, C8, C10,<br>C41, C42              | 10 $\mu$ F    | X5R / 6.3V<br>TDK: C1608X5R0J106MT<br>MURATA: GRM188R60J106ME47 |
| C2, C4  | 22 $\mu$ F    | X5R / 6.3V<br>TDK: C2012X5R0J226M<br>MURATA: GRM21BR60J226ME39  |
| C5, C9, C11                                       | 2.2 $\mu$ F   | X5R / 6.3V  |
| C23, C25, C27, C29, C31                           | 1 $\mu$ F     | X5R / 6.3V  |
| C13, C14  | 10nF          | X5R / 6.3V  |
| C15, C16, C17, C18, C12                           | 22nF          | X5R / 6.3V  |
| C19, C20  | 12pF          | C0G / 25V   |
| C21, C22, C33, C35, C37,<br>C39                   | 3.3 $\mu$ F   | X5R / 6.3V  |
| C26, C28, C30, C32, C34,<br>C36, C38, C40         | 1nF           | X5R   |
| L1, L2  | 2.2 $\mu$ H   | COILCRAFT: LPS3314-222  |



## 6. Absolute Maximum Ratings

**Table 6-1.** Absolute Maximum Ratings

|   |                                   |
|---|-----------------------------------|
| Operating Temperature (Industrial).....   | -40 C to + 85-C <sup>(1)</sup>    |
| Storage Temperature.....  | -55°C to + 150°C                  |
| Power Supply Input on V <sub>INSYS</sub> , V <sub>IN{0,1,3,4}</sub> , V <sub>PAD</sub> .. | -0.3V to + 5.5V                   |
| Power Supply Input on V <sub>IN2</sub> , A <sub>VDD</sub> ..                              | -0.3V to + 3.6V                   |
| Digital I/O Input Voltage.....  | -0.3V to + 5.5V                   |
| All Other Pins.....   | -0.3V to + 5.5V                   |
| ESD (all pins).....   | 2 KV HBM / 100V MM <sup>(2)</sup> |

\*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

- Notes: 1. Refer to Power Dissipation Rating section  
 2. According to specifications MIL-883-Method 3015.7 (HBM - Human Body Model) / JESD22 A115 (MM - Machine Model)

## 7. Recommended Operating Conditions

**Table 7-1.** Recommended Operating Conditions

| Parameter                                    | Condition                | Min  | Max | Units |
|--|--------------------------|------|-----|-------|
| Operating Ambient Temperature <sup>(1)</sup> |                          | -40  | 85  | °C    |
| Power Supply Input                           | V <sub>INSYS</sub>       | 2.5  | 5.5 | V     |
| Power Supply Input                           | V <sub>IN{0,1,3,4}</sub> | 2.9  | 5.5 | V     |
| Power Supply Input                           | V <sub>IN2</sub>         | 1.65 | 3.6 | V     |
| Power Supply Input                           | A <sub>VDD</sub>         | 2.7  | 3.6 | V     |
| Power Supply Input                           | V <sub>PAD</sub>         | 1.75 | 5.5 | V     |

- Note: 1. Refer to Power Dissipation Rating section

## 8. Power Dissipation Ratings

**Table 8-1.** Recommended Operating Conditions

| Parameter                         | Condition                                      | Min | Typ | Max | Units  |
|-----------------------------------|--|-----|-----|-----|--------|
| Junction Temperature (Tj)         |  | -40 |     | 125 | °C     |
| R <sub>THJA</sub> <sup>(1)</sup>  | Package thermal junction to ambient resistance |     | 30  | 35  | °C / W |
| Maximum On-chip Power Dissipation | Ambient temperature = 70°C                     |     | 1.8 | 1.6 | W      |
|                                   | Ambient temperature = 85°C                     |     | 1.3 | 1.1 | W      |

- Note: 1. According to specification JESD51-5

## 9. PMU Electrical Characteristics

### 9.1 Current Consumption Versus Modes

**Table 9-1.** Current Consumption Versus Modes

| Symbol        | Parameter                | Comments   | Min | Typ | Max | Units   |
|---------------|--------------------------|--|-----|-----|-----|---------|
| $V_{IN}$      | Operating Supply Voltage | $V_{INSYS}$ , $V_{IN\{0,1,3,4\}}$ present.                                   | 2.9 | 3.6 | 5.5 | V       |
| $I_{DD\_VIN}$ | POWERDOWN Mode.          | All LDOs and DCDC converters OFF. Audio OFF. RTC running.                    | -   | 20  | 40  | $\mu$ A |
|               | RUN Mode.                | All LDOs and DCDC converters running in PWM. Audio OFF. RTC running.         | -   | 7   | 15  | mA      |
|               | STANDBY Mode.            | Default setup: DCDC0 ON in low-power mode. LDO3 ON. All other functions OFF. | -   | 310 | 500 | $\mu$ A |
| $I_{DD\_RTC}$ | All Modes.               | RTC running. Total current entering pin $V_{BACKUP}$                         |     | 1   | 5   | $\mu$ A |

### 9.2 Supply Monitor Thresholds

The following table applies to functional state diagrams of [Figure 11-1 “AT73C246 Power Manager Functional State Diagram”](#) on page 25 and [Figure 11-2 “AT73C246 Start-up and Shutdown State Diagram”](#) on page 26.

**Table 9-2.** Supply Monitor Thresholds

| Symbol           | Parameter                            | Comments | Min   | Typ  | Max   | Units |
|------------------|--------------------------------------|----------|-------|------|-------|-------|
| $V_{IN} > 3.1V$  | PMU Input 3.1V Rising Threshold      |          | 3.070 | 3.1  | 3.130 | V     |
| $V_{IN} < 2.9V$  | PMU Input 2.9V Falling Threshold     |          | 2.870 | 2.9  | 2.930 | V     |
| $V_{IN} > 2.7V$  | PMU Input 2.7V Rising Threshold      |          | 2.70  | 2.75 | 2.85  | V     |
| $V_{IN} < 2.7V$  | PMU Input 2.7V Falling Threshold     |          | 2.60  | 2.65 | 2.70  | V     |
| $V_{BKP} > 1.8V$ | $V_{BACKUP}$ Input Rising Threshold  |          | 1.80  | 1.85 | 1.90  | V     |
| $V_{BKP} < 1.8V$ | $V_{BACKUP}$ Input Falling Threshold |          | 1.70  | 1.75 | 1.80  | V     |



### 9.3 Digital I/Os DC Characteristics

**Table 9-3.**  $V_{PAD}$  Referred Digital I/Os

| Symbol    | Parameter                       | Comments         | Min                   | Typ | Max                   | Units      |
|-----------|---------------------------------|------------------|-----------------------|-----|-----------------------|------------|
| $V_{PAD}$ | Operating Supply Voltage        |                  | 1.75                  | 3.6 | 5.5                   | V          |
| $V_{IL}$  | Input Low-Level Voltage         |                  | -0.3                  | -   | $0.3 \times V_{PAD}$  | V          |
| $V_{IH}$  | Input High-Level Voltage        |                  | $0.7 \times V_{PAD}$  | -   | $V_{PAD} + 0.3$       | V          |
| $V_{OH}$  | Output High-Level Voltage       | $I_O$ max.       | $0.75 \times V_{PAD}$ | -   | -                     | V          |
| $V_{OL}$  | Output Low-Level Voltage        | $I_O$ max        | -                     | -   | $0.25 \times V_{PAD}$ | V          |
| $I_O$     | Output Current                  |                  | -                     | -   | 8                     | mA         |
| $R_P$     | Pull-Up or Pull-Down Resistance | When applicable. | 70                    | 100 | 145                   | k $\Omega$ |

- Notes:
1.  $V_{PAD}$  referred pins ITB, RSTB: open drain outputs. Only  $V_{OL}$  and  $I_O$  parameters are applicable.
  2.  $V_{PAD}$  referred pins WAKEUP1, WAKEUP2, WAKEUP3, MCLK, DAI, TWCK: CMOS inputs. Only  $V_{IH}$  and  $V_{IL}$  parameters are applicable.
  3.  $V_{PAD}$  referred pins MCLK32K, DAO: CMOS outputs. Only  $V_{OL}$ ,  $V_{OH}$  and  $I_O$  parameters are applicable.
  4.  $V_{PAD}$  referred pin TWD: CMOS input and open drain output. Only  $V_{IL}$ ,  $V_{IH}$ ,  $V_{OL}$ ,  $I_O$  parameters are applicable.
  5.  $V_{PAD}$  referred pins LRFS, BCLK: CMOS BiDir. All parameters applicable

**Table 9-4.**  $V_{BACKUP}$  Referred Digital I/Os

| Symbol       | Parameter                       | Comments         | Min                      | Typ | Max                      | Units      |
|--------------|---------------------------------|------------------|--------------------------|-----|--------------------------|------------|
| $V_{BACKUP}$ | Operating Supply Voltage        |                  | 1.75                     | 2.5 | 2.65                     | V          |
| $V_{IL}$     | Input Low-Level Voltage         |                  | -0.3                     | -   | $0.3 \times V_{BACKUP}$  | V          |
| $V_{IH}$     | Input High-Level Voltage        |                  | $0.7 \times V_{BACKUP}$  | -   | $V_{BACKUP} + 0.3$       | V          |
| $V_{OH}$     | Output High-Level Voltage       | $I_O$ max.       | $0.75 \times V_{BACKUP}$ | -   | -                        | V          |
| $V_{OL}$     | Output Low-Level Voltage        | $I_O$ max        | -                        | -   | $0.25 \times V_{BACKUP}$ | V          |
| $I_O$        | Output Current                  |                  | -                        | -   | 8                        | mA         |
| $R_P$        | Pull-Up or Pull-Down resistance | When applicable. | 70                       | 100 | 145                      | k $\Omega$ |

- Note:  $V_{BACKUP}$  referred pins PWREN, HRST, WAKEUP0: CMOS inputs. Only  $V_{IL}$  and  $V_{IH}$  parameters are applicable.

## 9.4 DCDC0 and DCDC1

Unless otherwise specified: External components  $L=2.2\mu\text{H}$ ,  $C_{\text{OUT}}=22\mu\text{F}$  and  $C_{\text{IN}}=10\mu\text{F}$ .  $V_{\text{IN}(0,1)} > V_{\text{DD}(0,1)} + 500\text{mV}$ .  
 $T_j = [-40^\circ\text{C} ; +125^\circ\text{C}]$ .

**Table 9-5.** DCDC0 and DCDC1 Electrical Characteristics

| Symbol                      | Parameter                             | Comments   | Min  | Typ  | Max | Units                    |
|-----------------------------|---------------------------------------|--|------|------|-----|--------------------------|
| $V_{\text{IN}}$             | Operating Supply Voltage              | $V_{\text{IN}0}$ , $V_{\text{IN}1}$ and $V_{\text{INSYS}}$   | 2.9  | 3.6  | 5.5 | V                        |
| $I_{\text{DD}}$             | Supply Current <sup>(1)</sup>         | OFF  | -    | -    | 1   | $\mu\text{A}$            |
|                             |                                       | PFM operation.<br>$V_{\text{DD}0} = 1.85\text{V}$ , $V_{\text{DD}1} = 1.2\text{V}$   | -    | 40   | 80  | $\mu\text{A}$            |
|                             |                                       | PWM operation.<br>$V_{\text{DD}0} = 1.85\text{V}$ , $V_{\text{DD}1} = 1.2\text{V}$   | -    | 3    | 6.5 | mA                       |
| $I_{\text{O}}$              | Output Current                        | PFM operation.   | -    | -    | 50  | mA                       |
|                             |                                       | PWM operation.   | -    | -    | 600 | mA                       |
| $f_{\text{SW}}$             | Switching Frequency                   | PWM operation.   | 1.8  | 2    | 2.2 | MHz                      |
| $V_{\text{DD}0}$            | Default Output Voltage <sup>(2)</sup> | $V_{\text{DD}0}$   | -    | 1.85 | -   | V                        |
| $V_{\text{DD}1}$            |                                       | $V_{\text{DD}1}$   | -    | 1.2  | -   | V                        |
| $V_{\text{DD\_RANGE}}$      | Programmable Output Voltage Range     | PFM or PWM operation.  | 0.8  |      | 3.6 | V                        |
| $V_{\text{DD\_STEP}}$       | Output Voltage Steps                  | PFM or PWM operation.  |      | 50   |     | mV                       |
| $N_{\text{STEP}}$           | Number of Output Steps                | In case of direct output voltage programming. Automatic ramping not active.  |      |      | 4   | step / 100 $\mu\text{s}$ |
| $T_{\text{STEP}}$           | Step time                             | With automatic ramping.  | 260  | 280  | 300 | $\mu\text{s}$            |
| $V_{\text{DD\_ACC}}$        | DC Output Voltage Accuracy            | PFM; $T_j = 25^\circ\text{C}$ ; $I_{\text{O}} = 0\text{ mA}$   | -1.5 |      | 2.5 | %                        |
|                             |                                       | PFM; $T_j = [-40; 125^\circ\text{C}]$ ; $I_{\text{O}} = 0\text{ mA}$   | -2   |      | 3   |                          |
|                             |                                       | PWM; $T_j = 25^\circ\text{C}$ ; $I_{\text{O}} = 0\text{ mA}$   | -1.5 |      | 1.5 |                          |
|                             |                                       | PWM; $T_j = [-40; 125^\circ\text{C}]$ ; $I_{\text{O}} = 0\text{ mA}$   | -2   |      | 2   |                          |
| $V_{\text{DD\_RIPPLE}}$     | Ripple Voltage                        | PWM operation.   |      | 2    |     | mV                       |
| $\Delta V_{\text{DD\_IL}}$  | Static Load Regulation                | PWM operation. $I_{\text{O}}$ ranging from 0 to $I_{\text{O\_MAX}}$  |      | 2    | 5   | mV                       |
|                             | Dynamic Load Regulation               | PWM. $I_{\text{O}}$ : 0 to $I_{\text{O\_MAX}}$ ; 1 $\mu\text{s}$ rise time   |      | -40  |     |                          |
|                             |                                       | PWM. $I_{\text{O}}$ : $I_{\text{O\_MAX}}$ to 0; 1 $\mu\text{s}$ fall time  |      | 40   |     |                          |
| $\Delta V_{\text{DD\_VIN}}$ | Static Line Regulation                | $V_{\text{IN}0}$ and $V_{\text{INSYS}}$ from 2.9 to 5.5V<br>$V_{\text{DD}0} = 1.85\text{V}$ , $V_{\text{DD}1} = 1.2\text{V}$                                     |      |      | 5   | mV                       |
| Eff                         | Efficiency                            | PWM. $I_{\text{O\_MAX}}$ load. $V_{\text{DD}0} = 1.85\text{V}$ .<br>Relative to $V_{\text{IN}0}$ input supply.   |      | 85   |     | %                        |
|                             |                                       | PWM. $I_{\text{O\_MAX}}$ load. $V_{\text{DD}1} = 1.2\text{V}$ .<br>Relative to $V_{\text{IN}1}$ input supply.  |      | 78   |     | %                        |
| $I_{\text{INRUSH}}$         | Inrush Current <sup>(1)</sup>         | Current from $V_{\text{IN}(0,1)}$ and $V_{\text{INSYS}}$ from 0 to 100% $V_{\text{DD}(0,1)}$<br>$V_{\text{DD}0} = 1.85\text{V}$ , $V_{\text{DD}1} = 1.2\text{V}$ |      | 30   | 200 | mA                       |

**Table 9-5.** DCDC0 and DCDC1 Electrical Characteristics

| Symbol              | Parameter                              | Comments   | Min | Typ | Max | Units             |
|---------------------|--|--|-----|-----|-----|-------------------|
| OCP                 | Over-Current Protection                | Output current.  | 1   | 1.4 | 1.8 | A                 |
| T <sub>START</sub>  | Start-up Time                          | From OFF to PWM operation.<br>V <sub>DD(0,1)</sub> rising to 95% of final value. |     |     | 5   | ms                |
| T <sub>PWM</sub>    | PFM to PWM Settling Time               | No output load.  |     | 10  |     | μs                |
| PWRF <sub>DET</sub> | Power Fail Detector Threshold Accuracy | Overload of the programmed threshold by 10mV / 5us min <sup>(3)</sup> .          | -1  | -   | +1  | %·V <sub>DD</sub> |
| C <sub>OUT</sub>    | Total Capacitive Load                  | At V <sub>FB(0,1)</sub> pins.  | 8   |     | 36  | μF                |

- Notes:
1. Current consumption without load. One DCDC converter ON, the other one OFF.
  2. Default output voltage are set during manufacturing. Please contact Atmel for other default settings.
  3. Threshold levels are programmed in register PMU\_RST\_LVL (0x04)

## 9.5 LDO2

Unless otherwise specified: External components  $C_{OUT}=10\mu\text{F}$ ,  $C_{IN}=10\mu\text{F}$ ,  $T_J = [-40^\circ\text{C} ; +125^\circ\text{C}]$ .

**Table 9-6.** LDO2 Electrical Characteristics

| Symbol               | Parameter                              | Comments  | Min  | Typ  | Max  | Units              |
|----------------------|--|---|------|------|------|--------------------|
| $V_{IN}$             | Operating Supply Voltage               | $V_{IN2}$   | 1.65 | 1.8  | 3.6  | V                  |
| $I_{DD}$             | Supply Current <sup>(1)</sup>          | OFF   | -    | -    | 1    | $\mu\text{A}$      |
|                      |  | ON  | -    | -    | 250  | $\mu\text{A}$      |
| $I_O$                | Output Current                         | $V_{IN2} > V_{DD2} + 500\text{mV}$ .  | -    | -    | 300  | mA                 |
| $V_{DD2}$            | Default Output Voltage <sup>(2)</sup>  |   | -    | 1    | -    | V                  |
| $V_{DD\_RANGE}$      | Programmable Output Voltage Range      |   | 0.8  |      | 1.35 | V                  |
| $V_{DD\_STEP}$       | Output Voltage Steps                   |   |      | 50   |      | mV                 |
| $T_{STEP}$           | Step time                              | With automatic ramping.   | 570  | 600  | 630  | $\mu\text{s}$      |
| $V_{DD\_ACC}$        | DC Output Voltage Accuracy             | $V_{IN2} > V_{DD2} + 500\text{mV}$<br>$T_J = 25^\circ\text{C}$ ; $I_O = 0\text{ mA}$                        | -1   |      | 1    | %                  |
|                      |  | $V_{IN2} > V_{DD2} + 500\text{mV}$<br>$T_J = [-40^\circ\text{C} ; 125^\circ\text{C}]$ ; $I_O = 0\text{ mA}$ | -1.5 |      | 1.5  |                    |
| $\Delta V_{DD\_IL}$  | Static Load Regulation                 | $V_{IN2} > V_{DD2} + 500\text{mV}$<br>$I_O$ ranging from 0 to $I_{OMAX}$                                    |      | 0.05 | 1    | $\% \cdot V_{DD2}$ |
|                      | Dynamic Load Regulation                | $V_{IN2} > V_{DD2} + 500\text{mV}$<br>$I_O$ : 0 to $I_{OMAX}$ ; 1 $\mu\text{s}$ rise time                   |      | -50  |      | mV                 |
|                      |  | $V_{IN2} > V_{DD2} + 500\text{mV}$<br>$I_O$ : $I_{OMAX}$ to 0 ; 1 $\mu\text{s}$ fall time                   |      | 50   |      |                    |
| $\Delta V_{DD\_VIN}$ | Static Line Regulation                 | $I_O = 0\text{ mA}$<br>$V_{IN2}$ from 1.65 to 3.6V  |      |      | 5    | mV                 |
| $V_{DROPOUT}$        | Drop Out Voltage <sup>(4)</sup>        | $I_O = 200\text{mA}$  |      |      | 300  | mV                 |
|                      |  | $I_O = 300\text{mA}$  |      |      | 450  | mV                 |
| $I_{INRUSH}$         | Inrush Current                         | Current from $V_{IN2}$ from 0 to 95% of final value.  |      | 200  | 500  | mA                 |
| $T_{START}$          | Start-up Time                          | $V_{DD2}$ OFF and rising to 95% of final value. $I_O = 0\text{ mA}$   |      |      | 1    | ms                 |
| $PWRF_{DET}$         | Power Fail Detector Threshold Accuracy | Overload of the programmed threshold by 10mV / 5us min <sup>(3)</sup> .                                     | -1   | -    | +1   | $\% \cdot V_{DD2}$ |

- Notes:
1. Current consumption in  $V_{IN2}$  without load.
  2. Default output voltage are set during manufacturing. Please contact Atmel for other default settings.
  3. Threshold level is programmed in register PMU\_RST\_LVL (0x04)
  4.  $V_{DROPOUT} = V_{IN2} - V_{DD2}$  when  $V_{DD2} = 98\%$  of  $V_{DD2}$  obtained with  $V_{IN2} > V_{DD2} + 500\text{mV}$

## 9.6 LDO3

Unless otherwise specified: External components  $C_{OUT}=10\mu\text{F}$ ,  $C_{IN}=10\mu\text{F}$ ,  $T_J = [-40^\circ\text{C} ; +125^\circ\text{C}]$ .

**Table 9-7.** LDO3 Electrical Characteristics

| Symbol               | Parameter                              | Comments  | Min  | Typ  | Max | Units              |
|----------------------|--|---|------|------|-----|--------------------|
| $V_{IN}$             | Operating Supply Voltage               | $V_{IN3}$   | 2.9  | 3.6  | 5.5 | V                  |
| $I_{DD}$             | Supply Current <sup>(1)</sup>          | OFF   | -    | -    | 1   | $\mu\text{A}$      |
|                      |  | ON  | -    | -    | 350 | $\mu\text{A}$      |
| $I_O$                | Output Current                         | $V_{IN3} > V_{DD3} + 300\text{mV}$ .  | -    | -    | 200 | mA                 |
| $V_{DD3}$            | Default Output Voltage <sup>(2)</sup>  |   | -    | 3.3  | -   | V                  |
| $V_{DD\_RANGE}$      | Programmable Output Voltage Range      |   | 2.7  |      | 3.6 | V                  |
| $V_{DD\_STEP}$       | Output Voltage Steps                   |   |      | 50   |     | mV                 |
| $T_{STEP}$           | Step time                              | With automatic ramping.   | 570  | 600  | 630 | $\mu\text{s}$      |
| $V_{DD\_ACC}$        | DC Output Voltage Accuracy             | $V_{IN3} > V_{DD3} + 300\text{mV}$<br>$T_J = 25^\circ\text{C}$ ; $I_O = 0\text{ mA}$                        | -1   |      | 1   | %                  |
|                      |  | $V_{IN3} > V_{DD3} + 300\text{mV}$<br>$T_J = [-40^\circ\text{C} ; 125^\circ\text{C}]$ ; $I_O = 0\text{ mA}$ | -1.5 |      | 1.5 |                    |
| $\Delta V_{DD\_IL}$  | Static Load Regulation                 | $V_{IN3} > V_{DD3} + 300\text{mV}$<br>$I_O$ ranging from 0 to $I_{OMAX}$                                    |      | 0.05 | 0.5 | $\% \cdot V_{DD3}$ |
|                      | Dynamic Load Regulation                | $V_{IN3} > V_{DD3} + 300\text{mV}$<br>$I_O$ : 0 to $I_{OMAX}$ ; $1\mu\text{s}$ rise time                    |      | -40  |     | mV                 |
|                      |  | $V_{IN3} > V_{DD3} + 300\text{mV}$<br>$I_O$ : $I_{OMAX}$ to 0 ; $1\mu\text{s}$ fall time                    |      | 40   |     |                    |
| $\Delta V_{DD\_VIN}$ | Static Line Regulation                 | $V_{IN3} > V_{DD3} + 300\text{mV}$ . $I_O = 0\text{ mA}$<br>$V_{IN3}$ from 2.9 to 5.5V                      |      |      | 5   | mV                 |
| $V_{DROPOUT}$        | Drop Out Voltage <sup>(4)</sup>        | $I_O = 10\text{mA}$   |      |      | 50  | mV                 |
|                      |  | $I_O = 200\text{mA}$  |      |      | 250 | mV                 |
| PSRR                 | Power Supply Rejection Ratio           | $V_{IN3} > V_{DD3} + 300\text{mV}$<br>$I_O = 1\text{mA}$ . DC to 3kHz.                                      |      | 60   |     | dB                 |
|                      |  | $V_{IN3} > V_{DD3} + 300\text{mV}$<br>$I_O = 10\text{mA}$ . DC to 3kHz.                                     |      | 50   |     |                    |
| $I_{INRUSH}$         | Inrush Current                         | Current from $V_{IN3}$ from 0 to 95% of final value.  |      | 200  | 500 | mA                 |
| $T_{START}$          | Start-up Time                          | $V_{DD3}$ OFF and rising to 95% of final value. $I_O = 0\text{ mA}$   |      |      | 1   | ms                 |
| $PWRF_{DET}$         | Power Fail Detector Threshold Accuracy | Overload of the programmed threshold by $10\text{mV} / 5\mu\text{s min}^{(3)}$ .                            | -1   | -    | +1  | $\% \cdot V_{DD3}$ |

Notes: 1. Current consumption in  $V_{IN3}$  without load.

2. Default output voltage are set during manufacturing. Please contact Atmel for other default settings.

3. Threshold level is programmed in register PMU\_RST\_LVL (0x04)

4.  $V_{DROPOUT} = V_{IN3} - V_{DD3}$  when  $V_{DD3} = 98\%$  of  $V_{DD3}$  obtained with  $V_{IN3} > V_{DD3} + 300\text{mV}$

## 9.7 LDO4

Unless otherwise specified: External components  $C_{OUT}=10\mu\text{F}$ ,  $C_{IN}=10\mu\text{F}$ ,  $T_J = [-40^\circ\text{C} ; +125^\circ\text{C}]$ .

**Table 9-8.** LDO4 Electrical Characteristics

| Symbol               | Parameter                             | Comments   | Min  | Typ  | Max | Units              |
|----------------------|---------------------------------------|--|------|------|-----|--------------------|
| $V_{IN}$             | Operating Supply Voltage              | $V_{IN4}$  | 2.9  | 3.6  | 5.5 | V                  |
| $I_{DD}$             | Supply Current <sup>(1)</sup>         | OFF  | -    | -    | 1   | $\mu\text{A}$      |
|                      |                                       | ON   | -    | -    | 350 | $\mu\text{A}$      |
| $I_O$                | Output Current                        | $V_{IN4} > V_{DD4} + 300\text{mV}$ .   | -    | -    | 200 | mA                 |
| $V_{DD4}$            | Default Output Voltage <sup>(2)</sup> |  | -    | 3.3  | -   | V                  |
| $V_{DD\_RANGE}$      | Programmable Output Voltage Range     |  | 2.7  |      | 3.6 | V                  |
| $V_{DD\_STEP}$       | Output Voltage Steps                  |  |      | 50   |     | mV                 |
| $T_{STEP}$           | Step time                             | With automatic ramping.  | 570  | 600  | 630 | $\mu\text{s}$      |
| $V_{DD\_ACC}$        | DC Output Voltage Accuracy            | $V_{IN4} > V_{DD4} + 300\text{mV}$<br>$T_J = 25^\circ\text{C} ; I_O = 0 \text{ mA}$                        | -1   |      | 1   | %                  |
|                      |                                       | $V_{IN4} > V_{DD4} + 300\text{mV}$<br>$T_J = [-40^\circ\text{C} ; 125^\circ\text{C}] ; I_O = 0 \text{ mA}$ | -1.5 |      | 1.5 |                    |
| $\Delta V_{DD\_IL}$  | Static Load Regulation                | $V_{IN4} > V_{DD4} + 300\text{mV}$<br>$I_O$ ranging from 0 to $I_{OMAX}$                                   |      | 0.05 | 0.5 | $\% \cdot V_{DD4}$ |
|                      | Dynamic Load Regulation               | $V_{IN4} > V_{DD4} + 300\text{mV}$<br>$I_O$ : 0 to $I_{OMAX}$ ; 1 $\mu\text{s}$ rise time                  |      | -40  |     | mV                 |
|                      |                                       | $V_{IN4} > V_{DD4} + 300\text{mV}$<br>$I_O$ : $I_{OMAX}$ to 0 ; 1 $\mu\text{s}$ fall time                  |      | 40   |     |                    |
| $\Delta V_{DD\_VIN}$ | Static Line Regulation                | $V_{IN4} > V_{DD4} + 300\text{mV}$ . $I_O = 0 \text{ mA}$<br>$V_{IN4}$ from 2.9 to 5.5V                    |      |      | 5   | mV                 |
| $V_{DROPOUT}$        | Drop Out Voltage <sup>(3)</sup>       | $I_O = 10\text{mA}$  |      |      | 50  | mV                 |
|                      |                                       | $I_O = 200\text{mA}$   |      |      | 250 | mV                 |
| PSRR                 | Power Supply Rejection Ratio          | $V_{IN4} > V_{DD4} + 300\text{mV}$<br>$I_O = 1\text{mA}$ . DC to 3kHz.                                     |      | 60   |     | dB                 |
|                      |                                       | $V_{IN4} > V_{DD4} + 300\text{mV}$<br>$I_O = 10\text{mA}$ . DC to 3kHz.                                    |      | 50   |     |                    |
| $I_{INRUSH}$         | Inrush Current                        | Current from $V_{IN4}$ from 0 to 95% of final value.   |      | 200  | 500 | mA                 |
| $T_{START}$          | Start-up Time                         | $V_{DD4}$ OFF and rising to 95% of final value. $I_O = 0 \text{ mA}$                                       |      |      | 1   | ms                 |

- Notes:
1. Current consumption in  $V_{IN4}$  without load.
  2. Default output voltage are set during manufacturing. Please contact Atmel for other default settings.
  3.  $V_{DROPOUT} = V_{IN4} - V_{DD4}$  when  $V_{DD4} = 98\%$  of  $V_{DD4}$  obtained with  $V_{IN4} > V_{DD4} + 300\text{mV}$

## 9.8 LDO5

Unless otherwise specified: External components  $C_{OUT}=2.2\mu F$ ,  $C_{IN}=10\mu F$ ,  $T_J = [-40^{\circ}C ; +125^{\circ}C]$ .

**Table 9-9.** LDO5 Electrical Characteristics

| Symbol              | Parameter                     | Comments  | Min  | Typ | Max  | Units   |
|---------------------|-------------------------------|---|------|-----|------|---------|
| $V_{IN}$            | Operating Supply Voltage      | $V_{INSYS}$   | 2.7  | 3.6 | 5.5  | V       |
| $I_{DD}$            | Supply Current <sup>(1)</sup> | OFF   | -    | -   | 1    | $\mu A$ |
|                     |                               | ON  | -    | -   | 7    | $\mu A$ |
| $I_O$               | Output Current                |   | -    | -   | 10   | mA      |
| $V_{BACKUP}$        | Output Voltage Accuracy       |   | 2.42 | 2.5 | 2.58 | V       |
| $\Delta_{VDD\_VIN}$ | Static Line Regulation        | $V_{INSYS}$ from 2.7 to 5.5V  |      | 3   | 10   | mV      |
| $\Delta_{VDD\_VIN}$ | Static Line Regulation        | $V_{INSYS} = 3.6V$ , $I_O$ from 0 to $I_{OMAX}$                           |      | 10  | 15   | mV      |
| $I_{INRUSH}$        | Inrush Current                | Current from $V_{INSYS}$ from 0 to $T_{START(MAX)}$ ; $V_{BACKUP} = 2.5V$ |      | 180 | 350  | mA      |
| $T_{START}$         | Start-up Time                 | $V_{BACKUP}$ OFF and rising to 95% of final value.                        |      |     | 1    | ms      |

Note: 1. Current consumption in  $V_{INSYS}$  without plugged backup battery

## 9.9 Measurement Bridge and 10-bit ADC

**Table 9-10.** Measurement Bridge and 10-bit ADC Electrical Characteristics

| Symbol         | Parameter                               | Comments                                     | Min  | Typ  | Max         | Units      |
|----------------|---|--|------|------|-------------|------------|
| $V_{IN}$       | Operating Supply Voltage <sup>(1)</sup> | $V_{INSYS}$                                  | 2.9  | 3.6  | 5.5         | V          |
| $I_{DD}$       | Supply Current                          | OFF  | -    | -    | 1           | $\mu$ A    |
|                |   | ON   | -    | -    | 2           | mA         |
| $V_{REF}$      | Reference Voltage                       | Internally connected to VDDC pin.            | 1.75 | 1.8  | 1.85        | V          |
| INL            | Integral Non Linearity                  | End Point Method                             | -2   | -    | +2          | LSB        |
| DNL            | Differential Non Linearity              | End Point Method                             | -1   | -    | +1          | LSB        |
| Offset         | Offset Error                            |  | -2   |      | +2          | LSB        |
| GAIN           | Gain Error                              |  | -2   |      | +2          | LSB        |
| $F_S$          | Sampling Rate                           |  |      | 300  |             | kS/s       |
| $T_{ACQ}$      | Track and Hold Acquisition Time         |  | 500  |      |             | ns         |
| $V_{MEAS}$     | Measured Input Voltage Range            | External inputs ANA{0,1,2,3}                 | 0.4  |      | $V_{INSYS}$ | V          |
|                |   | $V_{DD\{0,1,2,3,4\}}$ inputs                 | 0.4  |      | 4           | V          |
|                |   | $V_{INSYS}$ input                            | 0.4  |      | 5.5         | V          |
| $ATT_{MEAS}$   | Measured Input Scaling Factor           | External inputs ANA{0,1,2,3}                 | -1%  | 0.25 | +1%         | V/V        |
|                |   | $V_{DD\{0,1,2,3,4,5\}}$ inputs               | -1%  | 0.4  | +1%         | V/V        |
|                |   | $V_{INSYS}$ input                            | -1%  | 0.25 | +1%         | V/V        |
| $R_{IN\_NOM}$  | ANA{0,1,2,3} Input resistance           | $T_j = 25C$                                  | 96   | 120  | 144         | k $\Omega$ |
| $R_{IN\_TEMP}$ | $R_{IN}$ deviation with temperature     | $T_j$ [-40 ; +25]. Relative to $R_{IN\_NOM}$ |      |      | + 20        | %          |
|                |   | $T_j$ [25 ; 125]. Relative to $R_{IN\_NOM}$  | -16  |      |             |            |
| $C_{IN}$       | ANA{0,1,2,3} Input capacitance          |  |      |      | 15          | pF         |

- Notes: 1. The 10-bit ADC is supplied from the regulated  $V_{DDC}$  voltage (1.8V) which is generated from  $V_{INSYS}$ .  
 2. Please refer to Atmel Data Converter Terminology literature



## 9.10 RTC Crystal Oscillator

**Table 9-11.** RTC Crystal Oscillator Electrical Characteristics

| Symbol             | Parameter                       | Comments              | Min  | Typ    | Max  | Units    |
|--------------------|---------------------------------|-----------------------|------|--------|------|----------|
| V <sub>IN</sub>    | Operating Supply Voltage        | V <sub>BACKUP</sub>   | 1.75 | 2.5    | 2.65 | V        |
| Freq               | Frequency                       | with crystal          | -    | 32.768 | -    | kHz      |
| Duty               | Duty Cycle                      |                       | 40   | 50     | 60   | %        |
| I <sub>DD</sub>    | Supply Current <sup>(1)</sup>   | OFF                   | -    | -      | 5    | nA       |
|                    |                                 | ON                    | -    | -      | 1.5  | μA       |
| T <sub>ON</sub>    | Startup Time                    | C <sub>L</sub> = 12pF | -    | 1000   | 1500 | ms       |
| V <sub>XIN</sub>   | Level Sinus Wave on XIN         |                       |      | 250    | 300  | mVpp     |
| V <sub>XOUT</sub>  | Vpp On XOUT                     |                       |      | 300    |      | mVpp     |
| R <sub>F</sub>     | Internal Resistor               | between xin and xout  |      | 10     |      | MΩ       |
| Drift              | Accuracy                        | @25°C, +/- 20ppm      |      |        | 1.5  | mn/month |
| Esr                | Equivalent Series Resistance Rs | Crystal @ 32.768kHz   |      | 50     | 100  | kΩ       |
| C <sub>M</sub>     | Motional Capacitance            | Crystal @ 32.768kHz   | 0.6  |        | 3    | fF       |
| C <sub>SHUNT</sub> | Shunt Capacitance               | Crystal @ 32.768kHz   | 0.6  |        | 2    | pF       |
| C <sub>LOAD</sub>  | Load Capacitance                | Crystal @ 32.768kHz   | 6    |        | 12.5 | pF       |

Note: 1. Current consumption in V<sub>BACKUP</sub> with crystal. In case of crystal not present on-board, back-up batteries or supercapacitors, must be avoided.

## 9.11 Die Temperature Sensor

**Table 9-12.** Die Temperature Sensor Electrical Characteristics

| Symbol                | Parameter                | Comments | Min | Typ | Max | Units |
|-----------------------|--------------------------|----------|-----|-----|-----|-------|
| T <sub>SHUTDOWN</sub> | 130°C Shutdown Threshold |          | 135 | 145 | 155 | °C    |
| T <sub>RESTART</sub>  | 110°C Restart Threshold  |          | 105 | 115 | 125 | °C    |

## 10. Audio Codec Electrical Characteristics

Unless otherwise specified: AVDD = 3.3V, T<sub>A</sub> = 25C, MCLK = 12.288MHz, F<sub>S</sub> = 48kHz. Master mode and 24-bit operation on I<sup>2</sup>S port. All gains set to 0dB, audio effects are off. Noise measurements are made in the [20Hz-20kHz] band using the A-Weighting filter. Distortion measurements are made from the 2<sup>nd</sup> to the 5<sup>th</sup> harmonic products of a 997Hz input sinewave. Input sources have an internal impedance of 50 Ohms. Audio Path without mixing capability.

**Table 10-1.** Audio Codec Bias

| Symbol               | Parameter   | Comments                     | Min | Typ      | Max | Units |
|----------------------|---|------------------------------|-----|----------|-----|-------|
| AVDD                 | Operating Supply Voltage                              |                              | 2.7 | 3.3      | 3.6 | V     |
| I <sub>DD</sub>      | Supply Current  | OFF                          |     |          | 20  | μA    |
|                      |   | STANDBY                      |     |          | 1   | mA    |
| V <sub>MID</sub>     | Mid-Supply Reference Voltage                          |                              | -1% | AVDD / 2 | +1% | V     |
| T <sub>MID_ON</sub>  | Time to charge V <sub>MID</sub> capacitor             | From 0 to 95% of final value |     |          | 350 | ms/μF |
| T <sub>MID_OFF</sub> | Time to discharge V <sub>MID</sub> capacitor          | From 0 to 95% of final value |     |          | 700 | ms/μF |
| V <sub>MICBIAS</sub> | Microphone Bias Reference Voltage                     | No load.                     |     | AVDD     |     | V     |
| R <sub>MICBIAS</sub> | Microphone Bias Reference Voltage Internal Resistance |                              | 1.5 | 1.9      | 2.3 | kΩ    |

**Table 10-2.** Line Record Path: Line or Auxiliary Input to ADC Output

| Symbol            | Parameter                                      | Comments                                    | Min | Typ        | Max | Units            |
|-------------------|--|---|-----|------------|-----|------------------|
| V <sub>FS</sub>   | Full Scale Input Voltage <sup>(1)</sup>        | Corresponds to 0dBFS digital output signal. |     | AVDD / 3.3 |     | V <sub>RMS</sub> |
| SNR               | Signal-to-Noise Ratio <sup>(2)</sup>           | AVDD = 3.3V                                 | 85  | 96         | -   | dB               |
|                   |  | AVDD = 2.7V                                 | 82  | 93         | -   | dB               |
| DR                | Dynamic Range <sup>(3)</sup>                   | AVDD = 3.3V                                 | 85  | 96         | -   | dB               |
|                   |  | AVDD = 2.7V                                 | 82  | 93         | -   | dB               |
| THD               | Total Harmonic Distortion                      | -1dBFS digital output                       | -   | -80        | -74 | dB               |
| XTALK             | Left / Right Channel separation <sup>(5)</sup> |   | 80  | 90         | -   | dB               |
| G <sub>LINE</sub> | Programmable Gain Range                        |   | -34 | 0          | 12  | dB               |
|                   | Gain Step Size                                 |   | -   | 1          | -   | dB               |
|                   | Mute Attenuation <sup>(6)</sup>                |   | 80  | -          | -   | dB               |
| R <sub>IN</sub>   | Input Resistance                               |   | 5.9 | 7          | 8.1 | kΩ               |
| C <sub>IN</sub>   | Input Capacitance                              |   | -   | -          | 10  | pF               |

**Table 10-3.** Microphone Record Path: Microphone Input to ADC Output

| Symbol          | Parameter                               | Comments                                    | Min | Typ        | Max | Units            |
|-----------------|---|---|-----|------------|-----|------------------|
| V <sub>FS</sub> | Full Scale Input Voltage <sup>(1)</sup> | Corresponds to 0dBFS digital output signal. |     | AVDD / 3.3 |     | V <sub>RMS</sub> |
| SNR             | Signal-to-Noise Ratio <sup>(2)</sup>    | AVDD = 3.3V                                 | 85  | 96         | -   | dB               |
|                 |   | AVDD = 2.7V                                 | 82  | 93         | -   | dB               |

**Table 10-3.** Microphone Record Path: Microphone Input to ADC Output

| Symbol            | Parameter                                      | Comments              | Min | Typ | Max  | Units |
|-------------------|--|-----------------------|-----|-----|------|-------|
| DR                | Dynamic Range <sup>(3)</sup>                   | AVDD = 3.3V           | 85  | 96  | -    | dB    |
|                   |  | AVDD = 2.7V           | 82  | 93  | -    | dB    |
| THD               | Total Harmonic Distortion                      | -1dBFS digital output | -   | -84 | -74  | dB    |
| XTALK             | Left / Right Channel separation <sup>(5)</sup> |                       | 80  | 90  | -    | dB    |
| G <sub>LINE</sub> | Programmable Gain Range                        |                       | 0   | -   | 46   | dB    |
|                   | Gain Step Size                                 |                       | -   | 1   | -    | dB    |
|                   | Mute Attenuation <sup>(6)</sup>                |                       | 80  | -   | -    | dB    |
| R <sub>IN</sub>   | Input Resistance                               | 0dB gain              | 8.4 | 12  | 15.6 | kΩ    |
| C <sub>IN</sub>   | Input Capacitance                              |                       | -   | -   | 10   | pF    |

**Table 10-4.** Playback Path: DAC Input to Headphone Output

| Symbol          | Parameter                                      | Comments                     | Min | Typ        | Max | Units            |
|-----------------|--|------------------------------|-----|------------|-----|------------------|
| V <sub>FS</sub> | Full Scale Output Voltage <sup>(1)</sup>       | 0dBFS digital input signal.  |     | AVDD / 3.3 |     | V <sub>RMS</sub> |
| SNR             | Signal-to-Noise Ratio <sup>(2)</sup>           | AVDD = 3.3V                  | 92  | 97         | -   | dB               |
|                 |  | AVDD = 2.7V                  | 89  | 94         | -   | dB               |
| DR              | Dynamic Range <sup>(3)</sup>                   | AVDD = 3.3V                  | 92  | 97         | -   | dB               |
|                 |  | AVDD = 2.7V                  | 89  | 94         | -   | dB               |
| THD             | Total Harmonic Distortion                      | 0dBFS input - 10kΩ load      | -   | -88        | -80 | dB               |
|                 |  | 20mW output - 32Ω load       | -   | -65        | -60 | dB               |
|                 |  | 20mW output - 16Ω load       | -   | -60        | -55 | dB               |
| P <sub>O</sub>  | Output Power                                   | 32Ω load - THD < -40dB or 1% |     | 30         |     | mW               |
|                 |  | 16Ω load - THD < -40dB or 1% |     | 50         |     | mW               |
| XTALK           | Left / Right Channel Separation <sup>(5)</sup> | 10kΩ AC coupled load         |     | 90         |     | dB               |
|                 |  | 16Ω DC coupled load          |     | 60         |     | dB               |
| G <sub>HS</sub> | Programmable Gain Range                        |                              | -77 | -          | +6  | dB               |
|                 | Gain Step Size                                 |                              | -   | 1          | -   | dB               |
|                 | Mute Attenuation <sup>(6)</sup>                |                              | 80  | -          | -   | dB               |

**Table 10-5.** Analog Bypass Path: Line / Auxiliary Input to Headphone Output

| Symbol          | Parameter                                | Comments    | Min | Typ        | Max | Units            |
|-----------------|--|-------------|-----|------------|-----|------------------|
| V <sub>FS</sub> | Full Scale Output Voltage <sup>(1)</sup> |             |     | AVDD / 3.3 |     | V <sub>RMS</sub> |
| SNR             | Signal-to-Noise Ratio <sup>(2)</sup>     | AVDD = 3.3V | 92  | 97         | -   | dB               |
|                 |  | AVDD = 2.7V | 89  | 94         | -   | dB               |
| DR              | Dynamic Range <sup>(3)</sup>             | AVDD = 3.3V | 92  | 97         | -   | dB               |
|                 |  | AVDD = 2.7V | 89  | 94         | -   | dB               |

**Table 10-5. Analog Bypass Path: Line / Auxiliary Input to Headphone Output**

| Symbol           | Parameter                                      | Comments                             | Min | Typ | Max | Units |
|------------------|--|--------------------------------------|-----|-----|-----|-------|
| THD              | Total Harmonic Distortion                      | 0dBFS input - 10k $\Omega$ load      | -   | -88 | -80 | dB    |
|                  |  | 20mW output - 32 $\Omega$ load       | -   | -65 | -60 | dB    |
|                  |  | 20mW output - 16 $\Omega$ load       | -   | -60 | -55 | dB    |
| P <sub>O</sub>   | Output Power                                   | 32 $\Omega$ load - THD < -40dB or 1% |     | 30  |     | mW    |
|                  |  | 16 $\Omega$ load - THD < -40dB or 1% |     | 50  |     | mW    |
| XTALK            | Left / Right Channel Separation <sup>(5)</sup> | 10k $\Omega$ AC coupled load         |     | 90  |     | dB    |
|                  |  | 16 $\Omega$ DC coupled load          |     | 60  |     | dB    |
| G <sub>BYP</sub> | Bypass Gain                                    |                                      | -1  | 0   | +1  | dB    |
|                  | Mute Attenuation <sup>(6)</sup>                |                                      | 80  | -   | -   | dB    |

**Table 10-6. Analog Sidetone Path: Microphone Input to Headphone Output**

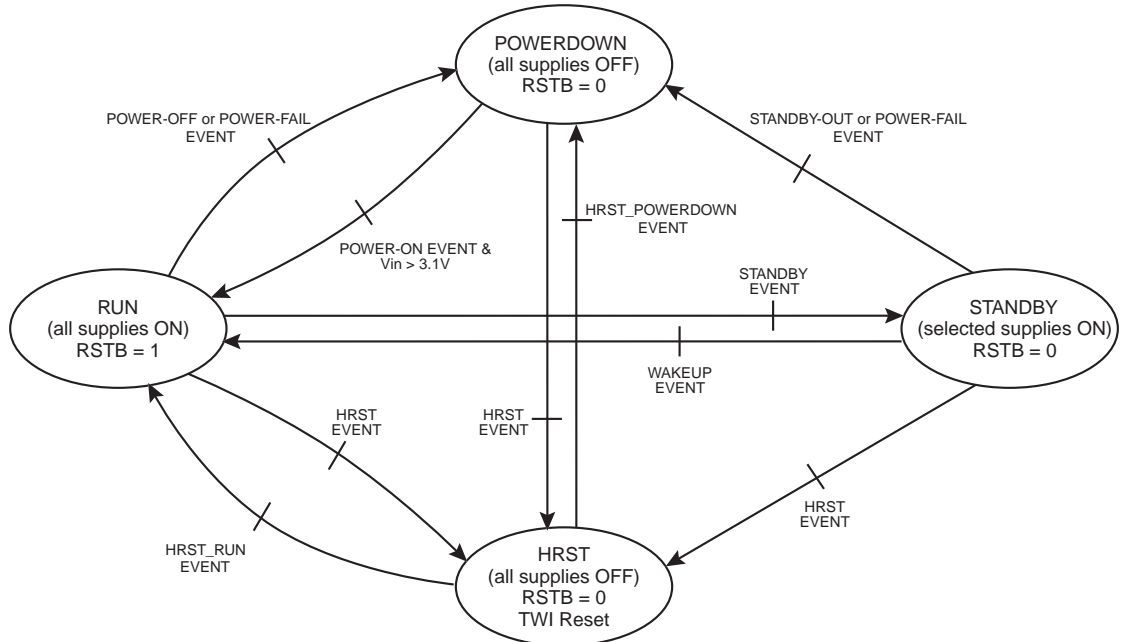
| Symbol                | Parameter                                      | Comments                             | Min | Typ        | Max | Units            |
|-----------------------|--|--------------------------------------|-----|------------|-----|------------------|
| V <sub>FS</sub>       | Full Scale Output Voltage <sup>(1)</sup>       |                                      |     | AVDD / 3.3 |     | V <sub>RMS</sub> |
| SNR                   | Signal-to-Noise Ratio <sup>(2)</sup>           | AVDD = 3.3V                          | 92  | 97         | -   | dB               |
|                       |  | AVDD = 2.7V                          | 89  | 94         | -   | dB               |
| DR                    | Dynamic Range <sup>(3)</sup>                   | AVDD = 3.3V                          | 92  | 97         | -   | dB               |
|                       |  | AVDD = 2.7V                          | 89  | 94         | -   | dB               |
| THD                   | Total Harmonic Distortion                      | 0dBFS input - 10k $\Omega$ load      | -   | -88        | -80 | dB               |
|                       |  | 20mW output - 32 $\Omega$ load       | -   | -65        | -60 | dB               |
|                       |  | 20mW output - 16 $\Omega$ load       | -   | -60        | -55 | dB               |
| P <sub>O</sub>        | Output Power                                   | 32 $\Omega$ load - THD < -40dB or 1% |     | 30         |     | mW               |
|                       |  | 16 $\Omega$ load - THD < -40dB or 1% |     | 50         |     | mW               |
| XTALK                 | Left / Right Channel Separation <sup>(5)</sup> | 10k $\Omega$ AC coupled load         |     | 90         |     | dB               |
|                       |  | 16 $\Omega$ DC coupled load          |     | 60         |     | dB               |
| G <sub>SIDETONE</sub> | Programmable Gain Range                        |                                      | -30 | -          | 0   | dB               |
|                       | Gain Steps                                     |                                      | 2.5 | 3          | 3.5 | dB               |
|                       | Mute Attenuation <sup>(6)</sup>                |                                      | 80  | -          | -   | dB               |

- Notes:
1. Full Scale: A linear extrapolation to 0dBFS of the measured level at -10dBFS.
  2. Signal-to-Noise Ratio: The ratio of the RMS value of a 997Hz full scale sine wave to the RMS value of output noise with no signal applied. Device is not muted.
  3. Dynamic Range: According to AES17-1991 (Audio Engineering Society) and EIAJ CP-307 (Electronic Industries Association of Japan), an extrapolation to 0dBFS input signal of the THD+N ratio measurement at -60dBFS. As an example, if THD+N @ -60dBFS = -36dB, then DR = 96dB.
  4. Total Harmonic Distortion + Noise Ratio: The ratio of the RMS sum of the noise and the distortion components to the RMS value of the signal.
  5. XTALK: Attenuation measurement from one channel to the other one. Measurement is performed by stimulated one channel with a 997Hz / -10dBFS sinewave and leaving the other channel unstimulated.
  6. Mute Attenuation: Attenuation measurement of a -10dBFS / 997Hz input signal when concerned gain is set to mute.

# 11. PMU Functional Description

## 11.1 Power Manager State Diagram

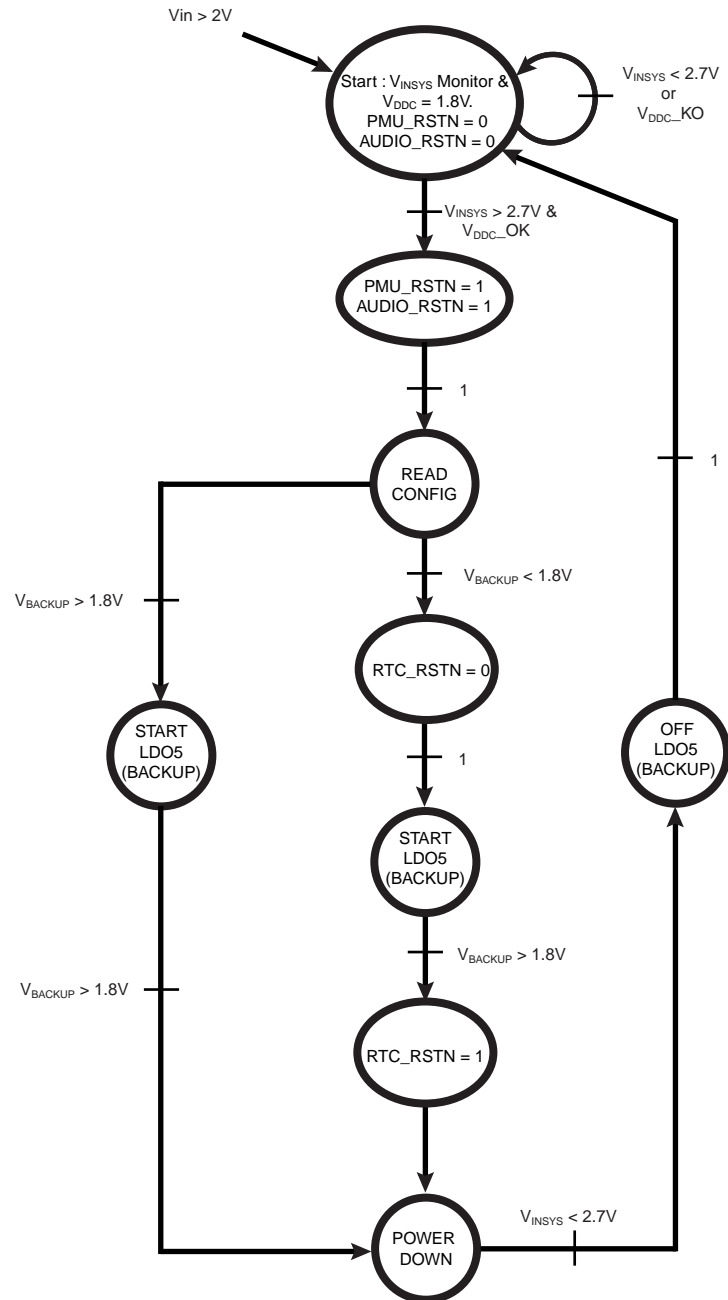
Figure 11-1. AT73C246 Power Manager Functional State Diagram



AT73C246 is placed in POWERDOWN state at VINSYS rising following the PMU startup state diagram described in [Figure 11-2 on page 26](#). From this POWERDOWN state, normal CPU supplies startup is achieved through validation of one of the POWER-ON events. From this state, the PMU may be placed in STANDBY state (e.g.: during CPU sleep periods) upon software request (STANDBY event). PMU wake-up is achieved if one of the WAKEUP events is detected. The PMU returns to the POWERDOWN state as soon as a POWER-OFF event is detected. A special HRST (Hard-Reset) state is provided to ensure complete stop and restart of the CPU supplies in case of a software crash. Moreover, die temperature and  $VDD_{\{0,1,2,3\}}$  supplies are supervised and may generate a POWER-FAIL event in case of out-of-specification detection.

## 11.2 PMU Startup and Shutdown State Diagram

Figure 11-2. AT73C246 Start-up and Shutdown State Diagram



The start-up of the AT73C246 follows the flow diagram of [Figure 11-2](#) and aims at placing the power manager in the POWERDOWN state.

When  $V_{INSYS}$  rises above 2V:

- An internal  $V_{INSYS}$  monitor starts and holds the internal PMU\_RSTN and AUDIO\_RSTN signals to 0, thus forcing a complete reset of AT73C246. The PMU digital core supply voltage

( $V_{DDC} = 1.8V$ ) is started. During this PMU reset, the 'LED' pin is driven to VINSYS (LED is OFF).

- When  $V_{DDC}$  is ready and  $V_{INSYS} > 2.7V$ , the internal reset signals previously mentioned are released, thus enabling the PMU digital core functions.
- Before starting the LDO5 (RTC supply),  $V_{BACKUP}$  voltage is monitored and if it is lower than 1.8V, the RTC function is resetted. In case of  $V_{BACKUP} > 1.8V$ , no reset is issued on the RTC function.
- At this step, the power manager is placed in POWERDOWN state.

## 11.3 Power Manager Conditional Transitions

### 11.3.1 POWER-ON EVENTS

POWER-ON EVENTS are validated if all these listed conditions are true:

- $V_{INSYS} > 3.1V$
- AT73C246 internal junction temperature  $T_j < 110^\circ C$
- PWREN pin is high for more than 100ms (see [Table 11-1 on page 28](#)).

Note: PWREN pin, with internal 100k pull-down resistor, is active high ( $V_{BACKUP}$  level). It is possible to hard wire the PWREN pin to  $V_{BACKUP}$  to always activate RUN state when  $V_{INSYS} > 3.1V$ . Consequently, using the software POWER-OFF EVENT (described in [Section 11.3.2](#)) will lead to going back to the RUN state just after the POWERDOWN STATE.

### 11.3.2 POWER-OFF EVENTS

POWER-OFF EVENTS are validated if one of these listed conditions is true:

- $V_{INSYS} < 2.9V$ .
- PWREN pin goes from low to high state and high state is held for more than 5s (see [Table 11-1 on page 28](#)).
- Software request: bit 0 (OFF) of register 0x00 (PMU\_MODES) is written to 1.

### 11.3.3 POWER-FAIL EVENTS

POWER-FAIL EVENTS are validated if one of these listed conditions is true:

- AT73C246 internal junction temperature  $T_j > 130^\circ C$
- Any internal power fail detection signal coming from any CPU power supply ( $V_{DD0}$ ,  $V_{DD1}$ ,  $V_{DD2}$ ,  $V_{DD3}$ ) goes from low to high level.

Note: In case of PWREN pin hard wired high ( $V_{BACKUP}$  level), the POWER-FAIL EVENTS will lead to the POWERDOWN state without possibility to go to the RUN state. The power manager will be able to reach the RUN state only after an HRST event. This prevents the power manager from oscillating between RUN and POWERDOWN states in case of permanent failure on CPU supplies.

### 11.3.4 STANDBY EVENT

STANDBY EVENT is validated if the following condition is true:

- Software request: bit 1 (STANDBY) of register 0x00 (PMU\_MODES) is written to 1.

### 11.3.5 STANDBY-OUT EVENT

STANDBY-OUT EVENT is validated if the following condition is true:

- $V_{INSYS} < 2.9V$ .

### 11.3.6 WAKEUP EVENTS

WAKEUP EVENTS are validated if one of the listed condition is true:

- WAKEUP0 pin goes from low to high state and WAKEUP0 bit is set to '1' (see [Table 11-1](#)) in register 0x01 (PMU\_WAKEUP\_EVENTS).
- WAKEUP1 pin goes from low to high state and WAKEUP1 bit is set to '1' (see [Table 11-1](#)) in register 0x01 (PMU\_WAKEUP\_EVENTS).
- WAKEUP2 pin goes from low to high state and WAKEUP2 bit is set to '1' (see [Table 11-1](#)) in register 0x01 (PMU\_WAKEUP\_EVENTS).
- WAKEUP3 pin goes from low to high state and WAKEUP3 bit is set to '1' (see [Table 11-1](#)) in register 0x01 (PMU\_WAKEUP\_EVENTS).
- PWREN pin goes from low to high state and high state is held for more than 10ms (see [Table 11-1](#)) and PWREN bit is set to '1' in register 0x01 (PMU\_WAKEUP\_EVENTS).
- An RTC alarm occurs and RTC bit is set to '1' in register 0x01 (PMU\_WAKEUP\_EVENTS).

- Notes:
1. WAKEUP0 and PWREN pins must be driven with  $V_{\text{BACKUP}}$  level, WAKEUP{1,2,3} pins must be driven with  $V_{\text{PAD}}$  level.
  2. If any WAKEUP EVENT is triggered while AT73C246 is going from RUN to STANDBY state, STANDBY state is then first reached before WAKEUP EVENT is taken into account.

### 11.3.7 HRST EVENT

HRST EVENT is validated if the following condition is true:

- HRST pin goes from low to high state and high state is held for more than 1s (see [Table 11-1](#)).

### 11.3.8 HRST RUN EVENTS

HRST RUN EVENTS are validated if all these listed conditions are true:

- HRST pin is at low level for more than 10ms (see [Table 11-1](#)).
- $V_{\text{INSYS}} > 3.1\text{V}$
- AT73C246 internal junction temperature  $T_j < 110^\circ\text{C}$

Note: In case of  $110^\circ\text{C} < T_j < 130^\circ\text{C}$ , HRST state is maintained. The self cooling down of the die will lead to  $T_j < 110^\circ\text{C}$ , thus exit of HRST state.

### 11.3.9 HRST POWERDOWN EVENTS

HRST POWERDOWN EVENTS are validated if all of these listed conditions are true:

- HRST pin is at low level for more than 10ms.
- $V_{\text{INSYS}} < 3.1\text{V}$  or AT73C246 internal junction temperature  $T_j > 130^\circ\text{C}$

**Table 11-1.** EVENTS Timing Table

| Pin   | Parameter  | Comments                         | Min  | Typ | Max  | Units |
|-------|--|----------------------------------|------|-----|------|-------|
| PWREN | Pin at $V_{\text{BACKUP}}$ Level. Debouncing Time. | Pin used as POWER-ON event       | 95   | 100 | 105  | ms    |
| PWREN | Pin at $V_{\text{BACKUP}}$ Level. Debouncing Time. | Pin used as POWER-OFF event      | 4.75 | 5   | 5.25 | sec   |
| PWREN | Pin at $V_{\text{BACKUP}}$ Level. Debouncing Time. | Pin used as WAKEUP event         | 9.5  | 10  | 10.5 | ms    |
| HRST  | Pin at $V_{\text{BACKUP}}$ Level. Debouncing Time. | Pin used as HRST event           | 0.95 | 1   | 1.05 | sec   |
| HRST  | Pin at GND Level. Debouncing Time.                 | Pin used as HRST RUN event       | 9.5  | 10  | 10.5 | ms    |
|       |  | Pin used as HRST POWERDOWN event |      |     |      |       |



**Table 11-1.** EVENTS Timing Table

| Pin     | Parameter   | Comments                 | Min | Typ | Max | Units |
|---------|---|--------------------------|-----|-----|-----|-------|
| WAKEUP0 | Pin pulsed to $V_{\text{BACKUP}}$ Level. Pulse Width. | Pin used as WAKEUP event | 5   | -   | -   | ns    |
| WAKEUP1 | Pin pulsed to $V_{\text{PAD}}$ Level. Pulse Width.    | Pin used as WAKEUP event | 5   | -   | -   | ns    |
| WAKEUP2 | Pin pulsed to $V_{\text{PAD}}$ Level. Pulse Width.    | Pin used as WAKEUP event | 5   | -   | -   | ns    |
| WAKEUP3 | Pin pulsed to $V_{\text{PAD}}$ Level. Pulse Width.    | Pin used as WAKEUP event | 5   | -   | -   | ns    |

## 11.4 Power Manager State Description

AT73C246 ICs are available with 2 factory programmed power sequences. The following timing diagrams refer to “SEQUENCE A” and “SEQUENCE B” programmed ICs as defined in section 17. “Ordering Information” on page 154. See also the structure of register “VERSION (0x7F)”.

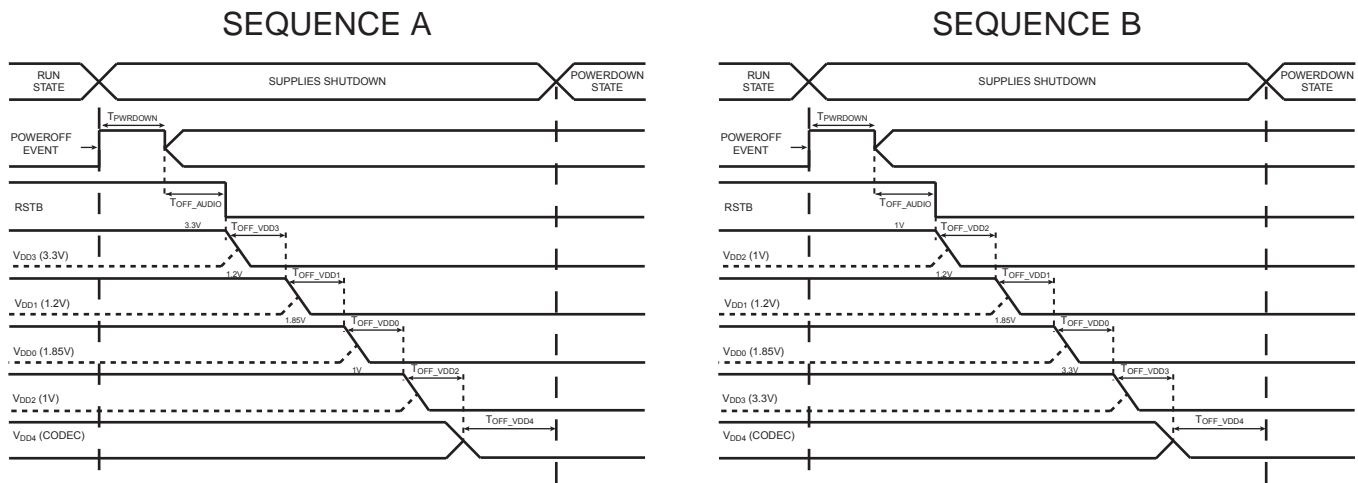
### 11.4.1 POWERDOWN STATE

When AT73C246 is in POWERDOWN state:

- Only  $V_{\text{BACKUP}}$  supply is active.  $VDD_{\{0,1,2,3,4\}}$  power supplies are OFF.
- Audio function is OFF.
- ADC function is OFF.
- RSTB pin is held low.
- Led pin is set as input with internal 120k pull-up resistor to VINSYS.
- TWI registers are reset to default value.

When the POWERDOWN state is reached from the RUN state, the CPU power supplies are switched off sequentially as described in [Figure 11-3 on page 30](#).

**Figure 11-3.** AT73C246 - RUN to POWERDOWN state Supplies Shutdown timing diagram.



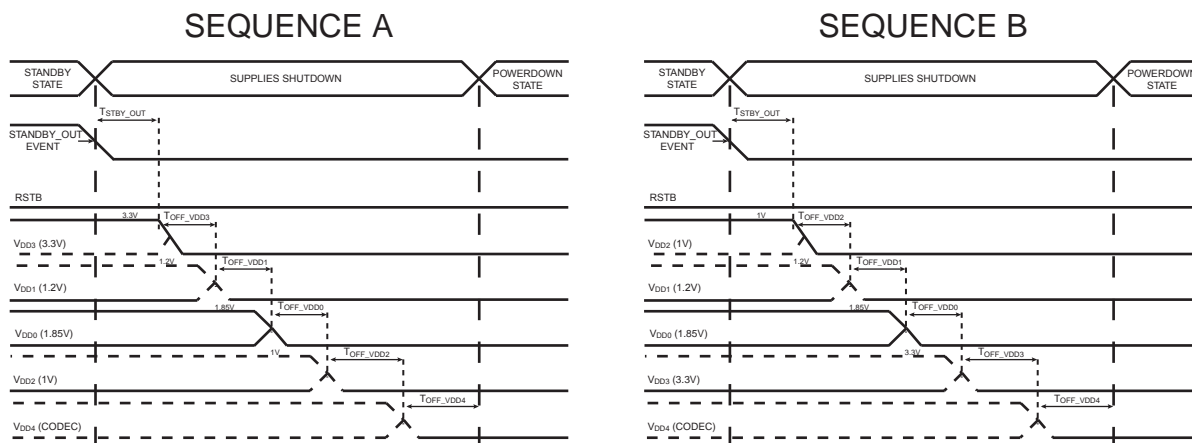
**Table 11-2.** RUN to POWERDOWN state timing table

| Symbol                 | Parameter                      | Comments                                | Min | Typ | Max | Units |
|------------------------|--------------------------------|---|-----|-----|-----|-------|
| T <sub>PWRDOWN</sub>   | POWERDOWN Event detection time |   | 58  | 62  | 66  | μs    |
| T <sub>OFF_AUDIO</sub> | Audio CODEC Shutdown Time      | Audio CODEC is OFF or Power Fail Occurs | 58  | 62  | 66  | μs    |
|                        |                                | Audio CODEC is ON                       | 486 | 512 | 538 | ms    |
| T <sub>OFF_VDDx</sub>  | VDDx SHUTDOWN Time             | VDDx is OFF in RUN state <sup>(1)</sup> | 58  | 62  | 66  | μs    |
|                        |                                | VDDx is ON in RUN state <sup>(1)</sup>  | 4.8 | 5.2 | 5.4 | ms    |

Note: 1. VDDx activity during RUN state is set by Bit7 of register VDDx\_CTRL.

When the POWERDOWN state is reached from the STANDBY state, the CPU power supplies are switched off sequentially as described in Figure 11-4.

**Figure 11-4.** AT73C246 - STANDBY to POWERDOWN state Supplies Shutdown timing diagram.



**Table 11-3.** STANDBY to POWERDOWN state timing table

| Symbol          | Parameter                        | Comments  | Min | Typ | Max | Units   |
|-----------------|----------------------------------|---|-----|-----|-----|---------|
| $T_{STBY\_OUT}$ | STANDBY OUT Event detection time |   | 95  | 100 | 105 | $\mu s$ |
| $T_{OFF\_VDDx}$ | VDDx SHUTDOWN Time               | VDDx is OFF during STANDBY state <sup>(1)</sup> | 58  | 62  | 66  | $\mu s$ |
|                 |                                  | VDDx is ON during STANDBY state <sup>(1)</sup>  | 4.8 | 5.2 | 5.4 | ms      |
| $T_{OFF\_VDD4}$ | VDD4 SHUTDOWN Time               | VDD4 is OFF in RUN state <sup>(2)</sup>         | 58  | 62  | 66  | $\mu s$ |
|                 |                                  | VDD4 is ON in RUN state <sup>(2)</sup>          | 4.8 | 5.2 | 5.4 | ms      |

- Notes:
- VDDx activity during STANDBY state is set by register PMU\_STANDBY\_SUPPLIES.
  - VDD4 activity during RUN state is set by Bit7 of register VDD4\_CTRL.

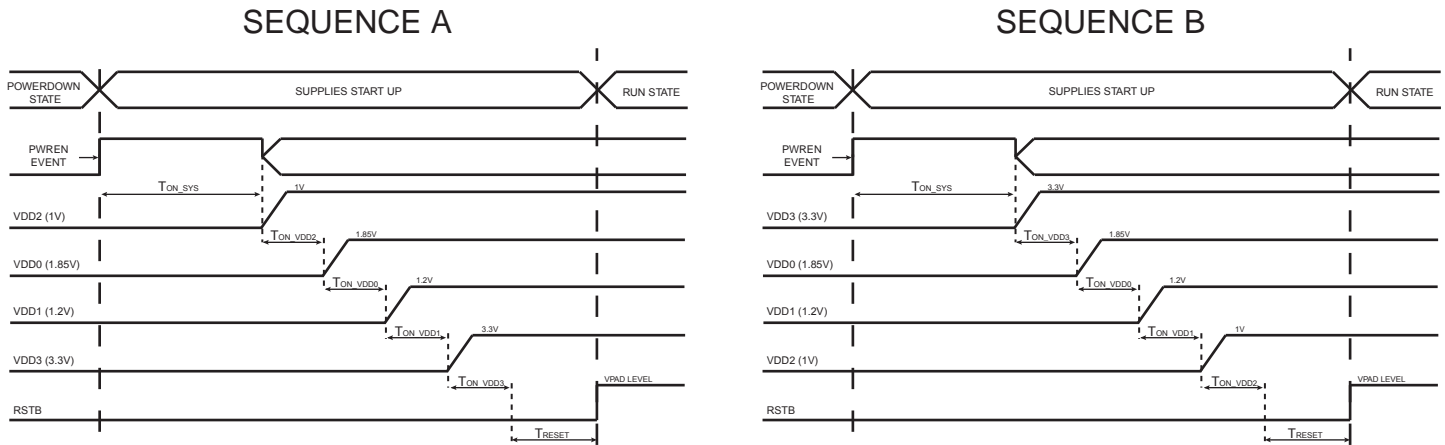
## 11.4.2 RUN STATE

When AT73C246 is in RUN state:

- VDD<sub>{0,1,2,3,5}</sub> power supplies are ON.
- RSTB pin is released.
- PMU functions are under software control (LDO4, AUDIO CODEC, ADC Controller)
- Led pin is driven according to register PMU\_LED (0x0B).

When RUN state is reached from the POWERDOWN state, the power supplies are sequentially started-up according to the [Figure 11-5](#)

**Figure 11-5.** AT73C246 - POWERDOWN to RUN state Supplies Start-Up timing diagram..

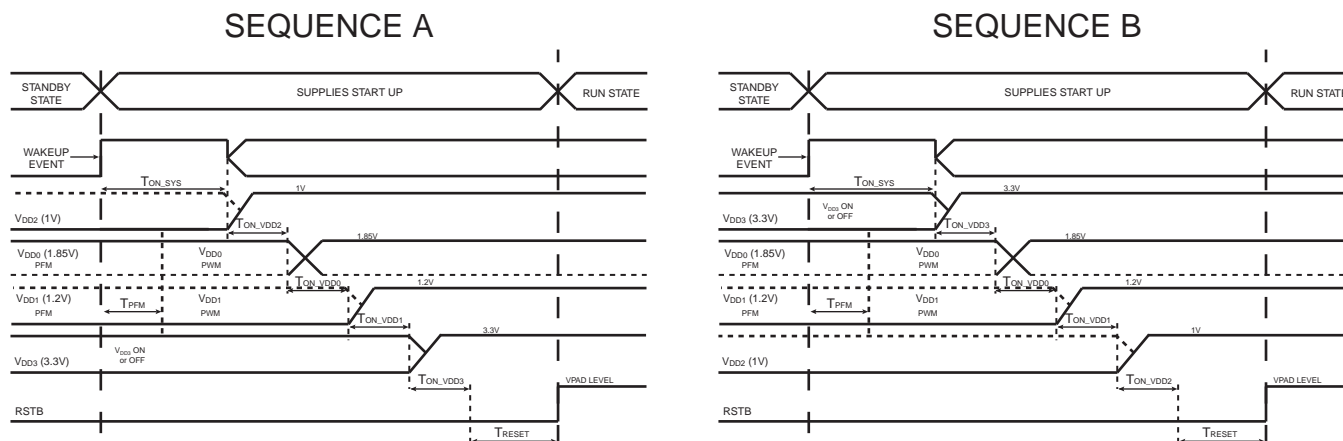


**Table 11-4.** POWERDOWN to RUN state timing table

| Symbol         | Parameter                      | Comments | Min  | Typ | Max  | Units |
|----------------|--------------------------------|----------|------|-----|------|-------|
| $T_{ON\_SYS}$  | POWER-ON Event Detection Time  |          | 1.7  | 1.8 | 1.9  | ms    |
| $T_{ON\_VDD0}$ | VDD0 Start-up Time             |          | 5    | 5.3 | 5.6  | ms    |
| $T_{ON\_VDD1}$ | VDD1 Start-up Time             |          | 5    | 5.3 | 5.6  | ms    |
| $T_{ON\_VDD2}$ | VDD2 Start-up Time             |          | 5.2  | 5.5 | 5.8  | ms    |
| $T_{ON\_VDD3}$ | VDD3 Start-up Time             |          | 5.2  | 5.5 | 5.8  | ms    |
| $T_{RESET}$    | All Regulators ON To RSTB High |          | 30.4 | 32  | 33.6 | ms    |

When RUN state is reached from the STANDBY state, the power supplies are sequentially started-up according to the [Figure 11-6](#).

**Figure 11-6.** AT73C246 - STANDBY to RUN state Supplies Start-Up timing diagram.



**Table 11-5.** STANDBY to RUN state timing table

| Symbol               | Parameter                      | Comments  | Min  | Typ | Max  | Units |
|----------------------|--------------------------------|---|------|-----|------|-------|
| T <sub>ON_SYS</sub>  | Start-up Time                  | Time from validated WAKEUP event (end of debounce time when applicable) to VDD2 or VDD3 power on.           | 810  | 900 | 990  | µs    |
| T <sub>PFM</sub>     | PFM/PWM Switching time         | Time from validated WAKEUP event (end of debounce time when applicable) to PFM/PWM switching if applicable. | 420  | 470 | 520  | µs    |
| T <sub>ON_VDDx</sub> | VDDx Start-up Time             | VDDx is OFF during STANDBY state <sup>(1)</sup>   | 5.2  | 5.4 | 5.7  | ms    |
|                      |                                | VDDx is ON during STANDBY state <sup>(1)</sup>  | 58   | 62  | 66   | µs    |
| T <sub>RESET</sub>   | All Regulators ON To RSTB High |   | 30.4 | 32  | 33.6 | ms    |

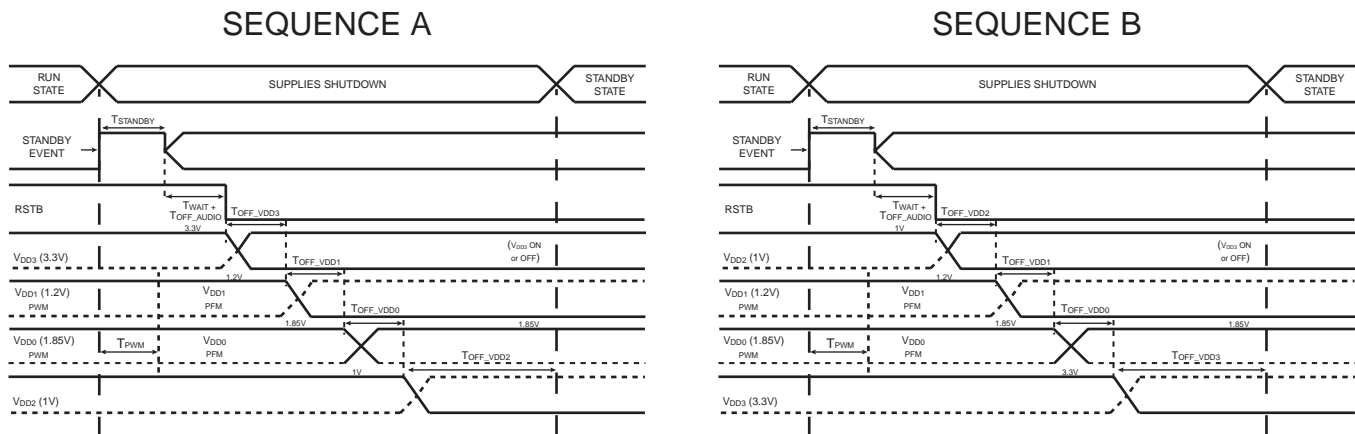
Note: 1. VDDx activity during STANDBY state is set by register PMU\_STANDBY\_SUPPLIES.

### 11.4.3 STANDBY STATE

When AT73C246 is in STANDBY state:

- V<sub>BACKUP</sub> is ON.
- VDD<sub>{0,1,2,3}</sub> are ON or OFF according to the status in register 0x03 (PMU\_STANDBY\_SUPPLIES)
- VDD<sub>4</sub> is ON or OFF according to the status in register 0x0A (VDD4\_CTRL)
- Audio function is OFF
- ADC function is ON or OFF according to the status in register 0x30 (ADC\_CTRL)
- RSTB pin is forced to ground.
- TWI pins are ignored to prevent TWI registers from corruption
- Led pin is driven according to register PMU\_LED (0x0B)

To reach the STANDBY state, the appropriate power supplies are shut down as described in the [Figure 11-7 on page 34](#).

**Figure 11-7.** AT73C246 - RUN to STANDBY state Supplies Shutdown timing diagram.

**Table 11-6.** RUN to STANDBY state timing table

| Symbol           | Parameter                     | Comments  | Min | Typ | Max | Units   |
|------------------|-------------------------------|---|-----|-----|-----|---------|
| $T_{STANDBY}$    | STANDBY Event Detection Time  |   | 150 | 160 | 170 | $\mu s$ |
| $T_{PWM}$        | PFM/PWM Switching time        | Time from validated WAKEUP event (end of debounce time when applicable) to PFM/PWM switching if applicable. | 460 | 500 | 540 | $\mu s$ |
| $T_{WAIT}$       | WAKEUP Event Detection Window | If a WAKEUP event occurs in this window the PMU automatically restart at the end of the STANDBY process.    | 150 | 160 | 170 | $\mu s$ |
| $T_{OFF\_AUDIO}$ | Audio CODEC Shutdown Time     | Audio CODEC is ON   | 486 | 512 | 538 | ms      |
|                  |                               | Audio CODEC is OFF  | 58  | 62  | 66  | $\mu s$ |
| $T_{OFF\_VDDx}$  | VDDx SHUTDOWN Time            | VDDx is OFF during both STANBY <sup>(1)</sup> and RUN <sup>(2)</sup> states.                                | 58  | 62  | 66  | $\mu s$ |
|                  |                               | VDDx is OFF during STANBY state <sup>(1)</sup> .<br>VDDx is ON during RUN state <sup>(2)</sup> .            | 4.8 | 5.2 | 5.4 | ms      |
| $T_{ON\_VDDx}$   | VDDx STARTUP Time             | VDDx is ON during STANBY state <sup>(1)</sup> .<br>VDDx is OFF during RUN state <sup>(2)</sup> .            | 4.8 | 5.2 | 5.4 | ms      |
|                  |                               | VDDx is ON during both STANBY <sup>(1)</sup> and RUN <sup>(2)</sup> states.                                 | 58  | 62  | 66  | $\mu s$ |

- Note: 1. VDDx activity during STANDBY state is set by register PMU\_STANDBY\_SUPPLIES.  
2. VDDx activity during RUN state is set by Bit7 of register VDDx\_CTRL.

#### 11.4.4 HRST STATE

HRST state is a transition state used to restart the CPU:

- VDD<sub>{0,1,2,3,4}</sub> are switched off according to figure [Figure 11-8 on page 35](#) depending on the previous state
- VDD<sub>5</sub> is ON
- RSTB pin is forced to ground

Figure 11-8. AT73C246 - HRST state Supplies Shutdown timing diagram.

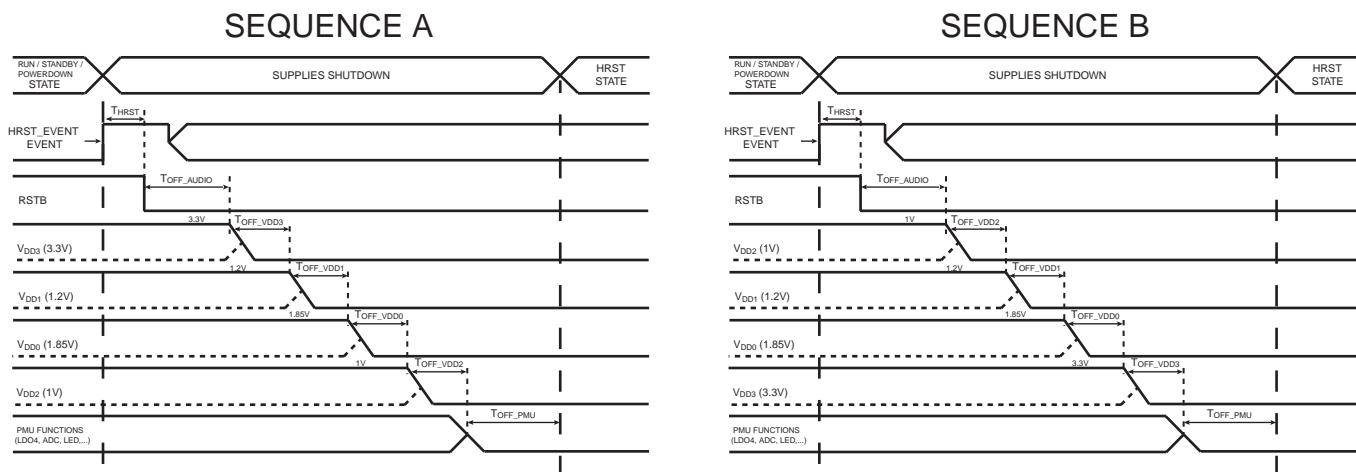


Table 11-7. HRST state timing table from RUN STATE

| Symbol           | Parameter                   | Comments                                | Min | Typ | Max | Units   |
|------------------|-----------------------------|---|-----|-----|-----|---------|
| $T_{HRST}$       | HRST Event Detection Time   |   | 58  | 62  | 66  | $\mu s$ |
| $T_{OFF\_AUDIO}$ | Audio CODEC Shutdown Time   | Audio CODEC is ON                       | 486 | 512 | 538 | ms      |
|                  |                             | Audio CODEC is OFF                      | 58  | 62  | 66  | $\mu s$ |
| $T_{OFF\_VDDx}$  | VDDx SHUTDOWN Time          | VDDx is OFF in RUN state <sup>(1)</sup> | 58  | 62  | 66  | $\mu s$ |
|                  |                             | VDDx is ON in RUN state <sup>(1)</sup>  | 4.8 | 5.2 | 5.4 | ms      |
| $T_{OFF\_PMU}$   | PMU Functions Shutdown Time |   | 1.4 | 1.5 | 1.6 | ms      |

Note: 1. VDDx activity during RUN state is set by Bit7 of register VDDx\_CTRL

Table 11-8. HRST state timing table from STANDBY STATE

| Symbol           | Parameter                   | Comments  | Min | Typ | Max | Units   |
|------------------|-----------------------------|---|-----|-----|-----|---------|
| $T_{HRST}$       | HRST Event Detection Time   |   | 58  | 62  | 66  | $\mu s$ |
| $T_{OFF\_AUDIO}$ | Audio CODEC Shutdown Time   | Audio CODEC is ON                               | 486 | 512 | 538 | ms      |
|                  |                             | Audio CODEC is OFF                              | 58  | 62  | 66  | $\mu s$ |
| $T_{OFF\_VDDx}$  | VDDx SHUTDOWN Time          | VDDx is OFF during STANDBY state <sup>(1)</sup> | 58  | 62  | 66  | $\mu s$ |
|                  |                             | VDDx is ON during STANDBY state <sup>(1)</sup>  | 4.8 | 5.2 | 5.4 | ms      |
| $T_{OFF\_VDD4}$  | VDD4 SHUTDOWN Time          | VDD4 is OFF in RUN state <sup>(2)</sup>         | 58  | 62  | 66  | $\mu s$ |
|                  |                             | VDD4 is ON in RUN state <sup>(2)</sup>          | 4.8 | 5.2 | 5.4 | ms      |
| $T_{OFF\_PMU}$   | PMU Functions Shutdown Time |   | 1.4 | 1.5 | 1.6 | ms      |

Notes: 1. VDDx activity during STANDBY state is set by register PMU\_STANDBY\_SUPPLIES.

2. VDD4 activity during RUN state is set by Bit7 of register VDD4\_CTRL.

## 11.5 DCDC0 and DCDC1 Functional Description

DCDC0 and DCDC1 are 2 identical high performance synchronous step-down (buck) converters. They feature:

- 2 control modes: PFM and PWM,
- A soft start circuit,
- A software programmable output voltage between 0.8 and 3.6V with automatic ramping for DVS application,
- An Over-Current-Protection circuit,
- A 180 degree out of phase operating mode.

### 11.5.1 PFM and PWM Control Modes

Pulse Frequency Modulation control is an hysteretic control of the output voltage. It is specially intended for light loads (< 50mA typ). In this mode, the DCDC converter exhibits a very low quiescent current (< 50 $\mu$ A) thus achieving very high efficiency at light loads. The frequency of operation in this mode is not fixed but proportional to the load current.

Pulse Width Modulation control is a fixed frequency, variable duty cycle control of the DCDC converter. It has a fast and precise feedback loop specially intended to handle hard loads and low output ripple voltage.

At start-up, DCDC0 and DCDC1 operate in PWM mode. This way, high load at CPU boot are properly handled. Through software control in registers VDD0\_CTRL (0x06) and VDD1\_CTRL (0x07), the user may enter the low-power mode (PFM) when the application consumption is reduced.

### 11.5.2 Soft-start Circuit

DCDC0 and DCDC1 feature a soft start circuit to prevent high input current while charging the output capacitor from 0V to the default output voltage. Typically, the in-rush current at start-up (with no load) is limited to 30 mA.

### 11.5.3 Output Voltage Programming

DCDC0 and DCDC1 output voltages can be managed through software control in registers VDD0\_CTRL (0x06) and VDD1\_CTRL (0x07). 50mV steps are provided from 0.8V to 3.6V. It is recommended to use the automatic ramping function in register PMU\_SUPPLY\_CTRL (0x04) to achieve smooth operation. When the DVS\_VDD<sub>{0,1}</sub> bit is active (default mode), output voltages are ramped from the current value to the final value in 50mV / 280us steps. For users who intend to disable the DVS\_VDD<sub>{0,1}</sub> bit, a maximum of 4 steps (= 200mV) per 100us is allowed.

At power up, DCDC0 and DCDC1 default output voltages are respectively 1.85V and 1.20V. For different default output voltages, please contact Atmel.

### 11.5.4 180° Out-of-phase Operation

DCDC0 and DCDC1 can be operated in-phase or at 180° out-of-phase according to the selection bit in register PMU\_SUPPLY\_CTRL (0x04). When operated in phase both converters will start charging their inductor at the same time. When operated at 180° out-of-phase, the inductor charge start time will be shifted by half a 2MHz clock delay (= 250ns) from one converter to the other. This latter scheme tends to average the input current of both DCDC converters.



## 11.6 LDO2 Functional Description

LDO2 is a linear voltage regulator intended to supply CPU core voltages in the range 0.8V to 1.35V. Its maximum input voltage is 3.6V. Thus, it must not be wired to the VIN plane with VINSYS, VIN0, VIN1, VIN3 and VIN4 if VIN is above 3.6V. Considering its low-output voltage and for the sake of efficiency and power dissipation, the user may connect it at the output of DCDC0.

This LDO features:

- A soft start circuit,
- A software programmable output voltage between 0.8 and 1.35V with automatic ramping for DVS application.

### 11.6.1 Soft-start Circuit

LDO2 features a soft start circuit to prevent high input current while charging the output capacitor from 0V to the default output voltage. This soft start circuit limits the input current during 5ms (+/-5%) at startup to 200mA in typical conditions. After this delay, LDO2 recovers full current capability.

### 11.6.2 Output Voltage Programming

LDO2 output voltage can be managed through software control in register VDD2\_CTRL (0x08). 50mV steps are provided from 0.8V to 1.35V. It is recommended to use the automatic ramping function in register PMU\_SUPPLY\_CTRL (0x04) to achieve smooth operation. When the DVS\_VDD2 bit is active (default mode), output voltages are ramped from the current value to the final value in 50mV / 600us steps.

At power up, LDO2 default output voltage is 1V. For different default output voltage, please contact Atmel.

## 11.7 LDO3 and LDO4 Functional Description

LDO3 and LDO4 are low dropout linear voltage regulators intended to supply CPU peripherals (I/Os, analog functions) in the range 2.7V to 3.6V. They can be operated directly from a 5.5V maximum input voltage. They feature:

- A soft start circuit,
- A software programmable output between 2.7V and 3.6V voltage with automatic ramping for DVS application,

### 11.7.1 Soft-start Circuit

LDO3 and LDO4 feature a soft start circuit to prevent high input current while charging the output capacitor from 0V to the default output voltage. This soft start circuit limits the input current during 5ms (+/-5%) at startup to 200mA in typical conditions. After this delay, LDO3(4) recovers full current capability.

### 11.7.2 Output Voltage Programming

LDO3 and LDO4 output voltages can be managed through software control in registers VDD3\_CTRL (0x09) and VDD4\_CTRL (0x0A). 50mV steps are provided from 2.7V to 3.6V. It is recommended to use the automatic ramping function in register PMU\_SUPPLY\_CTRL (0x04) to achieve smooth operation. When the DVS\_VDD<sub>{3,4}</sub> bit is active (default mode), output voltages are ramped from the current value to the final value in 50mV / 600us steps.

At power up, LDO3 and LDO4 default output voltages are both 3.3V. For different default output voltages, please contact Atmel.

## 11.8 Power Fail Detectors

AT73C246 features a Power Fail detector on each CPU supplies ( $V_{DD0}$ ,  $V_{DD1}$ ,  $V_{DD2}$ ,  $V_{DD3}$ ). This function is made of a comparator that toggles each time one of the listed power supplies goes below a defined threshold. The comparator toggling is considered by the PMU digital state machine as a POWER-FAIL event.

The threshold value of the power fail detector is proportional to the output voltage of the regulator. It is not a fixed voltage, it is adapted to the programmed output voltage. The default threshold value is set according to register PMU\_RST\_LVL (0x05) and can be programmed to another value through TWI access. For other default threshold values at startup, please contact Atmel.

## 11.9 Measurement Bridge and 10-bit ADC

AT73C246 features a 10-channel measurement chain including:

- A multiplexer + attenuator followed by a unity gain buffer
- A 300kS/s 10-bit SAR ADC.

ADC function is enabled through the register ADC\_CTRL (0x30). ADC\_MUX\_1 (0x31) and ADC\_MUX\_2 (0x32) allow the selection of inputs to be measured. 1 to 10 inputs can be selected. The ADC will then perform serial conversion on these inputs and write the corresponding result in registers 0x33 to 0x49.

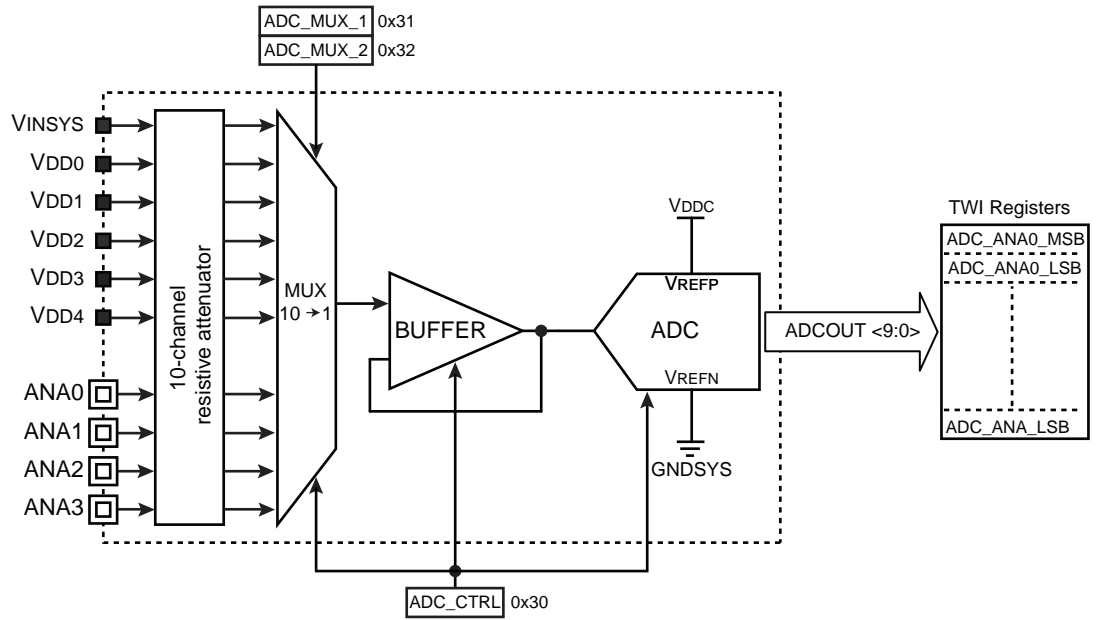
2 sampling modes are provided to perform periodic conversions:

- Max speed
- Low speed.

To enter these modes, refer to the sampling period bits (TS) in the register ADC\_CTRL (0x30).

When MAX\_SPEED mode is selected, the ADC runs at 300kS/s and loops without any dead time over the selected inputs. When a LOW\_SPEED sampling period is selected, the ADC performs a set of input conversions (1 to 10) at 300kS/s and then waits for one sampling period (defined by TS bits) to start another set of conversions.

Figure 11-9. Measurement Bridge and 10-bit ADC Block Diagram.



## 11.10 Real Time Clock (RTC) User Interface

Figure 11-10. RTC Block Diagram

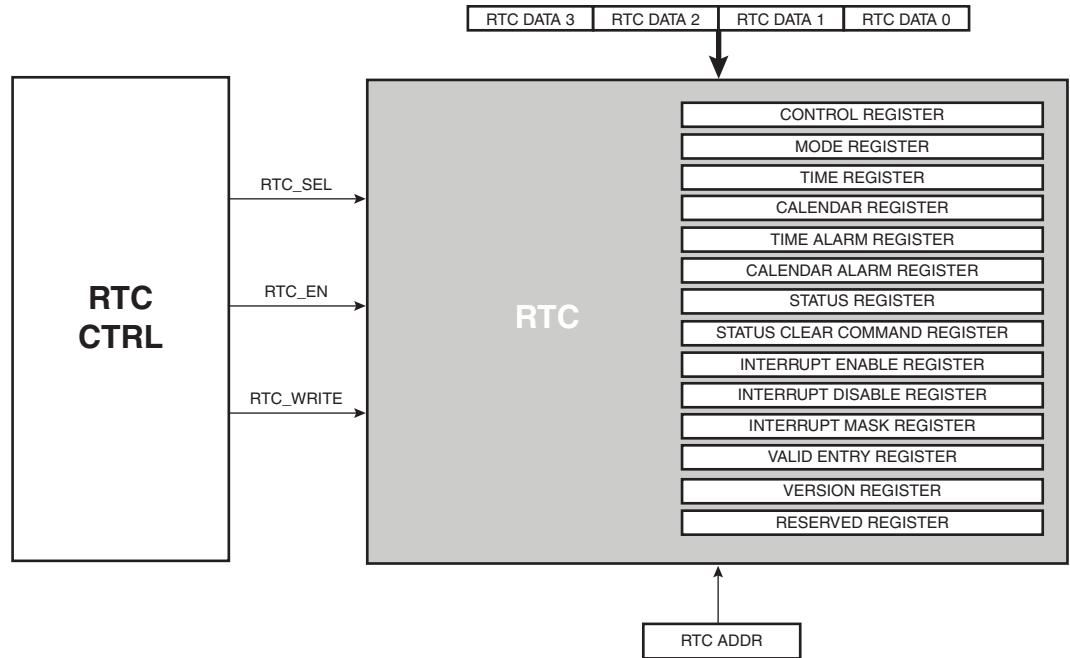


Table 11-9. Register Mapping

| Offset | Register                        | Name        | Access     | Reset      |
|--------|---------------------------------|-------------|------------|------------|
| 0x00   | Control Register                | RTC_CR      | Read-write | 0x0        |
| 0x04   | Mode Register                   | RTC_MR      | Read-write | 0x0        |
| 0x08   | Time Register                   | RTC_TIMR    | Read-write | 0x0        |
| 0x0C   | Calendar Register               | RTC_CALR    | Read-write | 0x01819819 |
| 0x10   | Time Alarm Register             | RTC_TIMALR  | Read-write | 0x0        |
| 0x14   | Calendar Alarm Register         | RTC_CALALR  | Read-write | 0x01010000 |
| 0x18   | Status Register                 | RTC_SR      | Read-only  | 0x0        |
| 0x1C   | Status Clear Command Register   | RTC_SCCR    | Write-only | ---        |
| 0x20   | Interrupt Enable Register       | RTC_IER     | Write-only | ---        |
| 0x24   | Interrupt Disable Register      | RTC_IDR     | Write-only | ---        |
| 0x28   | Interrupt Mask Register         | RTC_IMR     | Read-only  | 0x0        |
| 0x2C   | Valid Entry Register            | RTC_VER     | Read-only  | 0x0        |
| 0xFC   | Version Register <sup>(1)</sup> | RTC_VERSION | Read-only  | ---        |
| 0xFC   | Reserved Register               | ---         | ---        | ---        |

Note: 1. Values in the Version Register vary with the version of the IP block implementation.

11.10.1 RTC Register Read/Write Operation

Figure 11-11. RTC Read Operation

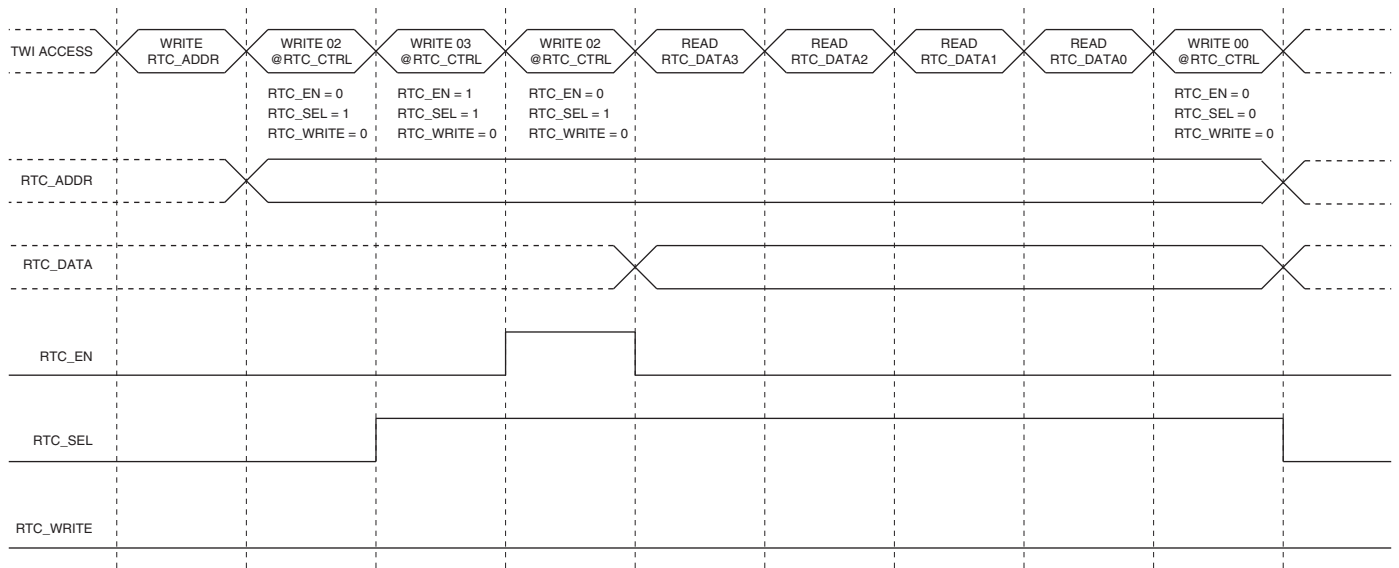
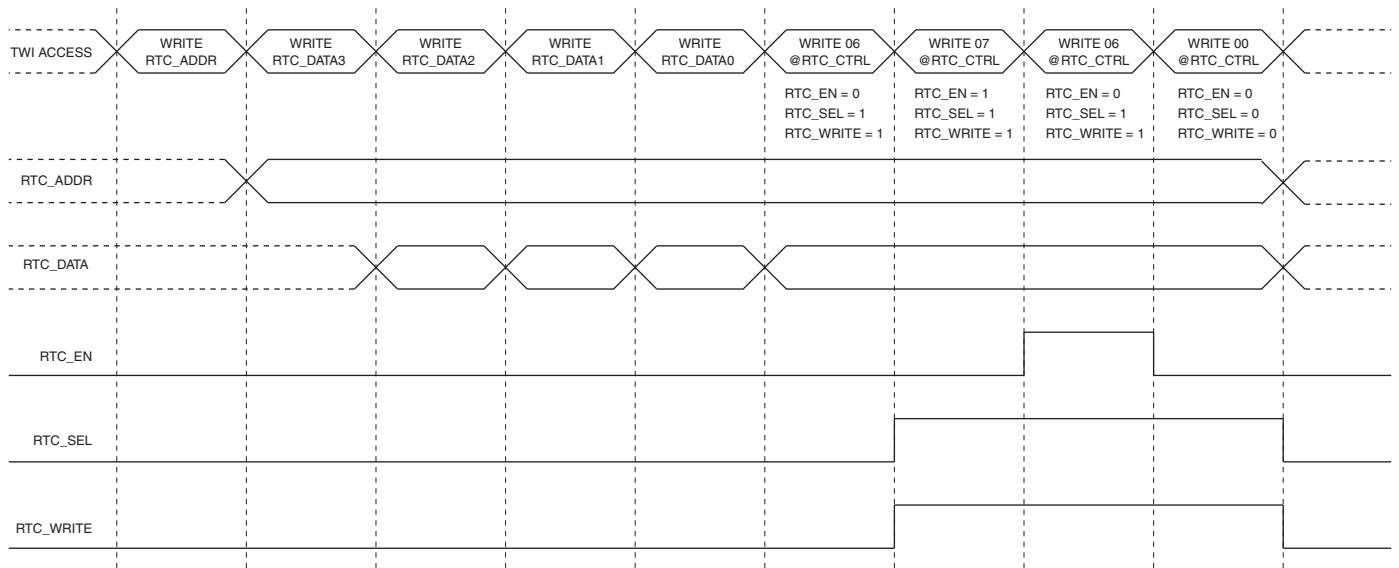


Figure 11-12. RTC Write Operation



### 11.10.2 RTC Control Register

**Name:** RTC\_CR  
**Access:** Read-write  
**Address:** 0x00

|    |    |    |    |    |    |          |        |
|----|----|----|----|----|----|----------|--------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25       | 24     |
| –  | –  | –  | –  | –  | –  | –        | –      |
| 23 | 22 | 21 | 20 | 19 | 18 | 17       | 16     |
| –  | –  | –  | –  | –  | –  | CALEVSEL |        |
| 15 | 14 | 13 | 12 | 11 | 10 | 9        | 8      |
| –  | –  | –  | –  | –  | –  | TIMEVSEL |        |
| 7  | 6  | 5  | 4  | 3  | 2  | 1        | 0      |
| –  | –  | –  | –  | –  | –  | UPDCAL   | UPDTIM |

- **UPDTIM: Update Request Time Register**

0 = No effect.

1 = Stops the RTC time counting.

Time counting consists of second, minute and hour counters. Time counters can be programmed once this bit is set and acknowledged by the bit ACKUPD of the Status Register.

- **UPDCAL: Update Request Calendar Register**

0 = No effect.

1 = Stops the RTC calendar counting.

Calendar counting consists of day, date, month, year and century counters. Calendar counters can be programmed once this bit is set.

- **TIMEVSEL: Time Event Selection**

The event that generates the flag TIMEV in RTC\_SR (Status Register) depends on the value of TIMEVSEL.

0 = Minute change.

1 = Hour change.

2 = Every day at midnight.

3 = Every day at noon.

- **CALEVSEL: Calendar Event Selection**

The event that generates the flag CALEV in RTC\_SR depends on the value of CALEVSEL.

0 = Week change (every Monday at time 00:00:00).

1 = Month change (every 01 of each month at time 00:00:00).

2, 3 = Year change (every January 1 at time 00:00:00)

**11.10.3 RTC Mode Register**

**Name:** RTC\_MR

**Access:** Read-write

**Address:** 0x04

|    |    |    |    |    |    |    |       |
|----|----|----|----|----|----|----|-------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24    |
| –  | –  | –  | –  | –  | –  | –  | –     |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16    |
| –  | –  | –  | –  | –  | –  | –  | –     |
| 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8     |
| –  | –  | –  | –  | –  | –  | –  | –     |
| 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0     |
| –  | –  | –  | –  | –  | –  | –  | HRMOD |

• **HRMOD: 12-/24-hour Mode**

0 = 24-hour mode is selected.

1 = 12-hour mode is selected.

All non-significant bits read zero.

#### 11.10.4 RTC Time Register

**Name:** RTC\_TIMR

**Access:** Read-write

**Address:** 0x08

|    |      |      |    |    |    |    |    |
|----|------|------|----|----|----|----|----|
| 31 | 30   | 29   | 28 | 27 | 26 | 25 | 24 |
| –  | –    | –    | –  | –  | –  | –  | –  |
| 23 | 22   | 21   | 20 | 19 | 18 | 17 | 16 |
| –  | AMPM | HOUR |    |    |    |    |    |
| 15 | 14   | 13   | 12 | 11 | 10 | 9  | 8  |
| –  | MIN  |      |    |    |    |    |    |
| 7  | 6    | 5    | 4  | 3  | 2  | 1  | 0  |
| –  | SEC  |      |    |    |    |    |    |

- **SEC: Current Second**

The range that can be set is 0 - 59 (BCD).

The lowest four bits encode the units. The higher bits encode the tens.

- **MIN: Current Minute**

The range that can be set is 0 - 59 (BCD).

The lowest four bits encode the units. The higher bits encode the tens.

- **HOUR: Current Hour**

The range that can be set is 1 - 12 (BCD) in 12-hour mode or 0 - 23 (BCD) in 24-hour mode.

- **AMPM: Ante Meridiem Post Meridiem Indicator**

This bit is the AM/PM indicator in 12-hour mode.

0 = AM.

1 = PM.

All non-significant bits read zero.



**11.10.5 RTC Calendar Register**

**Name:** RTC\_CALR  
**Access:** Read-write  
**Address:** 0x0C

|      |      |      |    |       |    |    |    |
|------|------|------|----|-------|----|----|----|
| 31   | 30   | 29   | 28 | 27    | 26 | 25 | 24 |
| –    | –    | DATE |    |       |    |    |    |
| 23   | 22   | 21   | 20 | 19    | 18 | 17 | 16 |
| DAY  |      |      |    | MONTH |    |    |    |
| 15   | 14   | 13   | 12 | 11    | 10 | 9  | 8  |
| YEAR |      |      |    |       |    |    |    |
| 7    | 6    | 5    | 4  | 3     | 2  | 1  | 0  |
| –    | CENT |      |    |       |    |    |    |

• **CENT: Current Century**

The range that can be set is 19 - 20 (BCD).  
 The lowest four bits encode the units. The higher bits encode the tens.

• **YEAR: Current Year**

The range that can be set is 00 - 99 (BCD).  
 The lowest four bits encode the units. The higher bits encode the tens.

• **MONTH: Current Month**

The range that can be set is 01 - 12 (BCD).  
 The lowest four bits encode the units. The higher bits encode the tens.

• **DAY: Current Day**

The range that can be set is 1 - 7 (BCD).  
 The coding of the number (which number represents which day) is user-defined as it has no effect on the date counter.

• **DATE: Current Date**

The range that can be set is 01 - 31 (BCD).  
 The lowest four bits encode the units. The higher bits encode the tens.  
 All non-significant bits read zero.



### 11.10.6 RTC Time Alarm Register

**Name:** RTC\_TIMALR

**Access:** Read-write

**Address:** 0x10

|        |      |      |    |    |    |    |    |
|--------|------|------|----|----|----|----|----|
| 31     | 30   | 29   | 28 | 27 | 26 | 25 | 24 |
| –      | –    | –    | –  | –  | –  | –  | –  |
| 23     | 22   | 21   | 20 | 19 | 18 | 17 | 16 |
| HOUREN | AMPM | HOUR |    |    |    |    |    |
| 15     | 14   | 13   | 12 | 11 | 10 | 9  | 8  |
| MINEN  | MIN  |      |    |    |    |    |    |
| 7      | 6    | 5    | 4  | 3  | 2  | 1  | 0  |
| SECEN  | SEC  |      |    |    |    |    |    |

- **SEC: Second Alarm**

This field is the alarm field corresponding to the BCD-coded second counter.

- **SECEN: Second Alarm Enable**

0 = The second-matching alarm is disabled.

1 = The second-matching alarm is enabled.

- **MIN: Minute Alarm**

This field is the alarm field corresponding to the BCD-coded minute counter.

- **MINEN: Minute Alarm Enable**

0 = The minute-matching alarm is disabled.

1 = The minute-matching alarm is enabled.

- **HOUR: Hour Alarm**

This field is the alarm field corresponding to the BCD-coded hour counter.

- **AMPM: AM/PM Indicator**

This field is the alarm field corresponding to the BCD-coded hour counter.

- **HOUREN: Hour Alarm Enable**

0 = The hour-matching alarm is disabled.

1 = The hour-matching alarm is enabled.

**11.10.7 RTC Calendar Alarm Register**

**Name:** RTC\_CALALR

**Access:** Read-write

**Address:** 0x14

|        |    |      |       |    |    |    |    |
|--------|----|------|-------|----|----|----|----|
| 31     | 30 | 29   | 28    | 27 | 26 | 25 | 24 |
| DATEEN | -  | DATE |       |    |    |    |    |
| 23     | 22 | 21   | 20    | 19 | 18 | 17 | 16 |
| MTHEN  | -  | -    | MONTH |    |    |    |    |
| 15     | 14 | 13   | 12    | 11 | 10 | 9  | 8  |
| -      | -  | -    | -     | -  | -  | -  | -  |
| 7      | 6  | 5    | 4     | 3  | 2  | 1  | 0  |
| -      | -  | -    | -     | -  | -  | -  | -  |

- **MONTH: Month Alarm**

This field is the alarm field corresponding to the BCD-coded month counter.

- **MTHEN: Month Alarm Enable**

0 = The month-matching alarm is disabled.

1 = The month-matching alarm is enabled.

- **DATE: Date Alarm**

This field is the alarm field corresponding to the BCD-coded date counter.

- **DATEEN: Date Alarm Enable**

0 = The date-matching alarm is disabled.

1 = The date-matching alarm is enabled.

### 11.10.8 RTC Status Register

**Name:** RTC\_SR  
**Access:** Read-only  
**Address:** 0x18

|    |    |    |       |       |     |       |        |
|----|----|----|-------|-------|-----|-------|--------|
| 31 | 30 | 29 | 28    | 27    | 26  | 25    | 24     |
| –  | –  | –  | –     | –     | –   | –     | –      |
| 23 | 22 | 21 | 20    | 19    | 18  | 17    | 16     |
| –  | –  | –  | –     | –     | –   | –     | –      |
| 15 | 14 | 13 | 12    | 11    | 10  | 9     | 8      |
| –  | –  | –  | –     | –     | –   | –     | –      |
| 7  | 6  | 5  | 4     | 3     | 2   | 1     | 0      |
| –  | –  | –  | CALEV | TIMEV | SEC | ALARM | ACKUPD |

- **ACKUPD: Acknowledge for Update**

0 = Time and calendar registers cannot be updated.  
 1 = Time and calendar registers can be updated.

- **ALARM: Alarm Flag**

0 = No alarm matching condition occurred.  
 1 = An alarm matching condition has occurred.

- **SEC: Second Event**

0 = No second event has occurred since the last clear.  
 1 = At least one second event has occurred since the last clear.

- **TIMEV: Time Event**

0 = No time event has occurred since the last clear.  
 1 = At least one time event has occurred since the last clear.

The time event is selected in the TIMEVSEL field in RTC\_CTRL (Control Register) and can be any one of the following events: minute change, hour change, noon, midnight (day change).

- **CALEV: Calendar Event**

0 = No calendar event has occurred since the last clear.  
 1 = At least one calendar event has occurred since the last clear.

The calendar event is selected in the CALEVSEL field in RTC\_CR and can be any one of the following events: week change, month change and year change.

**11.10.9 RTC Status Clear Command Register**

**Name:** RTC\_SCCR

**Access:** Write-only

**Address:** 0x1C

|    |    |    |        |        |        |        |        |
|----|----|----|--------|--------|--------|--------|--------|
| 31 | 30 | 29 | 28     | 27     | 26     | 25     | 24     |
| –  | –  | –  | –      | –      | –      | –      | –      |
| 23 | 22 | 21 | 20     | 19     | 18     | 17     | 16     |
| –  | –  | –  | –      | –      | –      | –      | –      |
| 15 | 14 | 13 | 12     | 11     | 10     | 9      | 8      |
| –  | –  | –  | –      | –      | –      | –      | –      |
| 7  | 6  | 5  | 4      | 3      | 2      | 1      | 0      |
| –  | –  | –  | CALCLR | TIMCLR | SECCLR | ALRCLR | ACKCLR |

• **ACKCLR: Acknowledge Clear**

0 = No effect.

1 = Clears corresponding status flag in the Status Register (RTC\_SR).

• **ALRCLR: Alarm Clear**

0 = No effect.

1 = Clears corresponding status flag in the Status Register (RTC\_SR).

• **SECCLR: Second Clear**

0 = No effect.

1 = Clears corresponding status flag in the Status Register (RTC\_SR).

• **TIMCLR: Time Clear**

0 = No effect.

1 = Clears corresponding status flag in the Status Register (RTC\_SR).

• **CALCLR: Calendar Clear**

0 = No effect.

1 = Clears corresponding status flag in the Status Register (RTC\_SR).

### 11.10.10 RTC Interrupt Enable Register

**Name:** RTC\_IER

**Access:** Write-only

**Address:** 0x20

|    |    |    |       |       |       |       |       |
|----|----|----|-------|-------|-------|-------|-------|
| 31 | 30 | 29 | 28    | 27    | 26    | 25    | 24    |
| –  | –  | –  | –     | –     | –     | –     | –     |
| 23 | 22 | 21 | 20    | 19    | 18    | 17    | 16    |
| –  | –  | –  | –     | –     | –     | –     | –     |
| 15 | 14 | 13 | 12    | 11    | 10    | 9     | 8     |
| –  | –  | –  | –     | –     | –     | –     | –     |
| 7  | 6  | 5  | 4     | 3     | 2     | 1     | 0     |
| –  | –  | –  | CALEN | TIMEN | SECEN | ALREN | ACKEN |

- **ACKEN: Acknowledge Update Interrupt Enable**

0 = No effect.

1 = The acknowledge for update interrupt is enabled.

- **ALREN: Alarm Interrupt Enable**

0 = No effect.

1 = The alarm interrupt is enabled.

- **SECEN: Second Event Interrupt Enable**

0 = No effect.

1 = The second periodic interrupt is enabled.

- **TIMEN: Time Event Interrupt Enable**

0 = No effect.

1 = The selected time event interrupt is enabled.

- **CALEN: Calendar Event Interrupt Enable**

0 = No effect.

• 1 = The selected calendar event interrupt is enabled.

## 11.10.11 RTC Interrupt Disable Register

**Name:** RTC\_IDR

**Access:** Write-only

**Address:** 0x24

|    |    |    |        |        |        |        |        |
|----|----|----|--------|--------|--------|--------|--------|
| 31 | 30 | 29 | 28     | 27     | 26     | 25     | 24     |
| –  | –  | –  | –      | –      | –      | –      | –      |
| 23 | 22 | 21 | 20     | 19     | 18     | 17     | 16     |
| –  | –  | –  | –      | –      | –      | –      | –      |
| 15 | 14 | 13 | 12     | 11     | 10     | 9      | 8      |
| –  | –  | –  | –      | –      | –      | –      | –      |
| 7  | 6  | 5  | 4      | 3      | 2      | 1      | 0      |
| –  | –  | –  | CALDIS | TIMDIS | SECDIS | ALRDIS | ACKDIS |

- **ACKDIS: Acknowledge Update Interrupt Disable**

0 = No effect.

1 = The acknowledge for update interrupt is disabled.

- **ALRDIS: Alarm Interrupt Disable**

0 = No effect.

1 = The alarm interrupt is disabled.

- **SECDIS: Second Event Interrupt Disable**

0 = No effect.

1 = The second periodic interrupt is disabled.

- **TIMDIS: Time Event Interrupt Disable**

0 = No effect.

1 = The selected time event interrupt is disabled.

- **CALDIS: Calendar Event Interrupt Disable**

0 = No effect.

1 = The selected calendar event interrupt is disabled.

### 11.10.12 RTC Interrupt Mask Register

**Name:** RTC\_IMR

**Access:** Read-only

**Address:** 0x28

|    |    |    |     |     |     |     |     |
|----|----|----|-----|-----|-----|-----|-----|
| 31 | 30 | 29 | 28  | 27  | 26  | 25  | 24  |
| –  | –  | –  | –   | –   | –   | –   | –   |
| 23 | 22 | 21 | 20  | 19  | 18  | 17  | 16  |
| –  | –  | –  | –   | –   | –   | –   | –   |
| 15 | 14 | 13 | 12  | 11  | 10  | 9   | 8   |
| –  | –  | –  | –   | –   | –   | –   | –   |
| 7  | 6  | 5  | 4   | 3   | 2   | 1   | 0   |
| –  | –  | –  | CAL | TIM | SEC | ALR | ACK |

- **ACK: Acknowledge Update Interrupt Mask**

0 = The acknowledge for update interrupt is disabled.

1 = The acknowledge for update interrupt is enabled.

- **ALR: Alarm Interrupt Mask**

0 = The alarm interrupt is disabled.

1 = The alarm interrupt is enabled.

- **SEC: Second Event Interrupt Mask**

0 = The second periodic interrupt is disabled.

1 = The second periodic interrupt is enabled.

- **TIM: Time Event Interrupt Mask**

0 = The selected time event interrupt is disabled.

1 = The selected time event interrupt is enabled.

- **CAL: Calendar Event Interrupt Mask**

0 = The selected calendar event interrupt is disabled.

1 = The selected calendar event interrupt is enabled.



**11.10.13 RTC Valid Entry Register**

**Name:** RTC\_VER

**Access:** Read-only

**Address:** 0x2C

|    |    |    |    |          |          |       |       |
|----|----|----|----|----------|----------|-------|-------|
| 31 | 30 | 29 | 28 | 27       | 26       | 25    | 24    |
| –  | –  | –  | –  | –        | –        | –     | –     |
| 23 | 22 | 21 | 20 | 19       | 18       | 17    | 16    |
| –  | –  | –  | –  | –        | –        | –     | –     |
| 15 | 14 | 13 | 12 | 11       | 10       | 9     | 8     |
| –  | –  | –  | –  | –        | –        | –     | –     |
| 7  | 6  | 5  | 4  | 3        | 2        | 1     | 0     |
| –  | –  | –  | –  | NVCALALR | NVTIMALR | NVCAL | NVTIM |

• **NVTIM: Non-valid Time**

0 = No invalid data has been detected in RTC\_TIMR (Time Register).

1 = RTC\_TIMR has contained invalid data since it was last programmed.

• **NVCAL: Non-valid Calendar**

0 = No invalid data has been detected in RTC\_CALR (Calendar Register).

1 = RTC\_CALR has contained invalid data since it was last programmed.

• **NVTIMALR: Non-valid Time Alarm**

0 = No invalid data has been detected in RTC\_TIMALR (Time Alarm Register).

1 = RTC\_TIMALR has contained invalid data since it was last programmed.

• **NVCALALR: Non-valid Calendar Alarm**

0 = No invalid data has been detected in RTC\_CALALR (Calendar Alarm Register).

1 = RTC\_CALALR has contained invalid data since it was last programmed.

### 11.10.14 RTC Version register

**Name:** RTC\_VERSION

**Access:** Read-only

**Address:** 0xFC

|         |    |    |    |         |     |    |    |   |
|---------|----|----|----|---------|-----|----|----|---|
| 31      | 30 | 29 | 28 | 27      | 26  | 25 | 24 |   |
| –       | –  | –  | –  | –       | –   | –  | –  |   |
| 23      | 22 | 21 | 20 | 19      | 18  | 17 | 16 |   |
| –       | –  | –  | –  | –       | MFN |    |    |   |
| 15      | 14 | 13 | 12 | 11      | 10  | 9  | 8  |   |
| –       | –  | –  | –  | VERSION |     |    |    | – |
| 7       | 6  | 5  | 4  | 3       | 2   | 1  | 0  |   |
| VERSION |    |    |    |         |     |    |    |   |

- VERSION

Reserved. Value subject to change. No functionality associated. This is the Atmel internal version of the macrocell.

- MFN

Reserved. Value subject to change. No functionality associated.

### 11.11 Die Temperature Sensor

The AT73C246 features a die temperature sensor for protection reasons. If the junction temperature rises above the shutdown threshold for a minimum time of 1ms (+/- 5%), the power manager event  $T_j > 130^\circ\text{C}$  is asserted. In a similar fashion, if the temperature falls through the restart threshold for more than 1ms, the power manager event  $T_j < 110^\circ\text{C}$  is asserted.

The two internal thresholds shutdown and restart are defined in [Section 9.11 “Die Temperature Sensor” on page 21](#).

## 12. Audio Codec Functional Description

### 12.1 Description

AT73C246 features a high quality, low power stereo audio codec with integrated headphone amplifier.

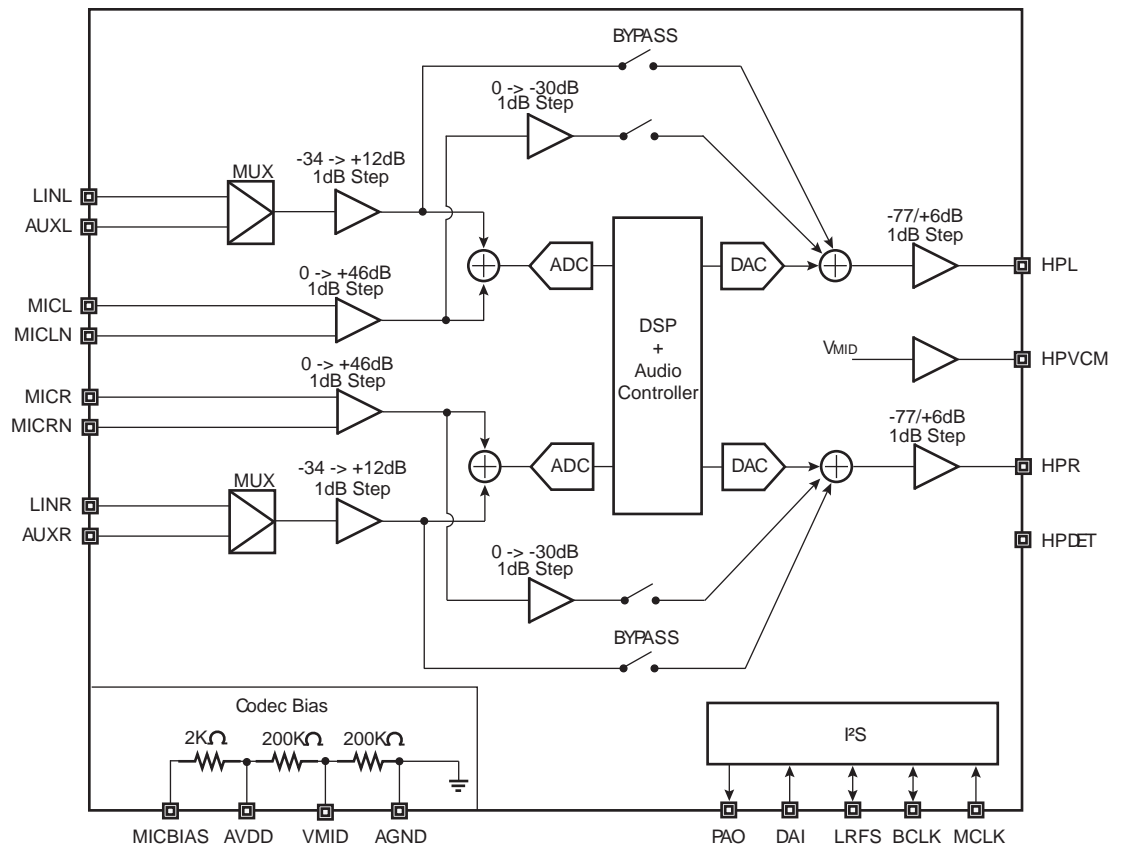
The playback channel accommodates 16 to 24-bit stereo programmable format entering the digital audio interface (I<sup>2</sup>S) and delivers an internal analog audio output through a 100dB SNR Sigma Delta Stereo DAC. An output mixer allows to mix this DAC output with a line / aux or microphone input.

A 16-32 Ohms Stereo headphone amplifier with virtual ground output provides a 97dB SNR output for line / headphone loads. The virtual ground output allows to remove 2 space demanding coupling capacitors on board.

On the record side, a multiplexer can select between a main stereo line input and a stereo auxiliary input such as an FM radio. A stereo microphone input with up to 46dB gain is provided. A stereo input mixer allows mixing between line (or aux) and microphone channels before entering a 96dB SNR Stereo Sigma Delta ADC. The digital audio signal is then digitally filtered and transferred to the I<sup>2</sup>S audio interface.

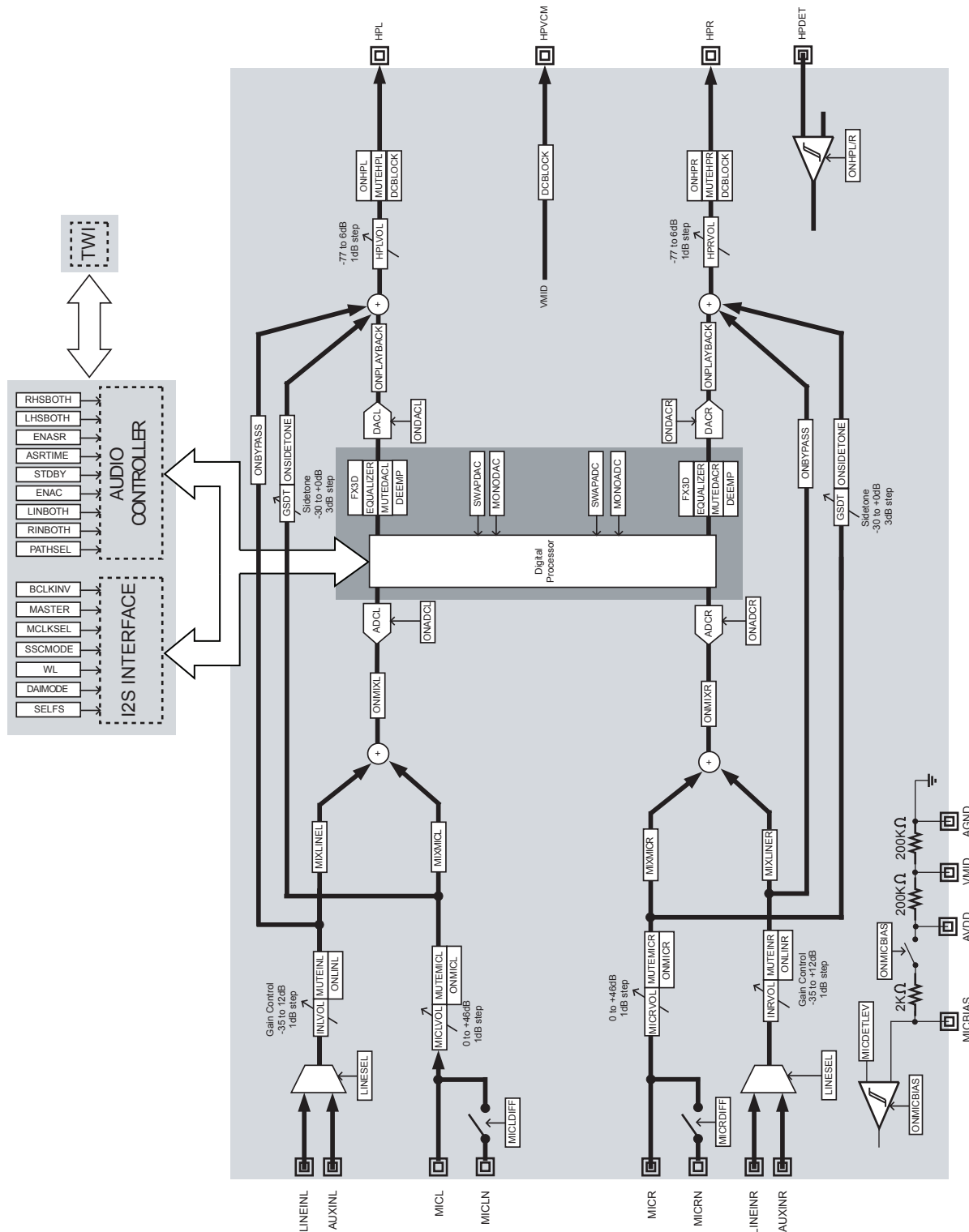
### 12.2 Audio Codec Block Diagram

Figure 12-1. Audio Codec Block Diagram



## 12.3 Audio Codec Controls

Figure 12-2. Audio Codec Controls



## 12.4 Audio Controller

The audio controller sequences the power-up and power-down of the audio codec sub-functions (Mic.amp / ADC / DAC / ...). During these transitioning phases, the controller also manages the gain steps to fade them in and out, thus providing smooth operation.

Depending on the application, two modes are provided:

1. Automatic path control

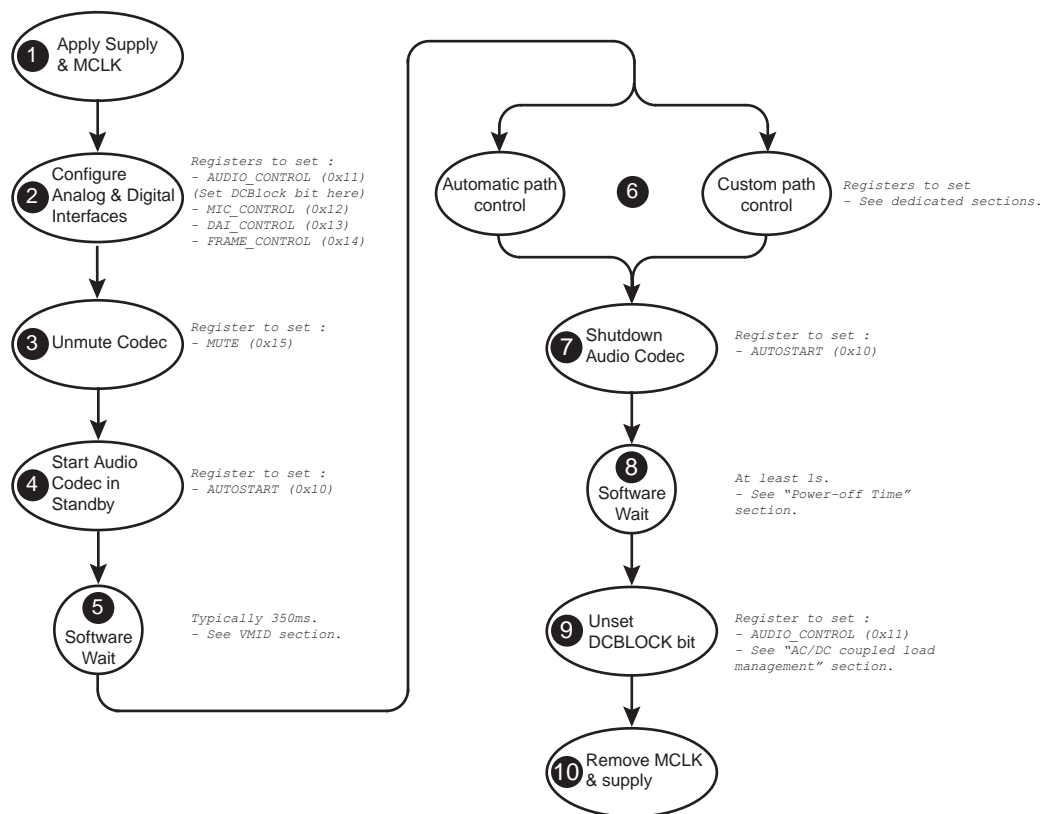
Dedicated to the major audio path scenarios (those described in [Table 13-25 on page 95](#)), this mode enables the whole audio path setup only via "PATHSEL" bits in register AUTOSTART (0x10).

2. Custom path control

Dedicated to audio path scenarios not described in the previously mentioned table, this mode brings the flexibility to start manually the audio sub-functions.

The following figure shows the global context of the audio codec control.

**Figure 12-3.** Audio Codec Typical Control Sequence



## 12.4.1 Audio Codec General Recommendations

### 12.4.1.1 $V_{MID}$

- $V_{MID}$  is the common mode voltage of the audio codec analog core. It is recommended to decouple this voltage with a 1uF capacitor to ensure low noise operation as well as slow (thus silent) transients at codec power up and power down.
- The  $V_{MID}$  capacitor is charged and discharged whenever the ENAC bit is set or cleared. Particularly, placing the audio codec in STANDBY mode does not discharge the  $V_{MID}$  capacitor. The software WAIT operations in the previous diagram (step #5 and step #8 in [“Audio Codec Typical Control Sequence” on page 57](#)) should accommodate  $V_{MID}$ 's settling time constant. See [“Audio Codec Bias” on page 22..](#)

### 12.4.1.2 AC / DC Coupled Load Management

- By default the audio codec is in DC-coupled load configuration: DCBLOCK = 0 in register AUDIO\_CONTROL(0x11). In this case, a virtual ground voltage is provided on pin HPVCM (a buffered version of  $V_{MID}$ ). It allows to directly connect headphones or line loads between HPVCM and HPL(or R) without any coupling capacitors. To prevent any audio pop at start-up or shutdown in this DC coupling mode, the audio codec fastly starts HPL, HPR and HPVCM outputs shorted all together. No software management is required to achieve pop-less operation.
- If output loads are AC coupled to the headphone amplifier, the audio codec DCBLOCK bit must be set and unset as described in [“Audio Codec Typical Control Sequence” on page 57](#). This bit partially controls the two switches S1 and S2 described in the following figure. When DCBLOCK = 1 and the headphone amplifier is OFF, the output coupling capacitors are charged and discharged by the amplifier “VMID\_BUFFER”. In order to achieve silent startup and shutdown, the following rules must be respected:
  - DCBLOCK = 0 at supply power-on and power-off. This ensures that the LDO4 power-on and power-off transients are not transmitted to the audio loads.
  - DCBLOCK = 1 when ENAC = 1. Particularly, DCBLOCK must be set before ENAC=1 and unset after ENAC=0. This ensures that the full VMID waveform is properly buffered to the output loads.
  - DCBLOCK = 1 after ENAC = 0 and until  $V_{MID}$  capacitor is fully discharged. At codec shutdown (ENAC=0), VMID will discharge slowly. The VMID\_BUFFER ensures slow and silent discharge of the output coupling capacitors, and needs S1 and S2 to be closed.

Figure 12-4. AC / DC Coupled Load Management Schematic View

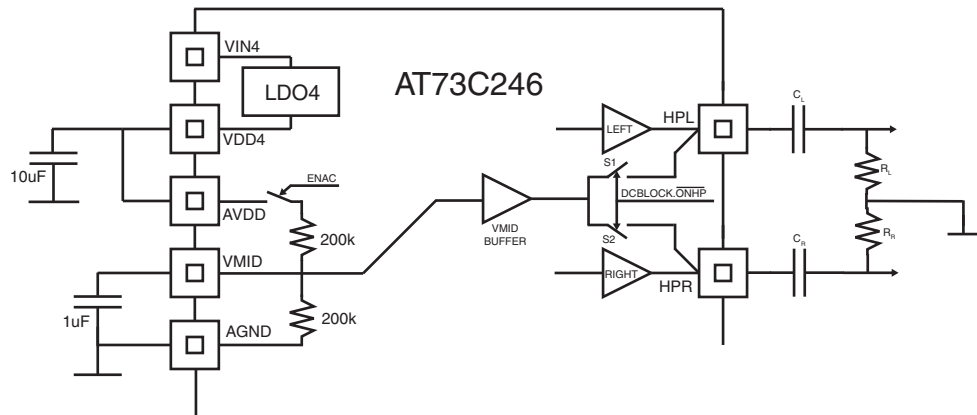
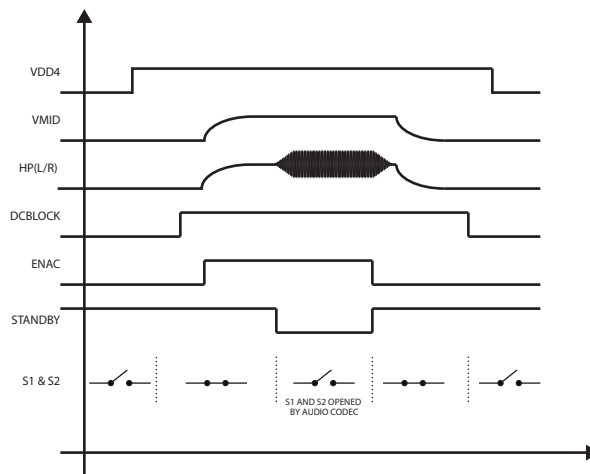


Figure 12-5. Audio Codec Typical Startup and Shutdown Waveforms With AC Coupled Loads.



### 12.4.1.3 MUTE Register

By default, the audio codec starts muted. To enable the audio processing, the MUTE register (0x15) must be cleared. Unmute operation can be performed before or after releasing the STANDBY mode. During operation, this register provides a convenient way of muting the audio signal without changing the various gain registers.

### 12.4.1.4 Master Clock Input (MCLK)

The Audio Controller is clocked by MCLK pin. Therefore a clock must be present at this pin before each codec control change. Particularly, the master clock must be present at power-on, power-off, gain change, path change. The master clock must also be available when fully analog path are used.

### 12.4.1.5 Power-off Conditions

Three audio codec power-off conditions can occur:

- Software request (ENAC = 0 in AUTOSTART register). In this case, the codec is smoothly powered off by the audio controller.
- PMU Power-off event or Standby event (as defined in [Section 11.3 “Power Manager Conditional Transitions” on page 27](#)). In this case, the codec is smoothly powered off with a

500ms timeout. Contrary to the first point, which has no timeout, the audio power-off time limit is here fixed to 500ms. Beyond this limit, the codec is hardly reseted as in the following point.

- PMU Power-fail event. In this case, the PMU finite state machine makes an immediate hard reset of the audio codec to ensure fast shutdown. This case may generate an audible click / pop noise.

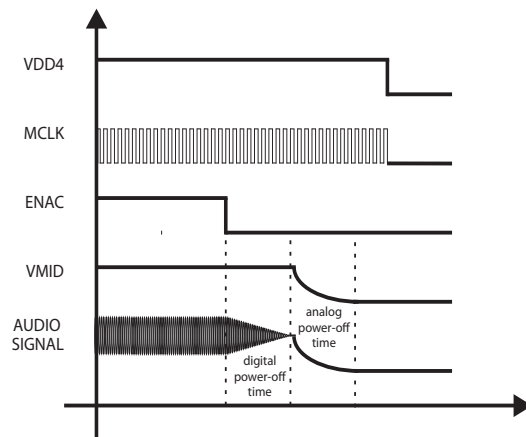
#### 12.4.1.6 Power-off Time

At power-off, the audio controller needs to perform several controls on audio codec sub-functions and to discharge the output coupling capacitors. Therefore, the codec's power-off time is divided into:

- a digital power-off time and,
- an analogue one.

During this power-off phase, the codec's master clock and supply must be present. See "Audio Codec Power-off Waveforms" on page 60.

**Figure 12-6.** Audio Codec Power-off Waveforms



The digital power-off time depends on the number of controls (power-off, gain steps ramping, ...) to perform and for this reason strongly varies according to:

- the master clock frequency,
- the current path,
- the current gains and
- the current Automatic Soft Ramping time (ASR\_TIME in AUDIO\_CONTROL(0x11)).

In worst case conditions (slowest clock, maximum ASR\_TIME, maximum complexity audio path, maximum gains everywhere), the power-off time reaches 3 seconds. During this period, the



master clock must be running to properly shutdown the codec. This time linearly varies with ASR\_TIME value. See [Table 12-1](#)

**Table 12-1.** Audio Codec Maximum Power-off Time

| ASR_TIME | Power-off time (ms) |
|----------|---------------------|
| 00       | 375                 |
| 01       | 750                 |
| 10       | 1500                |
| 11       | 3000                |

The analog power-off time corresponds to the VMID's discharge time specified in ["Audio Codec Bias" on page 22](#):  $T_{MID\_OFF}$ .

Finally, the wait step #8 in ["Audio Codec Typical Control Sequence" on page 57](#) needs to accommodate the digital power-off time + the analog power-off time.

## 12.4.2 Automatic Path Configuration

In this automatic path mode, the audio path control is fully managed by the AUTOSTART(0x10) register and more precisely by the following bits:

- ENAC (Enable Audio codec),
- STANDBY<sup>(1)</sup> (Audio standby) and
- PATHSEL (Audio path selection).

When the audio controller detects a change in these bits, it generates sequential controls to the audio codec sub-functions (power-up, gain ramping, unmute,...) with the right timing and order.

Notes: 1. Audio STANDBY does not refer to the PMU STANDBY state as defined in ["AT73C246 Power Manager Functional State Diagram" on page 25](#). The audio STANDBY mode activated by register AUTOSTART (0x10) only refers to the audio codec controller.

### 12.4.2.1 STANDBY Release

Once the CODEC is started and in standby mode (ENAC=1 and STANDBY=1, step #5 in ["Audio Codec Typical Control Sequence" on page 57](#)), the audio path is simply selected by PATHSEL bits.

At STANDBY release (STANDBY=0), the audio controller will:

- Power-up the requested audio sub-functions. To do so, the audio controller makes WRITE accesses to the registers
  - INPUT\_CONTROL (0x1E),
  - OUTPUT\_CONTROL (0x1F) and
  - INPUT\_MIXER (0x20).
- Ramp-up the concerned path gains from mute to their current register value.

Notes: 1. Changing PATHSEL value with STANDBY=1 does not changes the codec state. It remains in STANDBY mode.  
 2. The audio controller always ensures minimum power consumption by powering only needed sub-functions.  
 3. Audio parameters (volume, mute, effects...) can be modified before or after releasing the standby mode.

#### 12.4.2.2 *Pause Management With STANDBY Bit*

To pause the audio codec activity and reduce power consumption to few hundreds of micro-amps, the STANDBY bit can be activated in register AUTOSTART (0x10). The Audio codec will then:

- Softly ramp down all the path concerned gains down-to mute and
- Power off all the audio sub-functions. The registers INPUT\_CONTROL (0x1E), OUTPUT\_CONTROL (0x1F), and INPUT\_MIXER (0x20) are modified by the audio controller.

Notes: 1. Placing the codec in standby mode maintains the common mode voltage at VMID pin and thus allows to re-start fastly,  
2. Standby release is simply achieved by clearing the STANDBY bit (STANDBY = 0). The procedure described in [“STANDBY Release” on page 61](#) applies.

#### 12.4.2.3 *On-the-fly Path Change*

The audio controller is able to softly switch from one audio path configuration to another without shutting down the codec nor entering the STANDBY mode. As soon as it detects a change in the PATHSEL value, the following mechanism occurs:

- Power up and/or power down of the audio sub-functions according to the final state to reach. This operation generates automatic changes in the registers INPUT\_CONTROL (0x1E), OUTPUT\_CONTROL (0x1F), and INPUT\_MIXER (0x20).
- Ramp up and/or ramp down of the concerned path gain.

Notes: 1. A channel may be temporarily and smoothly switched off and on to reach the new path.  
2. Any software write operation in the registers INPUT\_CONTROL (0x1E), OUTPUT\_CONTROL (0x1F), and INPUT\_MIXER (0x20) will generate a series of control on the audio codec sub-functions. In automatic path control, the order of the write operations in those registers is of prime importance. Please note that changing those registers updates the used audio path without updating the PATHSEL value. Therefore, these write operations are not recommended and must be limited to simple ones (for example changing LINESEL bit in register INPUT\_CONTROL (0x1E) ).

#### 12.4.2.4 *Audio Codec Shutdown*

The Audio controller will start to shutdown the codec if ENAC = 0. The shutdown sequence is made of the following steps:

- Softly ramp down all the path concerned gains down-to mute,
- Power off all the audio sub-functions and,
- Power off the common voltage VMID.

Notes: 1. In this mode, the power consumption is reduced to few hundreds of nA.  
2. The common mode voltage power-off follows VMID time constant and thus may take a few hundreds of milliseconds depending on VMID capacitor. See [“Audio Codec Bias” on page 22](#).

A software example of audio codec control using automatic path control is provided in the section [“Basic Audio Codec Setting Using Automatic Path Control” on page 134](#).

#### 12.4.3 **Custom Path Configuration**

In this custom path mode, the audio path control is managed by the following registers:

- AUTOSTART (0x10) (ENAC and STANDBY bits only)
- AUDIO\_CONTROL (0x11) (ENCONF and CUSTCONF bits only)

- INPUT\_CONTROL (0x1E)
- OUTPUT\_CONTROL (0x1F)
- INPUT\_MIXER (0x20)

Like in the automatic path configuration, the audio controller will sequence audio codec sub-functions ON/OFF as well as gain stepping. However, the audio path is no more selected via the "PATHSEL" value in register AUTOSTART.

To specify a custom audio path:

- The bit CUSTCONF in register AUDIO\_CONTROL (0x11) must be set to '1' to specify the 'custom' path configuration mode.
- The registers INPUT\_CONTROL (0x1E), OUTPUT\_CONTROL (0x1F), and INPUT\_MIXER (0x20) are set to define the audio path,
- The bit ENCONF in register AUDIO\_CONTROL (0x11) is pulsed to '1' to enable the audio controller sequencing.

- Notes:
1. "Pulsed to '1'" means written to '1' and then written to '0'.
  2. In this mode, the STANDBY bit behaves like in the automatic mode. It is possible to place the CODEC in standby mode to reduce power consumption during audio pause by simply setting the STANDBY bit to 1. STANDBY release is achieved by clearing this bit.
  3. On-the-fly path change is achieved by modifying the registers INPUT\_CONTROL (0x1E), OUTPUT\_CONTROL (0x1F), and INPUT\_MIXER (0x20) to define the new audio path configuration and then pulsing to '1' the ENCONF bit. In this case, a channel may be temporarily (and smoothly) switched off and on to reach the new configuration.
  4. Changing the three registers INPUT\_CONTROL (0x1E), OUTPUT\_CONTROL (0x1F), and INPUT\_MIXER (0x20) with the ENCONF bit set to '1' makes the changes to take effect immediately. Therefore, the order of write operations is of prime importance. It is then recommended to write these registers with ENCONF set to 0 and then pulse ENCONF to '1' once the new audio path is fully specified. Knowing the final state to reach, the audio controller is able to sequence the controls with the right order and timings to ensure noise-free operation.
  5. In this custom mode, the Audio Controller may forbid any configuration that does not make sense. For example, it will prevent the headphone amplifier from being switched on if it has no input source (DAC, Microphone, or Line).
  6. It is possible and sometimes convenient to switch from an automatically set path to a custom one. In this case, the audio controller softly performs the required path change. However, activating an automatic path configuration from a current custom path configuration is not allowed. The audio codec must be switched off first (ENAC=0).

A software example of audio codec control using custom path control is provided in the section ["Basic Audio Codec Setting Using Custom Path Control"](#) on page 135.

## 12.5 Audio Codec Power Consumption Versus Programmed Audio Path

Unless otherwise specified:

- $A_{VDD} = 3.3V$
- MCLK = 12.288MHz , FS = 48KHz
- All Gains set to 0dB
- No audio signal
- $T_A = 25^{\circ}C$ .
- Headphone amplifier set in AC coupling mode.

- Current consumptions don't account for load consumption and are measured in  $A_{VDD}$  pin and  $V_{INSYS}$  pin.

**Table 12-2.** Audio PATH Power Consumption

| PATH_SEL | AUDIO PATH                                 | Description  | Consumption |           | Units |
|----------|--|--|-------------|-----------|-------|
|          |  |  | $V_{INSYS}$ | $A_{VDD}$ |       |
| 00000    | No Path                                    |  | 0.10        | 0.61      | mA    |
| 00001    | DAC Playback                               | Digital IN - Headphone OUT                               | 1.80        | 5.2       | mA    |
| 00010    | Mic Sidetone                               | Microphone IN - Headphone OUT                            | 0.10        | 2.65      | mA    |
| 00011    | Aux Bypass                                 | Aux IN - Headphone OUT                                   | 0.10        | 2.65      | mA    |
| 00100    | Line Bypass                                | Line IN - Headphone OUT                                  | 0.10        | 2.65      | mA    |
| 00101    | Mic Record                                 | Mic IN - Digital OUT                                     | 2.00        | 3.40      | mA    |
| 00110    | Aux Record                                 | Aux IN - Digital OUT                                     | 2.00        | 3.40      | mA    |
| 00111    | Line Record                                | Line IN - DIGITAL OUT                                    | 2.00        | 3.40      | mA    |
| 01000    | Mic Sidetone + Record                      | Mic IN - Headphone and Digital OUT                       | 2.00        | 5.05      | mA    |
| 01001    | Aux Bypass + Record                        | Aux IN - Headphone and Digital OUT                       | 2.00        | 5.05      | mA    |
| 01010    | Line Bypass + Record                       | Line IN - Headphone and Digital OUT                      | 2.00        | 5.05      | mA    |
| 01011    | Mic + Aux Record                           | Mic + Aux IN - Digital OUT                               | 2.00        | 3.70      | mA    |
| 01100    | Mic + Line Record                          | Mic + Line IN - Digital OUT                              | 2.00        | 3.70      | mA    |
| 01101    | DAC Playback + Mic Sidetone                | Digital + Mic IN - Headphone OUT                         | 1.80        | 5.60      | mA    |
| 01110    | DAC Playback + Aux Bypass                  | Digital + Aux IN - Headphone OUT                         | 1.80        | 5.60      | mA    |
| 01111    | DAC Playback + Line Bypass                 | Digital + Line IN - Headphone OUT                        | 1.80        | 5.60      | mA    |
| 10000    | DAC Playback + Mic Sidetone + Aux Bypass   | Digital + Mic + Aux IN - Headphone OUT                   | 1.80        | 5.85      | mA    |
| 10001    | DAC Playback + Mic Sidetone + Line Bypass  | Digital + Mic + Line IN - Headphone OUT                  | 1.80        | 5.85      | mA    |
| 10010    | DAC Playback and MIC Record                | Digital IN - Headphone OUT<br>Mic IN - Digital OUT       | 3.80        | 8.00      | mA    |
| 10011    | DAC Playback and Aux Record                | Digital IN - Headphone OUT<br>Aux IN - Digital OUT       | 3.80        | 8.00      | mA    |
| 10100    | DAC Playback and Line Record               | Digital IN - Headphone OUT<br>Line IN - Digital OUT      | 3.80        | 8.00      | mA    |
| 10101    | DAC Playback + Mic Sidetone and Mic Record | Digital + Mic IN - Headphone OUT<br>Mic IN - Digital OUT | 3.80        | 8.00      | mA    |
| 10110    | DAC Playback + Aux Bypass and Aux Record   | Digital + Aux IN - Headphone OUT<br>Aux IN - Digital OUT | 3.80        | 8.00      | mA    |

**Table 12-2.** Audio PATH Power Consumption

| PATH_SEL | AUDIO PATH  | Description  | Consumption        |                  | Units |
|----------|---|--|--------------------|------------------|-------|
|          |   |  | V <sub>INSYS</sub> | A <sub>VDD</sub> |       |
| 10111    | DAC Playback + Line Bypass and Line Record                      | Digital + Line IN - Headphone OUT<br>Line IN - Digital OUT             | 3.80               | 8.00             | mA    |
| 11000    | DAC Playback + Mic Sidetone + Aux Bypass and Mic + Aux Record   | Digital + Mic + Aux IN - Headphone OUT<br>Mic + Aux IN - Digital OUT   | 3.80               | 8.25             | mA    |
| 11001    | DAC Playback + Mic Sidetone + Line Bypass and Mic + Line Record | Digital + Mic + Line IN - Headphone OUT<br>Mic + Line IN - Digital OUT | 3.80               | 8.25             | mA    |

## 12.6 Digital Audio Interface

### 12.6.1 General Description

AT73C246 features a 16 to 24-bit multi-mode master / slave I<sup>2</sup>S port. The following modes are provided:

- I2S,
- Left Justified,
- Right Justified, and
- SSC

The I<sup>2</sup>S port is configured through register I2S\_CONTROL (0x13) and FRAME\_CONTROL (0x14). For each of the listed modes, the data transfer is described in the following sections.

The following table provides authorized MCLK / FS ratios and associated filter types:

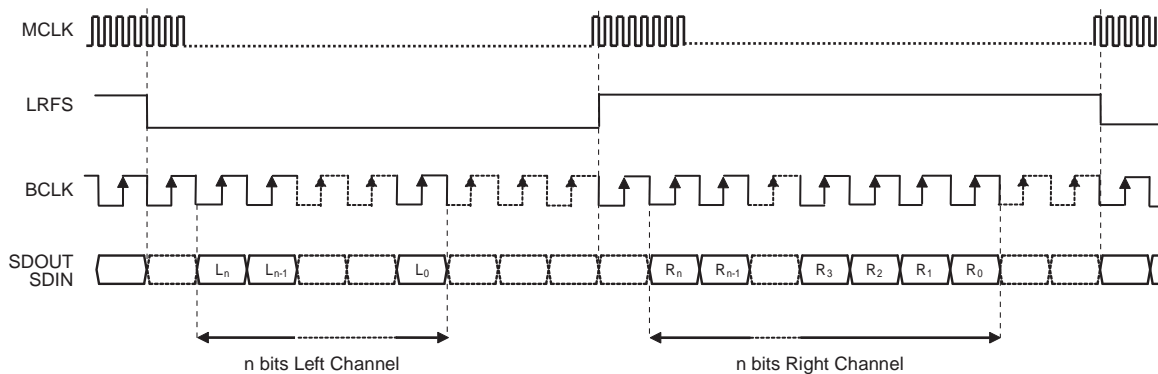
**Table 12-3.** Authorized MCLK / FS Ratios & Filter Types

|           | 12 MHz <sup>(1)</sup> | 12.288 MHz | 18.432 MHz | 11.2896 MHz | 16.9344 MHz |
|-----------|-----------------------|------------|------------|-------------|-------------|
| 8 KHz     | 0                     | 2          | 2          | NA          | NA          |
| 16 KHz    | 0                     | 2          | 2          | NA          | NA          |
| 32 KHz    | 0                     | 2          | 2          | NA          | NA          |
| 48 KHz    | 3                     | 1          | 1          | NA          | NA          |
| 96 KHz    | 4                     | 3          | 3          | NA          | NA          |
| 22.05 KHz | 1                     | NA         | NA         | 1           | 1           |
| 44.1 KHz  | 1                     | NA         | NA         | 1           | 1           |
| 88.2 KHz  | 3                     | NA         | NA         | 3           | 3           |

Note: 1. 12.0000 MHz case is not provided if DAI is configured in Right-Justified and Master mode in DAI\_CONTROL (0x13) and FRAME\_CONTROL registers (0x14).

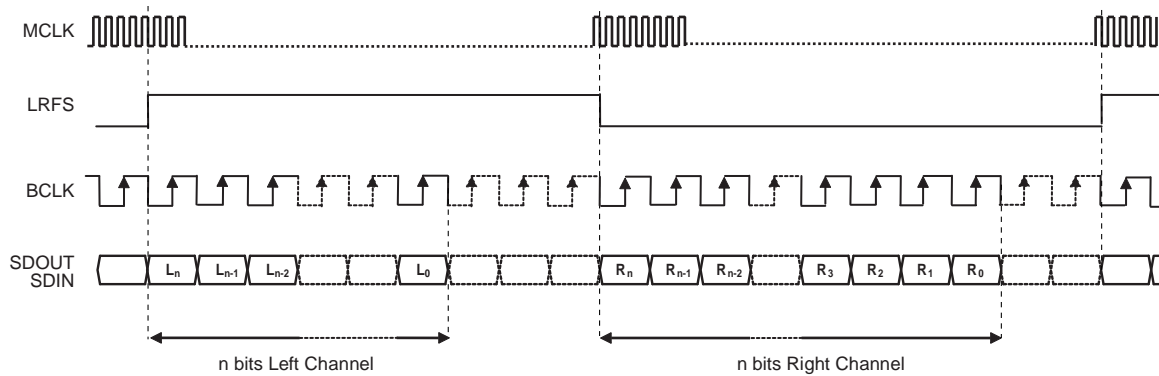
### 12.6.2 Data Transfer: I<sup>2</sup>S MODE

**Figure 12-7.** N-bit I<sup>2</sup>S Mode (FS = 44.1KHz - MCLK = 256 x FS)



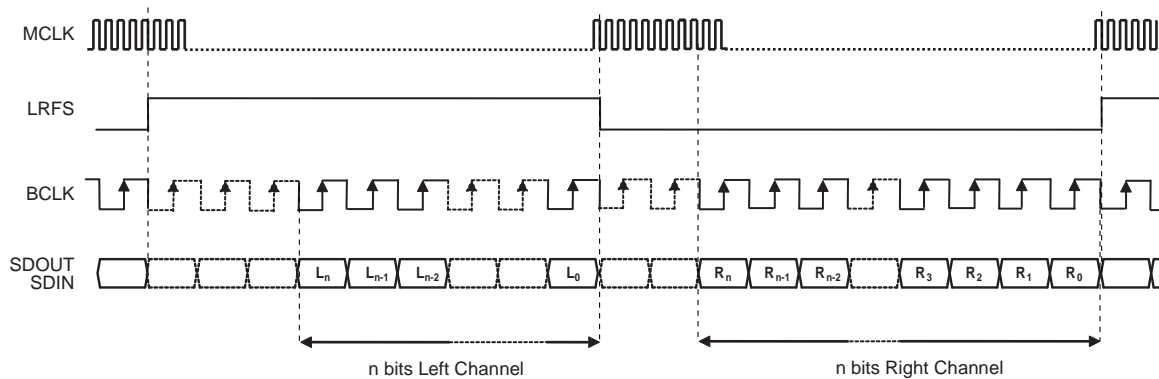
12.6.3 Data Transfer: Left Justified Mode

Figure 12-8. N-bit Left Justified Mode (FS = 44.1KHz - MCLK = 256 x FS)



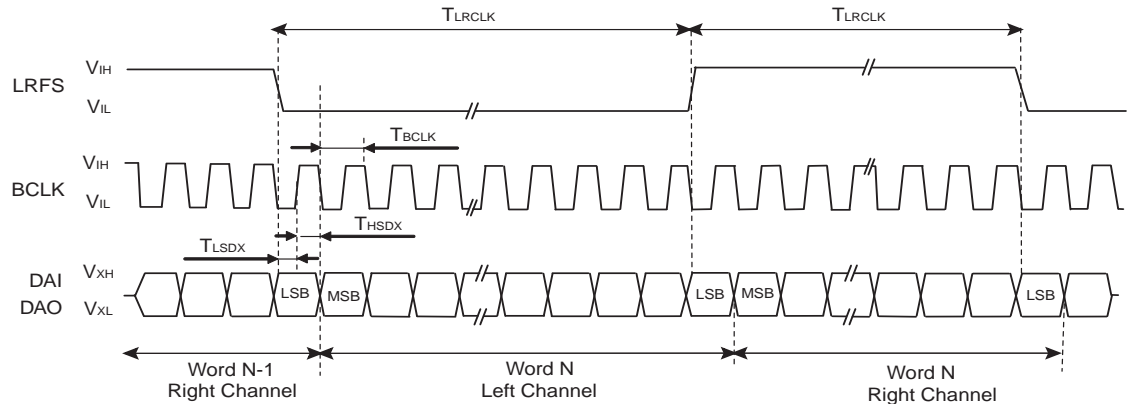
12.6.4 Data Transfer: Right Justified Mode

Figure 12-9. N-bit Right Justified Mode (FS = 44.1KHz - MCLK = 256 x FS)



## 12.6.5 Timing Specifications

**Figure 12-10.** Timing Diagram of data interface (I<sup>2</sup>S Mode)



**Table 12-4.** Digital Audio Interface Timing Specifications

| Parameter   | Symbols     | Min            | Typ                  | Max | Unit |
|---|-------------|----------------|----------------------|-----|------|
| Left/Right Word Cycle Time                            | $T_{LRCLK}$ |                | $1 / (2 \times F_S)$ |     | s    |
| Bit Clock Period                                      | $T_{BCLK}$  | $T_{MCLK} / 2$ |                      |     | s    |
| BCLK Posedge to {DAI, DAO and LRFS} Change Hold Time  | $T_{HSDX}$  | 5              |                      |     | ns   |
| {DAI, DAO and LRFS} Change to BCLK Posedge Setup Time | $T_{LSDX}$  | 5              |                      |     | ns   |

## 12.7 Digital Filters Transfer Function

### 12.7.1 DAC Frequency Response

The following diagrams are referred to  $F_S = 1$  (Sampling Frequency).

**Figure 12-11.** DAC Type 0 Frequency Response

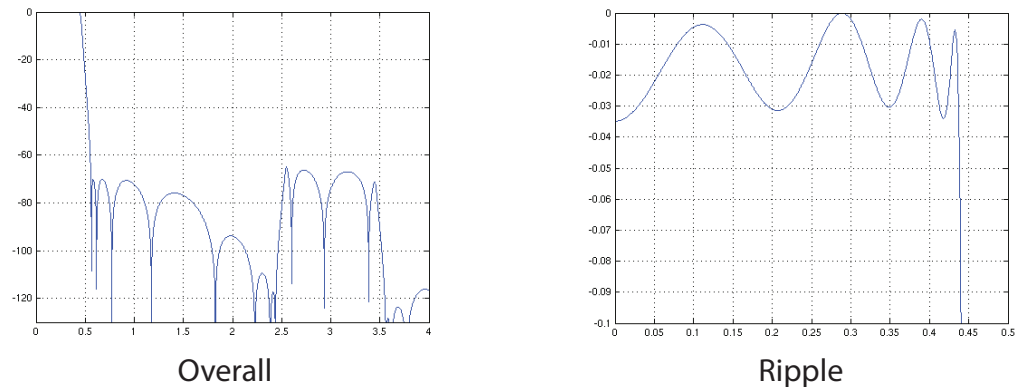
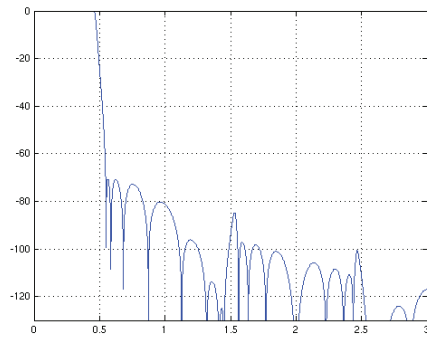
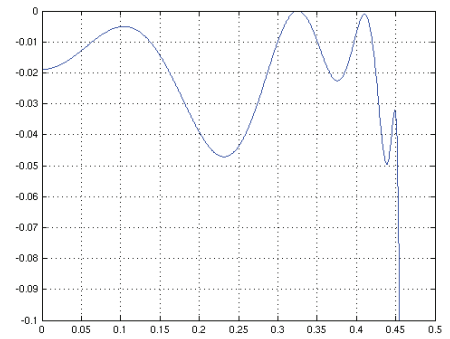




Figure 12-12. DAC Type 1 Frequency Response

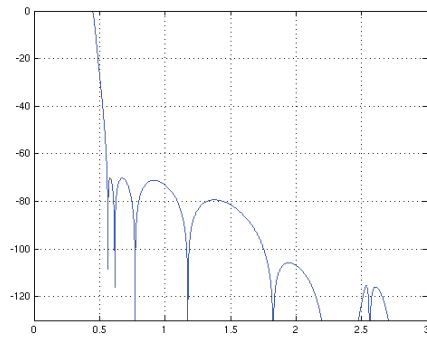


Overall

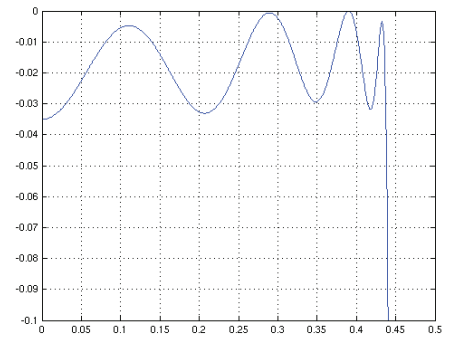


Ripple

Figure 12-13. DAC Type 2 Frequency Response

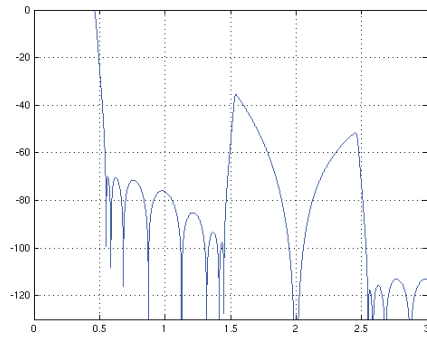


Overall

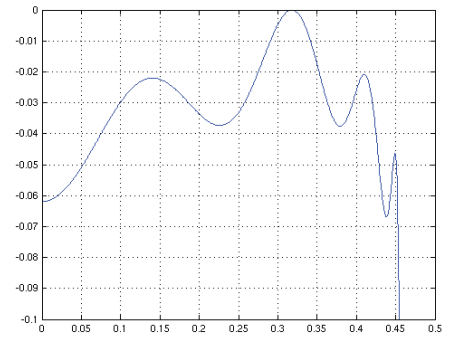


Ripple

Figure 12-14. DAC Type 3 Frequency Response

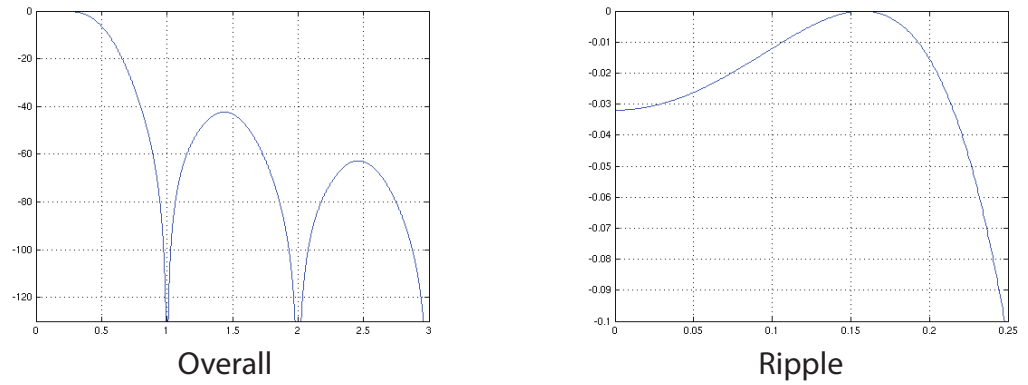


Overall



Ripple

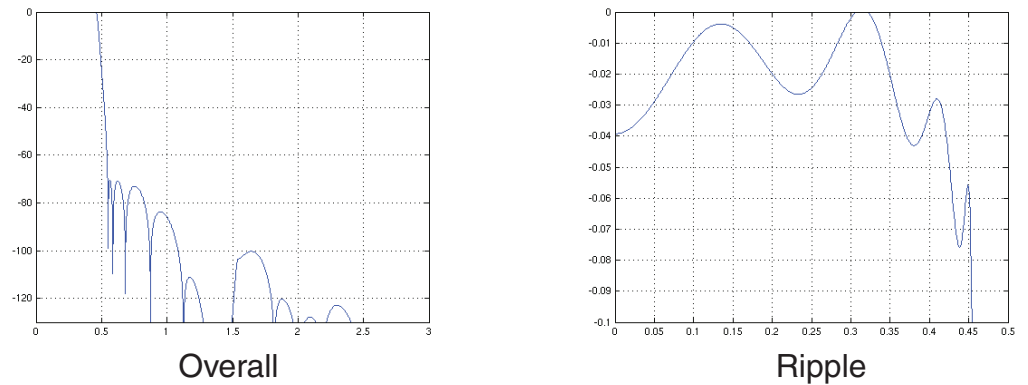
**Figure 12-15. DAC Type 4 Frequency Response**



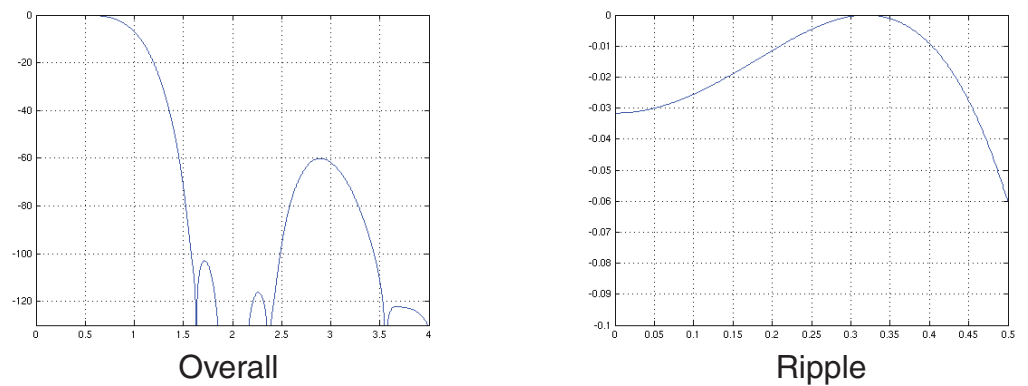
**12.7.2 ADC Frequency Response**

The following diagrams are referred to FS = 1 (Sampling Frequency).

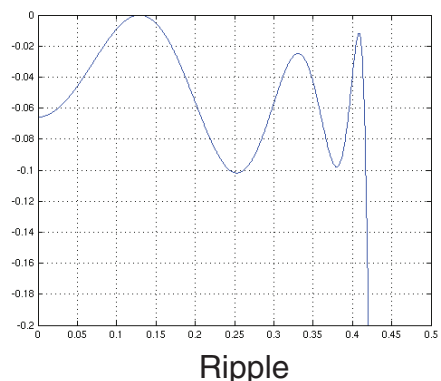
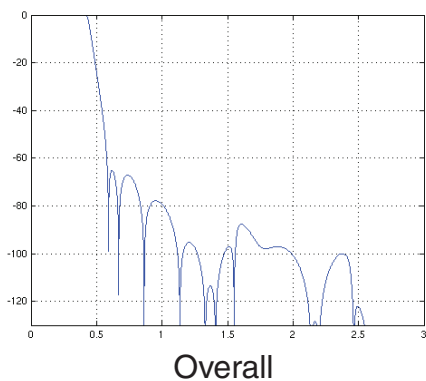
**Figure 12-16. ADC Type 0 Frequency Response**



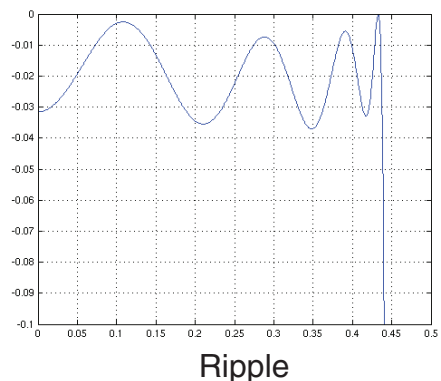
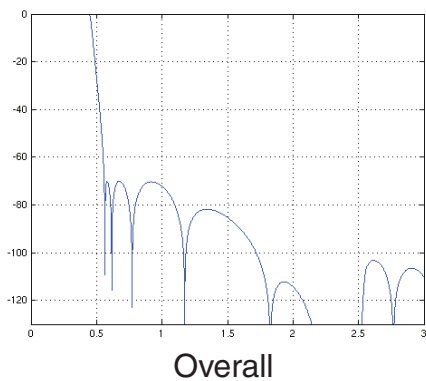
**Figure 12-17. ADC Type 1 Frequency Response**



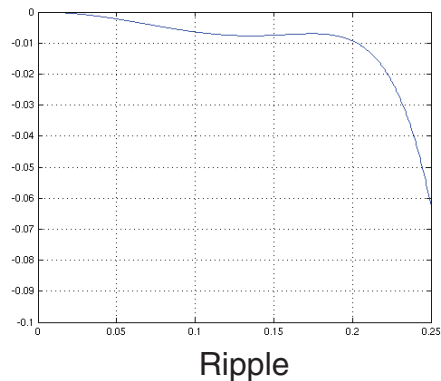
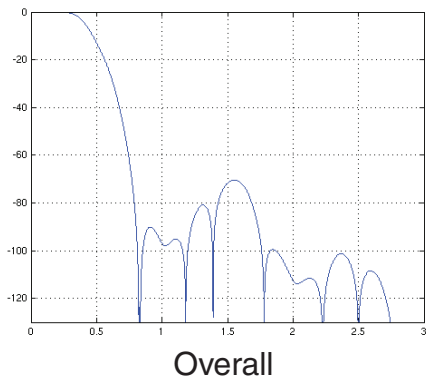
**Figure 12-18. ADC Type 2 Frequency Response**



**Figure 12-19. ADC Type 3 Frequency Response**



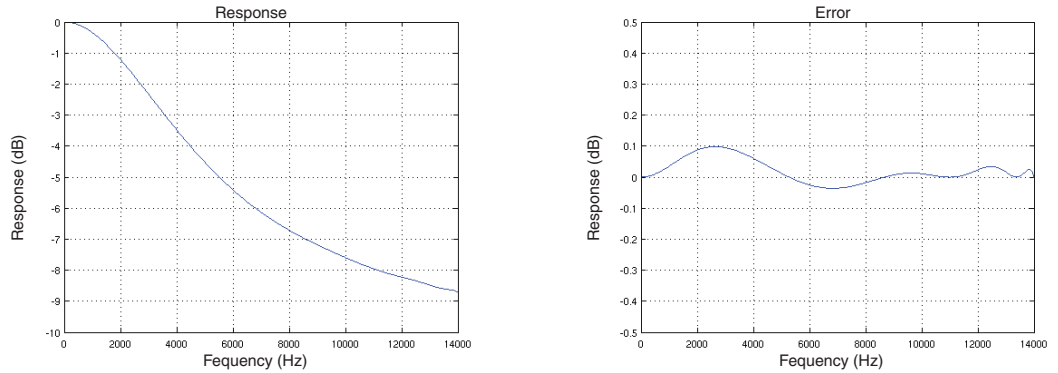
**Figure 12-20. ADC Type 4 Frequency Response**



### 12.7.3 De-Emphasis Filter Frequency Response

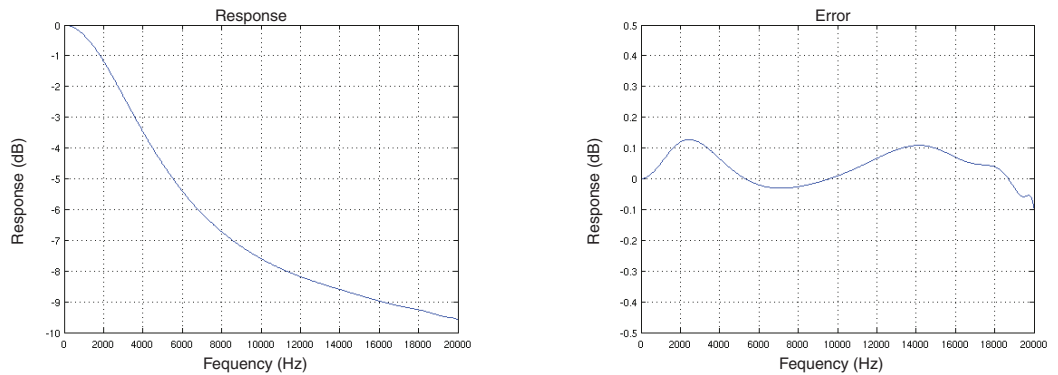
#### 12.7.3.1 De-Emphasis Filter: Frequency Response & Error (FS = 32kHz)

**Figure 12-21.** De-Emphasis Filter: Frequency Response & Error (FS = 32kHz)



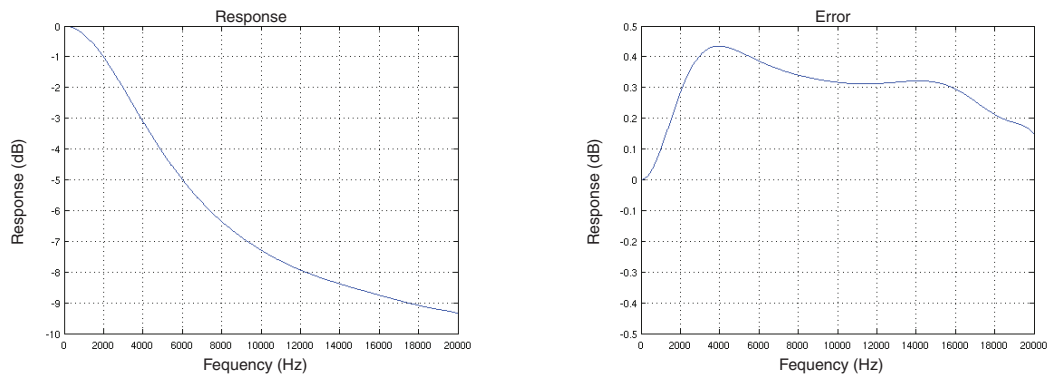
#### 12.7.3.2 De-Emphasis Filter: Frequency Response & Error (FS = 44.1kHz)

**Figure 12-22.** De-Emphasis Filter: Frequency Response & Error (FS = 44.1kHz)



#### 12.7.3.3 De-Emphasis Filter: Frequency Response & Error (FS = 48kHz)

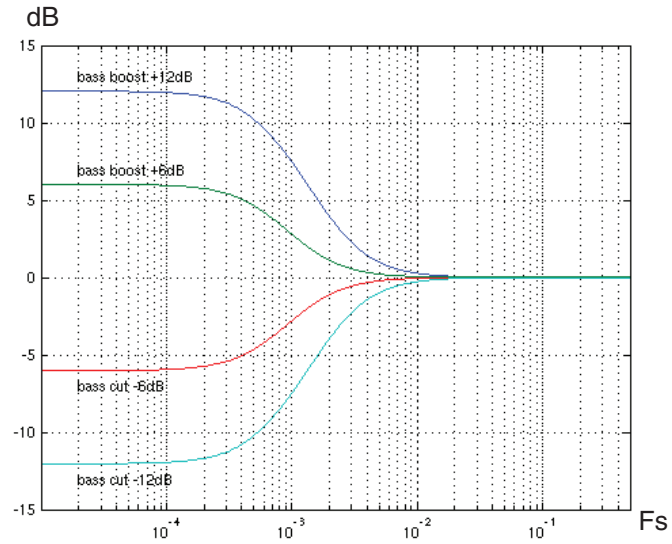
**Figure 12-23.** De-Emphasis Filter: Frequency Response & Error (FS = 48kHz)



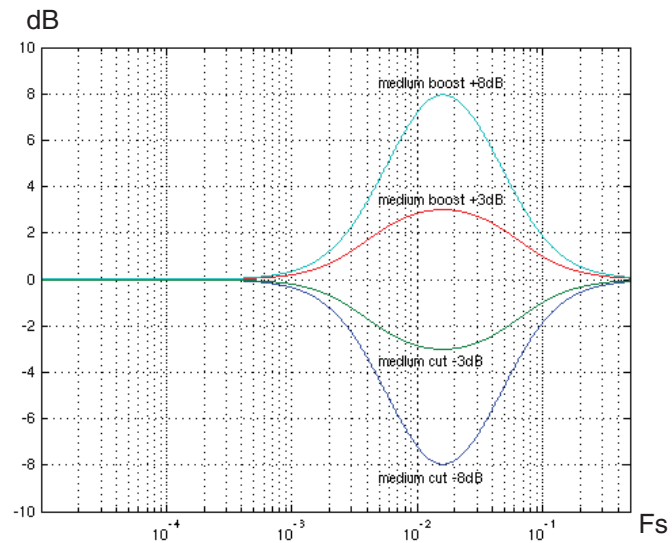
**12.7.4 Equalizer Frequency Response**

The following figures show the frequency response of the equalizer function implemented in the D/A channels.

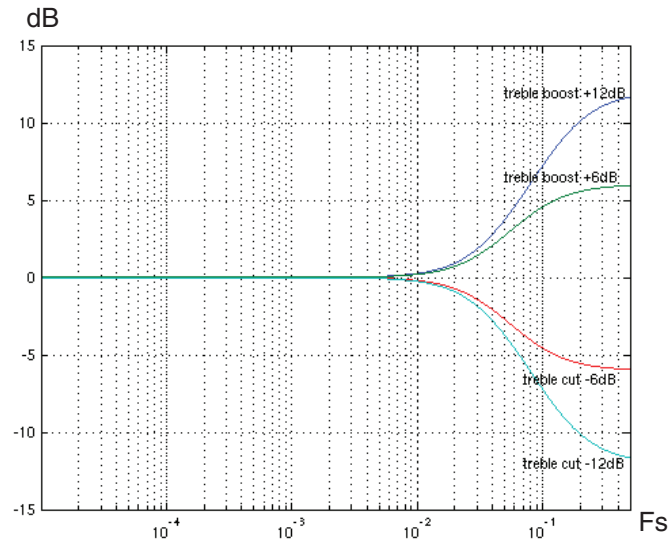
**Figure 12-24. Bass Filters Response**



**Figure 12-25. Medium Filters Response**



**Figure 12-26. Treble Filters Response**



## 12.8 Analog Audio Interfaces

### 12.8.1 Microphone Inputs

The following figures show recommended application circuits for microphone inputs configurations:

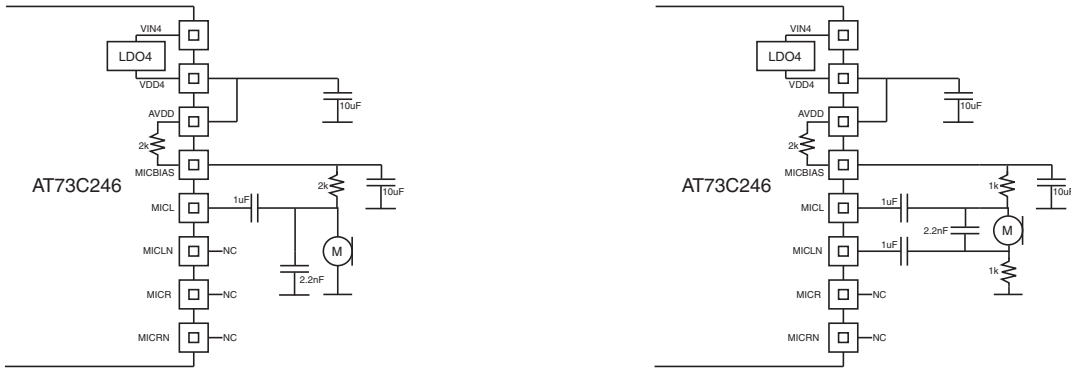
- Mono - single-ended and differential microphone
- Stereo - single ended and differential microphone
- Long-wires microphone

Recommended resistor / capacitor / inductor value may be tuned to the final application, depending on:

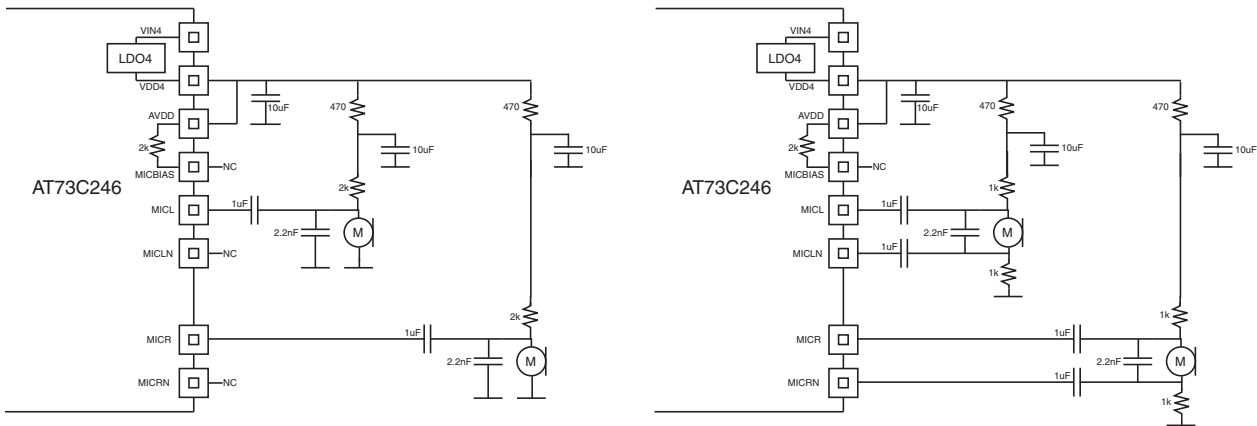
- the microphone specified load resistance,
- the high pass filter desired corner frequency,
- the level and frequency of unwanted signals to be rejected.

Depending also on desired high frequency filtering: common-mode or differential, the differential suggested application diagrams may be modified.

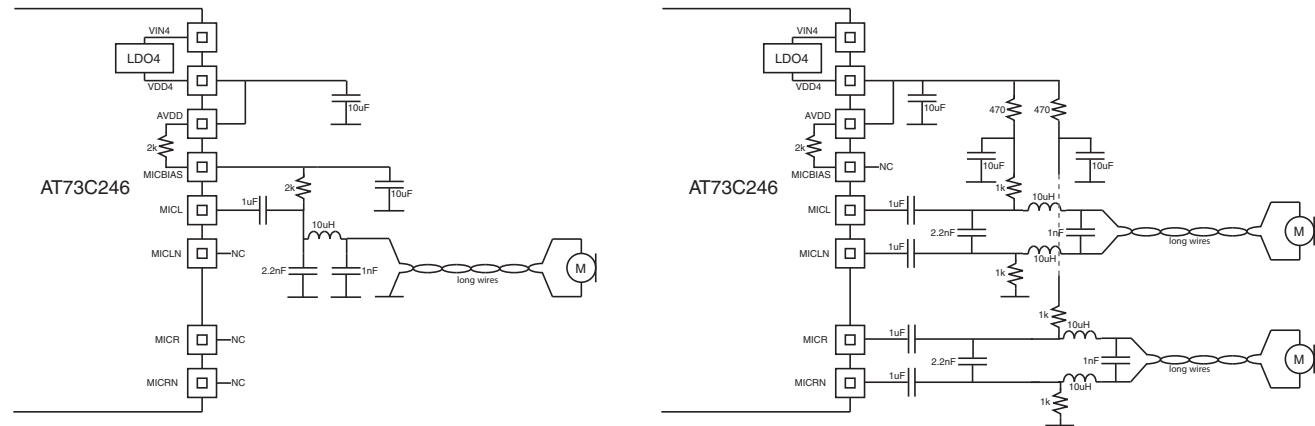
**Figure 12-27. Mono - Single Ended and Differential Microphone Applications**



**Figure 12-28. Stereo - Single Ended and Differential Microphone Applications**

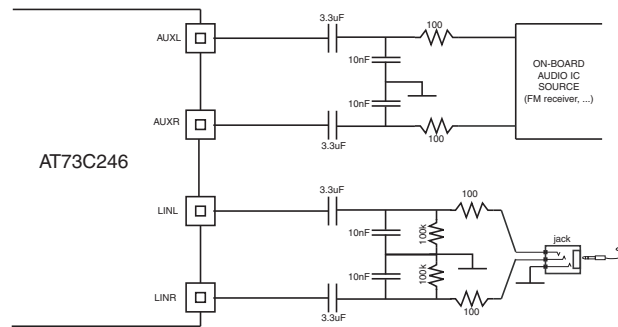


**Figure 12-29. Long Wires Microphone Applications**



### 12.8.2 Aux / Line Inputs

Figure 12-30. Aux and Line Input Application Circuits



### 12.8.3 Line / Headphone Outputs

Figure 12-31. AC Coupled Output Application Circuits

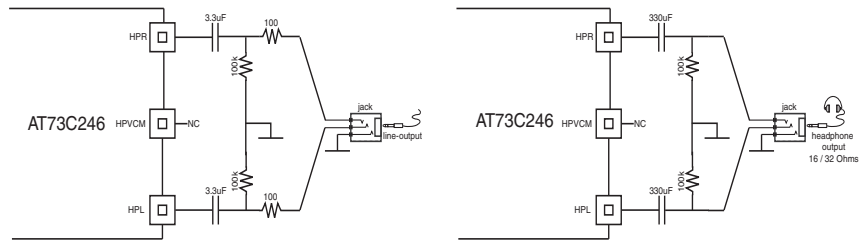
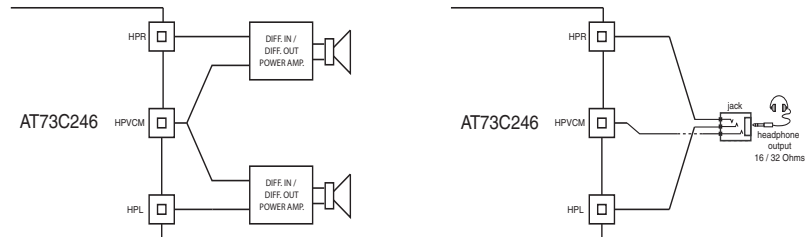


Figure 12-32. DC Coupled (CAPLESS) Application Circuits





## 13. Two Wire Interface and Control Registers

### 13.1 Two-wire Interface (TWI) Protocol

The two-wire interface interconnects components on a unique two-wire bus, made up of one clock line and one data line with speeds up to 400 Kbits per second, based on a byte oriented transfer format. The TWI is slave only and single byte access.

The interface adds flexibility to the power supply solution, enabling LDO regulators to be controlled depending on the instantaneous application requirements.

The AT73C246 has the following 7-bit address: 1001001.

Attempting to read data from register addresses not listed in this section results in 0xFF being read out.

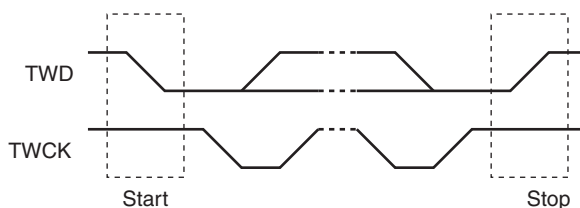
- TWCK is an input pin for the clock
- TWD is an open-drain pin that drives or receives the serial data

The data put on the TWD line must be 8 bits long. Data is transferred MSB first. Each byte must be followed by an acknowledgement.

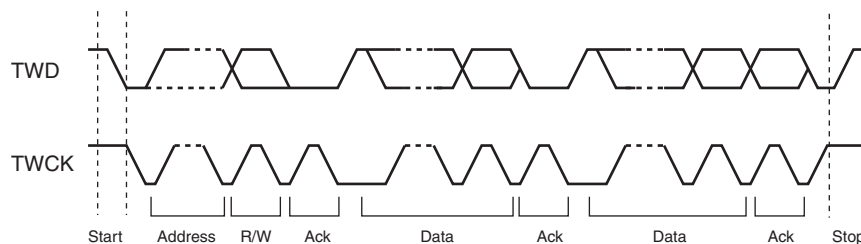
Each transfer begins with a START condition and terminates with a STOP condition.

- A high-to-low transition on TWD while TWCK is high defines a START condition.
- A low-to-high transition on TWD while TWCK is high defines a STOP condition.

**Figure 13-1.** TWI Start/Stop Cycle



**Figure 13-2.** TWI Data Cycle



After the host initiates a Start condition, it sends the 7-bit slave address defined above to notify the slave device. A Read/Write bit follows (Read = 1, Write = 0).

The device acknowledges each received byte.

The first byte sent after device address and R/W bit is the address of the device register the host wants to read or write.

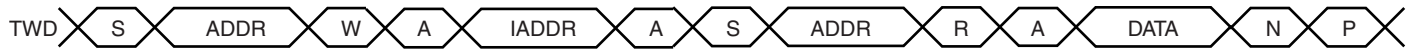
For a write operation the data follows the internal address

For a read operation a repeated Start condition needs to be generated followed by a read on the device.

**Figure 13-3.** TWD Write Operation



**Figure 13-4.** TWD Read Operation



- S = Start
- P = Stop
- W = Write
- R = Read
- A = Acknowledge
- N = Not Acknowledge
- ADDR = Device address
- IADDR = Internal address

## 13.2 PMU Register Tables

### 13.2.1 Register Mapping

Table 13-1. Register Mapping

| Addr | Name                 | 7          | 6          | 5          | 4            | 3        | 2        | 1         | 0         |
|------|----------------------|------------|------------|------------|--------------|----------|----------|-----------|-----------|
| 0x00 | PMU_MODES            | -          | -          | -          | -            | -        | STANDBY  | PWRDOWN   | RUN       |
| 0x01 | PMU_WAKEUP_EVENTS    | -          | -          | RTC        | PWREN        | WAKEUP3  | WAKEUP2  | WAKEUP1   | WAKEUP0   |
| 0x02 | PMU_WAKEUP_TRIG      | -          | -          | RTCR       | PWREN        | WAKEUP3  | WAKEUP2  | WAKEUP1   | WAKEUP0   |
| 0x03 | PMU_STANDBY_SUPPLIES | -          | -          | LP_VDD1    | LP_VDD0      | VDD3     | VDD2     | VDD1      | VDD0      |
| 0x04 | PMU_SUPPLY_CTRL      | -          | -          | IN_PHASE   | DVS_VDD4     | DVS_VDD3 | DVS_VDD2 | DVS_VDD1  | DVS_VDD0  |
| 0x05 | PMU_RST_LEVEL        | RST_VDD3   |            | RST_VDD2   |              | RST_VDD1 |          | RST_VDD0  |           |
| 0x06 | VDD0_CTRL            | ON_VDD0    | LPMODE     | VDD0_SEL   |              |          |          |           |           |
| 0x07 | VDD1_CTRL            | ON_VDD1    | LPMODE     | VDD1_SEL   |              |          |          |           |           |
| 0x08 | VDD2_CTRL            | ON_VDD2    | -          | -          | VDD2_SEL     |          |          |           |           |
| 0x09 | VDD3_CTRL            | ON_VDD3    | -          | -          | VDD3_SEL     |          |          |           |           |
| 0x0A | VDD4_CTRL            | ON_VDD4    | -          | -          | VDD4_SEL     |          |          |           |           |
| 0x0B | PMU_LED              | TON_LED    |            |            | PERIOD_LED   |          |          | BLINK     | ON_LED    |
| 0x0C | PMU_MASK             | -          | -          | -          | -            | -        | -        | RTC_ALARM | RTC_IT    |
| 0x0D | PMU_IT               | -          | -          | -          | -            | -        | -        | RTC_ALARM | RTC_IT    |
| 0x0E | PMU_WAKEUP_SUPPLIES  | -          | -          | -          | -            | VDD0_WUP | VDD1_WUP | VDD2_WUP  | VDD3_WUP  |
| 0x10 | AUTOSTART            | -          | ENAC       | STANDBY    | PATH_SEL     |          |          |           |           |
| 0x11 | AUDIO_CONTROL        | -          | BCLKINV    | DCBLOCK    | ENCONF       | CUSTCONF | ENASR    | ASR_TIME  |           |
| 0x12 | MIC_CONTROL          | -          | -          | MICLDIFF   | MICRDIFF     | MICDET   |          | ONMICBIAS | MICDET_ST |
| 0x13 | DAI_CONTROL          | -          | -          | -          | -            | MASTER   | MCLKSEL  |           |           |
| 0x14 | FRAME_CONTROL        | SSCMODE    | WL         |            | DAIMODE      |          | SELFS    |           |           |
| 0x15 | MUTE                 | MUTEDACL   | MUTEDACR   | MUTEINL    | MUTEINR      | MUTEMICL | MUTEMICR | MUTEHPL   | MUTEHPR   |
| 0x16 | MICLVOL              | -          | -          | MICLVOL    |              |          |          |           |           |
| 0x17 | MICRVOL              | -          | -          | MICRVOL    |              |          |          |           |           |
| 0x18 | INLVOL               | INLBOTH    | INLVOL     |            |              |          |          |           |           |
| 0x19 | INRVOL               | INRBOTH    | INRVOL     |            |              |          |          |           |           |
| 0x1A | HPLVOL               | HPLVOL     |            |            |              |          |          |           |           |
| 0x1B | HPRVOL               | HPRVOL     |            |            |              |          |          |           |           |
| 0x1C | HP_CONTROL           | -          | -          | -          | -            | -        | HPDET_ST | LHPBOTH   | RHPBOTH   |
| 0x1D | AUDIO_EFFECTS        | 3DFX_DEPTH |            | ON3DFX     | SWAP_DAC     | SWAP_ADC | MONO_DAC | MONO_ADC  | ONDEEMP   |
| 0x1E | INPUT_CONTROL        | -          | LINESEL    | ONMICL     | ONMICR       | ONADCL   | ONADCR   | ONLINL    | ONLINR    |
| 0x1F | OUTPUT_CONTROL       | -          | ONSIDETONE | ONPLAYBACK | ONBYPASS     | ONHPL    | ONHPR    | ONDAACL   | ONDACR    |
| 0x20 | INPUT_MIXER          | -          | -          | MIXMICL    | MIXMICR      | MIXLINEL | MIXLINER | ONMIXL    | ONMIXR    |
| 0x21 | SIDETONE_VOL         | -          | -          | -          | SIDETONE_VOL |          |          |           |           |
| 0x22 | EQUALIZER            | -          | -          | -          | -            | EQ_SEL   |          |           |           |
| 0x30 | ADC_CTRL             | ON_ADC     | ON_BUF     | TS         |              |          |          |           |           |
| 0x31 | ADC_MUX_1            | -          | VIN        | -          | VDD4         | VDD3     | VDD2     | VDD1      | VDD0      |
| 0x32 | ADC_MUX_2            | -          | -          | -          | -            | ANA3     | ANA2     | ANA1      | ANA0      |
| 0x33 | ADC_ANA0_MSB         | ADC<9:2>   |            |            |              |          |          |           |           |

**Table 13-1. Register Mapping**

| Addr | Name         | 7             | 6 | 5             | 4 | 3             | 2         | 1             | 0        |  |
|------|--------------|---------------|---|---------------|---|---------------|-----------|---------------|----------|--|
| 0x34 | ADC_ANA0_LSB | -             | - | -             | - | -             | -         | ADC<1:0>      |          |  |
| 0x35 | ADC_ANA1_MSB | ADC<9:2>      |   |               |   |               |           |               |          |  |
| 0x36 | ADC_ANA1_LSB | -             | - | -             | - | -             | -         | ADC<1:0>      |          |  |
| 0x37 | ADC_ANA2_MSB | ADC<9:2>      |   |               |   |               |           |               |          |  |
| 0x38 | ADC_ANA2_LSB | -             | - | -             | - | -             | -         | ADC<1:0>      |          |  |
| 0x39 | ADC_ANA3_MSB | ADC<9:2>      |   |               |   |               |           |               |          |  |
| 0x3A | ADC_ANA3_LSB | -             | - | -             | - | -             | -         | ADC<1:0>      |          |  |
| 0x3B | ADC_VDD0_MSB | ADC<9:2>      |   |               |   |               |           |               |          |  |
| 0x3C | ADC_VDD0_LSB | -             | - | -             | - | -             | -         | ADC<1:0>      |          |  |
| 0x3D | ADC_VDD1_MSB | ADC<9:2>      |   |               |   |               |           |               |          |  |
| 0x3E | ADC_VDD1_LSB | -             | - | -             | - | -             | -         | ADC<1:0>      |          |  |
| 0x3F | ADC_VDD2_MSB | ADC<9:2>      |   |               |   |               |           |               |          |  |
| 0x40 | ADC_VDD2_LSB | -             | - | -             | - | -             | -         | ADC<1:0>      |          |  |
| 0x41 | ADC_VDD3_MSB | ADC<9:2>      |   |               |   |               |           |               |          |  |
| 0x42 | ADC_VDD3_LSB | -             | - | -             | - | -             | -         | ADC<1:0>      |          |  |
| 0x43 | ADC_VDD4_MSB | ADC<9:2>      |   |               |   |               |           |               |          |  |
| 0x44 | ADC_VDD4_LSB | -             | - | -             | - | -             | -         | ADC<1:0>      |          |  |
| 0x47 | ADC_VIN_MSB  | ADC<9:2>      |   |               |   |               |           |               |          |  |
| 0x48 | ADC_VIN_LSB  | -             | - | -             | - | -             | -         | ADC<1:0>      |          |  |
| 0x49 | ADC_ANA_LSB  | ADC_ANA3<1:0> |   | ADC_ANA2<1:0> |   | ADC_ANA1<1:0> |           | ADC_ANA0<1:0> |          |  |
| 0x50 | RTC_CTRL     | -             | - | -             | - | -             | RTC_WRITE | RTC_SEL       | RTC_EN   |  |
| 0x51 | RTC_ADDR     | RTC_ADDR      |   |               |   |               |           |               |          |  |
| 0x52 | RTC_DATA0    | RTC_DATA0     |   |               |   |               |           |               |          |  |
| 0x53 | RTC_DATA1    | RTC_DATA1     |   |               |   |               |           |               |          |  |
| 0x54 | RTC_DATA2    | RTC_DATA2     |   |               |   |               |           |               |          |  |
| 0x55 | RTC_DATA3    | RTC_DATA3     |   |               |   |               |           |               |          |  |
| 0x56 | BACKUP_CTRL  | -             | - | -             | - | OSC_UPDT      | OSC_EN    | OSC_STAT      | RST_BKUP |  |
| 0x7F | VERSION      | SOFTWARE_TAG  |   |               |   | VERSION       |           |               |          |  |

13.2.2 PMU Control

**Name:** PMU\_MODES

**Access:** Read / Write

**Address:** 0x00

|   |   |   |   |   |         |         |     |
|---|---|---|---|---|---------|---------|-----|
| 7 | 6 | 5 | 4 | 3 | 2       | 1       | 0   |
| - | - | - | - | - | STANDBY | PWRDOWN | RUN |

**Table 13-2.** PMU\_MODES (0x00) Structure

| Bit | Name    | Description  | Reset value |
|-----|---------|--|-------------|
| 7:3 | -       | unused   | 00000       |
| 2   | STANDBY | STANDBY request<br>0: Default value.<br>1: STANDBY request. Reset to 0 at STANDBY exit.                  | 0           |
| 1   | PWRDOWN | POWERDOWN request<br>0: Default value.<br>1: POWERDOWN request. Reset to 0 when POWERDOWN state reached. | 0           |
| 0   | RUN     | RUN mode   | 0           |

- Notes:
1. Please refer to [Section 11. "PMU Functional Description" on page 25](#)
  2. 'RUN' bit is read-only. Only 'STANDBY' and 'PWRDOWN' bits can be written

**Name:** PMU\_WAKEUP\_EVENTS

**Access:** Read / Write

**Address:** 0x01

|   |   |     |       |         |         |         |         |
|---|---|-----|-------|---------|---------|---------|---------|
| 7 | 6 | 5   | 4     | 3       | 2       | 1       | 0       |
| - | - | RTC | PWREN | WAKEUP3 | WAKEUP2 | WAKEUP1 | WAKEUP0 |

**Table 13-3.** PMU\_WAKEUP\_EVENTS (0x01) Structure

| Bit | Name    | Description   | Reset value |
|-----|---------|---|-------------|
| 7:6 | -       | unused  | 00          |
| 5   | RTC     | Wake up by RTC alarm input<br>0: disabled<br>1: enabled | 0           |
| 4   | PWREN   | Wake up by PWREN input<br>0: disabled<br>1: enabled     | 0           |
| 3   | WAKEUP3 | Wake up by WAKEUP3 input<br>0: disabled<br>1: enabled   | 0           |
| 2   | WAKEUP2 | Wake up by WAKEUP2 input<br>0: disabled<br>1: enabled   | 0           |
| 1   | WAKEUP1 | Wake up by WAKEUP1 input<br>0: disabled<br>1: enabled   | 0           |
| 0   | WAKEUP0 | Wake up by WAKEUP0 input<br>0: disabled<br>1: enabled   | 1           |

Note: Please refer to [Section 11. "PMU Functional Description" on page 25](#)

**Name:** PMU\_WAKEUP\_TRIG

**Access:** Read Only

**Address:** 0x02

|   |   |      |       |         |         |         |         |
|---|---|------|-------|---------|---------|---------|---------|
| 7 | 6 | 5    | 4     | 3       | 2       | 1       | 0       |
| - | - | RTCR | PWREN | WAKEUP3 | WAKEUP2 | WAKEUP1 | WAKEUP0 |

**Table 13-4.** PMU\_WAKEUP\_TRIG (0x02) Structure

| Bit | Name    | Description                         | Reset value |
|-----|---------|-------------------------------------|-------------|
| 7:6 | -       | unused                              | 00          |
| 5   | RTCR    | WAKEUP_EVENT triggered on RTC alarm | 0           |
| 4   | PWREN   | WAKEUP_EVENT triggered on PWREN     | 0           |
| 3   | WAKEUP3 | WAKEUP_EVENT triggered on WAKEUP3   | 0           |
| 2   | WAKEUP2 | WAKEUP_EVENT triggered on WAKEUP2   | 0           |
| 1   | WAKEUP1 | WAKEUP_EVENT triggered on WAKEUP1   | 0           |
| 0   | WAKEUP0 | WAKEUP_EVENT triggered on WAKEUP0   | 0           |

Note: Please refer to [Section 11. "PMU Functional Description" on page 25](#)

**Name:** PMU\_STANDBY\_SUPPLIES

**Access:** Read / Write

**Address:** 0x03

|   |   |         |         |      |      |      |      |
|---|---|---------|---------|------|------|------|------|
| 7 | 6 | 5       | 4       | 3    | 2    | 1    | 0    |
| - | - | LP_VDD1 | LP_VDD0 | VDD3 | VDD2 | VDD1 | VDD0 |

**Table 13-5.** PMU\_STANDBY\_SUPPLIES (0x03) Structure

| Bit | Name    | Description   | Reset value |
|-----|---------|---|-------------|
| 7:6 | -       | unused  | 00          |
| 5   | LP_VDD1 | VDD1 Low power mode in STANDBY<br>0: Full power (PWM)<br>1: Low power (PFM) | 1           |
| 4   | LP_VDD0 | VDD0 Low power mode in STANDBY<br>0: Full power (PWM)<br>1: Low power (PFM) | 1           |
| 3   | VDD3    | VDD3 in STANDBY state<br>0: OFF<br>1: ON                                    | 1           |
| 2   | VDD2    | VDD2 in STANDBY state<br>0: OFF<br>1: ON                                    | 0           |
| 1   | VDD1    | VDD1 in STANDBY state<br>0: OFF<br>1: ON                                    | 0           |
| 0   | VDD0    | VDD0 in STANDBY state<br>0: OFF<br>1: ON                                    | 1           |



**Name:** PMU\_SUPPLY\_CTRL

**Access:** Read / Write

**Address:** 0x04

|   |   |          |          |          |          |          |          |
|---|---|----------|----------|----------|----------|----------|----------|
| 7 | 6 | 5        | 4        | 3        | 2        | 1        | 0        |
| - | - | IN_PHASE | DVS_VDD4 | DVS_VDD3 | DVS_VDD2 | DVS_VDD1 | DVS_VDD0 |

**Table 13-6.** PMU\_SUPPLY\_CTRL (0x04) Structure

| Bit | Name     | Description   | Reset value |
|-----|----------|---|-------------|
| 7:6 | -        | unused  | 00          |
| 5   | IN_PHASE | DCDC0 and DCDC1 phase operation<br>0: out-of phase<br>1: in-phase | 0           |
| 4   | DVS_VDD4 | DVS function on VDD4<br>0: OFF<br>1: ON                           | 1           |
| 3   | DVS_VDD3 | DVS function on VDD3<br>0: OFF<br>1: ON                           | 1           |
| 2   | DVS_VDD2 | DVS function on VDD2<br>0: OFF<br>1: ON                           | 1           |
| 1   | DVS_VDD1 | DVS function on VDD1<br>0: OFF<br>1: ON                           | 1           |
| 0   | DVS_VDD0 | DVS function on VDD0<br>0: OFF<br>1: ON                           | 1           |

**Name:** PMU\_RST\_LVL

**Access:** Read / Write

**Address:** 0x05

|          |   |          |   |          |   |          |   |
|----------|---|----------|---|----------|---|----------|---|
| 7        | 6 | 5        | 4 | 3        | 2 | 1        | 0 |
| RST_VDD3 |   | RST_VDD2 |   | RST_VDD1 |   | RST_VDD0 |   |

**Table 13-7.** PMU\_RST\_LVL (0x05) Structure

| Bit | Name     | Description       | Reset value |
|-----|----------|-------------------|-------------|
| 7:6 | RST_VDD3 | RST level on VDD3 | 01          |
| 5:4 | RST_VDD2 | RST level on VDD2 | 10          |
| 3:2 | RST_VDD1 | RST level on VDD1 | 10          |
| 1:0 | RST_VDD0 | RST level on VDD0 | 11          |

**Table 13-8.** VDDx Reset Level Selection Table

| RST_VDDx | RST LEVEL   |
|----------|-------------|
| 00       | 0.85 x VDDx |
| 01       | 0.90 x VDDx |
| 10       | 0.92 x VDDx |
| 11       | 0.95 x VDDx |

**Name:** VDD0\_CTRL

**Access:** Read / Write

**Address:** 0x06

|         |        |          |   |   |   |   |   |
|---------|--------|----------|---|---|---|---|---|
| 7       | 6      | 5        | 4 | 3 | 2 | 1 | 0 |
| ON_VDD0 | LPMODE | VDD0_SEL |   |   |   |   |   |

**Table 13-9.** VDD0\_CTRL (0x06) Structure

| Bit | Name     | Description  | Reset value |
|-----|----------|--|-------------|
| 7   | ON_VDD0  | VDD0 ON/OFF<br>0: OFF<br>1: ON                                   | 0           |
| 6   | LPMODE   | VDD0 Low power mode<br>0: Full power (PWM)<br>1: Low power (PFM) | 0           |
| 5:0 | VDD0_SEL | VDD0 voltage selection   | 010101      |

**Table 13-10.** VDD0 Voltage Selection Table

| VDD0_SEL | VDD0 (V) | VDD0_SEL | VDD0 (V) | VDD0_SEL | VDD0 (V) |
|----------|----------|----------|----------|----------|----------|
| 000000   | 0.80     | 010011   | 1.75     | 100110   | 2.70     |
| 000001   | 0.85     | 010100   | 1.80     | 100111   | 2.75     |
| 000010   | 0.90     | 010101   | 1.85     | 101000   | 2.80     |
| 000011   | 0.95     | 010110   | 1.90     | 101001   | 2.85     |
| 000100   | 1.00     | 010111   | 1.95     | 101010   | 2.90     |
| 000101   | 1.05     | 011000   | 2.00     | 101011   | 2.95     |
| 000110   | 1.10     | 011001   | 2.05     | 101100   | 3.00     |
| 000111   | 1.15     | 011010   | 2.10     | 101101   | 3.05     |
| 001000   | 1.20     | 011011   | 2.15     | 101110   | 3.10     |
| 001001   | 1.25     | 011100   | 2.20     | 101111   | 3.15     |
| 001010   | 1.30     | 011101   | 2.25     | 110000   | 3.20     |
| 001011   | 1.35     | 011110   | 2.30     | 110001   | 3.25     |
| 001100   | 1.40     | 011111   | 2.35     | 110010   | 3.30     |
| 001101   | 1.45     | 100000   | 2.40     | 110011   | 3.35     |
| 001110   | 1.50     | 100001   | 2.45     | 110100   | 3.40     |
| 001111   | 1.55     | 100010   | 2.50     | 110101   | 3.45     |
| 010000   | 1.60     | 100011   | 2.55     | 110110   | 3.50     |
| 010001   | 1.65     | 100100   | 2.60     | 110111   | 3.55     |
| 010010   | 1.70     | 100101   | 2.65     | 111000   | 3.60     |

**Name:** VDD1\_CTRL

**Access:** Read / Write

**Address:** 0x07

|         |        |          |   |   |   |   |   |
|---------|--------|----------|---|---|---|---|---|
| 7       | 6      | 5        | 4 | 3 | 2 | 1 | 0 |
| ON_VDD1 | LPMODE | VDD1_SEL |   |   |   |   |   |

**Table 13-11.** VDD1\_CTRL (0x07) Structure

| Bit | Name     | Description  | Reset value |
|-----|----------|--|-------------|
| 7   | ON_VDD1  | VDD1 ON / OFF<br>0: OFF<br>1: ON                                 | 0           |
| 6   | LPMODE   | VDD1 Low power mode<br>0: Full power (PWM)<br>1: Low power (PFM) | 0           |
| 5:0 | VDD1_SEL | VDD1 voltage selection   | 001000      |

**Table 13-12.** VDD1 Voltage Selection Table

| VDD1_SEL | VDD1 (V) | VDD1_SEL | VDD1 (V) | VDD1_SEL | VDD1 (V) |
|----------|----------|----------|----------|----------|----------|
| 000000   | 0.80     | 010011   | 1.75     | 100110   | 2.70     |
| 000001   | 0.85     | 010100   | 1.80     | 100111   | 2.75     |
| 000010   | 0.90     | 010101   | 1.85     | 101000   | 2.80     |
| 000011   | 0.95     | 010110   | 1.90     | 101001   | 2.85     |
| 000100   | 1.00     | 010111   | 1.95     | 101010   | 2.90     |
| 000101   | 1.05     | 011000   | 2.00     | 101011   | 2.95     |
| 000110   | 1.10     | 011001   | 2.05     | 101100   | 3.00     |
| 000111   | 1.15     | 011010   | 2.10     | 101101   | 3.05     |
| 001000   | 1.20     | 011011   | 2.15     | 101110   | 3.10     |
| 001001   | 1.25     | 011100   | 2.20     | 101111   | 3.15     |
| 001010   | 1.30     | 011101   | 2.25     | 110000   | 3.20     |
| 001011   | 1.35     | 011110   | 2.30     | 110001   | 3.25     |
| 001100   | 1.40     | 011111   | 2.35     | 110010   | 3.30     |
| 001101   | 1.45     | 100000   | 2.40     | 110011   | 3.35     |
| 001110   | 1.50     | 100001   | 2.45     | 110100   | 3.40     |
| 001111   | 1.55     | 100010   | 2.50     | 110101   | 3.45     |
| 010000   | 1.60     | 100011   | 2.55     | 110110   | 3.50     |
| 010001   | 1.65     | 100100   | 2.60     | 110111   | 3.55     |
| 010010   | 1.70     | 100101   | 2.65     | 111000   | 3.60     |

**Name:** VDD2\_CTRL

**Access:** Read / Write

**Address:** 0x08

|         |   |   |          |   |   |   |   |
|---------|---|---|----------|---|---|---|---|
| 7       | 6 | 5 | 4        | 3 | 2 | 1 | 0 |
| ON_VDD2 | - | - | VDD2_SEL |   |   |   |   |

**Table 13-13.** VDD2\_CTRL (0x08) Structure

| Bit | Name     | Description                      | Reset value |
|-----|----------|----------------------------------|-------------|
| 7   | ON_VDD2  | VDD2 ON / OFF<br>0: OFF<br>1: ON | 0           |
| 6:5 | -        | unused                           | 00          |
| 4:0 | VDD2_SEL | VDD2 voltage selection           | 00100       |

**Table 13-14.** VDD2 Voltage Selection Table

| VDD2_SEL | VDD2 (V) |
|----------|----------|
| 00000    | 0.80     |
| 00001    | 0.85     |
| 00010    | 0.90     |
| 00011    | 0.95     |
| 00100    | 1.00     |
| 00101    | 1.05     |
| 00110    | 1.10     |
| 00111    | 1.15     |
| 01000    | 1.20     |
| 01001    | 1.25     |
| 01010    | 1.30     |
| 01011    | 1.35     |

**Name:** VDD3\_CTRL

**Access:** Read / Write

**Address:** 0x09

|         |   |   |          |   |   |   |   |
|---------|---|---|----------|---|---|---|---|
| 7       | 6 | 5 | 4        | 3 | 2 | 1 | 0 |
| ON_VDD3 | - | - | VDD3_SEL |   |   |   |   |

**Table 13-15.** VDD3\_CTRL (0x09) Structure

| Bit | Name     | Description                      | Reset value |
|-----|----------|----------------------------------|-------------|
| 7   | ON_VDD3  | VDD3 ON / OFF<br>0: OFF<br>1: ON | 0           |
| 6:5 | -        | unused                           | 00          |
| 4:0 | VDD3_SEL | VDD3 voltage selection           | 01100       |

**Table 13-16.** VDD3 Voltage Selection Table

| VDD3_SEL     | VDD3 (V)    |
|--------------|-------------|
| 00000        | 2.70        |
| 00001        | 2.75        |
| 00010        | 2.80        |
| 00011        | 2.85        |
| 00100        | 2.90        |
| 00101        | 2.95        |
| 00110        | 3.00        |
| 00111        | 3.05        |
| 01000        | 3.10        |
| 01001        | 3.15        |
| 01010        | 3.20        |
| 01011        | 3.25        |
| <b>01100</b> | <b>3.30</b> |
| 01101        | 3.35        |
| 01110        | 3.40        |
| 01111        | 3.45        |
| 10000        | 3.50        |
| 10001        | 3.55        |
| 10010        | 3.60        |

**Name:** VDD4\_CTRL

**Access:** Read / Write

**Address:** 0x0A

|         |   |   |          |   |   |   |   |
|---------|---|---|----------|---|---|---|---|
| 7       | 6 | 5 | 4        | 3 | 2 | 1 | 0 |
| ON_VDD4 | - | - | VDD4_SEL |   |   |   |   |

**Table 13-17.** VDD4\_CTRL (0x0A) Structure

| Bit | Name     | Description                      | Reset value |
|-----|----------|----------------------------------|-------------|
| 7   | ON_VDD4  | VDD4 ON / OFF<br>0: OFF<br>1: ON | 0           |
| 6:5 | -        | unused                           | 00          |
| 4:0 | VDD4_SEL | VDD4 voltage selection           | 01100       |

**Table 13-18.** VDD4 Voltage Selection Table

| VDD4_SEL     | VDD4 (V)    |
|--------------|-------------|
| 00000        | 2.70        |
| 00001        | 2.75        |
| 00010        | 2.80        |
| 00011        | 2.85        |
| 00100        | 2.90        |
| 00101        | 2.95        |
| 00110        | 3.00        |
| 00111        | 3.05        |
| 01000        | 3.10        |
| 01001        | 3.15        |
| 01010        | 3.20        |
| 01011        | 3.25        |
| <b>01100</b> | <b>3.30</b> |
| 01101        | 3.35        |
| 01110        | 3.40        |
| 01111        | 3.45        |
| 10000        | 3.50        |
| 10001        | 3.55        |
| 10010        | 3.60        |

**Name:** PMU\_LED  
**Access:** Read / Write  
**Address:** 0x0B

|         |   |   |            |   |   |       |        |
|---------|---|---|------------|---|---|-------|--------|
| 7       | 6 | 5 | 4          | 3 | 2 | 1     | 0      |
| TON_LED |   |   | PERIOD_LED |   |   | BLINK | ON_LED |

**Table 13-19.** PMU\_LED (0x0B) Structure

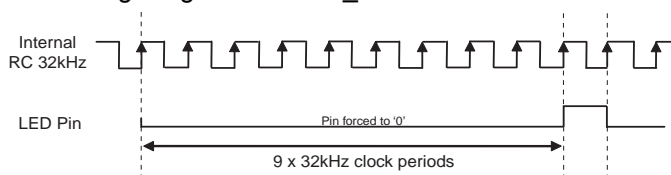
| Bit | Name       | Description                                   | Reset value |
|-----|------------|---|-------------|
| 7:5 | TON_LED    | LED 'ON' time                                 | 000         |
| 4:2 | PERIOD_LED | LED blinking period                           | 010         |
| 1   | BLINK      | Blinking function ON / OFF<br>0: OFF<br>1: ON | 0           |
| 0   | ON_LED     | Led ON / OFF<br>0: OFF<br>1: ON               | 0           |

**Table 13-20.** LED Blinking Function Parameters Selection Table

| TON_LED | LED 'ON' Time (ms) | PERIOD_LED | BLINKING PERIOD (s) |
|---------|--------------------|------------|---------------------|
| 000     | 25                 | 000        | 0.5                 |
| 001     | 50                 | 001        | 1                   |
| 010     | 75                 | 010        | 2                   |
| 011     | 100                | 011        | 3                   |
| 100     | 125                | 100        | 4                   |
| 101     | 150                | 101        | 5                   |
| 110     | 175                | 110        | 6                   |
| 111     | 200                | 111        | 8                   |

**Note:** In case of TON\_LED = 175ms, PERIOD\_LED=5s and BLINK=1 selection, the LED pin is driven according to the following diagram. During 9 clock periods (internal RC 32kHz oscillator) the pin is driven to 0, and during 1 clock period the pin is configured as 'input' with an internal pull up resistor to VINSYS.

**Figure 13-5.** LED Pin Timing Diagram for TON\_LED = 175ms and PERIOD\_LED=5s





**Name:** PMU\_MASK

**Access:** Read / Write

**Address:** 0x0C

|   |   |   |   |   |   |           |        |
|---|---|---|---|---|---|-----------|--------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1         | 0      |
| - | - | - | - | - | - | RTC_ALARM | RTC_IT |

**Table 13-21.** PMU\_MASK (0x0C) Structure

| Bit | Name      | Description                                      | Reset value |
|-----|-----------|--|-------------|
| 7:2 | -         | unused   | 111111      |
| 1   | RTC_ALARM | Mask RTC alarm<br>0: not masked<br>1: masked     | 1           |
| 0   | RTC_IT    | Mask RTC interrupt<br>0: not masked<br>1: masked | 1           |

**Name:** PMU\_IT

**Access:** Read Only

**Address:** 0x0D

|   |   |   |   |   |   |           |        |
|---|---|---|---|---|---|-----------|--------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1         | 0      |
| - | - | - | - | - | - | RTC_ALARM | RTC_IT |

**Table 13-22.** PMU\_IT (0x0D) Structure

| Bit | Name      | Description   | Reset value |
|-----|-----------|---|-------------|
| 7:2 | -         | unused  | 000000      |
| 1   | RTC_ALARM | RTC alarm interrupt<br>0: default value<br>1: RTC alarm has occurred. Reset to 0 at read. | 0           |
| 0   | RTC_IT    | RTC interrupt<br>0: default value<br>1: RTC interrupt has occurred. Reset to 0 at read.   | 0           |

**Name:** PMU\_WAKEUP\_SUPPLIES

**Access:** Read / Write

**Address:** 0x0E

|   |   |   |   |          |          |          |          |
|---|---|---|---|----------|----------|----------|----------|
| 7 | 6 | 5 | 4 | 3        | 2        | 1        | 0        |
| - | - | - | - | VDD0_WUP | VDD1_WUP | VDD2_WUP | VDD3_WUP |

**Table 13-23.** PMU\_WAKEUP\_SUPPLIES (0x0E) Structure

| Bit | Name     | Description   | Reset value |
|-----|----------|---|-------------|
| 7:4 | -        | unused  | 0000        |
| 3   | VDD0_WUP | VDD0 Value at WAKEUP<br>0: Programmed value<br>1: Default value | 1           |
| 2   | VDD1_WUP | VDD1 Value at WAKEUP<br>0: Programmed value<br>1: Default value | 1           |
| 1   | VDD2_WUP | VDD2 Value at WAKEUP<br>0: Programmed value<br>1: Default value | 1           |
| 0   | VDD3_WUP | VDD3 Value at WAKEUP<br>0: Programmed value<br>1: Default value | 1           |

**Name:** AUTOSTART

**Access:** Read / Write

**Address:** 0x10

|   |      |         |          |   |   |   |   |
|---|------|---------|----------|---|---|---|---|
| 7 | 6    | 5       | 4        | 3 | 2 | 1 | 0 |
| - | ENAC | STANDBY | PATH_SEL |   |   |   |   |

**Table 13-24.** AUTOSTART (0x10) Structure

| Bit | Name     | Description   | Reset value |
|-----|----------|---|-------------|
| 7   | -        | unused  | 0           |
| 6   | ENAC     | Audio Codec ON / OFF<br>0: OFF<br>1: ON   | 0           |
| 5   | STANDBY  | Audio STANDBY mode ON / OFF<br>0: Audio codec active<br>1: Audio codec in standby | 1           |
| 4:0 | PATH_SEL | Audio PATH selection  | 00000       |

**Table 13-25.** Audio Path Selection Table

| PATH_SEL | AUDIO PATH                                |  |
|----------|---|--|
| 00000    | No Path                                   |  |
| 00001    | DAC Playback                              | Digital IN - Headphone OUT                         |
| 00010    | Mic Sidetone                              | Microphone IN - Headphone OUT                      |
| 00011    | Aux Bypass                                | Aux IN - Headphone OUT                             |
| 00100    | Line Bypass                               | Line IN - Headphone OUT                            |
| 00101    | Mic Record                                | Mic IN - Digital OUT                               |
| 00110    | Aux Record                                | Aux IN - Digital OUT                               |
| 00111    | Line Record                               | Line IN - DIGITAL OUT                              |
| 01000    | Mic Sidetone + Record                     | Mic IN - Headphone and Digital OUT                 |
| 01001    | Aux Bypass + Record                       | Aux IN - Headphone and Digital OUT                 |
| 01010    | Line Bypass + Record                      | Line IN - Headphone and Digital OUT                |
| 01011    | Mic + Aux Record                          | Mic + Aux IN - Digital OUT                         |
| 01100    | Mic + Line Record                         | Mic + Line IN - Digital OUT                        |
| 01101    | DAC Playback + Mic Sidetone               | Digital + Mic IN - Headphone OUT                   |
| 01110    | DAC Playback + Aux Bypass                 | Digital + Aux IN - Headphone OUT                   |
| 01111    | DAC Playback + Line Bypass                | Digital + Line IN - Headphone OUT                  |
| 10000    | DAC Playback + Mic Sidetone + Aux Bypass  | Digital + Mic + Aux IN - Headphone OUT             |
| 10001    | DAC Playback + Mic Sidetone + Line Bypass | Digital + Mic + Line IN - Headphone OUT            |
| 10010    | DAC Playback and MIC Record               | Digital IN - Headphone OUT<br>Mic IN - Digital OUT |



**Table 13-25. Audio Path Selection Table**

| <b>PATH_SEL</b> | <b>AUDIO PATH</b>   |  |
|-----------------|---|--|
| 10011           | DAC Playback and Aux Record                                     | Digital IN - Headphone OUT<br>Aux IN - Digital OUT                     |
| 10100           | DAC Playback and Line Record                                    | Digital IN - Headphone OUT<br>Line IN - Digital OUT                    |
| 10101           | DAC Playback + Mic Sidetone and Mic Record                      | Digital + Mic IN - Headphone OUT<br>Mic IN - Digital OUT               |
| 10110           | DAC Playback + Aux Bypass and Aux Record                        | Digital + Aux IN - Headphone OUT<br>Aux IN - Digital OUT               |
| 10111           | DAC Playback + Line Bypass and Line Record                      | Digital + Line IN - Headphone OUT<br>Line IN - Digital OUT             |
| 11000           | DAC Playback + Mic Sidetone + Aux Bypass and Mic + Aux Record   | Digital + Mic + Aux IN - Headphone OUT<br>Mic + Aux IN - Digital OUT   |
| 11001           | DAC Playback + Mic Sidetone + Line Bypass and Mic + Line Record | Digital + Mic + Line IN - Headphone OUT<br>Mic + Line IN - Digital OUT |

**Name:** AUDIO\_CONTROL

**Access:** Read / Write

**Address:** 0x11

|   |         |         |        |           |       |          |   |
|---|---------|---------|--------|-----------|-------|----------|---|
| 7 | 6       | 5       | 4      | 3         | 2     | 1        | 0 |
| - | BCLKINV | DCBLOCK | ENCONF | CUST_CONF | ENASR | ASR_TIME |   |

**Table 13-26.** AUDIO\_CONTROL (0x11) Structure

| Bit | Name      | Description   | Reset value |
|-----|-----------|---|-------------|
| 7   | -         | -   | 0           |
| 6   | BLCKINV   | Bit clock inversion on I <sup>2</sup> S port<br>0: not inverted<br>1: inverted                            | 0           |
| 5   | DCBLOCK   | Headphone output coupling configuration<br>0: DC coupled (capless operation)<br>1: AC coupled             | 0           |
| 4   | ENCONF    | Custom configuration enable<br>0: Default value.<br>1: custom configuration is send to audio controller.  | 0           |
| 3   | CUST_CONF | Custom audio configuration<br>0: Audio path are set with PATH_SEL<br>1: Custom audio path set by software | 0           |
| 2   | ENASR     | Gain soft ramping ON / OFF<br>0: OFF<br>1: ON   | 1           |
| 1:0 | ASR_TIME  | Gain soft ramping timing selection  | 11          |

**Table 13-27.** Gain Soft Ramping Timing Selection Table

| ASR_TIME | Timing             |
|----------|--------------------|
| 00       | MCLK / (32 x 512)  |
| 01       | MCLK / (64 x 512)  |
| 10       | MCLK / (128 x 512) |
| 11       | MCLK / (256 x 512) |

**Name:** MIC\_CONTROL

**Access:** Read / Write

**Address:** 0x12

|   |   |          |          |        |   |           |           |
|---|---|----------|----------|--------|---|-----------|-----------|
| 7 | 6 | 5        | 4        | 3      | 2 | 1         | 0         |
| - | - | MICLDIFF | MICRDIFF | MICDET |   | ONMICBIAS | MICDET_ST |

**Table 13-28.** MIC\_CONTROL (0x12) Structure

| Bit | Name      | Description   | Reset value |
|-----|-----------|---|-------------|
| 7:6 | -         | unused  | 00          |
| 5   | MICLDIFF  | Left microphone differential configuration<br>0: Single-ended<br>1: Differential                  | 0           |
| 4   | MICRDIFF  | Right microphone differential configuration<br>0: Single-ended<br>1: Differential                 | 0           |
| 3:2 | MICDET    | Microphone detector threshold   | 00          |
| 1   | ONMICBIAS | Microphone bias generator ON / OFF<br>0: OFF<br>1: ON   | 0           |
| 0   | MICDET_ST | MICBIAS pin microphone detector status bit<br>0: No microphone detected<br>1: Microphone detected | 0           |

**Table 13-29.** Microphone Detector Threshold Selection Table

| MICDET | MICBIAS PIN LEVEL (V) |
|--------|-----------------------|
| 00     | AVDD - 0.1            |
| 01     | AVDD - 0.2            |
| 10     | AVDD - 0.3            |
| 11     | AVDD - 0.4            |

**Name:** DAI\_CONTROL

**Access:** Read / Write

**Address:** 0x13

|   |   |   |   |        |         |   |   |
|---|---|---|---|--------|---------|---|---|
| 7 | 6 | 5 | 4 | 3      | 2       | 1 | 0 |
| - | - | - | - | MASTER | MCLKSEL |   |   |

**Table 13-30.** DAI\_CONTROL (0x13) Structure

| Bit | Name                  | Description  | Reset value |
|-----|-----------------------|--|-------------|
| 7:4 | -                     | unused   | 0000        |
| 3   | MASTER <sup>(1)</sup> | MASTER / <b>SLAVE</b> operation on DAI port<br>0: Slave<br>1: Master | <b>0</b>    |
| 2:0 | MCLKSEL               | Audio Master clock frequency selection                               | <b>001</b>  |

Note: 1. The MASTER mode is not provided for 12.0000 MHz clock case and Right-Justified mode on DAI.

**Table 13-31.** Audio Master Clock Selection Table

| MCLKSEL | MCLK (MHz)    | MCLKSEL | MCLK (MHz) |
|---------|---------------|---------|------------|
| 000     | 12.000        | 100     | 16.9344    |
| 001     | <b>12.288</b> | 101     | -          |
| 010     | 11.2896       | 110     | -          |
| 011     | 18.432        | 111     | -          |

**Name:** FRAME\_CONTROL

**Access:** Read / Write

**Address:** 0x14

|         |    |   |          |   |       |   |   |
|---------|----|---|----------|---|-------|---|---|
| 7       | 6  | 5 | 4        | 3 | 2     | 1 | 0 |
| SSCMODE | WL |   | DAI_MODE |   | SELFS |   |   |

**Table 13-32.** FRAME\_CONTROL (0x14) Structure

| Bit | Name     | Description  | Reset value |
|-----|----------|--|-------------|
| 7   | SSCMODE  | SSC mode for DAI<br>0: DAI according to DAI_MODE bits<br>1: SSC mode | 0           |
| 6:5 | WL       | Word length selection  | <b>11</b>   |
| 4:3 | DAI_MODE | Digital Audio Interface mode control                                 | 00          |
| 2:0 | SELFS    | Audio Frame frequency selection                                      | <b>011</b>  |

**Table 13-33.** Digital Audio Interface Word Length Selection Table

| WL | MODE      |
|----|-----------|
| 00 | 16        |
| 01 | 18        |
| 10 | 20        |
| 11 | <b>24</b> |

**Table 13-34.** Digital Audio Interface Mode Selection Table

| DAIMODE | MODE                           |
|---------|--------------------------------|
| 00      | <b>I2S</b>                     |
| 01      | Left-Justified                 |
| 10      | Right-Justified <sup>(1)</sup> |
| 11      | N/A                            |

Note: 1. The Right-Justified mode is not provided for 12.0000 MHz clock case and MASTER mode on DAI.

**Table 13-35.** Audio Sampling Frequency Selection Table

| SELFS | FS (kHz)  | SELFS | FS (kHz) |
|-------|-----------|-------|----------|
| 000   | 8         | 100   | 96       |
| 001   | 16        | 101   | 22.050   |
| 010   | 32        | 110   | 44.100   |
| 011   | <b>48</b> | 111   | 88.200   |



**Name:** MUTE  
**Access:** Read / Write  
**Address:** 0x15

|          |          |         |         |          |          |         |         |
|----------|----------|---------|---------|----------|----------|---------|---------|
| 7        | 6        | 5       | 4       | 3        | 2        | 1       | 0       |
| MUTEDACL | MUTEDACR | MUTEINL | MUTEINR | MUTEMICL | MUTEMICR | MUTEHPL | MUTEHPR |

**Table 13-36.** MUTE (0x15) Structure

| Bit | Name     | Description                                    | Reset value |
|-----|----------|--|-------------|
| 7   | MUTEDACL | DAC Left mute<br>0: active<br>1: muted         | 1           |
| 6   | MUTEDACR | DACR Right mute<br>0: active<br>1: muted       | 1           |
| 5   | MUTEINL  | AUX / LINE Left mute<br>0: active<br>1: muted  | 1           |
| 4   | MUTEINR  | AUX / LINE Right mute<br>0: active<br>1: muted | 1           |
| 3   | MUTEMICL | MIC Left mute<br>0: active<br>1: muted         | 1           |
| 2   | MUTEMICR | MIC Right mute<br>0: active<br>1: muted        | 1           |
| 1   | MUTEHPL  | Headphone Left mute<br>0: active<br>1: muted   | 1           |
| 0   | MUTEHPR  | Headphone Right mute<br>0: active<br>1: muted  | 1           |

**Name:** MICLVOL  
**Access:** Read / Write  
**Address:** 0x16

|   |   |         |   |   |   |   |   |
|---|---|---------|---|---|---|---|---|
| 7 | 6 | 5       | 4 | 3 | 2 | 1 | 0 |
| - | - | MICLVOL |   |   |   |   |   |

**Table 13-37.** MICLVOL (0x16) Structure

| Bit | Name    | Description                      | Reset value |
|-----|---------|----------------------------------|-------------|
| 7:6 | -       | unused                           | 00          |
| 5:0 | MICLVOL | Microphone Left volume selection | 000000      |

**Table 13-38.** Microphone Left Volume Selection Table

| MICLVOL | GAIN(dB) | MICLVOL | GAIN(dB) | MICLVOL      | GAIN(dB) |
|---------|----------|---------|----------|--------------|----------|
| 000000  | 0        | 010000  | 16       | 100000       | 32       |
| 000001  | 1        | 010001  | 17       | 100001       | 33       |
| 000010  | 2        | 010010  | 18       | 100010       | 34       |
| 000011  | 3        | 010011  | 19       | 100011       | 35       |
| 000100  | 4        | 010100  | 20       | 100100       | 36       |
| 000101  | 5        | 010101  | 21       | 100101       | 37       |
| 000110  | 6        | 010110  | 22       | 100110       | 38       |
| 000111  | 7        | 010111  | 23       | 100111       | 39       |
| 001000  | 8        | 011000  | 24       | 101000       | 40       |
| 001001  | 9        | 011001  | 25       | 101001       | 41       |
| 001010  | 10       | 011010  | 26       | 101010       | 42       |
| 001011  | 11       | 011011  | 27       | 101011       | 43       |
| 001100  | 12       | 011100  | 28       | 101100       | 44       |
| 001101  | 13       | 011101  | 29       | 101101       | 45       |
| 001110  | 14       | 011110  | 30       | 101110       | 46       |
| 001111  | 15       | 011111  | 31       | Other values | 46       |

**Name:** MICRVOL  
**Access:** Read / Write  
**Address:** 0x17

|   |   |         |   |   |   |   |   |
|---|---|---------|---|---|---|---|---|
| 7 | 6 | 5       | 4 | 3 | 2 | 1 | 0 |
| - | - | MICRVOL |   |   |   |   |   |

**Table 13-39.** MICRVOL (0x17) Structure

| Bit | Name    | Description                       | Reset value |
|-----|---------|-----------------------------------|-------------|
| 7:6 | -       | unused                            | 0           |
| 5:0 | MICRVOL | Microphone Right volume selection | 000000      |

**Table 13-40.** Microphone Right Volume Selection Table

| MICRVOL | GAIN(dB) | MICRVOL | GAIN(dB) | MICRVOL      | GAIN(dB) |
|---------|----------|---------|----------|--------------|----------|
| 000000  | 0        | 010000  | 16       | 100000       | 32       |
| 000001  | 1        | 010001  | 17       | 100001       | 33       |
| 000010  | 2        | 010010  | 18       | 100010       | 34       |
| 000011  | 3        | 010011  | 19       | 100011       | 35       |
| 000100  | 4        | 010100  | 20       | 100100       | 36       |
| 000101  | 5        | 010101  | 21       | 100101       | 37       |
| 000110  | 6        | 010110  | 22       | 100110       | 38       |
| 000111  | 7        | 010111  | 23       | 100111       | 39       |
| 001000  | 8        | 011000  | 24       | 101000       | 40       |
| 001001  | 9        | 011001  | 25       | 101001       | 41       |
| 001010  | 10       | 011010  | 26       | 101010       | 42       |
| 001011  | 11       | 011011  | 27       | 101011       | 43       |
| 001100  | 12       | 011100  | 28       | 101100       | 44       |
| 001101  | 13       | 011101  | 29       | 101101       | 45       |
| 001110  | 14       | 011110  | 30       | 101110       | 46       |
| 001111  | 15       | 011111  | 31       | Other values | 46       |

**Name:** INLVOL  
**Access:** Read / Write  
**Address:** 0x18

|         |   |        |   |   |   |   |   |
|---------|---|--------|---|---|---|---|---|
| 7       | 6 | 5      | 4 | 3 | 2 | 1 | 0 |
| INLBOTH |   | INLVOL |   |   |   |   |   |

**Table 13-41.** INLVOL (0x18) Structure

| Bit | Name    | Description   | Reset value |
|-----|---------|---|-------------|
| 7   | INLBOTH | AUX / LINE Left volume controls Right channel<br>0: inactive<br>1: active. Priority bit over INRBOTH. | 1           |
| 6:0 | INLVOL  | AUX / LINE input Left volume selection  | 0000000     |

**Table 13-42.** AUX / LINE Left Volume Selection Table

| INLVOL   | GAIN(dB) | INLVOL  | GAIN(dB) | INLVOL   | GAIN(dB) |
|----------|----------|---------|----------|----------|----------|
| ≤1011100 | MUTE     | 1101101 | -19      | 1111110  | -2       |
| 1011101  | -35      | 1101110 | -18      | 1111111  | -1       |
| 1011110  | -34      | 1101111 | -17      | 0000000  | 0        |
| 1011111  | -33      | 1110000 | -16      | 0000001  | 1        |
| 1100000  | -32      | 1110001 | -15      | 0000010  | 2        |
| 1100001  | -31      | 1110010 | -14      | 0000011  | 3        |
| 1100010  | -30      | 1110011 | -13      | 0000100  | 4        |
| 1100011  | -29      | 1110100 | -12      | 0000101  | 5        |
| 1100100  | -28      | 1110101 | -11      | 0000110  | 6        |
| 1100101  | -27      | 1110110 | -10      | 0000111  | 7        |
| 1100110  | -26      | 1110111 | -9       | 0001000  | 8        |
| 1100111  | -25      | 1111000 | -8       | 0001001  | 9        |
| 1101000  | -24      | 1111001 | -7       | 0001010  | 10       |
| 1101001  | -23      | 1111010 | -6       | 0001011  | 11       |
| 1101010  | -22      | 1111011 | -5       | ≥0101111 | 12       |
| 1101011  | -21      | 1111100 | -4       |          |          |
| 1101100  | -20      | 1111101 | -3       |          |          |

**Name:** INRVOL  
**Access:** Read / Write  
**Address:** 0x19

|         |   |        |   |   |   |   |   |
|---------|---|--------|---|---|---|---|---|
| 7       | 6 | 5      | 4 | 3 | 2 | 1 | 0 |
| INRBOTH |   | INRVOL |   |   |   |   |   |

**Table 13-43.** INRVOL (0x19) Structure

| Bit | Name    | Description  | Reset value |
|-----|---------|--|-------------|
| 7   | INRBOTH | AUX / LINE Right volume controls left channel<br>0: inactive<br>1: active. | 0           |
| 6:0 | INRVOL  | AUX / LINE input Right volume selection                                    | 0000000     |

**Table 13-44.** AUX / LINE Right Volume Selection Table

| INLVOL   | GAIN(dB)    | INLVOL  | GAIN(dB) | INLVOL   | GAIN(dB) |
|----------|-------------|---------|----------|----------|----------|
| ≤1011100 | <b>MUTE</b> | 1101101 | -19      | 1111110  | -2       |
| 1011101  | -35         | 1101110 | -18      | 1111111  | -1       |
| 1011110  | -34         | 1101111 | -17      | 0000000  | 0        |
| 1011111  | -33         | 1110000 | -16      | 0000001  | 1        |
| 1100000  | -32         | 1110001 | -15      | 0000010  | 2        |
| 1100001  | -31         | 1110010 | -14      | 0000011  | 3        |
| 1100010  | -30         | 1110011 | -13      | 0000100  | 4        |
| 1100011  | -29         | 1110100 | -12      | 0000101  | 5        |
| 1100100  | -28         | 1110101 | -11      | 0000110  | 6        |
| 1100101  | -27         | 1110110 | -10      | 0000111  | 7        |
| 1100110  | -26         | 1110111 | -9       | 0001000  | 8        |
| 1100111  | -25         | 1111000 | -8       | 0001001  | 9        |
| 1101000  | -24         | 1111001 | -7       | 0001010  | 10       |
| 1101001  | -23         | 1111010 | -6       | 0001011  | 11       |
| 1101010  | -22         | 1111011 | -5       | ≥0101111 | 12       |
| 1101011  | -21         | 1111100 | -4       |          |          |
| 1101100  | -20         | 1111101 | -3       |          |          |

**Name:** HPLVOL  
**Access:** Read / Write  
**Address:** 0x1A

|        |   |   |   |   |   |   |   |
|--------|---|---|---|---|---|---|---|
| 7      | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| HPLVOL |   |   |   |   |   |   |   |

**Table 13-45.** HPLVOL (0x1A) Structure

| Bit | Name   | Description                     | Reset value |
|-----|--------|---------------------------------|-------------|
| 7:0 | HPLVOL | Headphone Left volume selection | 00000000    |

**Table 13-46.** Headphone Left Volume Selection Table

| HPLVOL    | GAIN (dB) | HPLVOL   | GAIN (dB) | HPLVOL   | GAIN (dB) | HPLVOL    | GAIN (dB) |
|-----------|-----------|----------|-----------|----------|-----------|-----------|-----------|
| ≤10110010 | MUTE      | 11001000 | -56       | 11011110 | -34       | 11110100  | -12       |
| 10110011  | -77       | 11001001 | -55       | 11011111 | -33       | 11110101  | -11       |
| 10110100  | -76       | 11001010 | -54       | 11100000 | -32       | 11110110  | -10       |
| 10110101  | -75       | 11001011 | -53       | 11100001 | -31       | 11110111  | -9        |
| 10110110  | -74       | 11001100 | -52       | 11100010 | -30       | 11111000  | -8        |
| 10110111  | -73       | 11001101 | -51       | 11100011 | -29       | 11111001  | -7        |
| 10111000  | -72       | 11001110 | -50       | 11100100 | -28       | 11111010  | -6        |
| 10111001  | -71       | 11001111 | -49       | 11100101 | -27       | 11111011  | -5        |
| 10111010  | -70       | 11010000 | -48       | 11100110 | -26       | 11111100  | -4        |
| 10111011  | -69       | 11010001 | -47       | 11100111 | -25       | 11111101  | -3        |
| 10111100  | -68       | 11010010 | -46       | 11101000 | -24       | 11111110  | -2        |
| 10111101  | -67       | 11010011 | -45       | 11101001 | -23       | 11111111  | -1        |
| 10111110  | -66       | 11010100 | -44       | 11101010 | -22       | 00000000  | 0         |
| 10111111  | -65       | 11010101 | -43       | 11101011 | -21       | 00000001  | 1         |
| 11000000  | -64       | 11010110 | -42       | 11101100 | -20       | 00000010  | 2         |
| 11000001  | -63       | 11010111 | -41       | 11101101 | -19       | 00000011  | 3         |
| 11000010  | -62       | 11011000 | -40       | 11101110 | -18       | 00000100  | 4         |
| 11000011  | -61       | 11011001 | -39       | 11101111 | -17       | 00000101  | 5         |
| 11000100  | -60       | 11011010 | -38       | 11110000 | -16       | ≥00000110 | 6         |
| 11000101  | -59       | 11011011 | -37       | 11110001 | -15       |           |           |
| 11000110  | -58       | 11011100 | -36       | 11110010 | -14       |           |           |
| 11000111  | -57       | 11011101 | -35       | 11110011 | -13       |           |           |

**Name:** HPRVOL  
**Access:** Read / Write  
**Address:** 0x1B

|        |   |   |   |   |   |   |   |
|--------|---|---|---|---|---|---|---|
| 7      | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| HPRVOL |   |   |   |   |   |   |   |

**Table 13-47.** HPRVOL (0x1B) Structure

| Bit | Name   | Description                    | Reset value |
|-----|--------|--------------------------------|-------------|
| 7:0 | HPRVOL | HEADSET Right volume selection | 00000000    |

**Table 13-48.** Headphone Right Volume Selection Table

| HPRVOL    | GAIN (dB) | HPRVOL   | GAIN (dB) | HPRVOL   | GAIN (dB) | HPRVOL    | GAIN (dB) |
|-----------|-----------|----------|-----------|----------|-----------|-----------|-----------|
| ≤10110010 | MUTE      | 11001000 | -56       | 11011110 | -34       | 11110100  | -12       |
| 10110011  | -77       | 11001001 | -55       | 11011111 | -33       | 11110101  | -11       |
| 10110100  | -76       | 11001010 | -54       | 11100000 | -32       | 11110110  | -10       |
| 10110101  | -75       | 11001011 | -53       | 11100001 | -31       | 11110111  | -9        |
| 10110110  | -74       | 11001100 | -52       | 11100010 | -30       | 11111000  | -8        |
| 10110111  | -73       | 11001101 | -51       | 11100011 | -29       | 11111001  | -7        |
| 10111000  | -72       | 11001110 | -50       | 11100100 | -28       | 11111010  | -6        |
| 10111001  | -71       | 11001111 | -49       | 11100101 | -27       | 11111011  | -5        |
| 10111010  | -70       | 11010000 | -48       | 11100110 | -26       | 11111100  | -4        |
| 10111011  | -69       | 11010001 | -47       | 11100111 | -25       | 11111101  | -3        |
| 10111100  | -68       | 11010010 | -46       | 11101000 | -24       | 11111110  | -2        |
| 10111101  | -67       | 11010011 | -45       | 11101001 | -23       | 11111111  | -1        |
| 10111110  | -66       | 11010100 | -44       | 11101010 | -22       | 00000000  | 0         |
| 10111111  | -65       | 11010101 | -43       | 11101011 | -21       | 00000001  | 1         |
| 11000000  | -64       | 11010110 | -42       | 11101100 | -20       | 00000010  | 2         |
| 11000001  | -63       | 11010111 | -41       | 11101101 | -19       | 00000011  | 3         |
| 11000010  | -62       | 11011000 | -40       | 11101110 | -18       | 00000100  | 4         |
| 11000011  | -61       | 11011001 | -39       | 11101111 | -17       | 00000101  | 5         |
| 11000100  | -60       | 11011010 | -38       | 11110000 | -16       | ≥00000110 | 6         |
| 11000101  | -59       | 11011011 | -37       | 11110001 | -15       |           |           |
| 11000110  | -58       | 11011100 | -36       | 11110010 | -14       |           |           |
| 11000111  | -57       | 11011101 | -35       | 11110011 | -13       |           |           |

**Name:** HP\_CONTROL

**Access:** Read / Write

**Address:** 0x1C

|   |   |   |   |   |          |         |         |
|---|---|---|---|---|----------|---------|---------|
| 7 | 6 | 5 | 4 | 3 | 2        | 1       | 0       |
| - | - | - | - | - | HPDET_ST | LHPBOTH | RHPBOTH |

**Table 13-49.** HP\_CONTROL (0x1C) Structure

| Bit | Name     | Description   | Reset value |
|-----|----------|---|-------------|
| 7:3 | -        | unused  | 00000       |
| 2   | HPDET_ST | Headphone plug in-out detector<br>0: OFF<br>1: ON   | 0           |
| 1   | LHPBOTH  | Right Headphone volume follows left<br>0: inactive<br>1: active. Priority bit over RHPBOTH. | 1           |
| 0   | RHPBOTH  | Left Headphone volume follows right<br>0: inactive<br>1: active                             | 0           |



**Name:** AUDIO\_EFFECTS

**Access:** Read / Write

**Address:** 0x1D

|            |   |        |          |          |          |          |         |
|------------|---|--------|----------|----------|----------|----------|---------|
| 7          | 6 | 5      | 4        | 3        | 2        | 1        | 0       |
| 3DFX_DEPTH |   | ON3DFX | SWAP_DAC | SWAP_ADC | MONO_DAC | MONO_ADC | ONDEEMP |

**Table 13-50.** AUDIO\_EFFECTS (0x1D) Structure

| Bit | Name       | Description   | Reset value |
|-----|------------|---|-------------|
| 7:6 | 3DFX_DEPTH | 3D effect depth control   | 00          |
| 5   | ON3DFX     | 3D effect<br>0: OFF<br>1: ON  | 0           |
| 4   | SWAP_DAC   | DAC Left / Right channel swap<br>0: Left / Right inputs on Left / Right outputs<br>1: Left / Right inputs on Right / Left outputs | 0           |
| 3   | SWAP_ADC   | ADC Left / Right channel swap<br>0: Left / Right inputs on Left / Right outputs<br>1: Left / Right inputs on Right / Left outputs | 0           |
| 2   | MONO_DAC   | (Left + Right) / 2 on Left and Right channels<br>0: inactive<br>1: active   | 0           |
| 1   | MONO_ADC   | Left ADC output on both Left and Right channels<br>0: inactive<br>1: active   | 0           |
| 0   | ONDEEMP    | De-emphasis filter<br>0: OFF<br>1: ON   | 0           |

**Table 13-51.** 3-D Effect Depth Control Table

| 3DFX_DEPTH | Attenuation |
|------------|-------------|
| 00         | 0dB         |
| 01         | -6dB        |
| 10         | -12dB       |
| 11         | -18dB       |

**Name:** INPUT\_CONTROL

**Access:** Read / Write.

This register is modified by Audio Controller at audio path change.

**Address:** 0x1E

|   |         |        |        |        |        |        |        |
|---|---------|--------|--------|--------|--------|--------|--------|
| 7 | 6       | 5      | 4      | 3      | 2      | 1      | 0      |
| - | LINESEL | ONMICL | ONMICR | ONADCL | ONADCR | ONLINL | ONLINR |

**Table 13-52.** INPUT\_CONTROL (0x1E) Structure

| Bit | Name    | Description  | Reset value |
|-----|---------|--|-------------|
| 7   |         | unused   | 0           |
| 6   | LINESEL | <b>LINE</b> / AUX input selection<br>0: Aux input selected<br>1: Line input selected | 1           |
| 5   | ONMICL  | Left microphone amplifier<br>0: OFF<br>1: ON   | 0           |
| 4   | ONMICR  | Right microphone amplifier<br>0: OFF<br>1: ON  | 0           |
| 3   | ONADCL  | Left ADC<br>0: OFF<br>1: ON  | 0           |
| 2   | ONADCR  | Right ADC<br>0: OFF<br>1: ON   | 0           |
| 1   | ONLINL  | Left line input amplifier<br>0: OFF<br>1: ON   | 0           |
| 0   | ONLINR  | Right line input amplifier<br>0: OFF<br>1: ON  | 0           |

**Name:** OUTPUT\_CONTROL

**Access:** Read / Write

This register is modified by Audio Controller at audio path change.

**Address:** 0x1F

|   |            |            |          |       |       |         |        |
|---|------------|------------|----------|-------|-------|---------|--------|
| 7 | 6          | 5          | 4        | 3     | 2     | 1       | 0      |
| - | ONSIDETONE | ONPLAYBACK | ONBYPASS | ONHPL | ONHPR | ONDAACL | ONDACR |

**Table 13-53.** OUTPUT\_CONTROL (0x1F) Structure

| Bit | Name       | Description                                  | Reset value |
|-----|------------|--|-------------|
| 7   |            | unused                                       | 0           |
| 6   | ONSIDETONE | Sidetone switch<br>0: muted<br>1: enabled    | 0           |
| 5   | ONPLAYBACK | Playback switch<br>0: muted<br>1: enabled    | 0           |
| 4   | ONBYPASS   | Bypass switch<br>0: muted<br>1: enabled      | 0           |
| 3   | ONHPL      | Left headphone amplifier<br>0: OFF<br>1: ON  | 0           |
| 2   | ONHPR      | Right headphone amplifier<br>0: OFF<br>1: ON | 0           |
| 1   | ONDAACL    | Left DAC<br>0: OFF<br>1: ON                  | 0           |
| 0   | ONDACR     | Right DAC<br>0: OFF<br>1: ON                 | 0           |

**Name:** INPUT\_MIXER

**Access:** Read / Write

This register is modified by Audio Controller at audio path change.

**Address:** 0x20

|   |   |         |         |          |          |        |        |
|---|---|---------|---------|----------|----------|--------|--------|
| 7 | 6 | 5       | 4       | 3        | 2        | 1      | 0      |
| - | - | MIXMICL | MIXMICR | MIXLINEL | MIXLINER | ONMIXL | ONMIXR |

**Table 13-54.** INPUT\_MIXER (0x20) Structure

| Bit | Name     | Description   | Reset value |
|-----|----------|---|-------------|
| 7:6 | -        | unused  | 00          |
| 5   | MIXMICL  | Left microphone input mixer switch<br>0: muted<br>1: enabled  | 0           |
| 4   | MIXMICR  | Right microphone input mixer switch<br>0: muted<br>1: enabled | 0           |
| 3   | MIXLINEL | Left line / aux input mixer switch<br>0: muted<br>1: enabled  | 0           |
| 2   | MIXLINER | Right line / aux input mixer switch<br>0: muted<br>1: enabled | 0           |
| 1   | ONMIXL   | Left input mixer ON / OFF<br>0: muted<br>1: enabled           | 0           |
| 0   | ONMIXR   | Right input mixer ON / OFF<br>0: muted<br>1: enabled          | 0           |

**Name:** SIDETONE\_VOL

**Access:** Read / Write

**Address:** 0x21

|   |   |   |              |   |   |   |   |
|---|---|---|--------------|---|---|---|---|
| 7 | 6 | 5 | 4            | 3 | 2 | 1 | 0 |
| - | - | - | SIDETONE_VOL |   |   |   |   |

**Table 13-55.** SIDETONE\_VOL (0x21) Structure

| Bit | Name         | Description                            | Reset value  |
|-----|--------------|--|--------------|
| 7:5 |              | unused                                 | 000          |
| 4:0 | SIDETONE_VOL | Left / Right sidetone path attenuation | <b>01011</b> |

**Table 13-56.** Left / Right Sidetone Path Attenuation Selection Table

| SIDETONE_VOL | ATT(dB) | SIDETONE_VOL | ATT(dB) | SIDETONE_VOL      | ATT(dB)   |
|--------------|---------|--------------|---------|-------------------|-----------|
| 00000        | 0       | 00100        | 12      | 01000             | 24        |
| 00001        | 3       | 00101        | 15      | 01001             | 27        |
| 00010        | 6       | 00110        | 18      | 01010             | 30        |
| 00011        | 9       | 00111        | 21      | <b>&gt;=01011</b> | <b>30</b> |

**Name:** EQUALIZER

**Access:** Read / Write

**Address:** 0x22

|   |   |   |   |        |   |   |   |
|---|---|---|---|--------|---|---|---|
| 7 | 6 | 5 | 4 | 3      | 2 | 1 | 0 |
| - | - | - | - | EQ_SEL |   |   |   |

**Table 13-57.** EQUALIZER (0x22) Structure

| Bit | Name   | Description         | Reset value |
|-----|--------|---------------------|-------------|
| 7:4 |        |                     | 0           |
| 3:0 | EQ_SEL | Equalizer selection | 0000        |

**Table 13-58.** Equalizer Selection Table(0x22) Structure

| EQ_SEL      | Description        |
|-------------|--------------------|
| 0000        | Flat Response      |
| 0001        | Bass boost +12dB   |
| 0010        | Bass boost +6dB    |
| 0011        | Bass cut -12dB     |
| 0100        | Bass cut -6dB      |
| 0101        | Medium boost +3dB  |
| 0110        | Medium boost +8dB  |
| 0111        | Medium cut -3dB    |
| 1000        | Medium cut -8dB    |
| 1001        | Treble boost +12dB |
| 1010        | Treble boost +6dB  |
| 1011        | Treble cut -12dB   |
| 1100        | Treble cut -6dB    |
| Other value | Flat response.     |

**Name:** ADC\_CTRL  
**Access:** Read / Write  
**Address:** 0x30

|        |        |   |   |   |    |   |   |
|--------|--------|---|---|---|----|---|---|
| 7      | 6      | 5 | 4 | 3 | 2  | 1 | 0 |
| ON_ADC | ON_BUF | - | - | - | TS |   |   |

**Table 13-59.** ADC\_CTRL (0x30) Structure

| Bit | Name   | Description                      | Reset value |
|-----|--------|----------------------------------|-------------|
| 7   | ON_ADC | ADC function<br>0: OFF<br>1: ON  | 0           |
| 6   | ON_BUF | Analog buffer<br>0: OFF<br>1: ON | 0           |
| 5:3 | unused | -                                | 000         |
| 2:0 | TS     | Sampling period                  | 000         |

**Table 13-60.** ADC Sampling Period Selection Table

| TS  | SAMPLING PERIOD (s) |
|-----|---------------------|
| 000 | 0.01                |
| 001 | 0.02                |
| 010 | 0.1                 |
| 011 | 1                   |
| 100 | 2                   |
| 101 | 3                   |
| 110 | 4                   |
| 111 | Max speed           |

**Name:** ADC\_MUX\_1

**Access:** Read / Write

**Address:** 0x31

|   |     |   |      |      |      |      |      |
|---|-----|---|------|------|------|------|------|
| 7 | 6   | 5 | 4    | 3    | 2    | 1    | 0    |
| - | VIN | - | VDD4 | VDD3 | VDD2 | VDD1 | VDD0 |

**Table 13-61.** ADC\_MUX1 (0x31) Structure

| Bit | Name   | Description  | Reset value |
|-----|--------|--|-------------|
| 7   | unused | -  | 0           |
| 6   | VIN    | VIN channel selection<br>0: Not selected<br>1: Selected  | 1           |
| 5   | unused | -  | 1           |
| 4   | VDD4   | VDD4 channel selection<br>0: Not selected<br>1: Selected | 1           |
| 3   | VDD3   | VDD3 channel selection<br>0: Not selected<br>1: Selected | 1           |
| 2   | VDD2   | VDD2 channel selection<br>0: Not selected<br>1: Selected | 1           |
| 1   | VDD1   | VDD1 channel selection<br>0: Not selected<br>1: Selected | 1           |
| 0   | VDD0   | VDD0 channel selection<br>0: Not selected<br>1: Selected | 1           |



**Name:** ADC\_MUX\_2

**Access:** Read / Write

**Address:** 0x32

|   |   |   |   |      |      |      |      |
|---|---|---|---|------|------|------|------|
| 7 | 6 | 5 | 4 | 3    | 2    | 1    | 0    |
| - | - | - | - | ANA3 | ANA2 | ANA1 | ANA0 |

**Table 13-62.** ADC\_MUX2 (0x32) Structure

| Bit | Name   | Description  | Reset value |
|-----|--------|--|-------------|
| 7:4 | unused | -  | 0000        |
| 3   | ANA3   | ANA3 channel selection<br>0: Not selected<br>1: Selected | 1           |
| 2   | ANA2   | ANA2 channel selection<br>0: Not selected<br>1: Selected | 1           |
| 1   | ANA1   | ANA1 channel selection<br>0: Not selected<br>1: Selected | 1           |
| 0   | ANA0   | ANA0 channel selection<br>0: Not selected<br>1: Selected | 1           |

**Name:** ADC\_ANA0\_MSB

**Access:** Read Only

**Address:** 0x33

|          |   |   |   |   |   |   |   |
|----------|---|---|---|---|---|---|---|
| 7        | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ADC<9:2> |   |   |   |   |   |   |   |

**Table 13-63.** ADC\_ANA0\_MSB (0x33) Structure

| Bit | Name     | Description                   | Reset value |
|-----|----------|-------------------------------|-------------|
| 7:0 | ADC<9:2> | ADC_OUT<9:2> for ANA0 Channel | 00000000    |

**Name:** ADC\_ANA0\_LSB

**Access:** Read Only

**Address:** 0x34

|   |   |   |   |   |   |   |          |
|---|---|---|---|---|---|---|----------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0        |
|   |   |   |   |   |   |   | ADC<1:0> |

**Table 13-64.** ADC\_ANA0\_LSB (0x34) Structure

| Bit | Name     | Description                   | Reset value |
|-----|----------|-------------------------------|-------------|
| 7:2 | -        | unused                        |             |
| 1:0 | ADC<1:0> | ADC_OUT<1:0> for ANA0 Channel | 00          |

**Name:** ADC\_ANA1\_MSB

**Access:** Read Only

**Address:** 0x35

|          |   |   |   |   |   |   |   |
|----------|---|---|---|---|---|---|---|
| 7        | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ADC<9:2> |   |   |   |   |   |   |   |

**Table 13-65.** ADC\_ANA1\_MSB (0x35) Structure

| Bit | Name     | Description                   | Reset value |
|-----|----------|-------------------------------|-------------|
| 7:0 | ADC<9:2> | ADC_OUT<9:2> for ANA1 Channel | 00000000    |

**Name:** ADC\_ANA1\_LSB

**Access:** Read Only

**Address:** 0x36

|   |   |   |   |   |   |   |          |
|---|---|---|---|---|---|---|----------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0        |
|   |   |   |   |   |   |   | ADC<1:0> |

**Table 13-66.** ADC\_ANA1\_LSB (0x36) Structure

| Bit | Name     | Description                   | Reset value |
|-----|----------|-------------------------------|-------------|
| 7:2 | -        | unused                        |             |
| 1:0 | ADC<1:0> | ADC_OUT<1:0> for ANA1 Channel | 00          |

**Name:** ADC\_ANA2\_MSB

**Access:** Read Only

**Address:** 0x37

|          |   |   |   |   |   |   |   |
|----------|---|---|---|---|---|---|---|
| 7        | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ADC<9:2> |   |   |   |   |   |   |   |

**Table 13-67.** ADC\_ANA2\_MSB (0x37) Structure

| Bit | Name     | Description                   | Reset value |
|-----|----------|-------------------------------|-------------|
| 7:0 | ADC<9:2> | ADC_OUT<9:2> for ANA2 Channel | 00000000    |

**Name:** ADC\_ANA2\_LSB

**Access:** Read Only

**Address:** 0x38

|   |   |   |   |   |   |   |          |
|---|---|---|---|---|---|---|----------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0        |
|   |   |   |   |   |   |   | ADC<1:0> |

**Table 13-68.** ADC\_ANA2\_LSB (0x38) Structure

| Bit | Name     | Description                   | Reset value |
|-----|----------|-------------------------------|-------------|
| 7:2 | -        | unused                        |             |
| 1:0 | ADC<1:0> | ADC_OUT<1:0> for ANA2 Channel | 00          |

**Name:** ADC\_ANA3\_MSB

**Access:** Read Only

**Address:** 0x39

|          |   |   |   |   |   |   |   |
|----------|---|---|---|---|---|---|---|
| 7        | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ADC<9:2> |   |   |   |   |   |   |   |

**Table 13-69.** ADC\_ANA3\_MSB (0x39) Structure

| Bit | Name     | Description                   | Reset value |
|-----|----------|-------------------------------|-------------|
| 7:0 | ADC<9:2> | ADC_OUT<9:2> for ANA3 Channel | 00000000    |

**Name:** ADC\_ANA3\_LSB

**Access:** Read Only

**Address:** 0x3A

|   |   |   |   |   |   |   |          |
|---|---|---|---|---|---|---|----------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0        |
|   |   |   |   |   |   |   | ADC<1:0> |

**Table 13-70.** ADC\_ANA3\_LSB (0x3A) Structure

| Bit | Name     | Description                   | Reset value |
|-----|----------|-------------------------------|-------------|
| 7:2 | -        | unused                        |             |
| 1:0 | ADC<1:0> | ADC_OUT<1:0> for ANA3 Channel | 00          |

**Name:** ADC\_VDD0\_MSB

**Access:** Read Only

**Address:** 0x3B

|          |   |   |   |   |   |   |   |
|----------|---|---|---|---|---|---|---|
| 7        | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ADC<9:2> |   |   |   |   |   |   |   |

**Table 13-71.** ADC\_VDD0\_MSB (0x3B) Structure

| Bit | Name     | Description                   | Reset value |
|-----|----------|-------------------------------|-------------|
| 7:0 | ADC<9:2> | ADC_OUT<9:2> for VDD0 Channel | 00000000    |

**Name:** ADC\_VDD0\_LSB

**Access:** Read Only

**Address:** 0x3C

|   |   |   |   |   |   |   |          |
|---|---|---|---|---|---|---|----------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0        |
|   |   |   |   |   |   |   | ADC<1:0> |

**Table 13-72.** ADC\_VDD0\_LSB (0x3C) Structure

| Bit | Name     | Description                   | Reset value |
|-----|----------|-------------------------------|-------------|
| 7:2 | -        | unused                        |             |
| 1:0 | ADC<1:0> | ADC_OUT<1:0> for VDD0 Channel | 00          |

**Name:** ADC\_VDD1\_MSB

**Access:** Read Only

**Address:** 0x3D

|          |   |   |   |   |   |   |   |
|----------|---|---|---|---|---|---|---|
| 7        | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ADC<9:2> |   |   |   |   |   |   |   |

**Table 13-73.** ADC\_VDD1\_MSB (0x3D) Structure

| Bit | Name     | Description                   | Reset value |
|-----|----------|-------------------------------|-------------|
| 7:0 | ADC<9:2> | ADC_OUT<9:2> for VDD1 Channel | 00000000    |

**Name:** ADC\_VDD1\_LSB

**Access:** Read Only

**Address:** 0x3E

|   |   |   |   |   |   |   |          |
|---|---|---|---|---|---|---|----------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0        |
|   |   |   |   |   |   |   | ADC<1:0> |

**Table 13-74.** ADC\_VDD1\_LSB (0x3E) Structure

| Bit | Name     | Description                   | Reset value |
|-----|----------|-------------------------------|-------------|
| 7:2 | -        | unused                        |             |
| 1:0 | ADC<1:0> | ADC_OUT<1:0> for VDD1 Channel | 00          |

**Name:** ADC\_VDD2\_MSB

**Access:** Read Only

**Address:** 0x3F

|          |   |   |   |   |   |   |   |
|----------|---|---|---|---|---|---|---|
| 7        | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ADC<9:2> |   |   |   |   |   |   |   |

**Table 13-75.** ADC\_VDD2\_MSB (0x3F) Structure

| Bit | Name     | Description                   | Reset value |
|-----|----------|-------------------------------|-------------|
| 7:0 | ADC<9:2> | ADC_OUT<9:2> for VDD2 Channel | 00000000    |

**Name:** ADC\_VDD2\_LSB

**Access:** Read Only

**Address:** 0x40

|   |   |   |   |   |   |   |          |
|---|---|---|---|---|---|---|----------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0        |
|   |   |   |   |   |   |   | ADC<1:0> |

**Table 13-76.** ADC\_VDD2\_LSB (0x40) Structure

| Bit | Name     | Description                   | Reset value |
|-----|----------|-------------------------------|-------------|
| 7:2 | -        | unused                        |             |
| 1:0 | ADC<1:0> | ADC_OUT<1:0> for VDD2 Channel | 00          |



**Name:** ADC\_VDD3\_MSB

**Access:** Read Only

**Address:** 0x41

|          |   |   |   |   |   |   |   |
|----------|---|---|---|---|---|---|---|
| 7        | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ADC<9:2> |   |   |   |   |   |   |   |

**Table 13-77.** ADC\_VDD3\_MSB (0x41) Structure

| Bit | Name     | Description                   | Reset value |
|-----|----------|-------------------------------|-------------|
| 7:2 | ADC<9:2> | ADC_OUT<9:2> for VDD3 Channel | 00000000    |

**Name:** ADC\_VDD3\_LSB

**Access:** Read Only

**Address:** 0x42

|   |   |   |   |   |   |   |          |
|---|---|---|---|---|---|---|----------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0        |
|   |   |   |   |   |   |   | ADC<1:0> |

**Table 13-78.** ADC\_VDD3\_LSB (0x42) Structure

| Bit | Name     | Description                   | Reset value |
|-----|----------|-------------------------------|-------------|
| 7:2 | -        | unused                        |             |
| 1:0 | ADC<1:0> | ADC_OUT<1:0> for VDD3 Channel | 00          |

**Name:** ADC\_VDD4\_MSB

**Access:** Read Only

**Address:** 0x43

|          |   |   |   |   |   |   |   |
|----------|---|---|---|---|---|---|---|
| 7        | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ADC<9:2> |   |   |   |   |   |   |   |

**Table 13-79.** ADC\_VDD4\_MSB (0x43) Structure

| Bit | Name     | Description                   | Reset value |
|-----|----------|-------------------------------|-------------|
| 7:0 | ADC<9:2> | ADC_OUT<9:2> for VDD4 Channel | 00000000    |

**Name:** ADC\_VDD4\_LSB

**Access:** Read Only

**Address:** 0x44

|   |   |   |   |   |   |   |          |
|---|---|---|---|---|---|---|----------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0        |
|   |   |   |   |   |   |   | ADC<1:0> |

**Table 13-80.** ADC\_VDD4\_LSB (0x44) Structure

| Bit | Name     | Description                   | Reset value |
|-----|----------|-------------------------------|-------------|
| 7:2 | -        | unused                        |             |
| 1:0 | ADC<1:0> | ADC_OUT<1:0> for VDD4 Channel | 00          |

**Name:** ADC\_VIN\_MSB

**Access:** Read Only

**Address:** 0x47

|          |   |   |   |   |   |   |   |
|----------|---|---|---|---|---|---|---|
| 7        | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ADC<9:2> |   |   |   |   |   |   |   |

**Table 13-81.** ADC\_VIN\_MSB (0x47) Structure

| Bit | Name     | Description                  | Reset value |
|-----|----------|------------------------------|-------------|
| 7:0 | ADC<9:2> | ADC_OUT<9:2> for VIN Channel | 00000000    |

**Name:** ADC\_VIN\_LSB

**Access:** Read Only

**Address:** 0x48

|   |   |   |   |   |   |   |          |
|---|---|---|---|---|---|---|----------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0        |
|   |   |   |   |   |   |   | ADC<1:0> |

**Table 13-82.** ADC\_VIN\_LSB (0x48) Structure

| Bit | Name     | Description                  | Reset value |
|-----|----------|------------------------------|-------------|
| 7:2 | -        | unused                       |             |
| 1:0 | ADC<1:0> | ADC_OUT<1:0> for VIN Channel | 00          |

**Name:** ADC\_ANA\_LSB

**Access:** Read Only

**Address:** 0x49

|               |   |               |   |               |   |               |   |
|---------------|---|---------------|---|---------------|---|---------------|---|
| 7             | 6 | 5             | 4 | 3             | 2 | 1             | 0 |
| ADC_ANA3<1:0> |   | ADC_ANA2<1:0> |   | ADC_ANA1<1:0> |   | ADC_ANA0<1:0> |   |

**Table 13-83.** ADC\_ANA\_LSB (0x49) Structure

| Bit | Name          | Description                    | Reset value |
|-----|---------------|--------------------------------|-------------|
| 7:6 | ADC_ANA3<1:0> | ADC_OUT<1:0:> for ANA3 Channel | 00          |
| 5:4 | ADC_ANA2<1:0> | ADC_OUT<1:0:> for ANA2 Channel | 00          |
| 3:2 | ADC_ANA1<1:0> | ADC_OUT<1:0:> for ANA1 Channel | 00          |
| 1:0 | ADC_ANA0<1:0> | ADC_OUT<1:0:> for ANA0 Channel | 00          |

**Name:** RTC\_CTRL

**Access:** Read / Write

**Address:** 0x50

|   |   |   |   |   |           |         |        |
|---|---|---|---|---|-----------|---------|--------|
| 7 | 6 | 5 | 4 | 3 | 2         | 1       | 0      |
| - | - |   |   |   | RTC_WRITE | RTC_SEL | RTC_EN |

**Table 13-84.** RTC\_CTRL (0x50) Structure

| Bit | Name      | Description   | Reset value |
|-----|-----------|---|-------------|
| 7:3 | -         | unused  |             |
| 2   | RTC_WRITE | <b>RTC read/write:</b><br>RTC_WRITE = 0: Read mode<br>RTC_WRITE = 1: Write mode | 0           |
| 1   | RTC_SEL   | <b>RTC block select:</b><br>RTC_SEL = 0: Not Selected<br>RTC_SEL = 1: Selected  | 0           |
| 0   | RTC_EN    | <b>RTC block enable:</b><br>RTC_EN = 0: Disabled<br>RTC_EN = 1: Enabled         | 0           |

**Name:** RTC\_ADDR  
**Access:** Read / Write  
**Address:** 0x51

|          |   |   |   |   |   |   |   |
|----------|---|---|---|---|---|---|---|
| 7        | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RTC_ADDR |   |   |   |   |   |   |   |

**Table 13-85.** RTC\_ADDR (0x51) Structure

| Bit | Name     | Description | Reset value |
|-----|----------|-------------|-------------|
| 7:0 | RTC_ADDR | RTC address | 0000        |

**Name:** RTC\_DATA0  
**Access:** Read / Write  
**Address:** 0x52

|           |   |   |   |   |   |   |   |
|-----------|---|---|---|---|---|---|---|
| 7         | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RTC_DATA0 |   |   |   |   |   |   |   |

**Table 13-86.** RTC\_DATA0 (0x52) Structure

| Bit | Name      | Description | Reset value |
|-----|-----------|-------------|-------------|
| 7:0 | RTC_DATA0 | RTC DATA 0  | 0000000     |

**Name:** RTC\_DATA1

**Access:** Read / Write

**Address:** 0x53

|           |   |   |   |   |   |   |   |
|-----------|---|---|---|---|---|---|---|
| 7         | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RTC_DATA1 |   |   |   |   |   |   |   |

**Table 13-87.** RTC\_DATA1 (0x53) Structure

| Bit | Name      | Description | Reset value |
|-----|-----------|-------------|-------------|
| 7:0 | RTC_DATA1 | RTC DATA 1  | 0000000     |

**Name:** RTC\_DATA2

**Access:** Read / Write

**Address:** 0x54

|           |   |   |   |   |   |   |   |
|-----------|---|---|---|---|---|---|---|
| 7         | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RTC_DATA2 |   |   |   |   |   |   |   |

**Table 13-88.** RTC\_DATA2 (0x54) Structure

| Bit | Name      | Description | Reset value |
|-----|-----------|-------------|-------------|
| 7:0 | RTC_DATA2 | RTC DATA 2  | 0000000     |

**Name:** RTC\_DATA3

**Access:** Read / Write

**Address:** 0x55

|           |   |   |   |   |   |   |   |
|-----------|---|---|---|---|---|---|---|
| 7         | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RTC_DATA3 |   |   |   |   |   |   |   |

**Table 13-89.** RTC\_DATA3 (0x55) Structure

| Bit | Name      | Description | Reset value |
|-----|-----------|-------------|-------------|
| 7:0 | RTC_DATA3 | RTC DATA 3  | 0000000     |

**Name:** BACKUP\_CTRL

**Access:** Read / Write

**Address:** 0x56

|   |   |   |   |          |        |          |          |
|---|---|---|---|----------|--------|----------|----------|
| 7 | 6 | 5 | 4 | 3        | 2      | 1        | 0        |
| - | - | - | - | OSC_UPDT | OSC_EN | OSC_STAT | RST_BKUP |

**Table 13-90.** BACKUP\_CTRL (0x56) Structure

| Bit | Name     | Description  | Reset value |
|-----|----------|--|-------------|
| 7:4 | -        | unused   | 0000        |
| 3   | OSC_UPDT | RTC Oscillator update<br>0: No action.<br>1: Update RTC oscillator with OSC_EN     | 0           |
| 2   | OSC_EN   | RTC Oscillator enable request<br>0: Oscillator off.<br>1: Oscillator on.           | 0           |
| 1   | OSC_STAT | RTC Oscillator status (read only)<br>0: Oscillator off.<br>1: Oscillator on.       | 0           |
| 0   | RST_BKUP | Reset of the Backup Area<br>0: Backup area active<br>1: Backup area in reset state | 0           |

**Name:** VERSION

**Access:** Read

**Address:** 0x7F

|              |   |   |   |         |   |   |   |
|--------------|---|---|---|---------|---|---|---|
| 7            | 6 | 5 | 4 | 3       | 2 | 1 | 0 |
| SOFTWARE_TAG |   |   |   | VERSION |   |   |   |

**Table 13-91.** VERSION (0x7F) Structure

| Bit | Name         | Description  | Reset value |
|-----|--------------|--|-------------|
| 7:4 | SOFTWARE_TAG | Software Tag to identify product specificities as described in Section 17. "Ordering Information" on page 154. | XXXX        |
| 3:0 | VERSION      | '0001': Rev. C samples<br>'0010': Rev. D samples   | XXXX        |

## 14. PMU and Audio Soft Control: Quick Start

### 14.1 RTC Examples

#### 14.1.1 RTC Oscillator POWER-ON

```
// Set OSC_EN = 1 and OSC_UPDT = 1
TWI_WRITE 0x0C @BACKUP_CTRL
// Wait > 200us.
WAIT 200us
// Set OSC_UPDT = 0
TWI_WRITE 0x04 @BACKUP_CTRL
// Read BACKUP_CTRL to verify OSC_STAT bit. Result = 0x06.
TWI_READ @BACKUP_CTRL
```

#### 14.1.2 RTC Oscillator POWER-OFF

```
// Set OSC_EN = 0 and OSC_UPDT = 1
TWI_WRITE 0x08 @BACKUP_CTRL
// Wait 200us
WAIT 200us
// Set OSC_UPDT = 0
TWI_WRITE 0x00 @BACKUP_CTRL
// Read BACKUP_CTRL to verify OSC_STAT bit. Result = 0x00.
TWI_READ @BACKUP_CTRL
```

#### 14.1.3 RTC Domain RESET

```
// Set RST_BKUP = 1
TWI_WRITE 0x01 @BACKUP_CTRL
// Wait 200s
WAIT 200us
// Set RST_BKUP = 0
TWI_WRITE 0x00 @BACKUP_CTRL
```

Note: Reset of the RTC domain powers off the RTC oscillator.

#### 14.1.4 RTC Write Operation

The following example makes a generic 32-bit write operation into the RTC macro. The 32-bit data is split into 4 bytes, that are successively sent over the TWI.

```
unsigned int RTC_DATA;
char DATA0 = (char) (RTC_DATA); // LSBs
char DATA1 = (char) (RTC_DATA >> 8);
char DATA2 = (char) (RTC_DATA >> 16);
char DATA3 = (char) (RTC_DATA >> 24); // MSBs
// Select RTC_ADDR = ADDR. ADDR is the RTC macro register to write,
TWI_WRITE ADDR @RTC_ADDR
// Set RTC_DATA0 to RTC_DATA4 registers.
TWI_WRITE DATA0 @RTC_DATA0
TWI_WRITE DATA1 @RTC_DATA1
```



```

TWI_WRITE DATA2 @RTC_DATA2
TWI_WRITE DATA3 @RTC_DATA3
// Set RTC_WRITE = 1 (write) and RTC_SEL = 1
TWI_WRITE 0x06 @ RTC_CTRL
// Pulse RTC_EN
TWI_WRITE 0x07 @ RTC_CTRL
TWI_WRITE 0x06 @ RTC_CTRL
// Disable RTC access
TWI_WRITE 0x00 @ RTC_CTRL

```

#### 14.1.5 RTC Read Operation

The following example makes a generic 32-bit read operation into the RTC macro. The 32-bit RTC data is split into 4 bytes, that are successively read over the TWI.

```

// Select RTC_ADDR = ADDR. ADDR is the RTC macro register to read,
TWI_WRITE ADDR @RTC_ADDR
// Set RTC_WRITE = 0 (read) and RTC_SEL = 1
TWI_WRITE 0x02 @ RTC_CTRL
// Pulse RTC_EN
TWI_WRITE 0x03 @ RTC_CTRL
TWI_WRITE 0x02 @ RTC_CTRL
// Read RTC_DATA0 to RTC_DATA4 registers.
TWI_READ @RTC_DATA0 // LSBs
TWI_READ @RTC_DATA1
TWI_READ @RTC_DATA2
TWI_READ @RTC_DATA3 // MSBs
// Disable RTC access
TWI_WRITE 0x00 @ RTC_CTRL

```

#### 14.1.6 RTC Date and Time Update

In the following example, the RTC date and time is set to “12 October 2004, 08h 49min 59s”. The WRITE\_RTC and READ\_RTC functions operate as described in the previous sections.

```

// Disable RTC interrupt MASK
TWI_WRITE 0xFE @PMU_MASK
// Enable RTC ACKUPD IT @RTC_IER (RTC_ADDR 0x20).
WRITE_RTC 0x00000001 @RTC_IER
// Set UPDTIME and UPDCAL @RTC_CR (RTC_ADDR 0x00).
WRITE_RTC 0x00000003 @RTC_CR
// Wait ITB low. This ensures that the RTC is ready to be updated.
// Reset IT by read operation, result is 0x01.
TWI_READ @PMU_IT
// Read in RTC_SR that ACKUPD = 1 (RTC_ADDR = 0x18)
READ_RTC @RTC_SR
// Disable ACKUPD IT @RTC_IDR (RTC_ADDR = 0x24)
WRITE_RTC 0x00000001 @RTC_IDR
// Write Date @RTC_CALR (RTC_ADDR = 0x0C) (12 October 2004)
WRITE_RTC 0x12300420 @RTC_CALR

```

```
// Write Time @RTC_TIMR (RTC_ADDR = 0x08) (08h 49min 59s)
WRITE_RTC 0x00084959 @RTC_TIMR
// Start RTC @RTC_CR (RTC_ADDR = 0x00)
WRITE_RTC 0x00000000 @RTC_CR
```

## 14.2 Audio Examples

### 14.2.1 Basic Audio Codec Setting Using Automatic Path Control

The following example demonstrates an automatic audio path setting. Assuming that the audio codec is supplied by the LDO4, the sequence is the following:

- Make the codec interface configuration,
- Set the Digital-IN to Headphone-OUT path,
- Put the audio codec in standby mode,
- Release the standby mode to re-activate the selected path,
- Change the path on-the-fly,
- Shutdown the codec.

```
// Start LDO4 @3.3V
TWI_WRITE 0x8C @ VDD4_CTRL

// Digital Audio Interface configuration
// Master clock = 12.288MHz, Master / Slave = slave.
// DAI mode = I2S mode, Word length = 24 bits, FS = 48kHz
TWI_WRITE 0x01 @ DAI_CONTROL
TWI_WRITE 0x63 @ FRAME_CONTROL

// Analog interface configuration
// Mic. config: L & R single ended, Micbias = OFF, Mic. detection = OFF.
// Headphone config: AC coupled,
// Automatic Soft Ramping = ON, ASR timing = 11 (~10ms / step)
TWI_WRITE 0x00 @ MIC_CONTROL
TWI_WRITE 0x27 @ AUDIO_CONTROL

// Analog gain
// Headphone (L & R) gain: -20dB. (LHPBOTH set by default in HP_CONTROL)
// Mic L & R gain: +26 dB.
// Unmute all gains. No power-up is performed.
TWI_WRITE 0xEC @ HPLVOL
TWI_WRITE 0x1A @ MICLVOL
TWI_WRITE 0x1A @ MICRVOL
TWI_WRITE 0x00 @ MUTE

// Audio Start
// ENAC = 1, STANDBY = 1. PATH = 1 (DAC playback)
// At the first start, VMID capacitor is charged.
```

```

// Wait (3.tau) = 300ms with 1uF before standby release. (VMID will be
// discharged only when ENAC = 0.)
// From this point Audio Data can be sent over the Digital audio interface.
TWI_WRITE 0x61 @ AUTOSTART.
WAIT 300ms
// Release standby. The audio codec starts silently, the gains are slowly
// ramped up from mute to the register gains. The codec is active.
TWI_WRITE 0x41 @ AUTOSTART

// Codec Pause by Standby
// All gains are softly ramped down to mute. The codec functions are
// shut down. Current consumption is reduced to a few hundreds of micro-
// amps. VMID remains charged
TWI_WRITE 0x61 @ AUTOSTART

// Pause out: Standby release. The codec softly re-starts.
TWI_WRITE 0x41 @ AUTOSTART

// On-the-fly path change
// PATH = 19: Digital IN to Headphone OUT + Mic IN to Digital OUT.
// The codec controller powers up automatically the new path. The DAC
// playback is not affected by starting the Mic. recording.
TWI_WRITE 0x52 @ AUTOSTART

// Codec Shutdown. ENAC = 0, STANDBY = 1. The codec turns off smoothly.
// In case of AC Coupling output configuration, HPR & HPL will slowly
// discharge following VMID time constant.
TWI_WRITE 0x20 @ AUTOSTART
WAIT 600ms
// Disable DCBLOCK bit.
TWI_WRITE 0x07 @ AUDIO_CONTROL
// LDO4 shutdown.
TWI_WRITE 0x0C @ VDD4_CONTROL

```

#### 14.2.2 Basic Audio Codec Setting Using Custom Path Control

The following example demonstrates a custom audio path setting. Assuming that the audio codec is supplied by the LDO4, the sequence is the following:

- Make the codec analog and digital interfaces configuration,
- Enter the custom path mode and configure a path with DAC input and Headphone Amplifier output,
- Put the audio codec in standby mode,
- Release the standby mode to re-activate the selected path,
- Change the path on-the-fly to add the microphone inputs to the DAC signal,
- Shutdown the codec.

```

// Start LDO4 @3.3V
TWI_WRITE 0x8C @ VDD4_CTRL

// Digital Audio Interface configuration
// Master clock = 12.288MHz, Master / Slave = slave.
// DAI mode = I2S mode, Word length = 24 bits, FS = 48kHz
TWI_WRITE 0x01 @ DAI_CONTROL
TWI_WRITE 0x63 @ FRAME_CONTROL

// Analog interface configuration
// Mic. config: L & R single ended, Micbias = OFF, Mic. detection = OFF.
// Headphone config: AC coupled,
// Automatic Soft Ramping = ON, ASR timing = 11 (~10ms / step)
TWI_WRITE 0x00 @ MIC_CONTROL
TWI_WRITE 0x27 @ AUDIO_CONTROL

// Analog gain
// Headphone (L & R) gain: -20dB. (LHPBOTH set by default in HP_CONTROL)
// Mic L & R gain: +26 dB.
// Unmute all gains. No power-up is performed.
TWI_WRITE 0xEC @ HPLVOL
TWI_WRITE 0x1A @ MICLVOL
TWI_WRITE 0x1A @ MICRVOL
TWI_WRITE 0x00 @ MUTE

// Enter the custom path configuration mode
TWI_WRITE 0x2F @ AUDIO_CONTROL

// Audio Start
// ENAC = 1, STANDBY = 1. PATH = 0 (Not read by the audio controller)
// At the first start, VMID capacitor is charged.
// Wait (3.tau) = 300ms with 1uF before standby release. (VMID will be
// discharged only when ENAC = 0.)
// From this point Audio Data can be sent over the Digital audio interface.
TWI_WRITE 0x60 @ AUTOSTART.
WAIT 300ms

// Audio path definition: DAC input to Headphone output. The software sets
// the bits: ONDAACL, ONDACR, ONHPL, ONHPR and PLAYBACK by writing
// the registers INPUT_CONTROL, OUTPUT_CONTROL, and INPUT_MIXER.
// The changes are not taken immediately into account (ENCONF = 0).
TWI_WRITE 0x40 @ INPUT_CTRL
TWI_WRITE 0x2F @ OUTPUT_CTRL
TWI_WRITE 0x00 @ INPUT_MIXER

// ENCONF pulse: the audio controller takes the requested changes into

```

```
// account.
TWI_WRITE 0x3F @ AUDIO_CONTROL
TWI_WRITE 0x2F @ AUDIO_CONTROL

// STANDBY release. The codec softly starts.
TWI_WRITE 0x40 @ AUTOSTART.

// Codec Pause by Standby
// All gains are softly ramped down to mute. The codec functions are
// shut down. Current consumption is reduced to a few hundreds of micro-
// amps. VMID remains charged
TWI_WRITE 0x60 @ AUTOSTART

// Pause out: Standby release. The codec softly re-starts.
TWI_WRITE 0x40 @ AUTOSTART

// On-the-fly path change: the stereo microphone inputs are added to the
// DAC playback. The software sets: ONMICL, ONMICR, and ONSIDETONE.
TWI_WRITE 0x70 @ INPUT_CTRL
TWI_WRITE 0x6F @ OUTPUT_CTRL
TWI_WRITE 0x00 @ INPUT_MIXER

// Sidetone gain
TWI_WRITE 0x00 @ SIDETONE_VOL

// ENCONF pulse: the audio controller takes the requested changes into
// account. The path modification is here immediate because STANDBY=0.
TWI_WRITE 0x3F @ AUDIO_CONTROL
TWI_WRITE 0x2F @ AUDIO_CONTROL

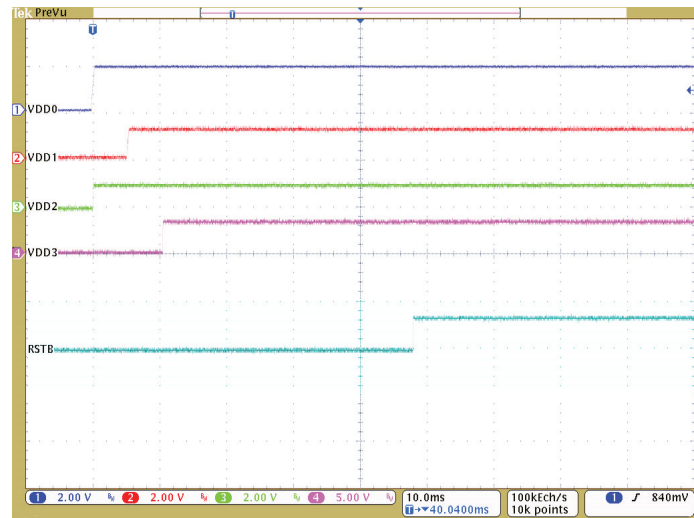
// Codec Shutdown. ENAC = 0, STANDBY = 1. The codec turns off smoothly.
// In case of AC Coupling output configuration, HPR & HPL will slowly
// discharge following VMID time constant.
TWI_WRITE 0x20 @ AUTOSTART
WAIT 600ms
// Disable DCBLOCK bit.
TWI_WRITE 0x07 @ AUDIO_CONTROL
// LDO4 shutdown.
TWI_WRITE 0x0C @ VDD4_CONTROL
```



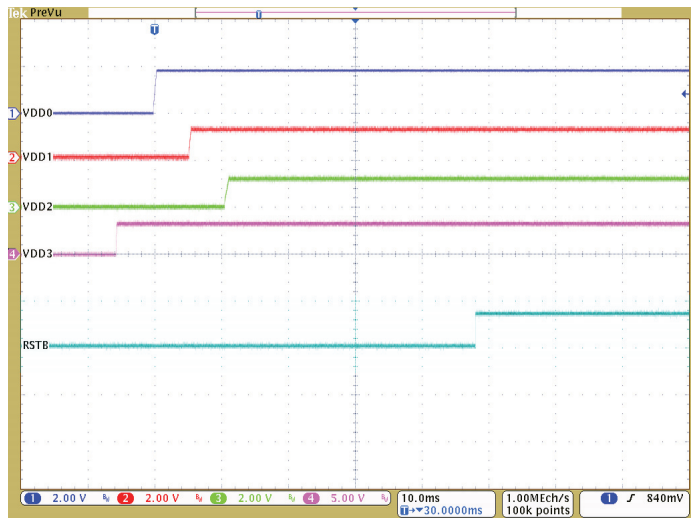
## 15. Typical Performance Characteristics

### 15.1 PMU: Power Supply Sequences

Figure 15-1. Powerdown State to Run State Supplies Start-Up

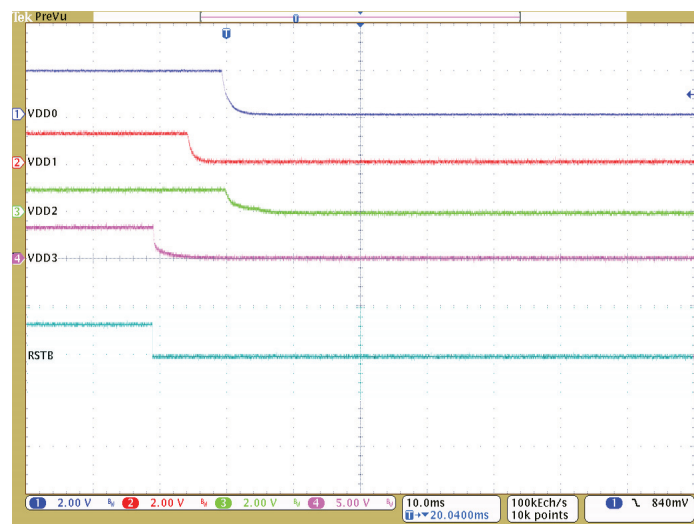


Powerdown to Run State  
SEQUENCE A

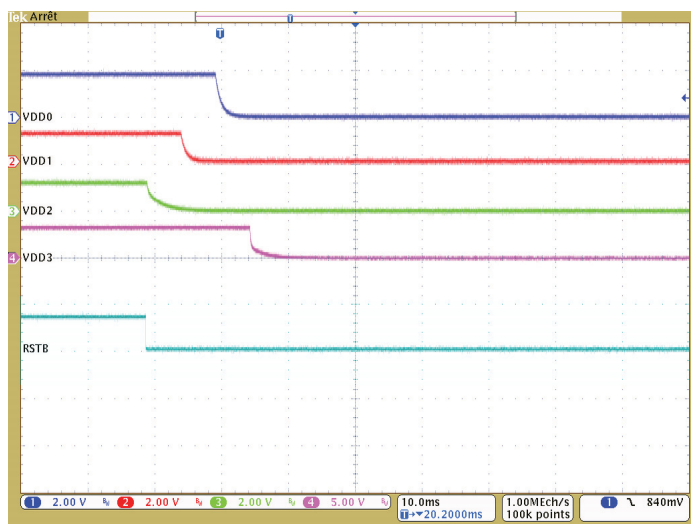


Powerdown to Run State  
SEQUENCE B

Figure 15-2. Run State to Powerdown State Supplies Shut-Down



Run to Powerdown State  
SEQUENCE A

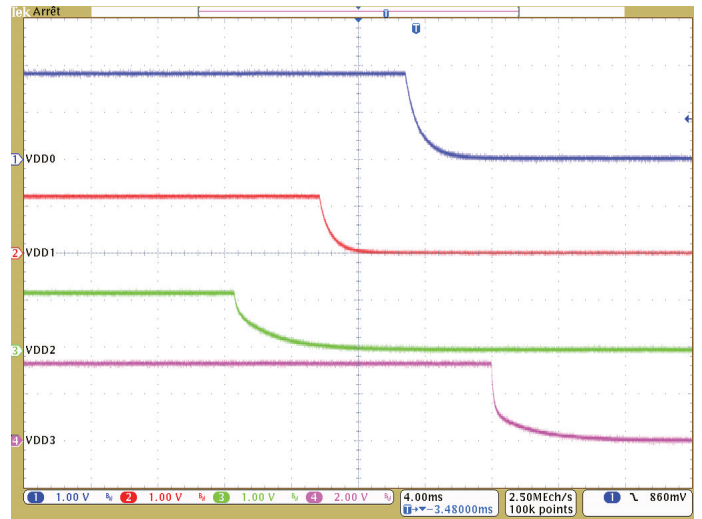


Run to Powerdown State  
SEQUENCE B

**Figure 15-3. Detailed Supplies Start-Up**

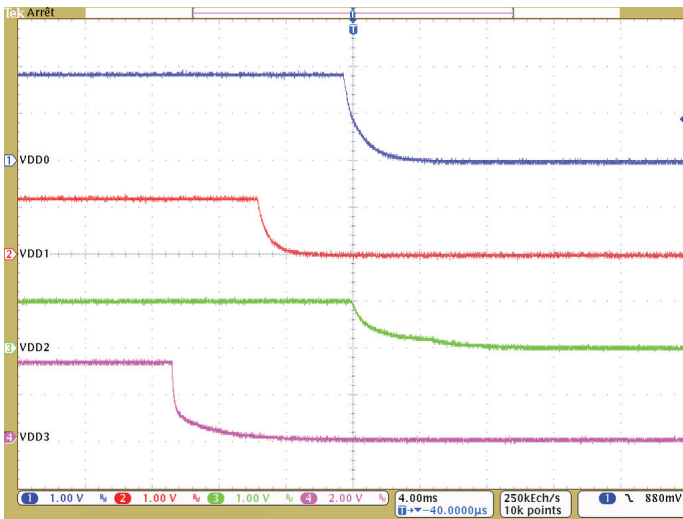


Detailed Supplies Start-Up  
SEQUENCE A

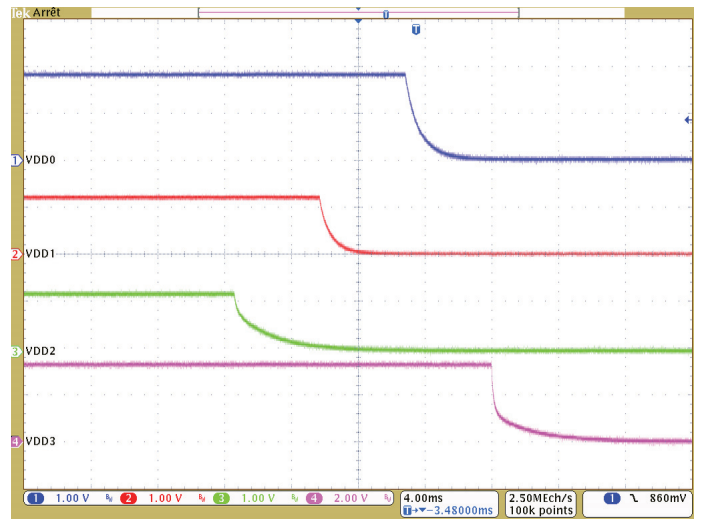


Detailed Supplies Start-Up  
SEQUENCE B

**Figure 15-4. Detailed Supplies Shutdown**



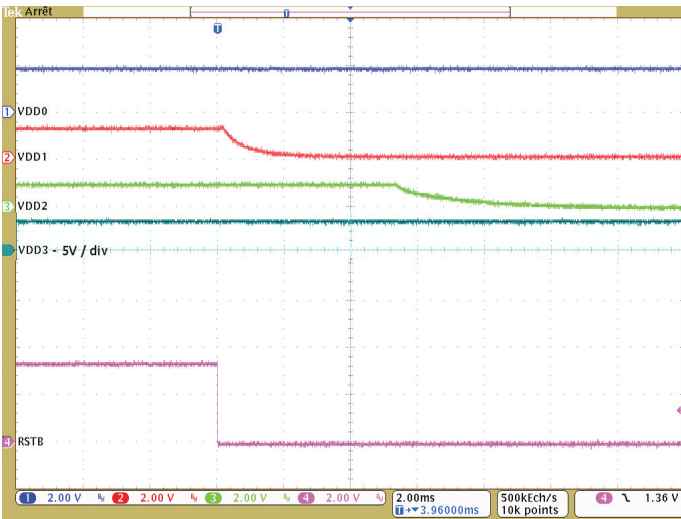
Detailed Supplies Shutdown  
SEQUENCE A



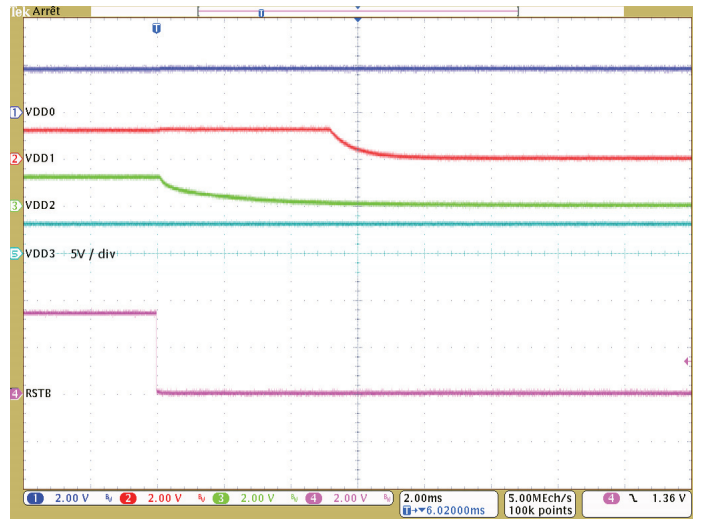
Detailed Supplies shutdown  
SEQUENCE B



Figure 15-5. Run State to Standby State

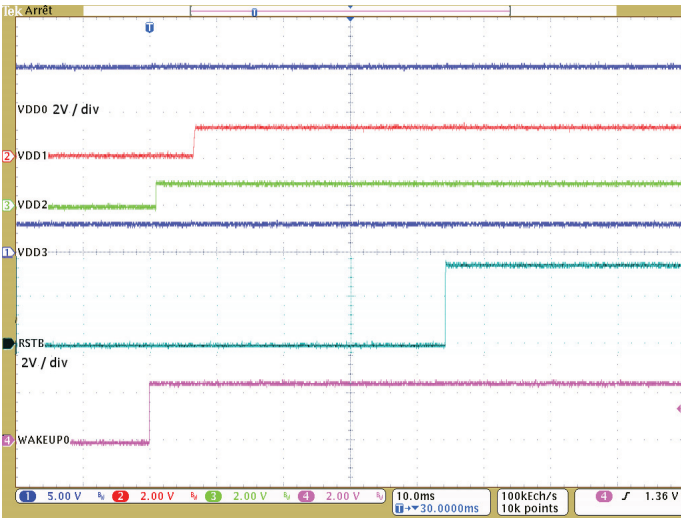


Run To Standby State (default setting)  
SEQUENCE A

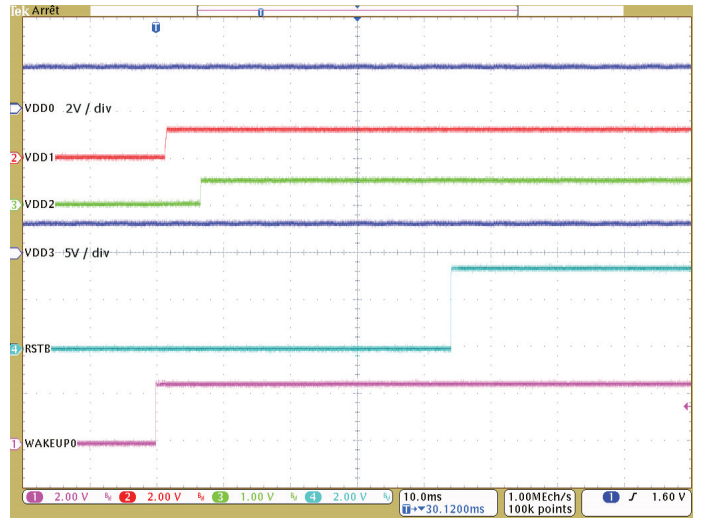


Run To Standby State (default setting)  
SEQUENCE B

Figure 15-6. Standby To Run State



Standby To Run State (default setting)  
SEQUENCE A

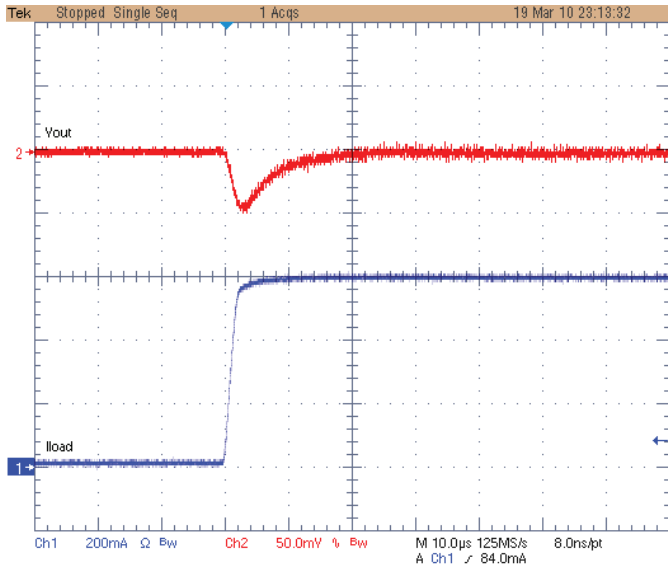


Standby To Run State (default setting)  
SEQUENCE B

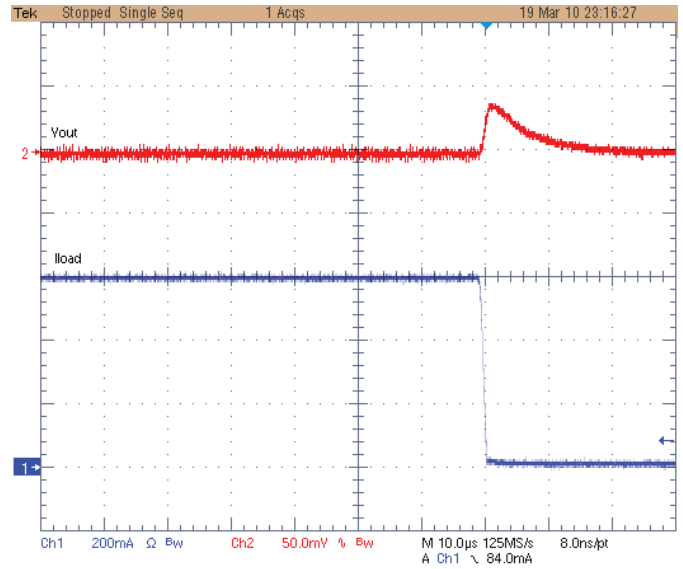
## 15.2 DCDC0 and DCDC1

Unless otherwise noted, the reported measurement were performed at room temperature. External components are those described in [Section 5. "Application Block Diagram" on page 8.](#)

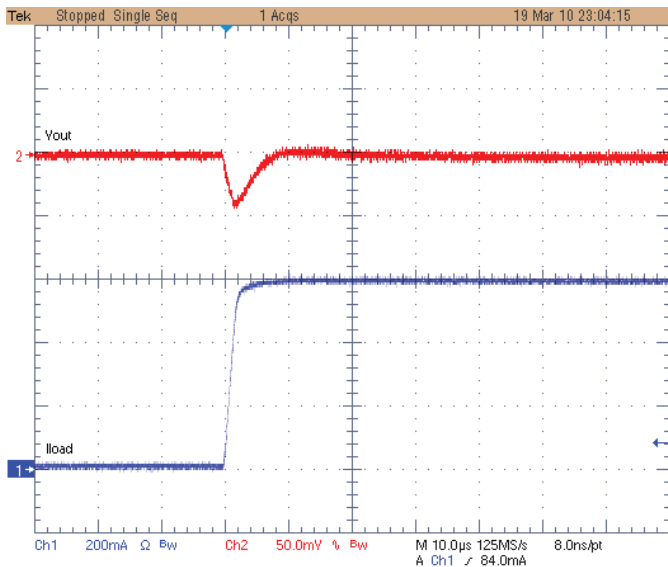
**Figure 15-7.** DCDC0 Transient Load Regulation Performance



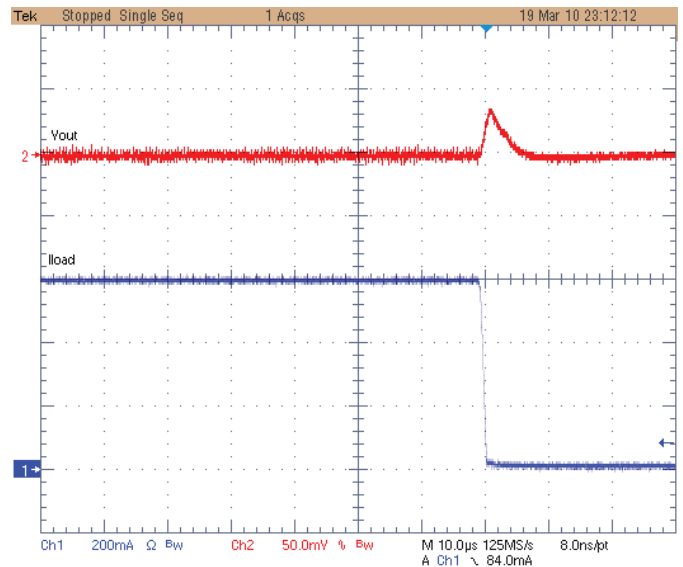
DCDC0 - VIN = 3.3V - VOUT = 1.85V  
Load Step 0 To 600mA / 1us



DCDC0 - VIN = 3.3V - VOUT = 1.85V  
Load Step 600 To 0mA / 1us

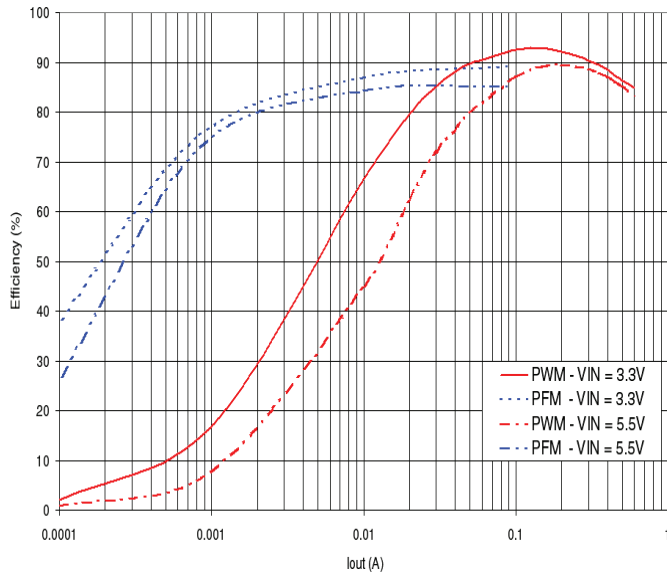


DCDC0 - VIN = 5.5V - VOUT = 1.85V  
Load Step 0 To 600mA / 1us

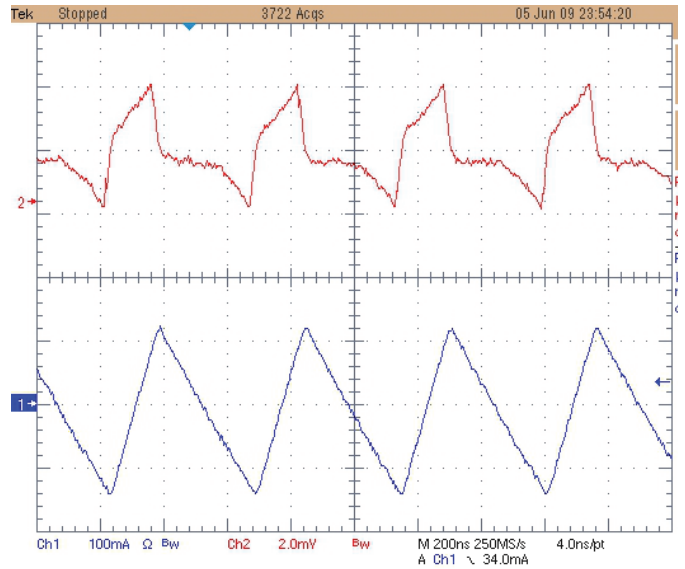


DCDC0 - VIN = 5.5V - VOUT = 1.85V  
Load Step 600 To 0mA / 1us

Figure 15-8. DCDC0 Ripple and Efficiency Performance

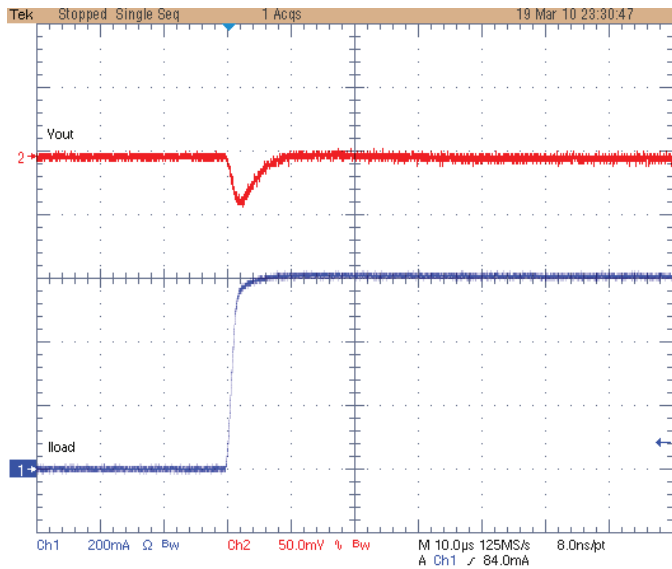


DCDC0 - V<sub>OUT</sub> = 1.8V  
Efficiency in PFM and PWM modes

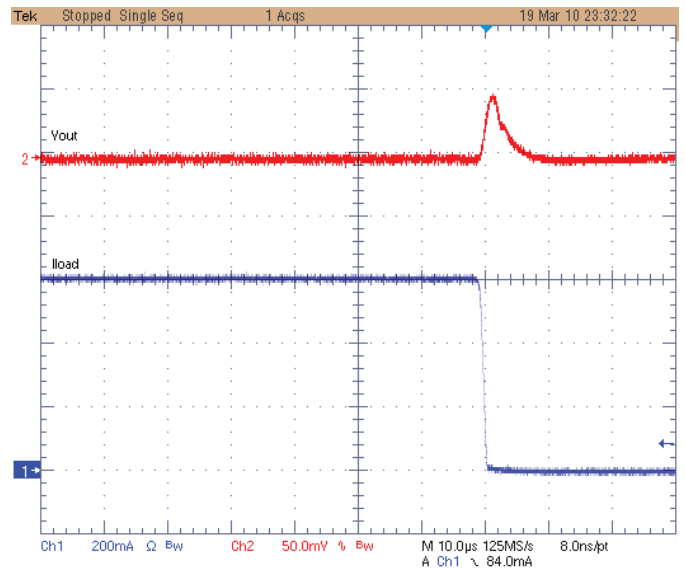


DCDC0 - VIN = 5.5V - V<sub>OUT</sub> = 1.8V  
Output Voltage Ripple

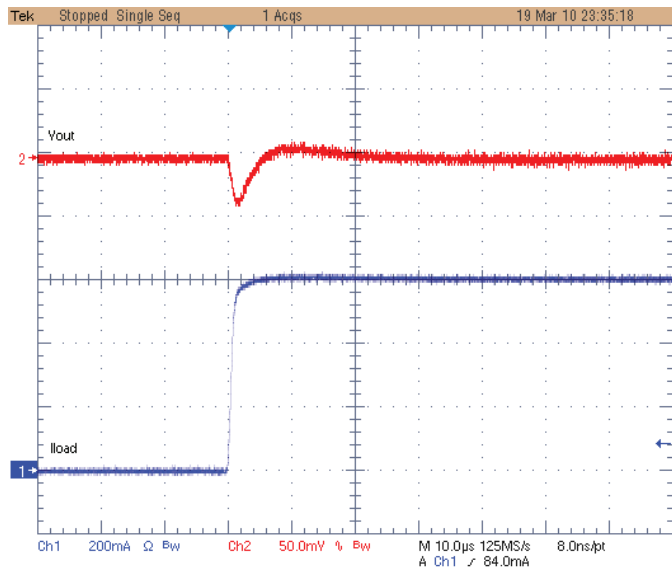
**Figure 15-9. DCDC1 Transient Load Regulation Performance**



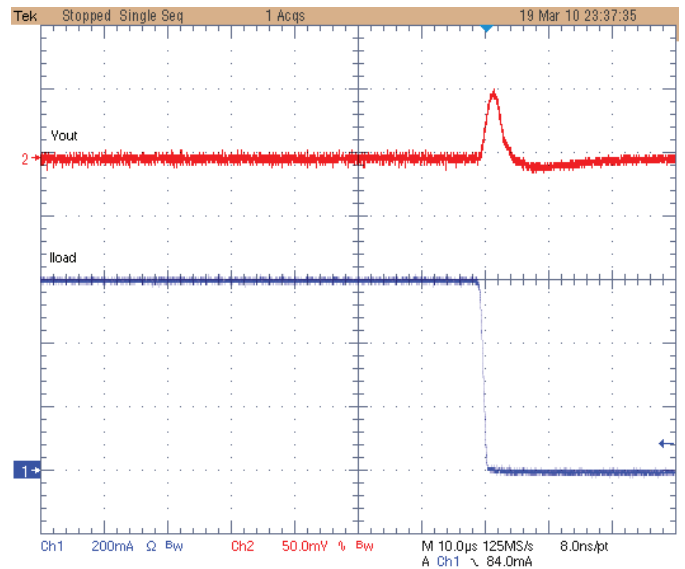
DCDC0 - VIN = 3.3V - VOUT = 1.2V  
Load Step 0 To 600mA / 1µs



DCDC0 - VIN = 3.3V - VOUT = 1.2V  
Load Step 600 To 0mA / 1µs

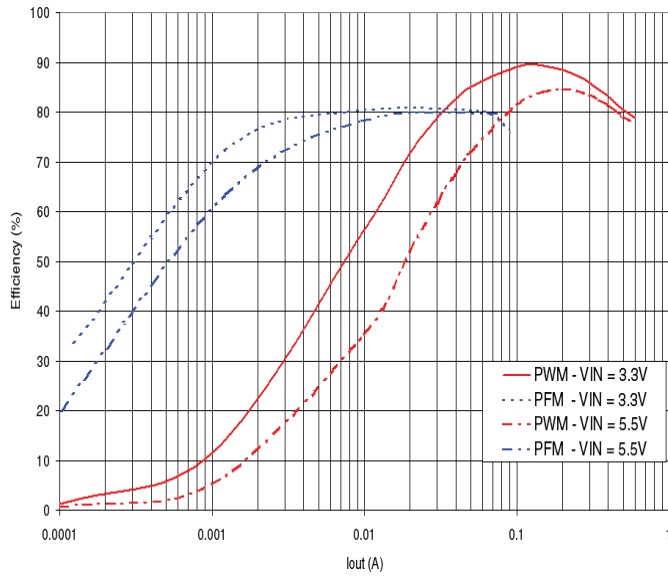


DCDC0 - VIN = 5.5V - VOUT = 1.2V  
Load Step 0 To 600mA / 1µs

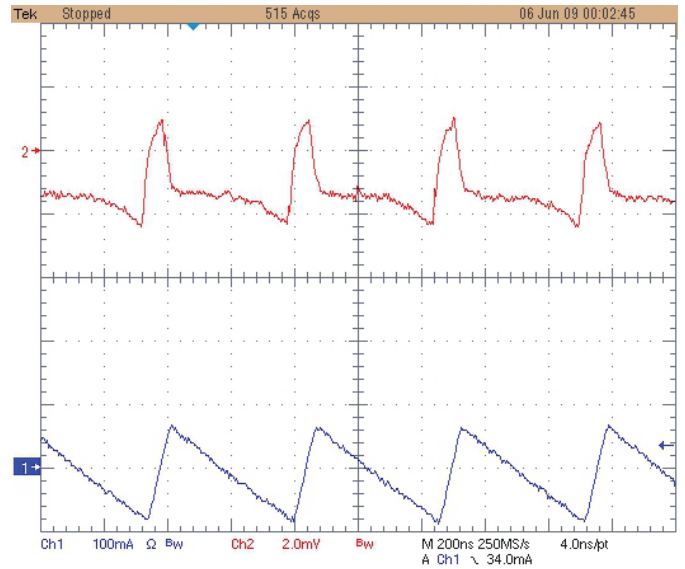


DCDC0 - VIN = 5.5V - VOUT = 1.2V  
Load Step 600 To 0mA / 1µs

Figure 15-10. DCDC0 Ripple and Efficiency Performance



DCDC1 - V<sub>OUT</sub> = 1.2V  
Efficiency in PFM and PWM modes

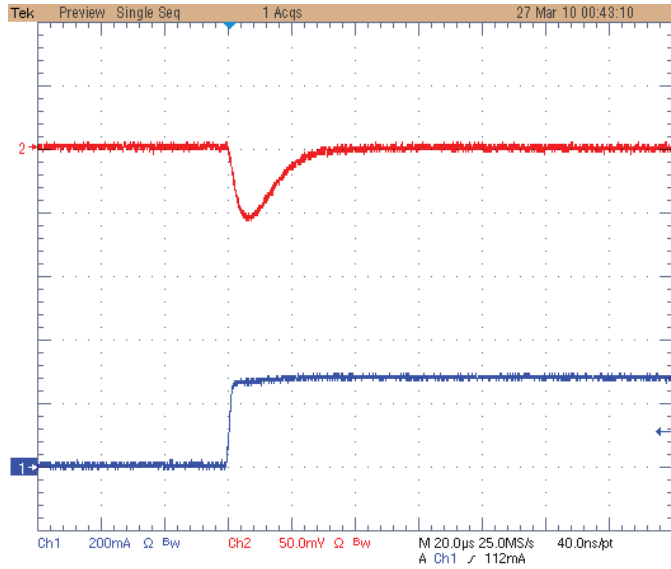


DCDC1 - V<sub>IN</sub> = 5.5V - V<sub>OUT</sub> = 1.2V  
Output Voltage Ripple

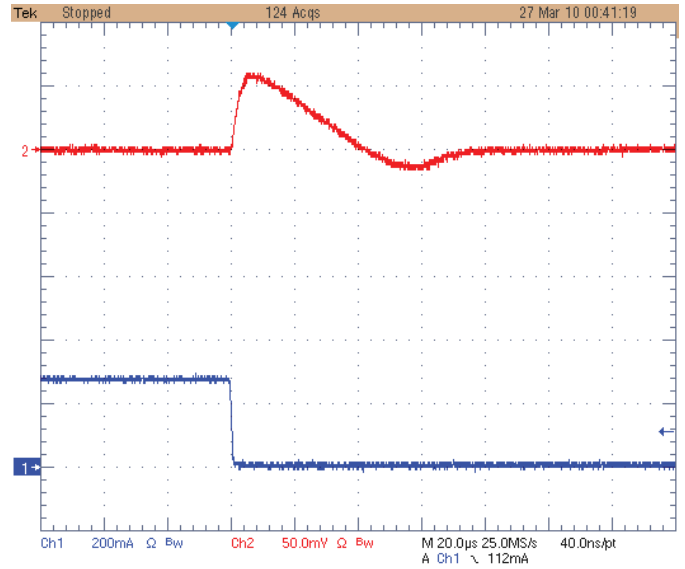
### 15.3 LDO2

Unless otherwise noted, the reported measurement were performed at room temperature. External components are those described in Section 5. "Application Block Diagram" on page 8.

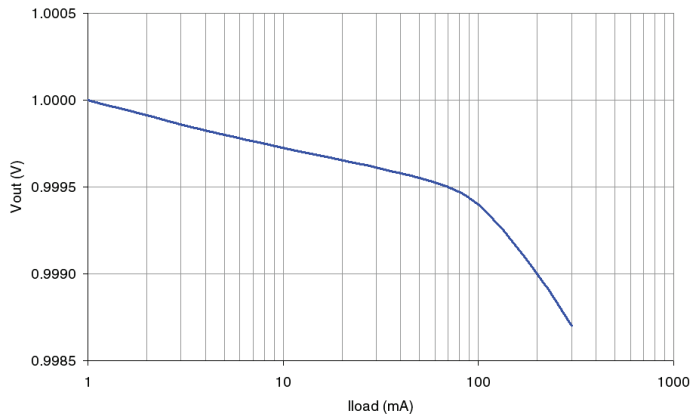
**Figure 15-11. LDO2 Tansient and Static Load Regulation Performance**



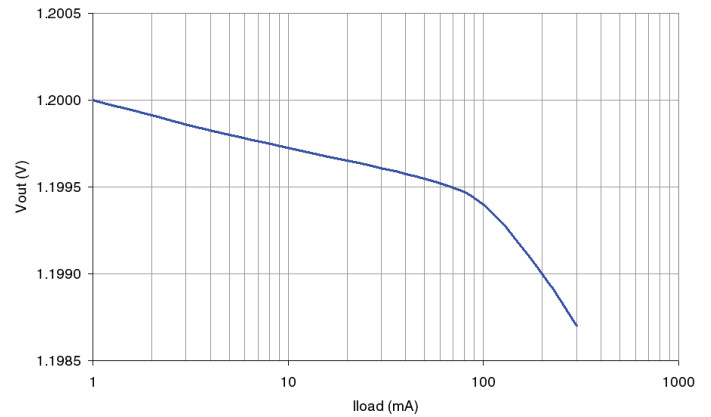
LDO2- VIN = 1.8V - VOUT = 1V  
Load Step 0 To 300mA / 1us



LDO2 - VIN = 1.8V - VOUT = 1V  
Load Step 300 To 0mA / 1us



LDO2 - VIN = 1.8V - VOUT = 1V  
Static Load Regulation - 0 To 300mA

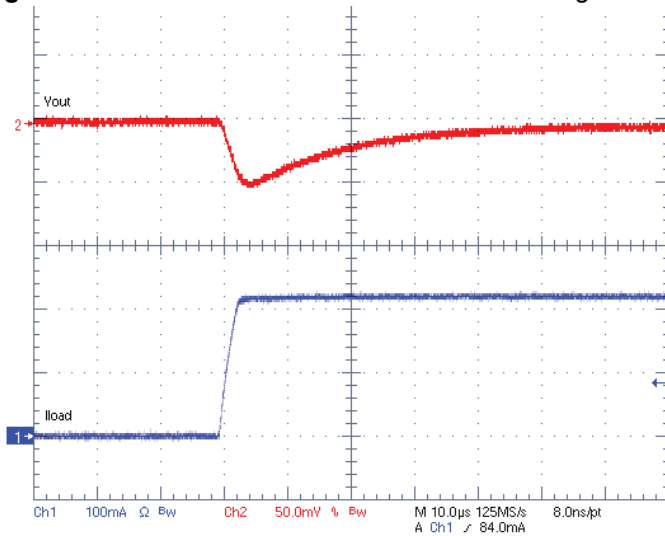


LDO2 - VIN = 1.7V - VOUT = 1.2V  
Static Load Regulation - 0 To 300mA

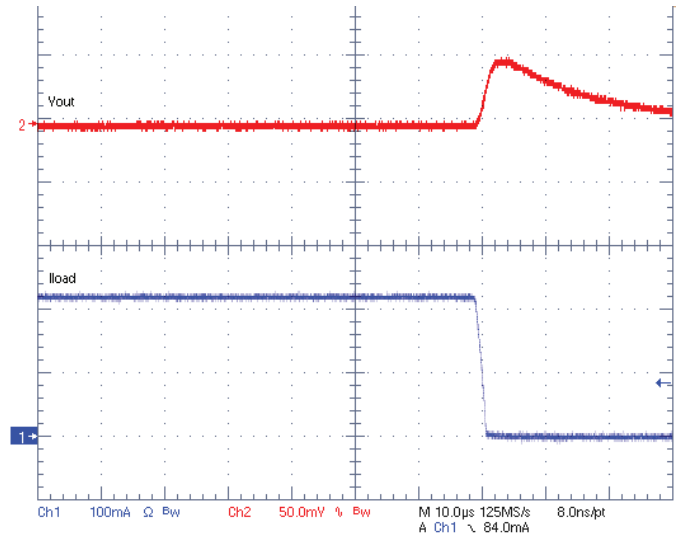
### 15.4 LDO3

Unless otherwise noted, the reported measurement were performed at room temperature. External components are those described in Section 5. "Application Block Diagram" on page 8.

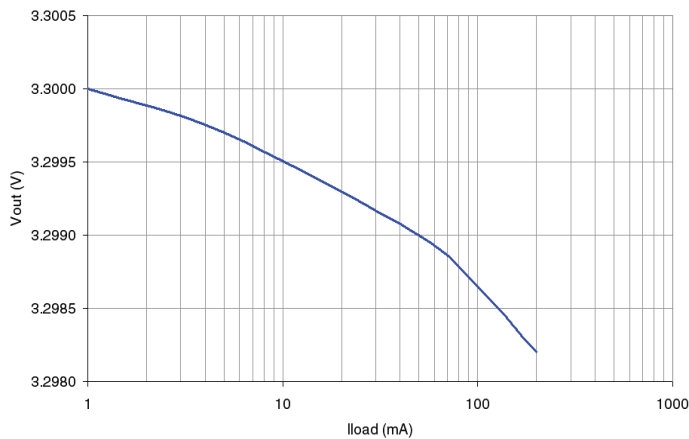
Figure 15-12. LDO3 Transient and Static Load Regulation Performance



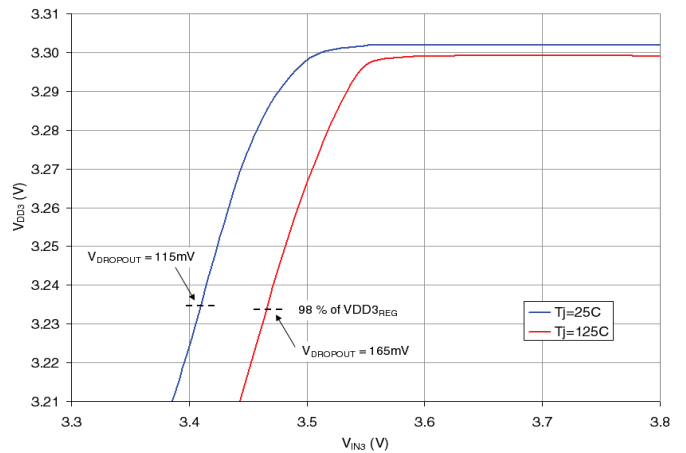
LDO3- VIN = 5.5V - VDD3 = 3.3V  
Load Step 0 To 200mA / 1us



LDO3 - VIN = 5.5V - VDD3 = 3.3V  
Load Step 200 To 0mA / 1us



LDO3 - VIN = 3.6V - VDD3 = 3.3V  
Static Load Regulation - 0 To 200mA

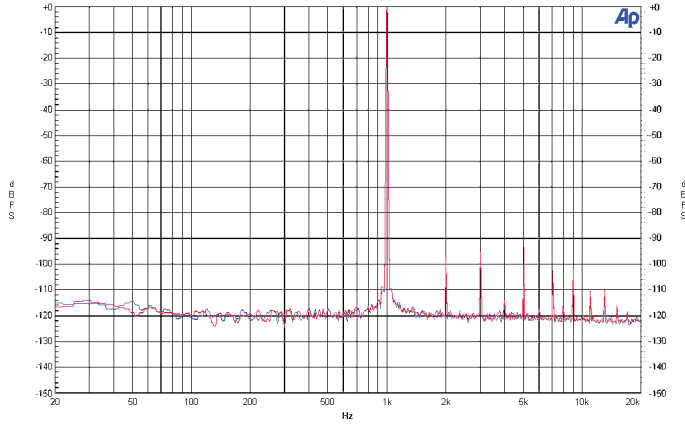


LDO3 - VDD3 = 3.3V - 200mA output load  
Drop Out Characteristic.  
(VDD3<sub>REG</sub> = VDD3 with VIN3 > VDD3 + 300mV)

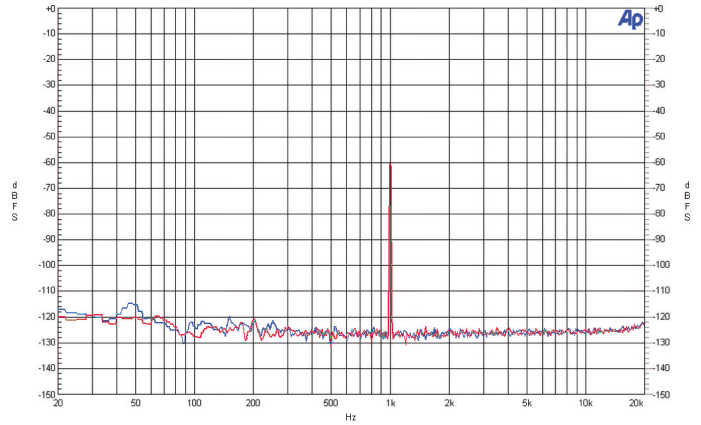
## 15.5 AUDIO

Unless otherwise noted, the reported measurement were performed at room temperature with AVDD = 3.3V supplied from LDO4. Typical components as described in Section 5. “Application Block Diagram” on page 8 are used.

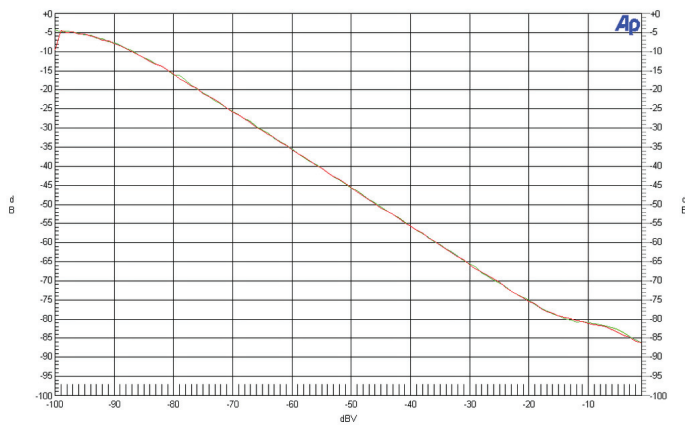
**Figure 15-13. Microphone Recording Waveforms**



Differential Microphone Recording ( Path 5)  
-1dBV / 1kHz Input - Fs = 48kHz - 16kpts FFT



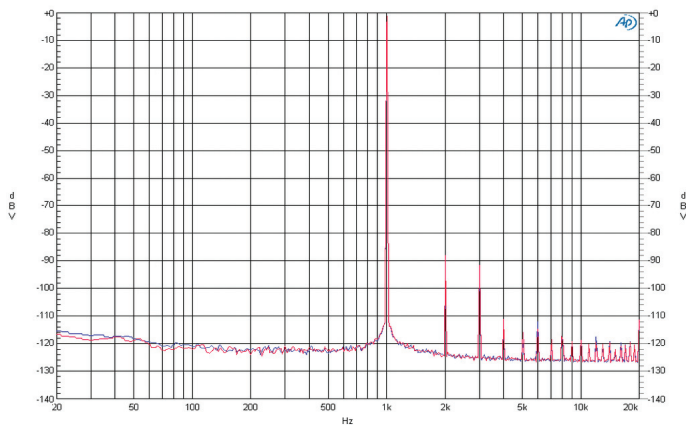
Differential Microphone Recording ( Path 5)  
-60dBV / 1kHz Input - Fs = 48kHz - 16kpts FFT



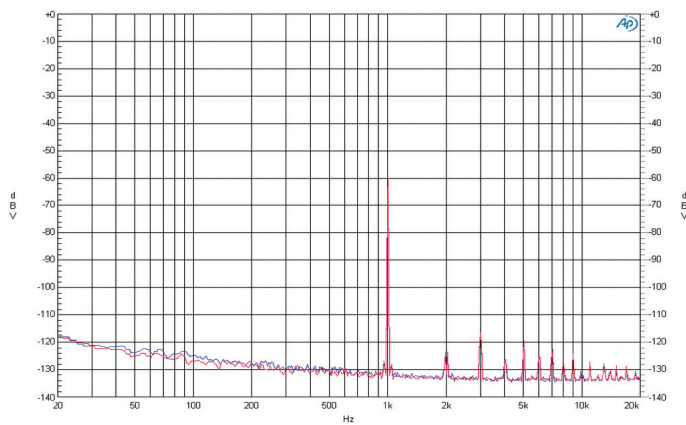
Differential Microphone Recording ( Path 5)  
THD+N Ratio Versus Input Level



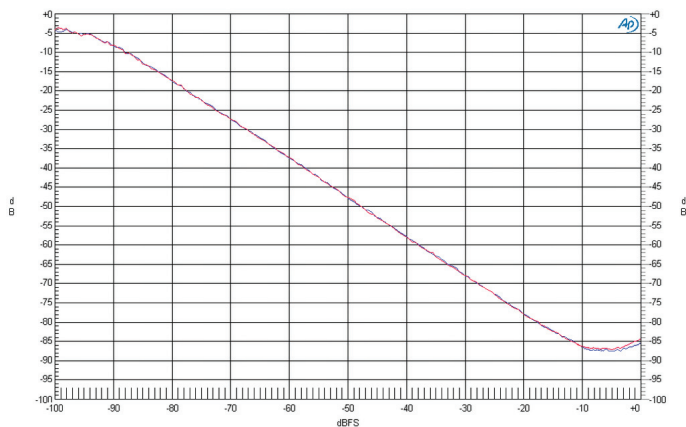
**Figure 15-14. DAC Playback Waveforms**



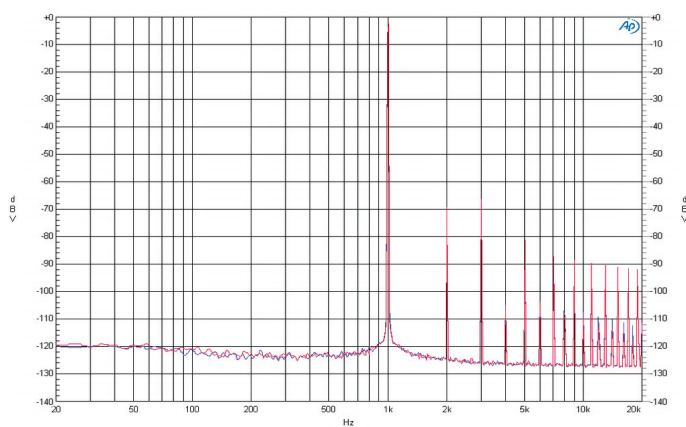
DAC playback ( Path 1) - Load 10k  
0 dBFs / 1kHz Input - Fs = 48kHz - 32kpts FFT



DAC playback ( Path 1) - Load 10k  
-60 dBFs / 1kHz Input - Fs = 48kHz - 32kpts FFT

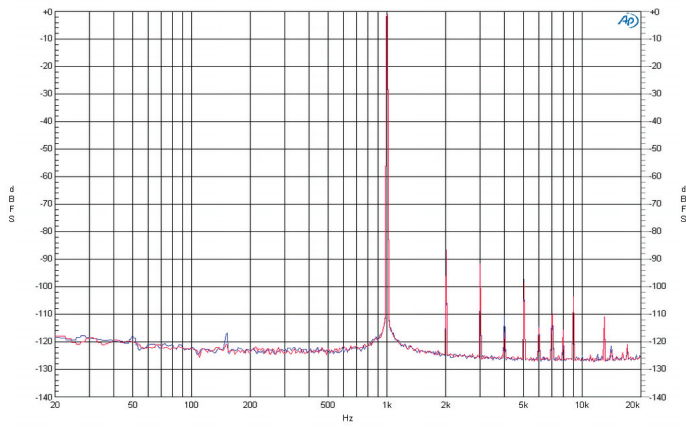


DAC playback ( Path 1) - Load 10k  
THD+N Ratio Versus Input Level

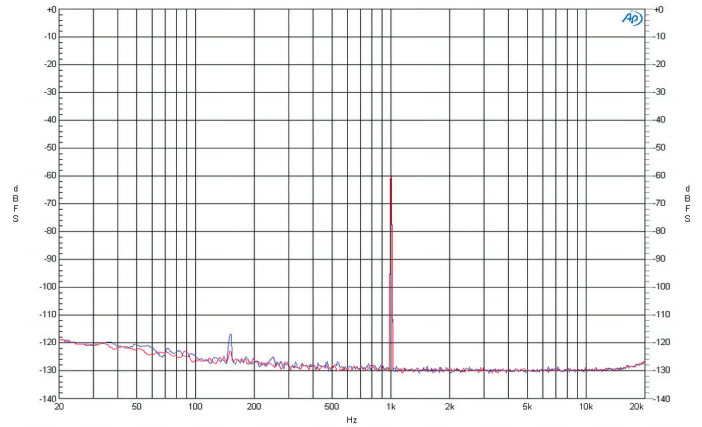


DAC playback ( Path 1) - Load 32 Ohms AC coupled  
20mW Ouput Power - Fs = 48kHz - 32kpts FFT

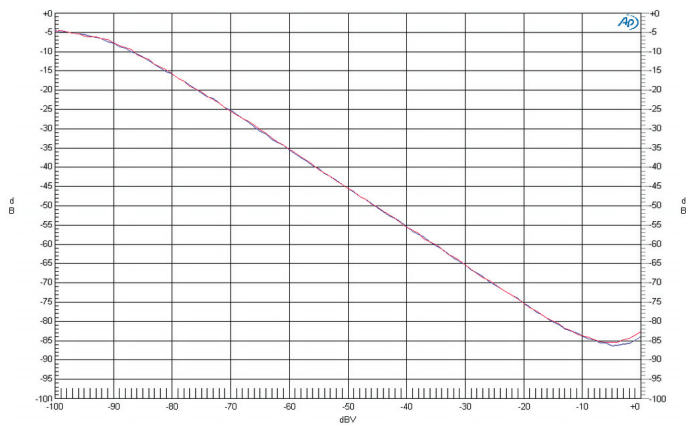
**Figure 15-15. Line Record Waveforms**



Line Record (path 7)  
-1 dBV / 1kHz Input -  $F_s = 48\text{kHz}$  - 32kpts FFT

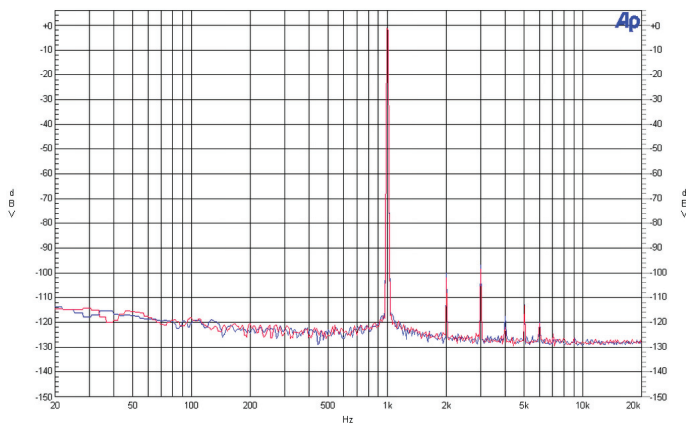


Line Record (path 7)  
-60 dBV / 1kHz Input -  $F_s = 48\text{kHz}$  - 32kpts FFT

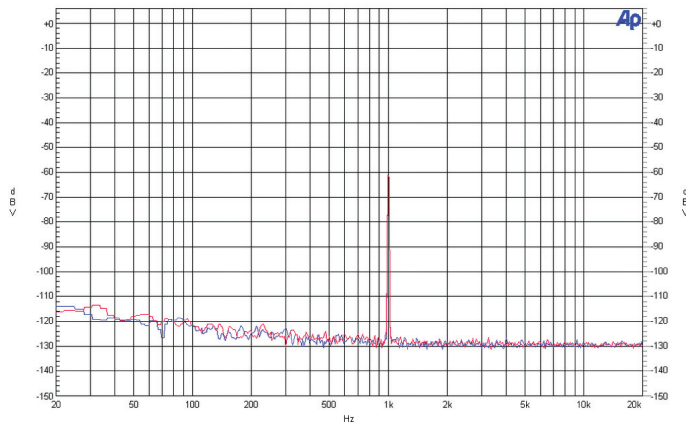


Line Record (path 7)  
THD+N Ratio Versus Input Level

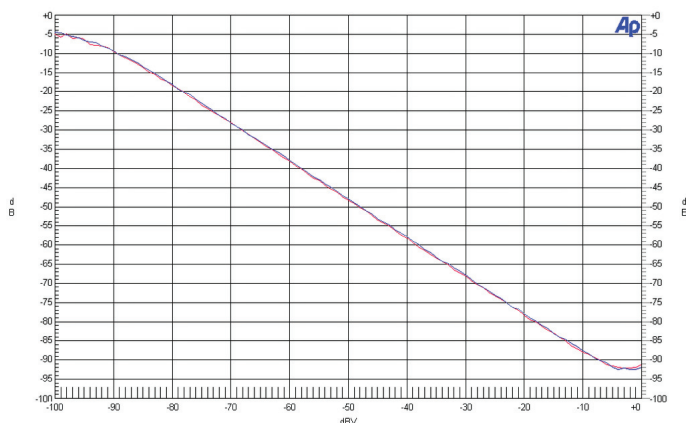
**Figure 15-16. Line Bypass Waveforms**



Line Bypass (path 5)  
0 dBV / 1kHz Input - 10k load - 16kpts FFT



Line Bypass (path 5)  
-60 dBV / 1kHz Input - 10k load - 16kpts FFT

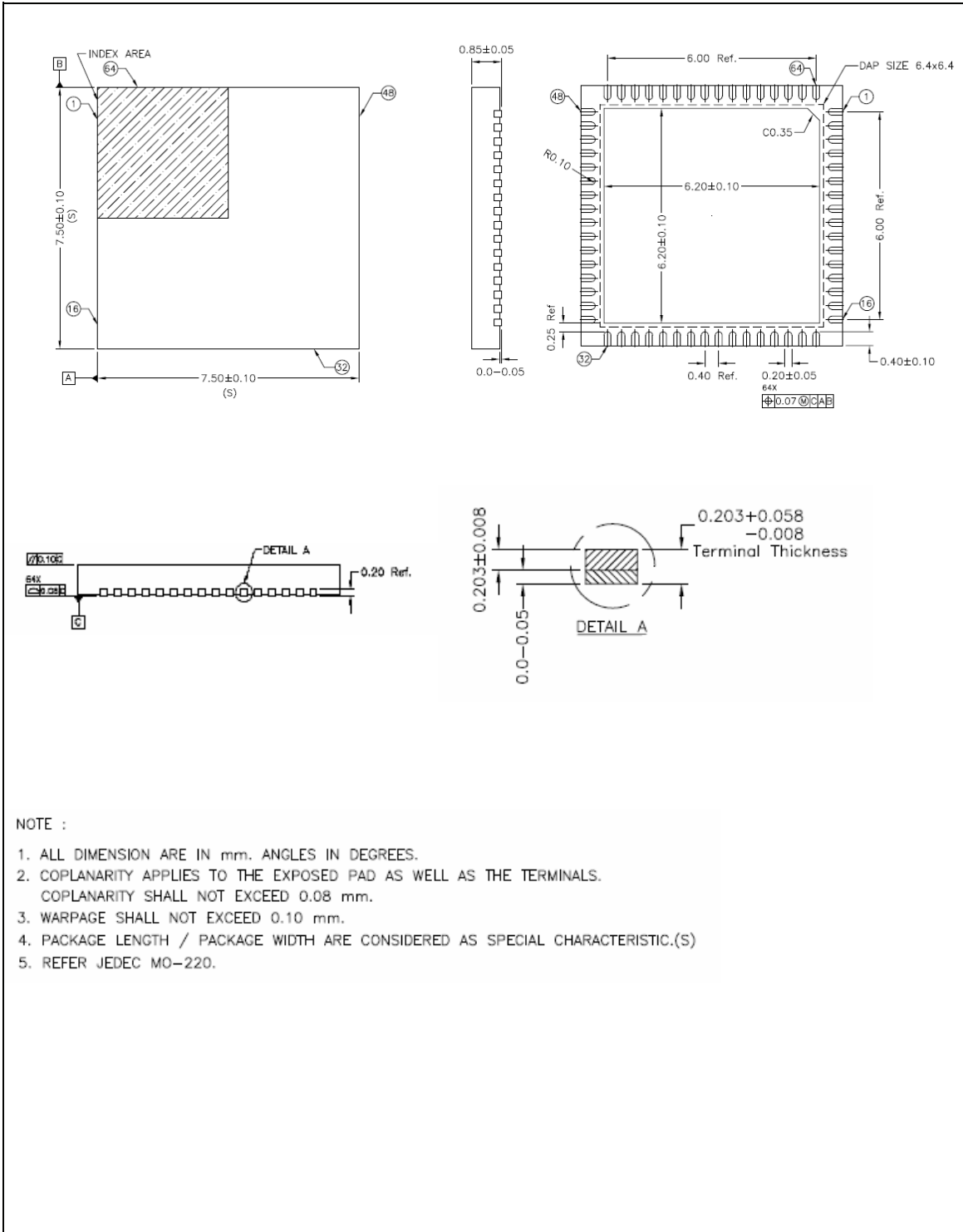


Line Record (path 5) - 10k load  
THD+N Ratio Versus Input Level



## 16. Package Information

Figure 16-1. Mechanical Package Drawing for 64-lead Quad Flat No Lead Package



## 17. Ordering Information

**Table 17-1.** Ordering Information

| Ordering Code and Marking | Package                   | Temperature Operating Range | Supplies Default Values  | Power Sequence Type <sup>(2)</sup> | Software Tag <sup>(1)</sup> |
|---------------------------|---------------------------|-----------------------------|--|------------------------------------|-----------------------------|
| AT73C246                  | QFN64 7.5 x7.5mm<br>Green | -40°C to +85°C              | VDD0 = 1.85V<br>VDD1 = 1.20V<br>VDD2 = 1.00V<br>VDD3 = 3.30V<br>VDD4 = 3.30V               | A                                  | 0000                        |
| AT73C246-A                | QFN64 7.5 x7.5mm<br>Green | -40°C to +85°C              | <b>VDD0 = 1.80V</b><br>VDD1 = 1.20V<br><b>VDD2 = 1.20V</b><br>VDD3 = 3.30V<br>VDD4 = 3.30V | B                                  | 0001                        |
| AT73C246-B                | QFN64 7.5 x7.5mm<br>Green | -40°C to +85°C              | <b>VDD0 = 1.80V</b><br><b>VDD1 = 1.00V</b><br>VDD2 = 1.00V<br>VDD3 = 3.30V<br>VDD4 = 3.30V | B                                  | 0010                        |

- Notes: 1. See "VERSION" (0x7F) register definition.  
 2. See "Power Manager State Description" on page 29 and "Typical Performance Characteristics" on page 139.

## 18. Revision History

**Table 18-1.** Revision History

| <b>Doc. Rev</b> | <b>Date</b> | <b>Comments</b> | <b>Change Request Ref.</b> |
|-----------------|-------------|-----------------|----------------------------|
| 11050A          | 07-Apr-10   | First issue     |                            |







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