T-51-09-90

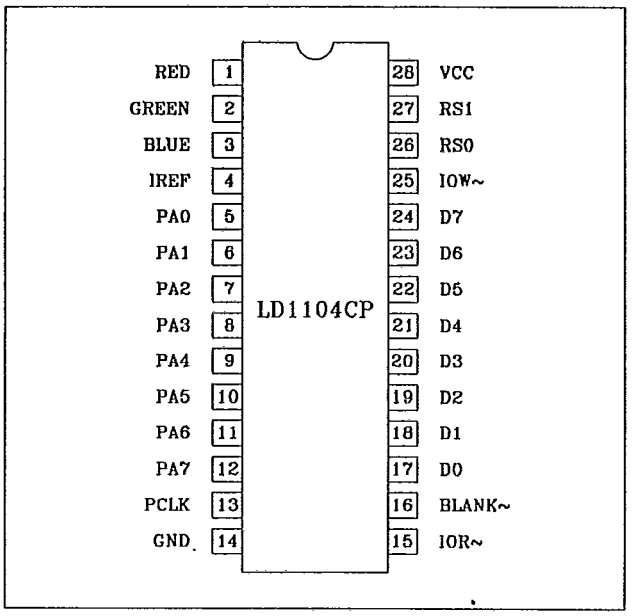
SILICON LOGIC™

LD1104

VIDEO DAC WITH LOOK-UP TABLE

DESCRIPTION

The LD1104 is a digital to analog converter with an internal look-up table designed to drive a 75 ohm line. The output of the DAC is designed to produce 0.7 volts peak white amplitude when driving a 75 ohm line with an IREF of 4.4 mA or when driving a doubly terminated 75 ohm load with an IREF of 8.8 mA. The DAC outputs will be set to their minimum values during the blanking pulse period.



FEATURES

* Pin to pin compatible with IMS G171/G176
* 256K possible colors
* Microprocessor compatible interface
* Low power CMOS design
* 6 bit DAC per gun and RGB analog output
* Pixel rates up to 65 MHz
* Pixel word mask
* TTL compatible inputs
* Single 5 volts operating voltage

APPLICATIONS

* VGA graphic card
* Workstations with color output
* Color terminals
* Raster scan video systems

ORDERING INFORMATION

Part number	Package	Operating temperature
LD1104CP28-65	Plastic	0°C to 70°C
LD1104CJ44-65	PLCC	0°C to 70°C
LD1104CP28-50	Plastic	0°C to 70°C
LD1104CJ44-50	PLCC	0°C to 70°C

GENERAL DESCRIPTION

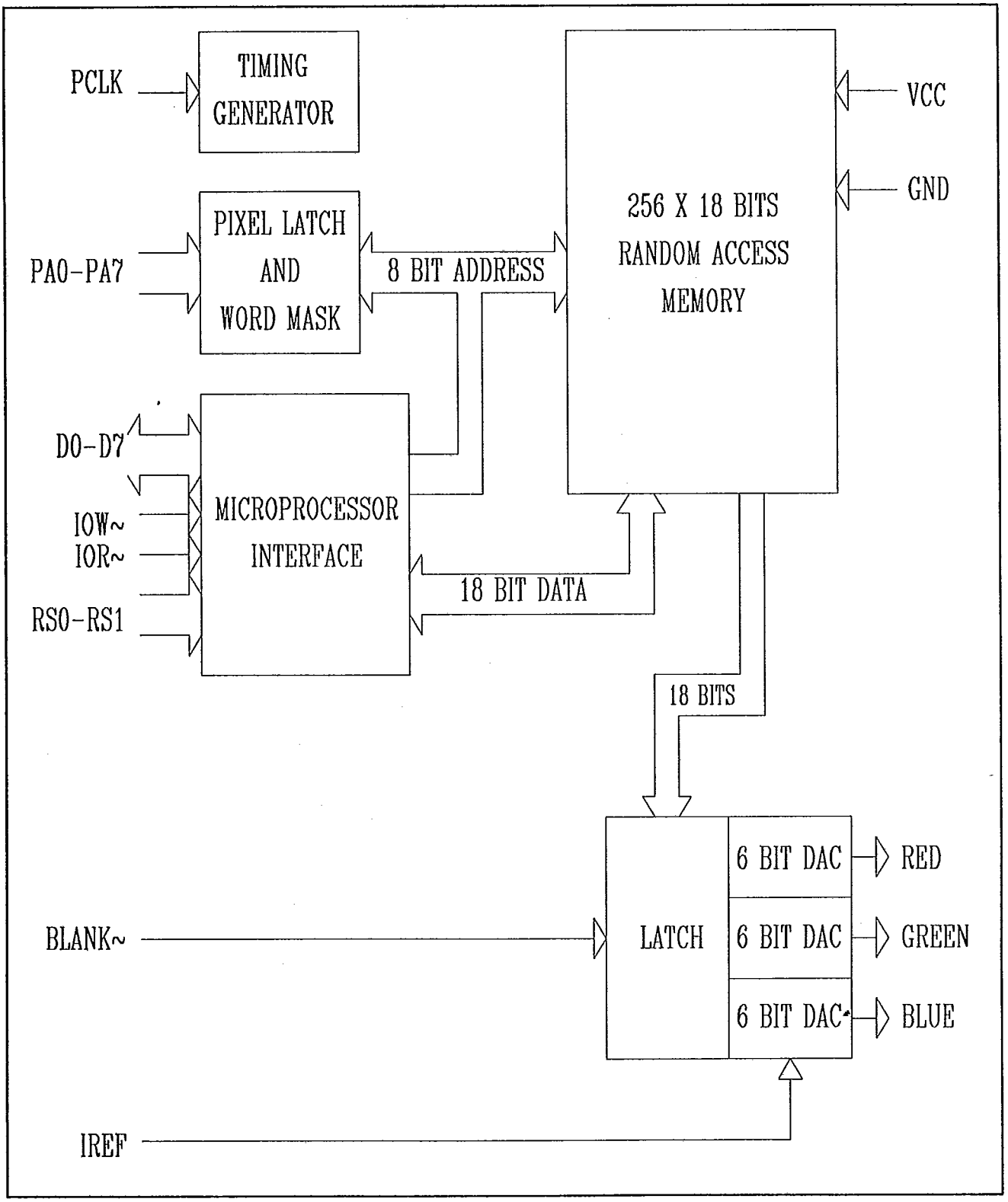
The LD1104 is designed to operate in a high speed analog and digital video interface environment to provide 256 different colors.

The display colors can be changed to facilitate animation, flashing or overlay objects with a single write cycle, by utilizing the pixel word mask capability without modifying the look-up table. A high speed internal random access memory has been provided to pipeline a 65 MHz pixel rate output in three clock cycles. An external blanking signal can be input to the LD1104 to synchronize the pixel stream.

The contents of the look-up table (random access memory) can be accessed via an 8 bit wide microprocessor interface bus without disturbing the video path.

LD1104

BLOCK DESCRIPTION



SYMBOL DESCRIPTION

Symbol	Pin	Symbol type	Pin description
RED	1	O	Video DAC RED signal output.
GREEN	2	O	Video DAC GREEN signal output.
BLUE	3	O	Video DAC BLUE signal output.
IREF	4	I	Reference current input. The external current source is applied to this pin to regulate the internal DAC current source. Each current source produces 1/30 of the IREF when turned on.
PA0-PA7	5-12	I	Pixel address. The byte wide value sampled on these inputs is masked by the pixel Mask Register and then used as the address into the color look-up table.
PCLK	13	I	Pixel clock. The pixel address and blanking inputs are sampled at the rising edge of PCLK.
GND	14	O	Ground. Signal and power ground.
IOR~	15	I	I/O read strobe. (active low) A low on this pin will transfer the contents of the addressed memory or the color information to the data bus.
BLANK~	16	I	Blanking input. (active low) A low level on this input, when sampled at the rising edge of PCLK, will cause a color value of zero to be applied to the inputs of the three DACs regardless of the color value of the current pixel.
D0-D7	17-24	I/O	Bidirectional I/O data bus. The contents of the data bus are transferred from the LD1104 internal registers to the host processor or vice-versa.
IOW~	25	I	I/O write strobe. (active low) A low on this pin will transfer the contents of the data bus to the addressed register or the internal memory (RAM).
RS0	26	I	Least significant bit of the register select.
RS1	27	I	Most significant bit of the register select.
V_{cc}	28	I	Power supply input.

LD1104

REGISTERS PROGRAMMING TABLE:

RS1	RS0	IOW~	IOR~
0	0	PIXEL ADDRESS A	PIXEL ADDRESS A
0	1	COLOR VALUE	COLOR VALUE
1	0	PIXEL MASK	
1	1	PIXEL ADDRESS B	PIXEL ADDRESS B

REGISTER DESCRIPTIONS

PIXEL ADDRESS REGISTER A/B

The contents of the PIXEL ADDRESS REGISTER A are identical to the contents of the PIXEL ADDRESS REGISTER B during the read operation.
Writing to PIXEL ADDRESS A will specify an address within the color look-up table and initializes the color value register. Writing into PIXEL ADDRESS REGISTER B specifies an address within the color look-up table and loads the color value register with the contents of the location in the color look-up table address and then increments the PIXEL ADDRESS REGISTER.

COLOR VALUE REGISTER

The color value register is internally an 18 bit wide (6 bits per color) register used as a buffer between the microprocessor interface and the color look-up table. To perform a read or write to this register it is required to have a sequence of three byte transfers from or to the register. Note that only the six least significant bits of the bus are used during the write mode and the rest are set to zero during the read mode. The internal address pointer is set to the RED color address and then increments to the GREEN and BLUE color addresses regardless of the read or write operation sequence.
After writing three values to this register its contents are written to the location in the color look-up table specified by the pixel address register and copied into the COLOR VALUE REGISTER. The PIXEL ADDRESS REGISTER then increments.

PIXEL MASK REGISTER

The PIXEL MASK REGISTER can be used to mask selected bits of the pixel address value applied to the PIXEL ADDRESS input (PA7-PA0). The PIXEL MASK REGISTER is logically anded with the PIXEL ADDRESS bits, writing a zero in each bit position will alter the values to zero. Note that writing a one to this register will not alter the PIXEL ADDRESS bits.

WRITING TO THE LOOK-UP TABLE

The color of each pixel can be changed by specifying the location (address of the pixel) in the look-up table via PIXEL ADDRESS REGISTER A. The intensity of each color (RED, GREEN, BLUE) should be written successively in the COLOR VALUE REGISTER (note that three 8 bit data are required). After the last value (BLUE) the address of the PIXEL ADDRESS REGISTER is incremented automatically to reduce the write cycle for consecutive pixel color changes.

READING FROM THE LOOK-UP TABLE

The color intensity of each pixel can be read by writing the location (address of the pixel) in the look-up table via PIXEL ADDRESS REGISTER B. The color values (intensity) of each color gun (RED, GREEN, BLUE) can be accessed from the COLOR VALUE REGISTER (note that, three consecutive reads are required to complete the read cycle). After reading the last value (BLUE) the PIXEL ADDRESS REGISTER B is incremented to reduce the read cycle for consecutive pixel reads. The read cycle can be reduced if fewer values are needed to be read by changing the PIXEL ADDRESS REGISTER B. This will terminate the previous read cycle.

T-51-09-90

AC ELECTRICAL CHARACTERISTICS

T_A=25°C , V_{CC}=5.0 V± 5% unless otherwise specified

Symbol	Parameters	Limits			Units	Conditions
		min	typ	max		
T_1	PCLK period	20		10000	nS	
T_2	PCLK jitter			±2.5	%	note:1
T_3	PCLK low width	6		10000	nS	
T_4	PCLK high width	6		10000	nS	
T_5	Pixel Word setup time	4			nS	note:2
T_6	Pixel Word hold time	4			nS	note:2
T_7	Blank~ setup time	4			nS	
T_8	Blank~ hold time	4			nS	
T_9	PCLK to valid DAC output	5		30	nS	note:3
T_{10}	Differential output delay			1	nS	note:4
T_{11}	Pixel clock transition time			50	nS	
T_{12}	IOW~ pulse width low	50			nS	
T_{13}	IOR~ pulse width low	50			nS	
T_{14}	Register select setup time	10			nS	
T_{15}	Register select setup time	10			nS	
T_{16}	Register select hold time	10			nS	
T_{17}	Register select hold time	10			nS	
T_{18}	Write data setup time	10			nS	
T_{19}	Write data hold time	10			nS	
T_{20}	Output turn on delay	5			nS	
T_{21}	Read enable access time			40	nS	
T_{22}	Output hold time	5			nS	
T_{23}	Output turn off delay time			20	nS	note:5
T_{24}	Successive write interval	$3*T_1$			nS	
T_{25}	Write followed by read interval	$3*T_1$			nS	
T_{26}	Successive read interval	$3*T_1$			nS	
T_{27}	Read followed by write interval	$3*T_1$			nS	
T_{28}	Write after color write	$3*T_1$			nS	note:6
T_{29}	Read after color write	$3*T_1$			nS	note:6
T_{30}	Read after color read	$3*T_1$			nS	note:6
T_{31}	Write after color read	$3*T_1$			nS	note:6
T_{32}	Read after read address write	$3*T_1$			nS	note:6
T_{33}	Write/Read enable transition time	50			nS	

LD1104

ABSOLUTE MAXIMUM RATINGS

Operating supply range	5 Volts ±5%
Voltage at any pin	GND-0.3V to V_{CC}+0.3V
Storage temperature	-40°C to +150°C
Operating temperature	0°C to 70°C
Package dissipation	500mW

DC ELECTRICAL CHARACTERISTICS

T_A=25°C, V_{CC}=5.0V ± 5% unless otherwise specified

Symbol	Parameters	Limits			Units	Conditions
		min	typ	max		
V_{CC}	Operating supply	4.5	5.0	5.5	V	
I_{CC}	Operating current			190	mA	
I_{REF}	Reference current	4.0	8.8	10	mA	
V_{AO}	DAC output level	1.5			V	
I_{AO}	DAC output current	21			mA	
D_{DTD}	DAC to DAC correlation	±2			%	
D_{DIL}	DAC internal linearity	±0.5			LSB	
I_{IL}	Input Low current	-10			uA	
I_{IH}	Input High current			10	uA	
V_{IL}	Input Low level			0.8	V	
V_{IH}	Input High level	2.0			V	
V_{OL}	Output Low level pin D0-D7			0.4	V	Isink=8mA
V_{OH}	Output High level pin D0-D7		2.4		V	Isource=8mA

Note: 1
This parameter for allowed variation in the PCLK frequency but does not permit the PCLK period to vary outside the minimum and maximum values for PCLK period specified above.

Note: 2
It is required that the Pixel address input to the color look-up table be set up as a valid logic level with the appropriate setup and hold times to each rising of PCLK.

Note: 3
A valid analog output is defined when the changing analog signal is half way between its successive values. This parameter is stable with time but can vary between different devices and may vary with different DC operating conditions.

Note: 4
Between different analog outputs on the same device.

Note: 5
Measured ±200 mV from steady state output voltage.

Note: 6
This parameter allows for synchronization between operations on the microprocessor interface and the pixel stream being processed by the color lookup table.

DESIGN CONSIDERATIONS

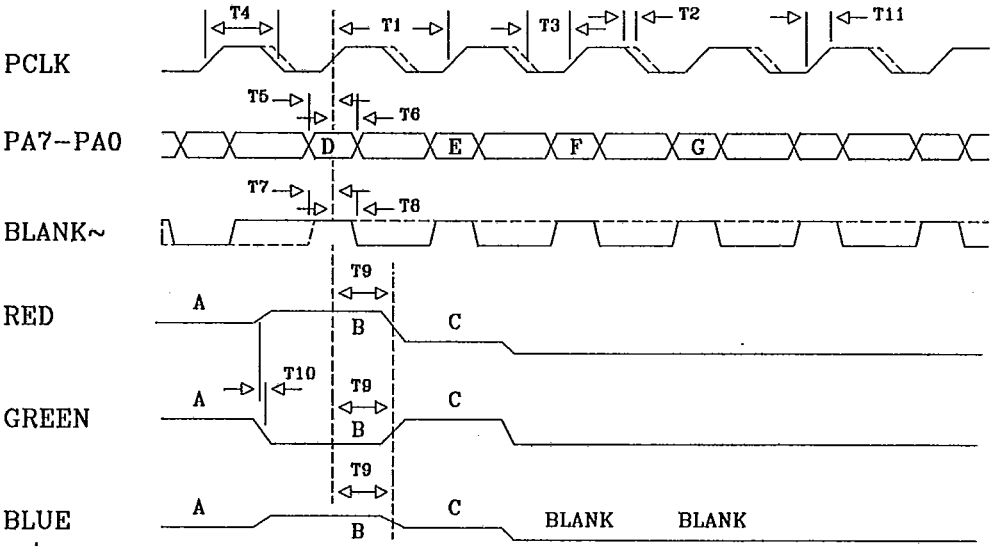
The LD1104 is fabricated in 2u CMOS technology to meet 50 MHz pixel speed requirements. Extra precautions are required to prevent damages due to electrostatic voltage discharge during handling and system manufacturing.

To reduce the high speed video DAC switching noises from the board or other logics, a large value capacitor (typ. 47 uF) is recommended to be connected from V_{CC} to GND pin. RGB outputs should be protected with high speed diodes going to GND and V_{CC}.

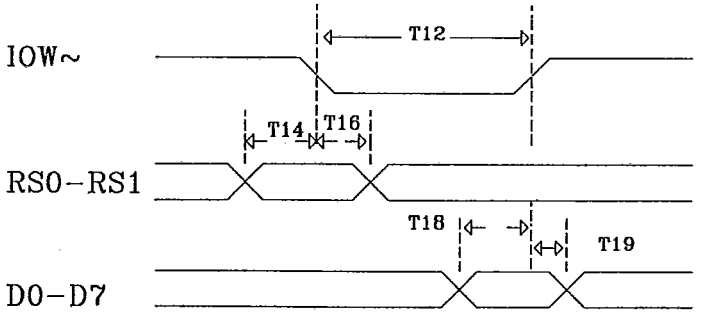
For stable output levels over the temperature variations, an active current source is recommended for IREF input connection.

LD1104

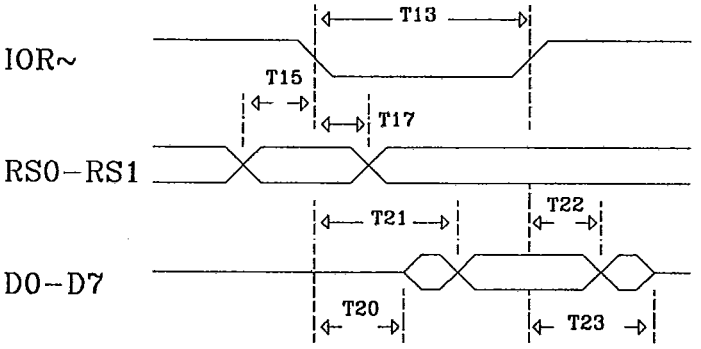
TIMING DIAGRAM



WRITE CYCLE



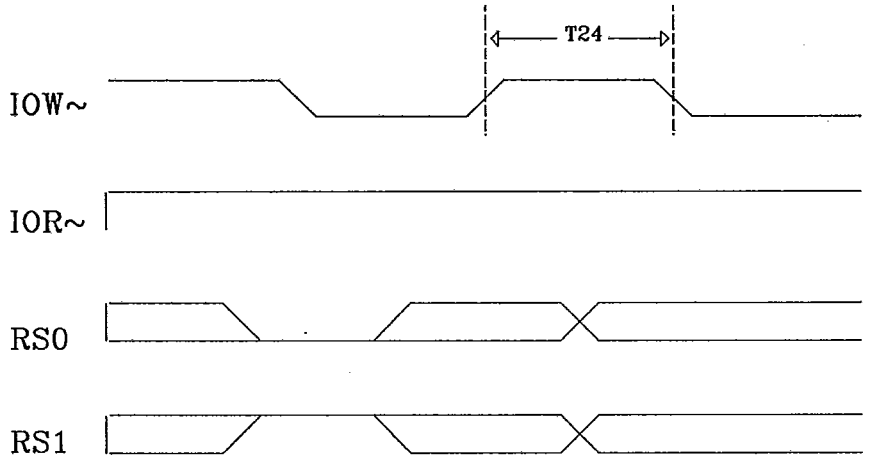
READ CYCLE

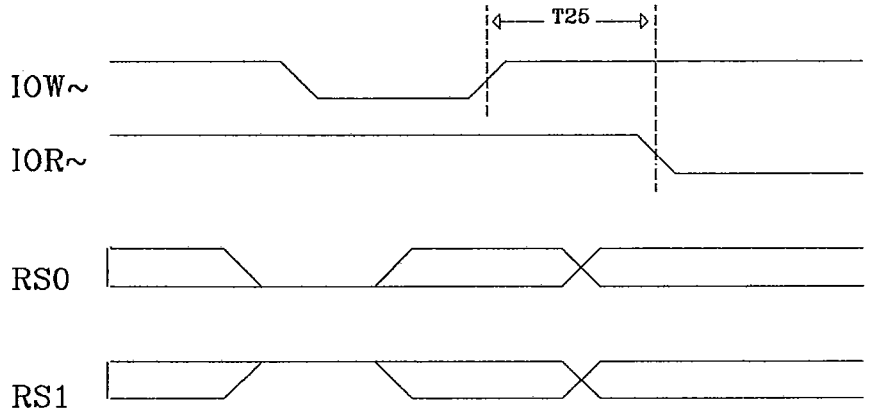


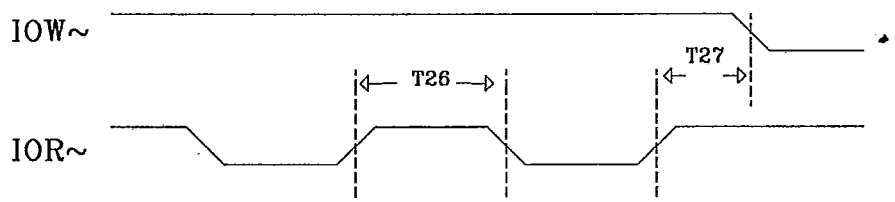
T-51-09-90

TIMING DIAGRAM

WRITE TO PIXEL MASK REGISTER FOLLOWED BY ANY ACCESS



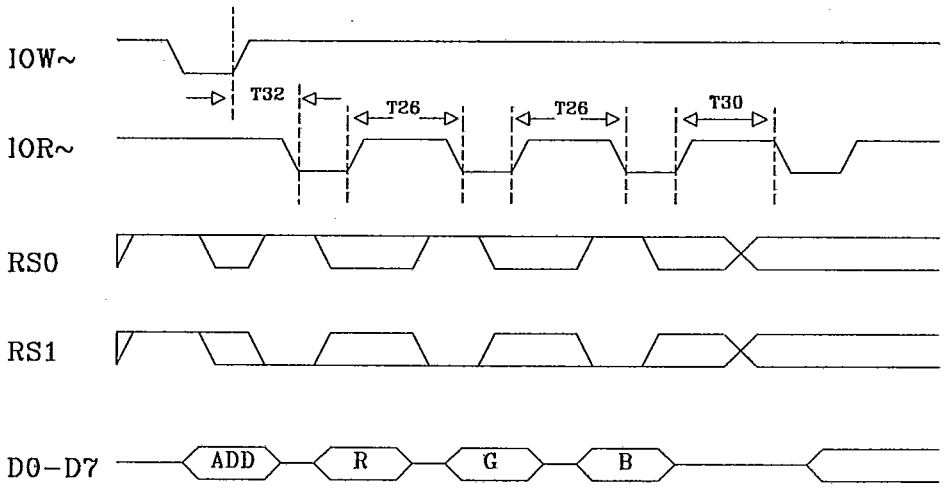




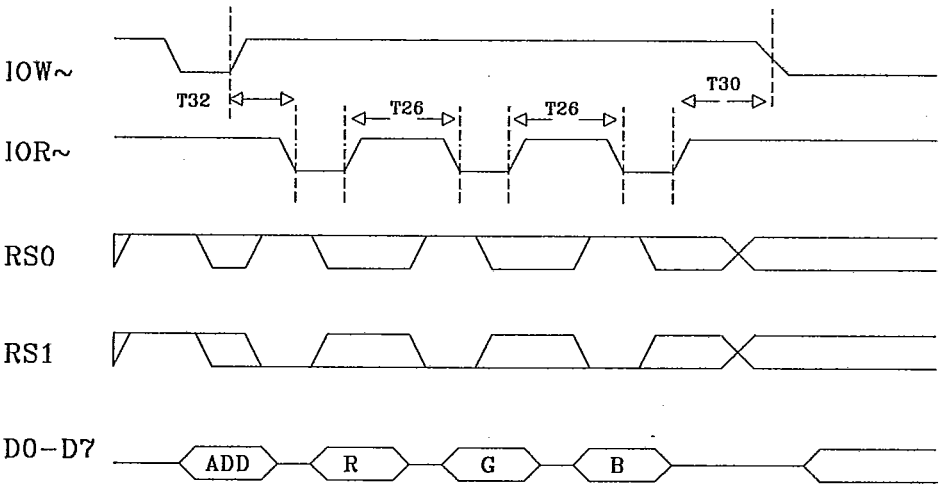
LD1104

TIMING DIAGRAM

COLOR VALUE READ FOLLOWED BY ANY READ



COLOR VALUE READ FOLLOWED BY ANY WRITE

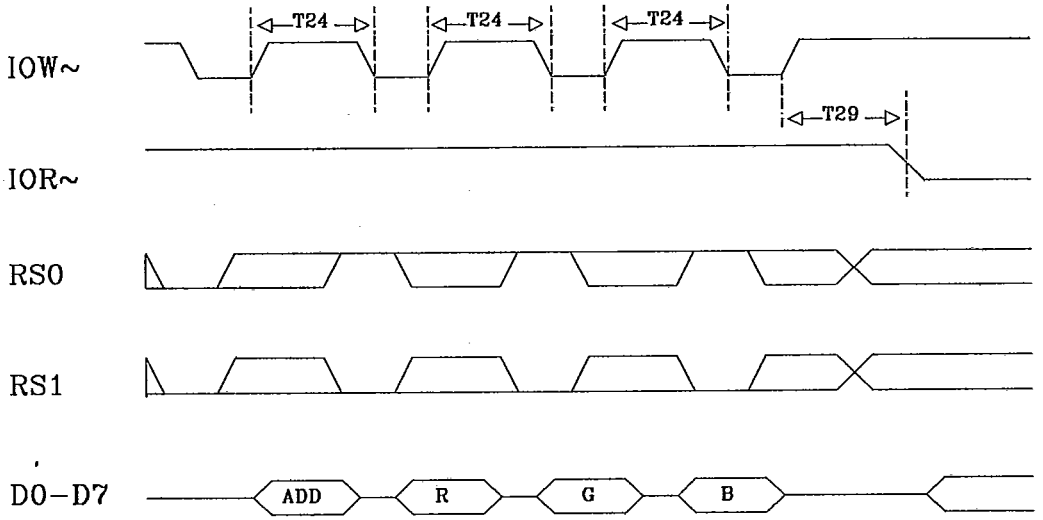


ADD=ADDRESS
R=RED
G=GREEN
B=BLUE

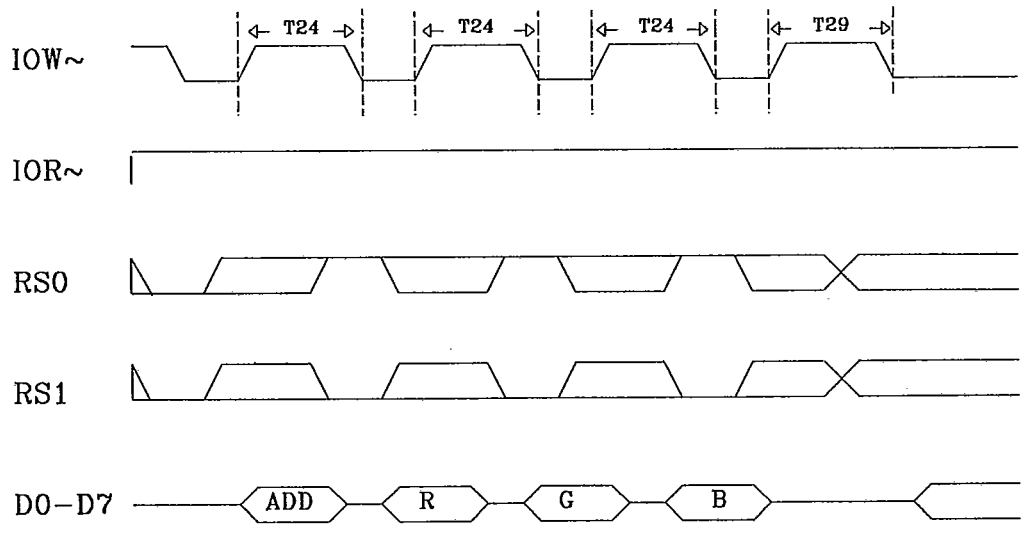
T-51-09-90

TIMING DIAGRAM

COLOR VALUE WRITE FOLLOWED BY ANY READ



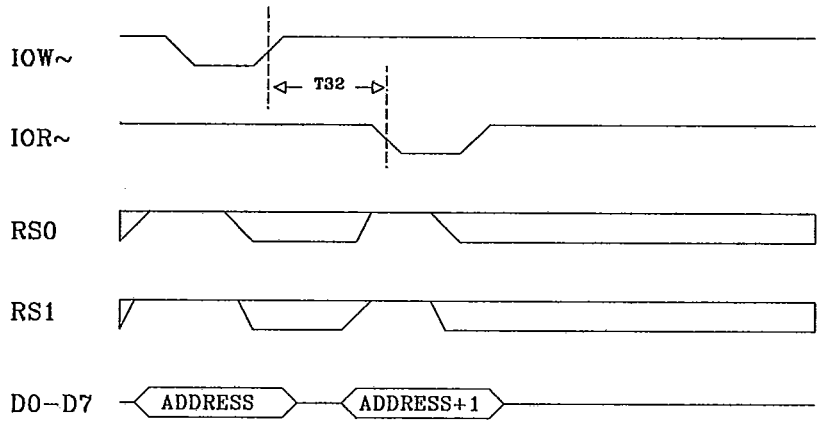
COLOR VALUE WRITE FOLLOWED BY ANY WRITE

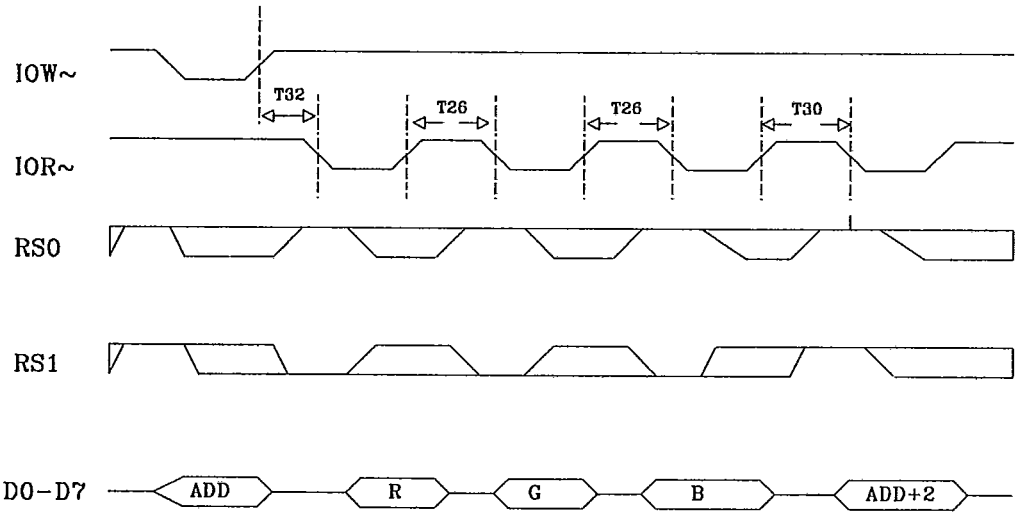


LD1104

TIMING DIAGRAM

WRITE AND READ BACK ADDRESS REGISTER





T-51-09-9D

44 PIN PLCC PINOUT